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DLD610/D
Rev. 1, Oct-2005

Selection. Service. Support.

DC-DC Power Conversion Products

DC-DC Power Conversion Products

DLD610/D
Rev. 1, OCT-2005

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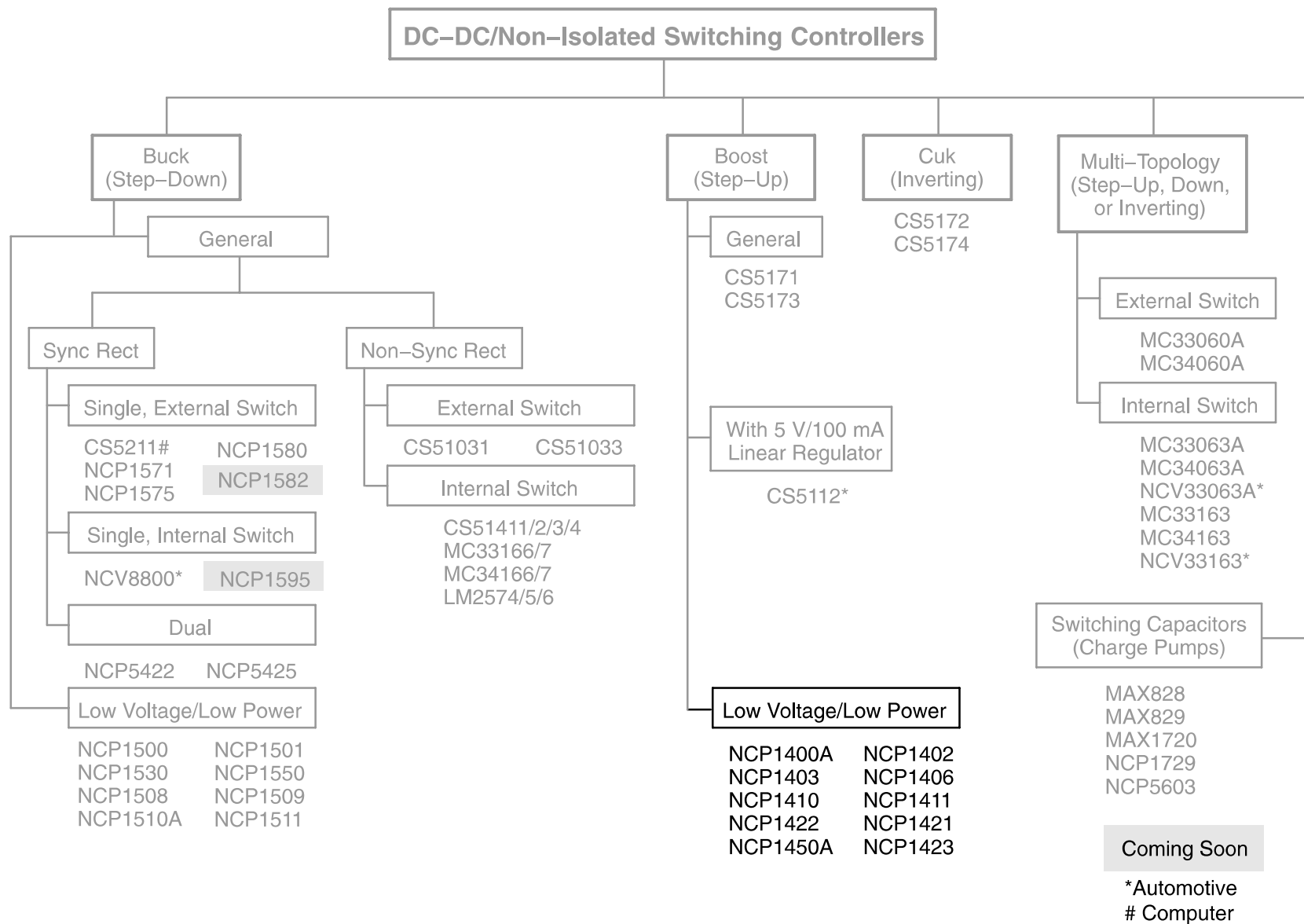
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CHAPTER 1

Selector Guide

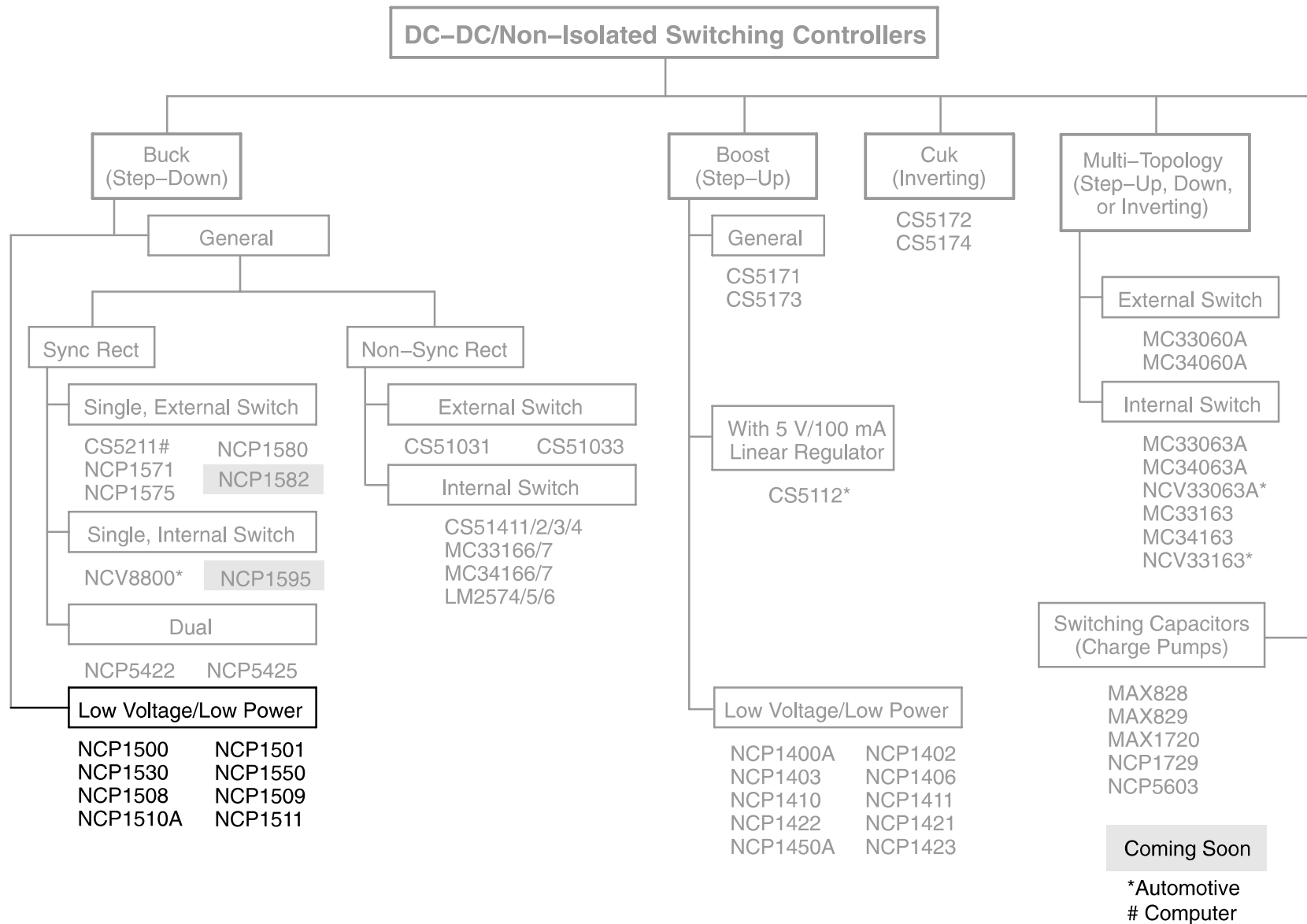


Boost Controllers (Low-Voltage, Low-Power/Portable Applications)

Converter/IC Min. Input Voltage	Switch Current	Control	Freq.	Temp. (T _A)	Package	Converter Output Voltage	Part No.	Features
0.8 V	100 mA	PWM	180 kHz	−40 to +85°C	TSOP−5	1.9 V	NCP1400ASN19T1	• CE pin (chip enable)
						2.2 V	NCP1400ASN22T1	
						2.5 V	NCP1400ASN25T1	
						2.7 V	NCP1400ASN27T1	
						3.0 V	NCP1400ASN30T1	
						3.3 V	NCP1400ASN33T1	
						3.8 V	NCP1400ASN38T1	
						4.5 V	NCP1400ASN45T1	
						5.0 V	NCP1400ASN50T1	
0.8 V	200 mA	PFM	Max 180 kHz	−40 to +85°C	TSOP−5	1.9 V	NCP1402SN19T1	• CE pin (chip enable)
						2.7 V	NCP1402SN27T1	
						3.0 V	NCP1402SN30T1	
						3.3 V	NCP1402SN33T1	
						5.0 V	NCP1402SN50T1	
0.8 V	Ext. N-FET	PWM	180 kHz	−40 to +85°C		1.9 V	NCP1450ASN19T1	• CE pin (chip enable)
						2.7 V	NCP1450ASN27T1	
						3.0 V	NCP1450ASN30T1	
						3.3 V	NCP1450ASN33T1	
						5.0 V	NCP1450ASN50T1	
1.0 V	250 mA	Sync. Rect. PFM	Max 600 kHz	−40 to +85°C	Micro8	1.5 V to 5.5 V	NCP1411DMR2	• Low-battery detector • Ring killer for efficiency
							NCP1410DMR2	• Low-battery detector
0.8 V	400 mA	Sync. Rect. PFM	Max 600 kz	−40 to +85°C	Micro10	1.8 V to 3.3 V	NCP1423DMR2	• True-cutoff • Ring killer for efficiency • Low battery detect input/output • Auto discharge input • Enable pin

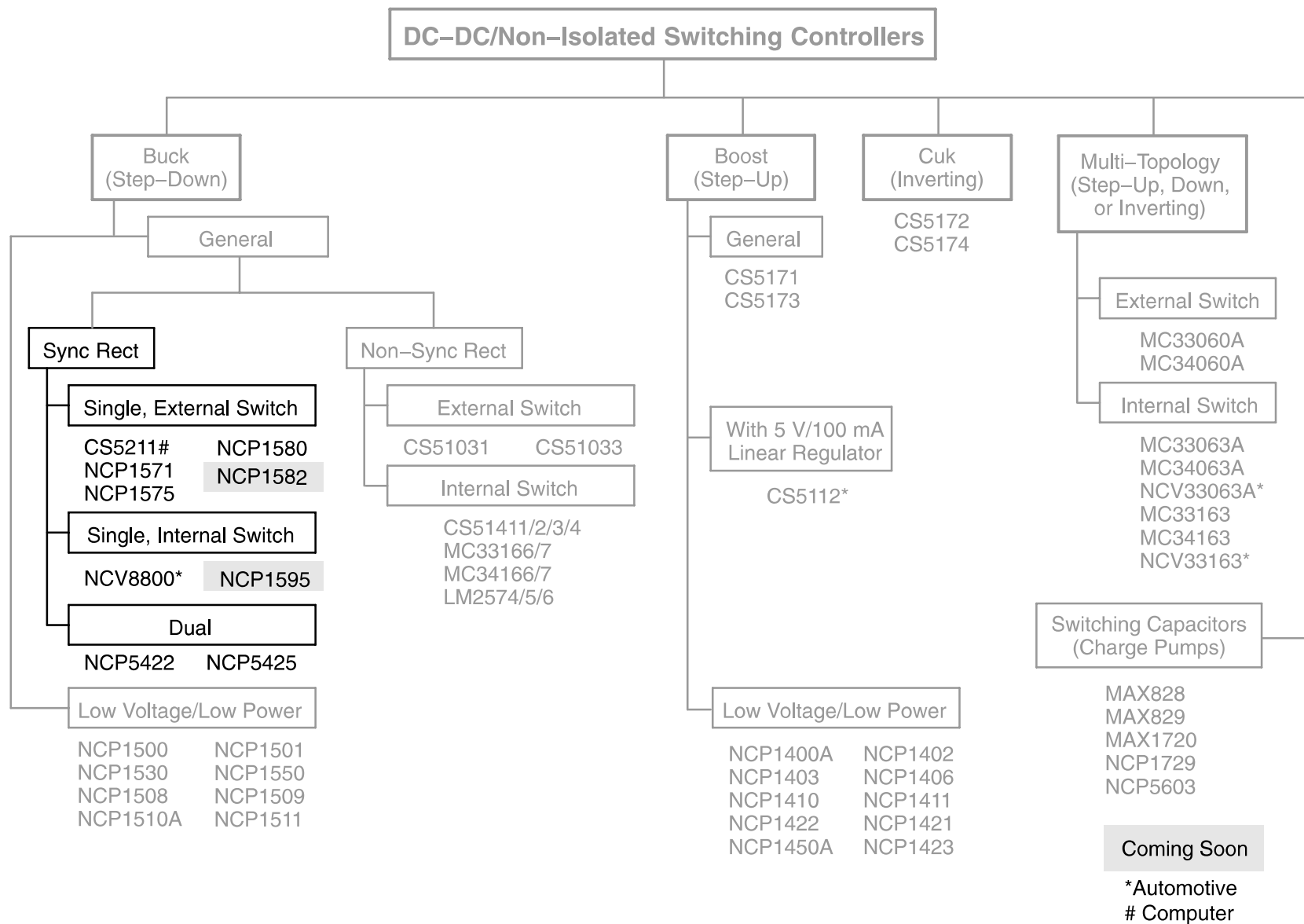
Boost Controllers (Low-Voltage, Low-Power/Portable Applications) (continued)

Converter/IC Min. Input Voltage	Switch Current	Control	Freq.	Temp. (T _A)	Package	Converter Output Voltage	Part No.	Features
1.0 V	600 mA	Sync. Rect. PFM	Max 1.2 MHz	-40 to +85°C	Micro8	1.5 V to 5.0 V	NCP1421DMR2	• True-cutoff • Ring killer for efficiency • Low battery detect
1.0 V	800 mA	Sync. Rect. PFM	Max 1.2 MHz	-40 to +85°C	DFN-10	1.5 V to 5.0 V	NCP1422MNR2	• Ring killer for efficiency • Low battery detector • Thermal shutdown
1.8 V	100 mA	PFM	Max 300 kHz	-40 to +85°C	TSOP-5	Up to 15 V	NCP1403SNT1	• CE pin (chip enable)
1.2 V	50 mA	PFM	Max 1.0 MHz	-40 to +85°C	TSOP-5	1.5 V to 25 V	NCP1406SNT1	• CE pin (chip enable)



Buck Controllers (Low-Voltage, Low-Power/Portable Applications)

Converter Input Voltage	Switch Current	Control	Freq.	Temp.	Package	Converter Output Voltage	Part No.	Features
2.5 to 5.2 V	500 mA	Sync. Rect. PWM/ Pulsed	1.0 MHz or sync 450 kHz to 1.0 MHz	-30 to +85°C (T _A)	Micro Bump-9	1.05 V, 1.35 V, 1.57 V, 1.8 V	NCP1510AFCT1	• Ultra low 14 µA quiescent current at light load • Operation depends on SYNC pin in three modes (Pulsed, PWM or synchronized) • Suffix G for Lead-free package • (Coming soon)
						1.0 V, 1.3 V, 1.5 V, 1.89 V	NCP1511FCT1	
					DFN-10	1.0 V, 1.3 V, 1.5 V, 1.89 V	NCP1508MNR2	
						1.35 V, 1.57 V, 1.8 V	NCP1509MNR2	
1.1 * V _{out} to 5.5 V	600 mA	PFM/ PWM	600 kHz	-40 to +85°C (T _A)	Micro8	2.5 V	NCP1530DM25R2	• External sync up to 1.2 MHz
						2.7 V	NCP1530DM27R2	
						3.0 V	NCP1530DM30R2	
						3.3 V	NCP1530DM33R2	
2.7 to 5.4 V	800 mA	Linear/ PFM/ PWM	Sync 270 to 630 kHz	-40 to +85°C (T _A)	Micro8	1.0 V, 1.3 V, 1.5 V, 1.8 V Digitally programmable	NCP1500DMR2	• Shutdown pin • Thermal shutdown • Linear/switching mode options • No internal oscillator
2.7 to 5.2 V		Sync. Rect. PWM/ Linear	Sync 500 kHz to 1.0 MHz	-30 to +85°C (T _A)		1.05 V, 1.35 V, 1.57 V, 1.8 V	NCP1501DMR2	
UVLO: 2.15/ 2.2 V Max: 5.5 V	Ext. P-FET	PFM/ PWM	600 kHz	-40 to +85°C (T _A)	TSOP-5	1.8 V	NCP1550SN18T1	• CE pin (chip enable) • Circuit operates at PFM at light load to maintain high efficiency
						1.9 V	NCP1550SN19T1	
						2.5 V	NCP1550SN25T1	
						2.7 V	NCP1550SN27T1	
						3.3 V	NCP1550SN33T1	



Buck Controllers (Sync. Rect., Single, External Switch)

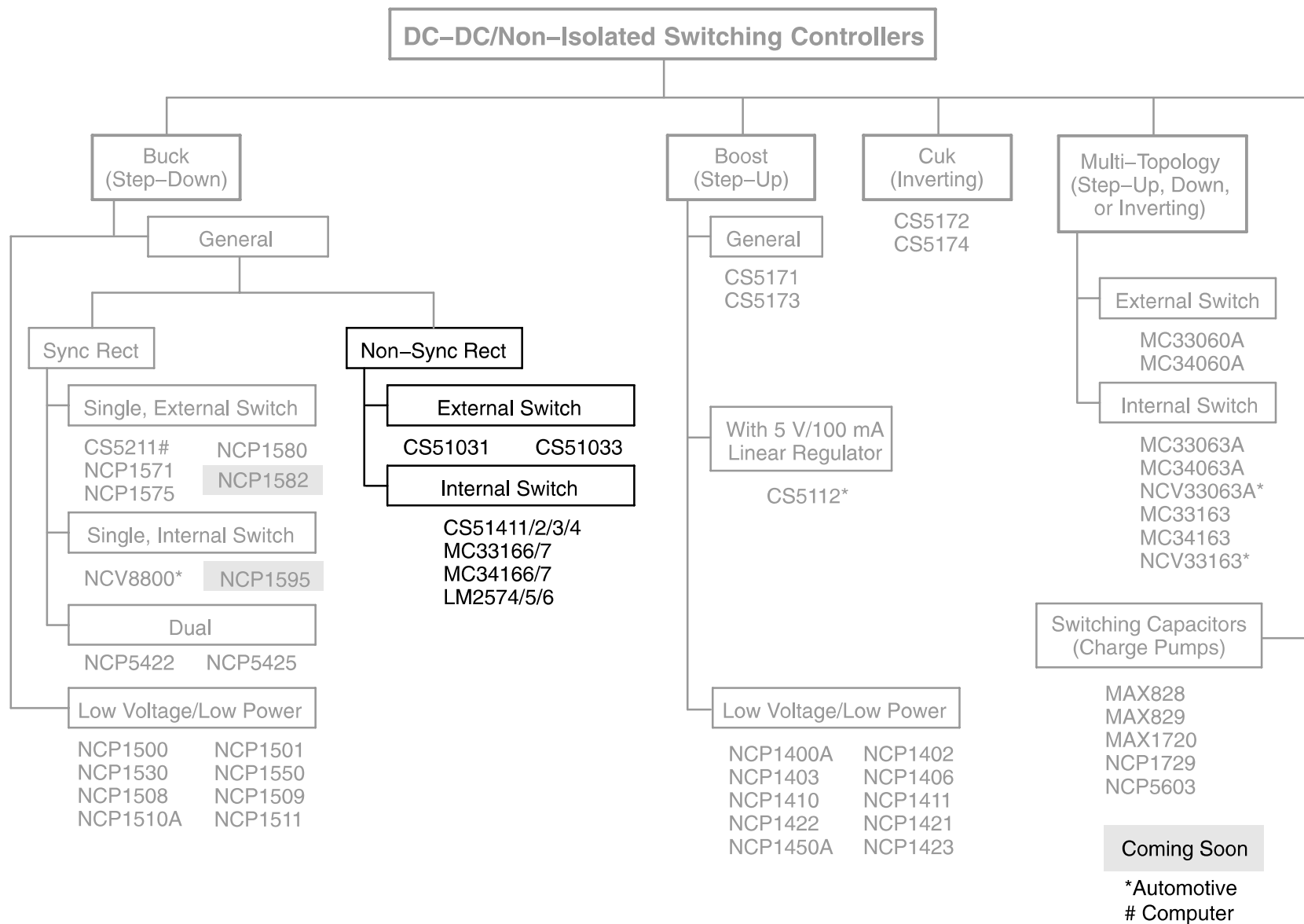
IC Operating Voltage	Converter Input Voltage	Output Voltage	Freq.	Temp.	Control	Package	Part No.	Features
UVLO: 3.9/4.05 V Max: 16 V	(V _{gate} max: 20 V)	Min. 1.0 V	150 to 750 kHz	-40 to +85°C (T _A)	Sync. Rect. PWM V ² mode	SO-14	CS5211ED14	• Driving dual N-FET • Programmable soft-start • Hiccup mode short circuit protection
				0 to +70°C (T _A)			CS5211GD14	
UVLO: 2.7/2.8 V Max: 4 V				-40 to +85°C (T _A)			CS5212ED14	
				0 to +70°C (T _A)			CS5212GD14	
UVLO: 7.5/8.5 V Max: 15 V	(V _{gate} max: 15 V)	Min. 0.980 V	Fixed 200 kHz	0 to +125°C (T _J)		SO-8	NCP1571D	• Driving dual N-FET • Power good • Programmable power good delay • Programmable soft-start (Not for NCP1573) • Overvoltage protection
Max: 15 V		Min. 0.980 V					NCP1573D	
UVLO: 7.5/8.5 V Max: 20 V	(V _{gate} max: 20 V)	Min. 0.980 V	Adjustable 200 to 500 kHz				NCP1575D	• Driving dual N-FET • Programmable soft-start • Overvoltage protection
UVLO: 3.7/4.2 V Max: 15 V	(V _{gate} max: 30 V)	Min. 0.8 V	Fixed 350 kHz		-40 to +125°C (T _J)	PWM V-mode	SO-8	NCP1580DR2

Buck Regulators (Sync. Rect., Single, Internal Switch)

IC Operating Voltage	Converter Output Voltage	Switch	Freq.	Temp.	Control	Option	Package	Part No.	Features
Sequenced: 3.5 to 16 V High Voltage: 6.0 to 16 V Max: 45 V	2.6 V	(1.6 A Current limit)	Fixed 200 kHz	-40 to +125°C (T _J)	Sync. Rect. PWM V ² mode	Sequenced	SO-16L	NCV8800SDW26	- Reset pin - Enable pin - Thermal shutdown
						High Voltage		NCV8800HDW26	
	3.3 V					Sequenced		NCV8800SDW33	
						High Voltage		NCV8800HDW33	
	5.0 V					High Voltage		NCV8800HDW50	
	7.5 V					High Voltage		NCV8800HDW75	
Max: 7.0 V	1.2 V to 3.375 V	(2.5 A Current limit)	Fixed 1.2 MHz	-40 to +125°C (T _A)	PWM I-mode	N/A	3x3 DFN	NCP1595	- Enable pin - Thermal shutdown (130/160°C) (Coming soon)

Buck Controllers (Sync. Rect., Dual)

IC Operating Voltage	Converter Input Voltage	Output Voltage	Freq.	Temp.	Control	Package	Part No.	Features
UVLO: 7.8/ 8.6 V Max: 16 V	(V _{gate} max: 20 V)	Min. 1.0 V	15 to 600 kHz	0 to +70°C (T _A)	Sync. Rect. PWM V ² mode	SO-16	NCP5422ADR2	• Out-of-phase for ripple cancellation • Driving dual N-FET • Programmable soft-start • Hiccup mode overcurrent protection in NCP5422A • Single or dual output mode pin in NCP5425
UVLO: 4.0/ 4.2 V Max: 16 V	(V _{gate} max: 20 V)	Min. 0.8 V	150 to 750 kHz	0 to +125°C (T _A)		TSSOP-20	NCP5425DB	



Buck Controllers (Non-Sync. Rect., Internal Switch)

Converter Input Voltage	Converter Output Voltage	Switch	Freq.	Temp. (T _A)	Max. Duty	Control	Package	Part No.	Features
4.5 to 40 V (Boots-trap pin max 40 V)	Min. 1.276 V	1.5 A	Fixed 260 kHz	-40 to +85°C	90%	PWM V ² mode	SO-8	CS51411ED8	- Frequency decrease of 4:1 in short-circuit conditions - Soft-start - Thermal shutdown - Shutdown - Synchronous option of CS51411/3 or bias option for CS51412/4
				0 to +70°C				CS51412ED8	
			Fixed 520 kHz	-40 to +85°C				CS51411GD8	
				0 to +70°C				CS51412GD8	
				-40 to +85°C				CS51413ED8	
				0 to +70°C				CS51414ED8	
				-40 to +85°C				CS51413GD8	
				0 to +70°C				CS51414GD8	
4.75 to 40 V	Fixed 3.3 V	0.5 A	Fixed 52 kHz	-40 to +125°C	98%	PWM V mode	DIP-8	LM2574N-3.3	- ON/OFF - Thermal shutdown - Current limit protection
		1.0 A					D2PAK-5	LM2575D2T-3.3	
							TO-220-5	LM2575T-3.3	
							TO-220-5 VER	LM2575TV-3.3	
6.0 to 40 V		3.0 A					D2PAK-5	LM2576D2T-3.3	
							TO-220-5	LM2576T-3.3	
7.0 to 40 V	Fixed 5.0 V	0.5 A	Fixed 52 kHz	-40 to +125°C	98%	PWM V mode	DIP-8	LM2574N-5	- ON/OFF - Thermal shutdown - Current limit protection
		1.0 A					D2PAK-5	LM2575D2T-5	
							TO-220-5	LM2575T-5	
							TO-220-5 VER	LM2575TV-5	
8.0 to 40 V		3.0 A					D2PAK-5	LM2576D2T-5	
							TO-220-5	LM2576T-5	

Buck Controllers (Non-Sync. Rect., Internal Switch) (continued)

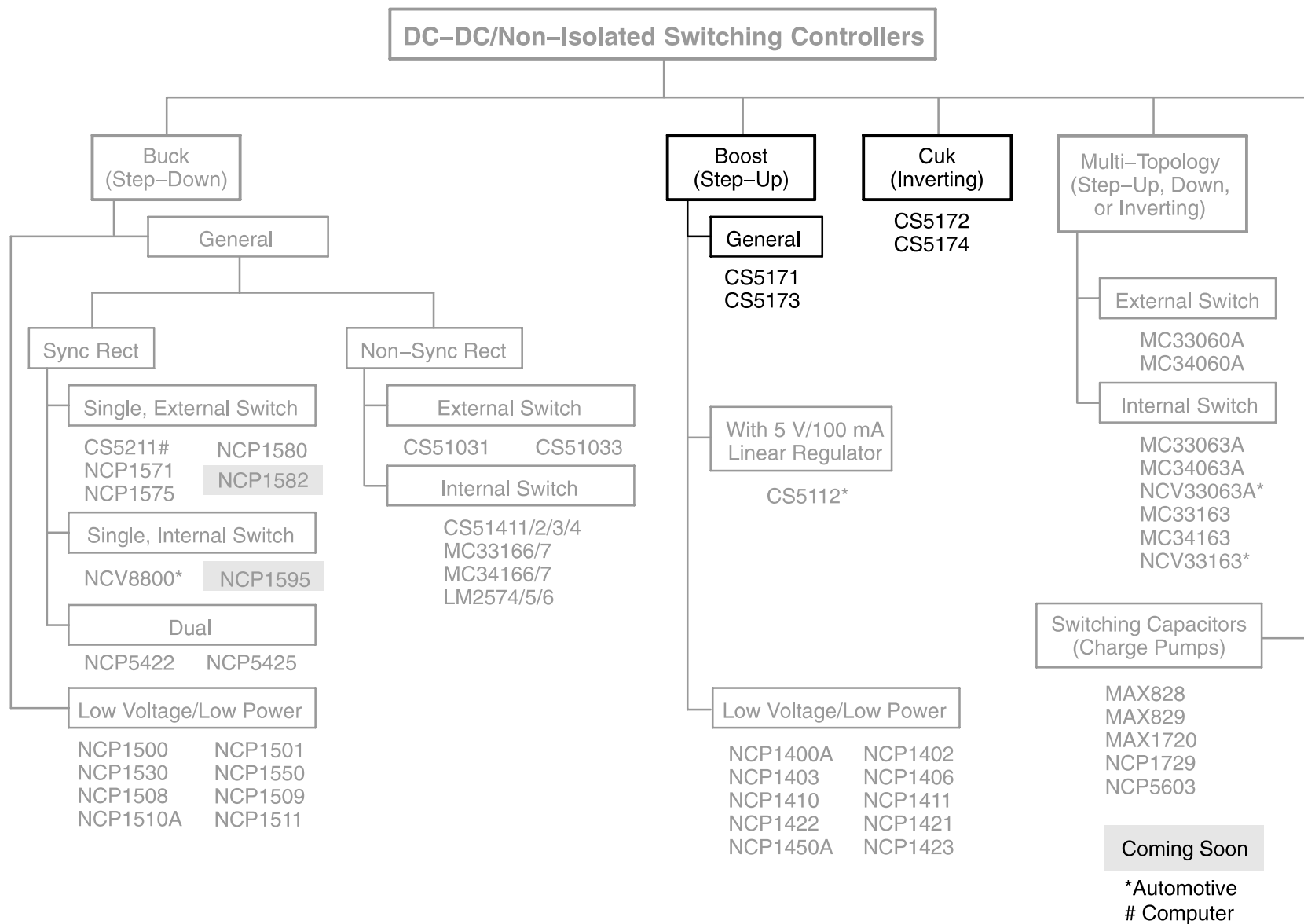
Converter Input Voltage	Converter Output Voltage	Switch	Freq.	Temp. (T _A)	Max. Duty	Control	Package	Part No.	Features						
UVLO: 5.9/ 6.8 V Max: 40 V	Min. 5.0 V	3.0 A	Fixed 72 kHz	–40 to +85°C	95%	PWM V mode	D2PAK–5	MC33166D2T	• Compensation pin • Internal thermal shutdown • Cycle-by-cycle current limiting						
							TO–220–5	MC33166T							
							TO–220–5 HOR	MC33166TH							
							TO–220–5 VER	MC33166TV							
		5.0 A		0 to +70°C	95%		D2PAK–5	MC34166D2T							
							TO–220–5	MC34166T							
							TO–220–5 HOR	MC34166TH							
							TO–220–5 VER	MC34166TV							
				–40 to +85°C			95%			D2PAK–5	MC33167D2T				
										TO–220–5	MC33167T				
										TO–220–5 HOR	MC33167TH				
										TO–220–5 VER	MC33167TV				
				0 to +70°C						D2PAK–5	MC34167D2T				
										TO–220–5	MC34167T				
										TO–220–5 HOR	MC34167TH				
										TO–220–5 VER	MC34167TV				

Buck Controllers (Non-Sync. Rect., Internal Switch) (continued)

Converter Input Voltage	Converter Output Voltage	Switch	Freq.	Temp. (T _A)	Max. Duty	Control	Package	Part No.	Features
15 to 40 V	Fixed 12 V	0.5 A	Fixed 52 kHz	-40 to +125°C	98%	PWM V mode	DIP-8	LM2574N-12	• ON/OFF • Thermal shutdown • Current limit protection
		D2PAK-5					LM2575D2T-12		
18 to 40 V	Fixed 15 V	0.5 A					DIP-8	LM2574N-15	• ON/OFF • Thermal shutdown • Current limit protection
		1.0 A					D2PAK-5	LM2575D2T-15	
8.0 to 40 V	1.23 to 37 V	0.5 A					SO-16W	LM2574DW-ADJ	• ON/OFF • Thermal shutdown • Current limit protection
		1.0 A					DIP-8	LM2574N-ADJ	
							D2PAK-5	LM2575D2T-ADJ	
							TO-220-5	LM2575T-ADJ	
		3.0 A	TO-220-5 VER	LM2575TV-ADJ					
			D2PAK-5	LM2576D2T-ADJ					
			TO-220-5	LM2576T-ADJ					
		TO-220-5 VER	LM2576TV-ADJ						

Buck Controllers (Non-Sync. Rect., External Switch)

IC Operating Voltage	Output Voltage	Max. Duty	External Switch	Freq.	Control	Temp. (T _A)	Package	Part No.	Features
3.1 to 5.0 V	Min. 1.25 V	83.3%	P-FET	Up to 700 kHz	Burst mode V-mode	-40 to +85°C	SO-8	CS51033YD8	• Frequency foldback 1/30 during overcurrent • Programmable soft-start • Programmable frequency • Lossless short circuit protection
UVLO: 4.3/4.4 V Max: 16 V						0 to +70°C		CS51033GD8	
						-40 to +85°C		CS51031YD8	
						0 to +70°C		CS51031GD8	

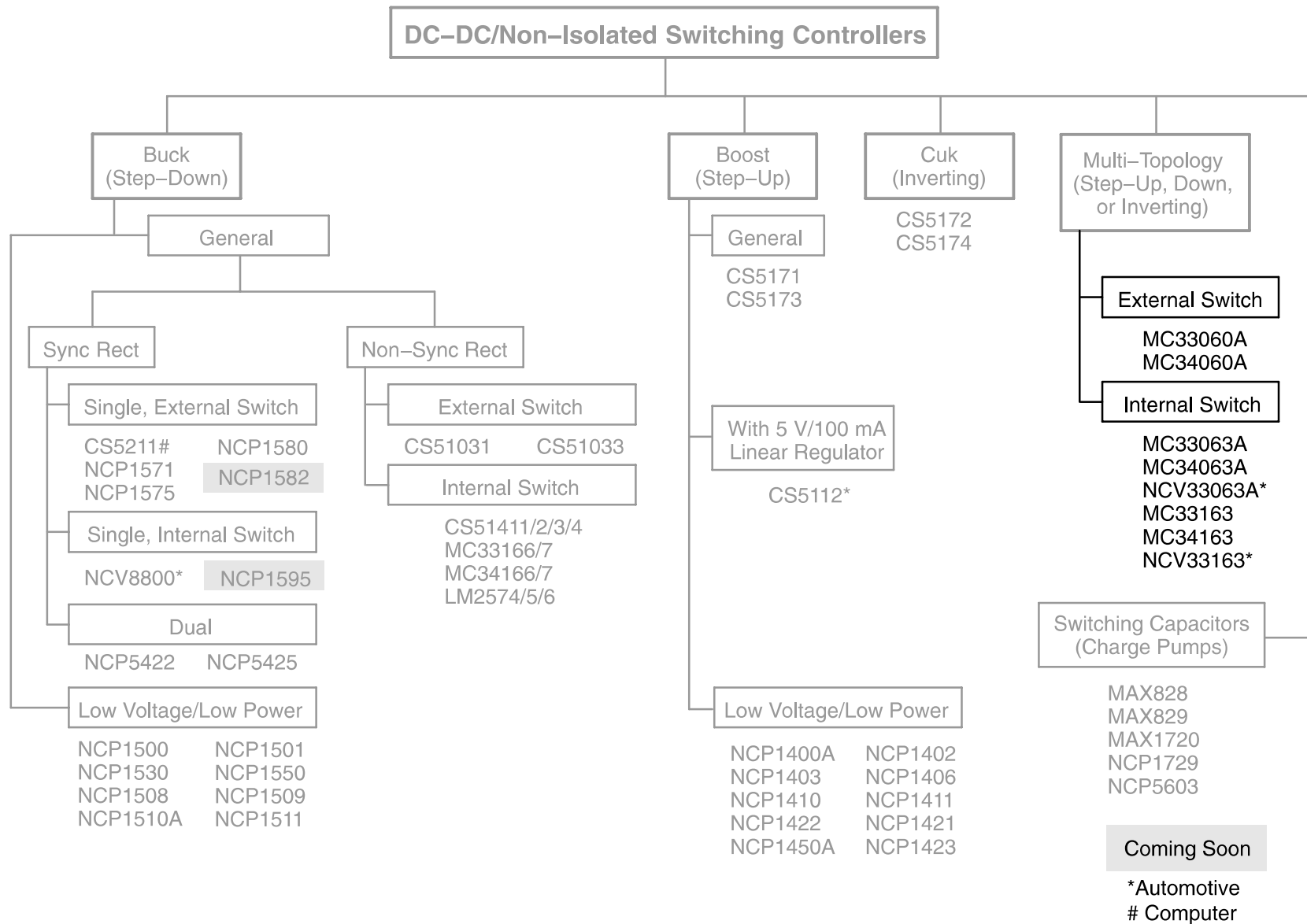


Boost/Sepic Controllers (Internal Switch)

IC Operating Voltage	Converter Output Voltage	Switch	Package	Freq.	Max. Duty	Temp. (T _A)	Part No.	Features
2.7 V to 30 V	(V _{sw} < 40 V) (V _{ref} = 1.276 V)	1.5 A ^(*)	SO-8	Fixed 280 kHz	94%	-40 to +85°C	CS5171ED8	• Overcurrent protection • Thermal shutdown with hysteresis • Frequency foldback 1/5 during overcurrent • Synchronization and shutdown pin • PWM I-mode control • (*) Guaranteed by design
						0 to +70°C	CS5171GD8	
				Fixed 560 kHz	90%	-40 to +85°C	CS5173ED8	
						0 to +70°C	CS5173GD8	

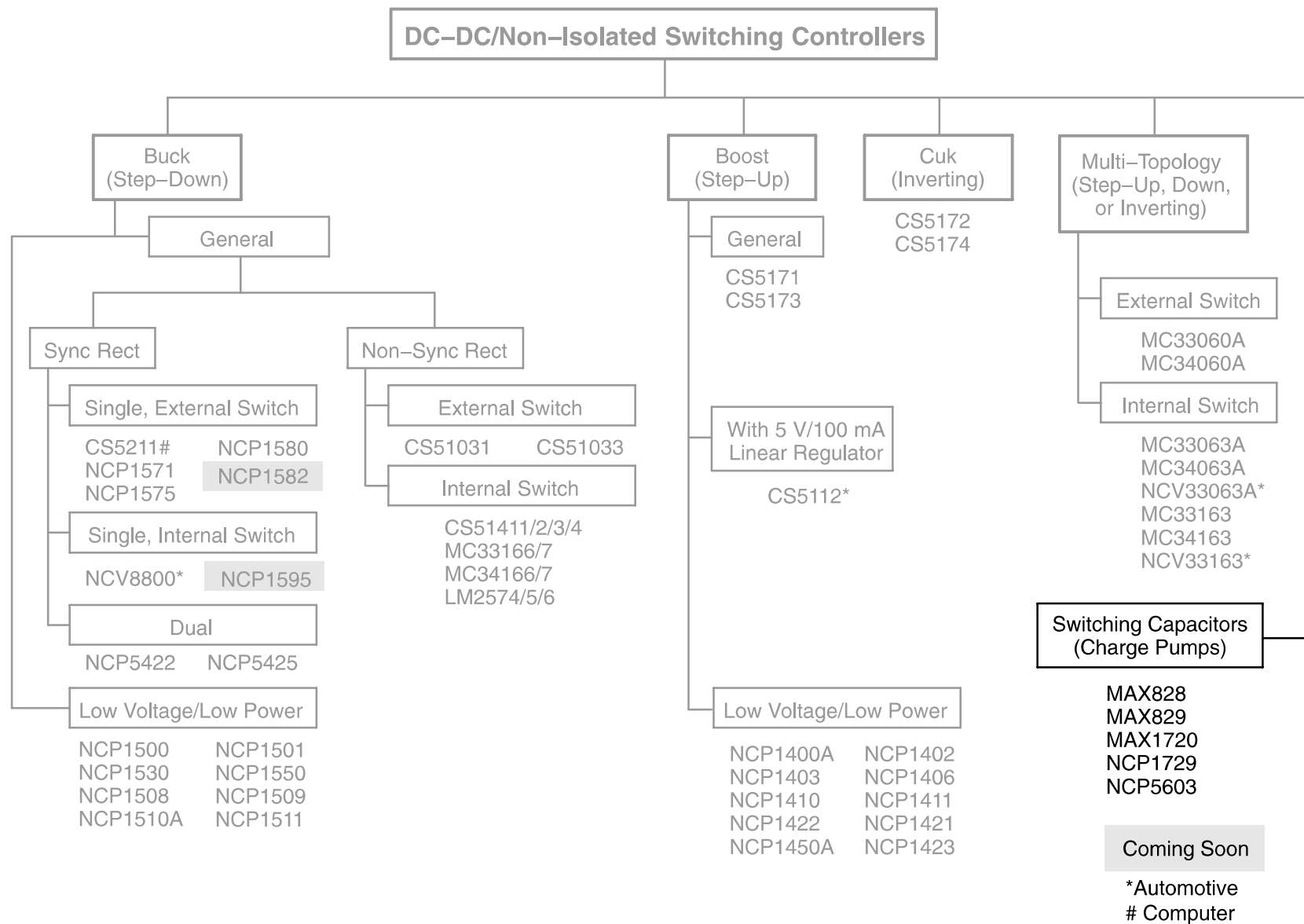
Cuk Controllers (Internal Switch)

IC Operating Voltage	Converter Output Voltage	Switch	Package	Freq.	Max. Duty	Temp. (T _A)	Part No.	Features
2.7 V to 30 V	(V _{sw} < 40 V) (V _{ref} = -2.5 V)	1.5 A ^(*)	SO-8	Fixed 280 kHz	94%	-40 to +85°C	CS5172ED8	• Overcurrent protection • Thermal shutdown with hysteresis • Frequency foldback during overcurrent • Synchronization and shutdown pin • PWM I-mode control • (*) Guaranteed by design
						0 to +70°C	CS5172GD8	
				Fixed 560 kHz	90%	-40 to +85°C	CS5174ED8	
						0 to +70°C	CS5174GD8	

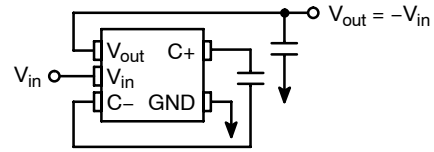


Multi-Topology Controllers (Step-Up, Down, or Inverting)

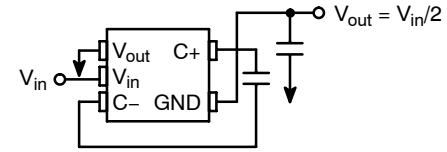
IC Operating Voltage	Converter Input Voltage	Reference Voltage	Switch	Control	Freq.	Max. Duty	Temp. (T _A)	Package	Part No.	Features	
2.5 to 40 V	(Max. VSW = 40 V)	1.25 V	3.4 A max	Burst mode V-mode	Around 50 kHz	TBD	0 to +70°C	SO-16W	MC34163DW	• Current limit • Thermal shutdown	
								DIP-16	MC34163P		
							-40 to +85°C	SO-16W	MC33163DW		
								DIP-16	MC33163P		
2.5 to 60 V	(Max. VSW = 60 V)		2.5 A max	TBD	-40 to +115°C	SO-16W	NCV33163DW				
						DIP-16	NCV33163P				
3.0 to 40 V	(Max. VSW = 40 V)		1.5 A max	Burst mode V-mode	Up to 100 kHz	TBD	0 to +70°C	SO-8	MC34063AD		• Current limit
								DIP-8	MC34063AP1		
							-40 to +85°C	SO-8	MC33063AD		
								DIP-8	MC33063AP1		
		-40 to +125°C					SO-8	MC33063AVDR2			
							DIP-8	MC33063AVP			
UVLO: 4.55/ 4.7 V Max: 42 V	Nil	(External ref.) (*)	External	PWM V-mode	Up to 200 kHz	92/ 96%	0 to +70°C	SO-14	MC34060AD	• (*) 5.0 V reference pin	
								DIP-14	MC34060AP		
							-40 to +85°C	SO-14	MC33060AD		
								DIP-14	MC33060AP		



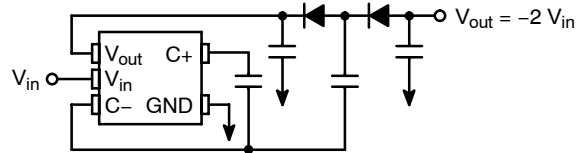
Charge Pump, Application



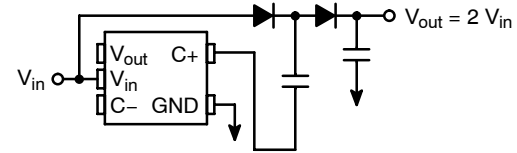
Inverting



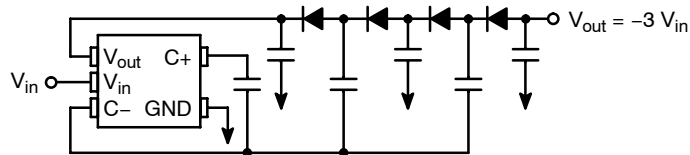
Half Splitter



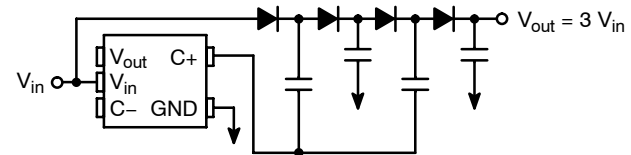
Negative Doubler



Doubler



Negative Tripler



Tripler

Charge Pump Converters

Output Current (Typ mA)	Part No.	Output Voltage	Input Voltage Range (V)	Oscillator Frequency (kHz)	Quiescent Supply Current* (Max μ A @ 25°C)	Package	Features
25	MAX828EUK	$V_{out} = -V_{in}$ or $V_{out} = 2 V_{in}$	1.15 $\rightarrow$ 5.5	12	90	TSOP-5†	
25	MAX829EUK	$V_{out} = -V_{in}$ or $V_{out} = 2 V_{in}$	1.15 $\rightarrow$ 5.5	35	200	TSOP-5†	
25	MAX1720EUT	$V_{out} = -V_{in}$ or $V_{out} = 2 V_{in}$	1.15 $\rightarrow$ 5.5	12	90	TSOP-6†	with Enable
50	NCP1729SN35T1	$V_{out} = -V_{in}$ or $V_{out} = 2 V_{in}$	1.15 $\rightarrow$ 5.5	35	200	TSOP-6†	with Enable
350 (Pulsed)/ 200 mA (DC)	NCP5603MNR2	$V_{out} = 4.5$ V or 5.0 V	2.7 to 5.5	262 or 650	2.5	DFN-10	90% Efficiency with 1x, 1.5x and 2x Automatic Operating Mode

*Measured at $V_{DD} = 5.0$ V at 25°C and no load.

†TSOP-5/6 – Also known as Thin SOT23-5/6.

CHAPTER 2

Datasheets

CS51031

Fast P-Ch FET Buck Controller

The CS51031 is a switching controller for use in DC-DC converters. It can be used in the buck topology with a minimum number of external components. The CS51031 consists of a V_{CC} monitor for controlling the state of the device, 1.0 A power driver for controlling the gate of a discrete P-Channel transistor, fixed frequency oscillator, short circuit protection timer, programmable Soft-Start, precision reference, fast output voltage monitoring comparator, and output stage driver logic with latch.

The high frequency oscillator allows the use of small inductors and output capacitors, minimizing PC board area and systems cost. The programmable Soft-Start reduces current surges at startup. The short circuit protection timer significantly reduces the duty cycle to approximately 1/30 of its cycle during short circuit conditions.

Features

- Pb-Free Package is Available
- 1.0 A Totem Pole Output Driver
- High Speed Oscillator (700 kHz max)
- No Stability Compensation Required
- Lossless Short Circuit Protection
- V_{CC} Monitor
- 2.0% Precision Reference
- Programmable Soft-Start
- Wide Ambient Temperature Range:
 - ◆ Industrial Grade: -40°C to 85°C
 - ◆ Commercial Grade: 0°C to 70°C



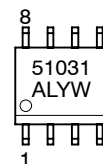
ON Semiconductor®

<http://onsemi.com>



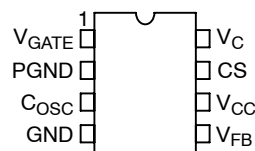
**SOIC-8
D SUFFIX
CASE 751**

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 38 of this data sheet.

CS51031

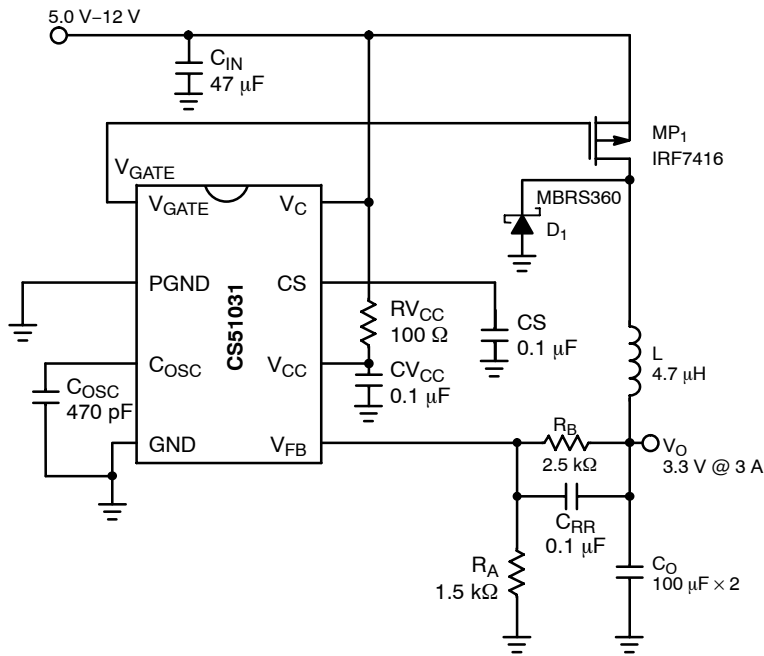


Figure 1. Typical Application Diagram

MAXIMUM RATINGS

Rating	Value	Unit
Power Supply Voltage, V_{CC}	20	V
Driver Supply Voltage, V_C	20	V
Driver Output Voltage, V_{GATE}	20	V
C_{OSC} , CS, V_{FB} (Logic Pins)	6.0	V
Peak Output Current	1.0	A
Steady State Output Current	200	mA
Operating Junction Temperature, T_J	150	°C
Operating Temperature Range, T_A	–40 to 85	°C
Storage Temperature Range, T_S	–65 to 150	°C
ESD (Human Body Model)	2.0	kV
Lead Temperature Soldering:	Wave Solder: (through hole styles only) (Note 1) Reflow (SMD styles only) (Note 2)	260 peak 230 peak
		°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. 10 sec. maximum.
2. 60 sec. max above 183°C.

CS51031

ELECTRICAL CHARACTERISTICS (Specifications apply for $4.5 \leq V_{CC} \leq 16 \text{ V}$, $3.0 \text{ V} \leq V_C \leq 16 \text{ V}$;

Industrial Grade: $-40^\circ\text{C} < T_A < 85^\circ\text{C}$; $-40^\circ\text{C} < T_J < 125^\circ\text{C}$; Commercial Grade: $0^\circ\text{C} < T_A < 70^\circ\text{C}$; $0^\circ\text{C} < T_J < 125^\circ\text{C}$, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Oscillator $V_{FB} = 1.2 \text{ V}$					
Frequency	$C_{OSC} = 470 \text{ pF}$	160	200	240	kHz
Charge Current	$1.4 \text{ V} < V_{COSC} < 2.0 \text{ V}$	–	110	–	μA
Discharge Current	$2.7 \text{ V} > V_{COSC} > 2.0 \text{ V}$	–	660	–	μA
Maximum Duty Cycle	$1 - (t_{OFF}/t_{ON})$	80.0	83.3	–	%
Short Circuit Timer $V_{FB} = 1.0 \text{ V}$; $CS = 0.1 \mu\text{F}$; $V_{COSC} = 2.0 \text{ V}$					
Charge Current	$1.0 \text{ V} < V_{CS} < 2.0 \text{ V}$	175	264	325	μA
Fast Discharge Current	$2.55 \text{ V} > V_{CS} > 2.4 \text{ V}$	40	66	80	μA
Slow Discharge Current	$2.4 \text{ V} > V_{CS} > 1.5 \text{ V}$	4.0	6.0	10	μA
Start Fault Inhibit Time	$0 \text{ V} < V_{CS} < 2.5 \text{ V}$	0.70	0.85	1.40	ms
Valid Fault Time	$2.6 \text{ V} > V_{CS} > 2.4 \text{ V}$	0.2	0.3	0.45	ms
GATE Inhibit Time	$2.4 \text{ V} > V_{CS} > 1.5 \text{ V}$	9.0	15	23	ms
Fault Duty Cycle	–	2.5	3.1	4.6	%
CS Comparator $V_{FB} = 1.0 \text{ V}$					
Fault Enable CS Voltage	–	–	2.5	–	V
Max CS Voltage	$V_{FB} = 1.5 \text{ V}$	–	2.6	–	V
Fault Detect Voltage	V_{CS} when GATE goes high	–	2.4	–	V
Fault Inhibit Voltage	Minimum V_{CS}	–	1.5	–	V
Hold Off Release Voltage	$V_{FB} = 0 \text{ V}$	0.4	0.7	1.0	V
Regulator Threshold Voltage Clamp	$V_{CS} = 1.5 \text{ V}$	0.725	0.866	1.035	V
V_{FB} Comparators $V_{COSC} = V_{CS} = 2.0 \text{ V}$					
Regulator Threshold Voltage	$T_J = 25^\circ\text{C}$ (Note 3)	1.225	1.250	1.275	V
	$T_J = -40$ to 125°C	1.210	1.250	1.290	V
Fault Threshold Voltage	$T_J = 25^\circ\text{C}$ (Note 3)	1.12	1.15	1.17	V
	$T_J = -40$ to 125°C	1.10	1.15	1.19	V
Threshold Line Regulation	$4.5 \text{ V} \leq V_{CC} \leq 16 \text{ V}$	–	6.0	15	mV
Input Bias Current	$V_{FB} = 0 \text{ V}$	–	1.0	4.0	μA
Voltage Tracking	(Regulator Threshold – Fault Threshold Voltage)	70	100	120	mV
Input Hysteresis Voltage	–	–	4.0	20	mV
Power Stage $V_{CC} = V_C = 10 \text{ V}$; $V_{FB} = 1.2 \text{ V}$					
GATE DC Low Saturation Voltage	$V_{COSC} = 1.0 \text{ V}$; 200 mA Sink	–	1.2	1.5	V
GATE DC High Saturation Voltage	$V_{COSC} = 2.7 \text{ V}$; 200 mA Source; $V_C = V_{GATE}$	–	1.5	2.1	V
Rise Time	$C_{GATE} = 1.0 \text{ nF}$; $1.5 \text{ V} < V_{GATE} < 9.0 \text{ V}$	–	25	60	ns
Fall Time	$C_{GATE} = 1.0 \text{ nF}$; $9.0 \text{ V} > V_{GATE} > 1.5 \text{ V}$	–	25	60	ns

CS51031

ELECTRICAL CHARACTERISTICS (Specifications apply for $4.5 \leq V_{CC} \leq 16 \text{ V}$, $3.0 \text{ V} \leq V_C \leq 16 \text{ V}$;

Industrial Grade: $-40^\circ\text{C} < T_A < 85^\circ\text{C}$; $-40^\circ\text{C} < T_J < 125^\circ\text{C}$; Commercial Grade: $0^\circ\text{C} < T_A < 70^\circ\text{C}$; $0^\circ\text{C} < T_J < 125^\circ\text{C}$, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit

V_{CC} Monitor

Turn-On Threshold	–	4.200	4.400	4.600	V
Turn-Off Threshold	–	4.085	4.300	4.515	V
Hysteresis	–	65	130	200	mV

Current Drain

I_{CC}	$4.5 \text{ V} < V_{CC} < 16 \text{ V}$, Gate switching	–	4.5	6.0	mA
I_C	$3.0 \text{ V} < V_C < 16 \text{ V}$, Gate non-switching	–	2.7	4.0	mA
Shutdown I_{CC}	$V_{CC} = 4.0$	–	500	900	μA

3. Guaranteed by design, not 100% tested in production.

PACKAGE LEAD DESCRIPTION

Package Pin Number	Pin Symbol	Function
SOIC–8		
1	V_{GATE}	Driver pin to gate of external P–Ch FET.
2	PGND	Output power stage ground connection.
3	C_{OSC}	Oscillator frequency programming capacitor.
4	GND	Logic ground.
5	V_{FB}	Feedback voltage input.
6	V_{CC}	Logic supply voltage.
7	CS	Soft–Start and fault timing capacitor.
8	V_C	Driver supply voltage.

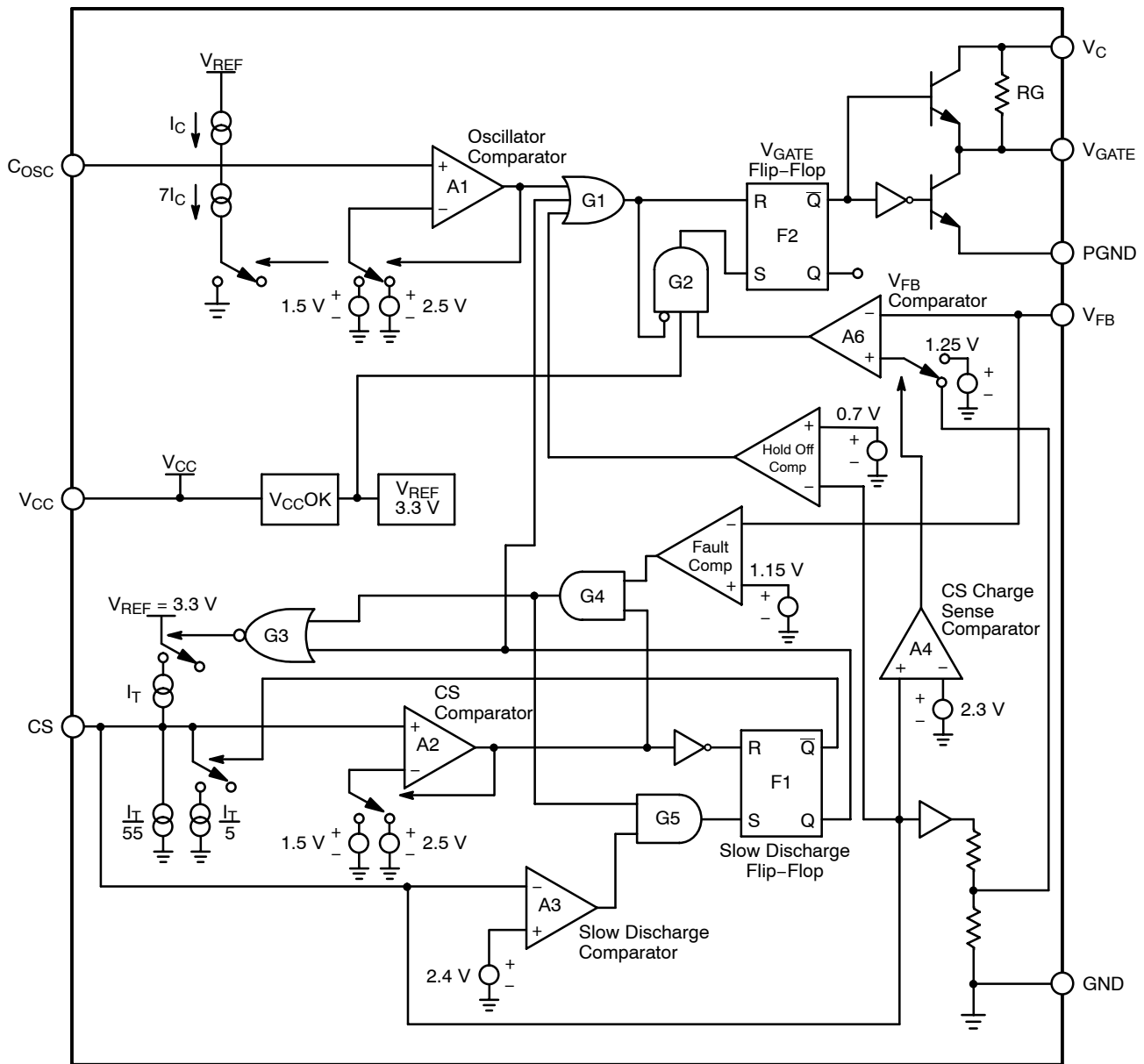


Figure 2. Block Diagram

CIRCUIT DESCRIPTION

THEORY OF OPERATION

Control Scheme

The CS51031 monitors the output voltage to determine when to turn on the P-Ch FET. If V_{FB} falls below the internal reference voltage of 1.25 V during the oscillator's charge cycle, the P-Ch FET is turned on and remains on for the

duration of the charge time. The P-Ch FET gets turned off and remains off during the oscillator's discharge time with the maximum duty cycle to 80%. It requires 7.0 mV typical, and 20 mV maximum ripple on the V_{FB} pin is required to operate. This method of control does not require any loop stability compensation.

Startup

The CS51031 has an externally programmable Soft-Start feature that allows the output voltage to come up slowly, preventing voltage overshoot on the output.

At startup, the voltage on all pins is zero. As V_{CC} rises, the V_C voltage along with the internal resistor R_G keeps the P-Ch FET off. As V_{CC} and V_C continue to rise, the oscillator capacitor (C_{OSC}) and the Soft-Start/Fault Timing capacitor (CS) charges via internal current sources. C_{OSC} gets charged by the current source I_C and CS gets charged by the I_T source combination described by:

$$I_{CS} = I_T - \left(\frac{I_T}{55} + \frac{I_T}{5} \right)$$

The internal Holdoff Comparator ensures that the external P-Ch FET is off until $V_{CS} > 0.7$ V, preventing the GATE flip-flop (F2) from being set. This allows the oscillator to reach its operating frequency before enabling the drive output. Soft-Start is obtained by clamping the V_{FB} comparator's (A6) reference input to approximately 1/2 of the voltage at the CS pin during startup, permitting the control loop and the output voltage to slowly increase. Once the CS pin charges above the Holdoff Comparator trip point of 0.7 V, the low feedback to the V_{FB} Comparator sets the GATE flip-flop during C_{OSC} 's charge cycle. Once the GATE flip-flop is set, V_{GATE} goes low and turns on the P-Ch FET. When V_{CS} exceeds 2.3 V, the CS charge sense

comparator (A4) sets the V_{FB} comparator reference to 1.25 V completing the startup cycle.

Lossless Short Circuit Protection

The CS51031 has "lossless" short circuit protection since there is no current sense resistor required. When the voltage at the CS pin (the fault timing capacitor voltage) reaches 2.5 V during startup, the fault timing circuitry is enabled by A2. During normal operation the CS voltage is 2.6 V. During a short circuit or a transient condition, the output voltage moves lower and the voltage at V_{FB} drops. If V_{FB} drops below 1.15 V, the output of the fault comparator goes high and the CS51031 goes into a fast discharge mode. The fault timing capacitor, CS, discharges to 2.4 V. If the V_{FB} voltage is still below 1.15 V when the CS pin reaches 2.4 V, a valid fault condition has been detected. The slow discharge comparator output goes high and enables gate G5 which sets the slow discharge flip-flop. The V_{GATE} flip-flop resets and the output switch is turned off. The fault timing capacitor is slowly discharged to 1.5 V. The CS51031 then enters a normal startup routine. If the fault is still present when the fault timing capacitor voltage reaches 2.5 V, the fast and slow discharge cycles repeat as shown in figure 3.

If the V_{FB} voltage is above 1.15 V when CS reaches 2.4 V a fault condition is not detected, normal operation resumes and CS charges back to 2.6 V. This reduces the chance of erroneously detecting a load transient as a fault condition.

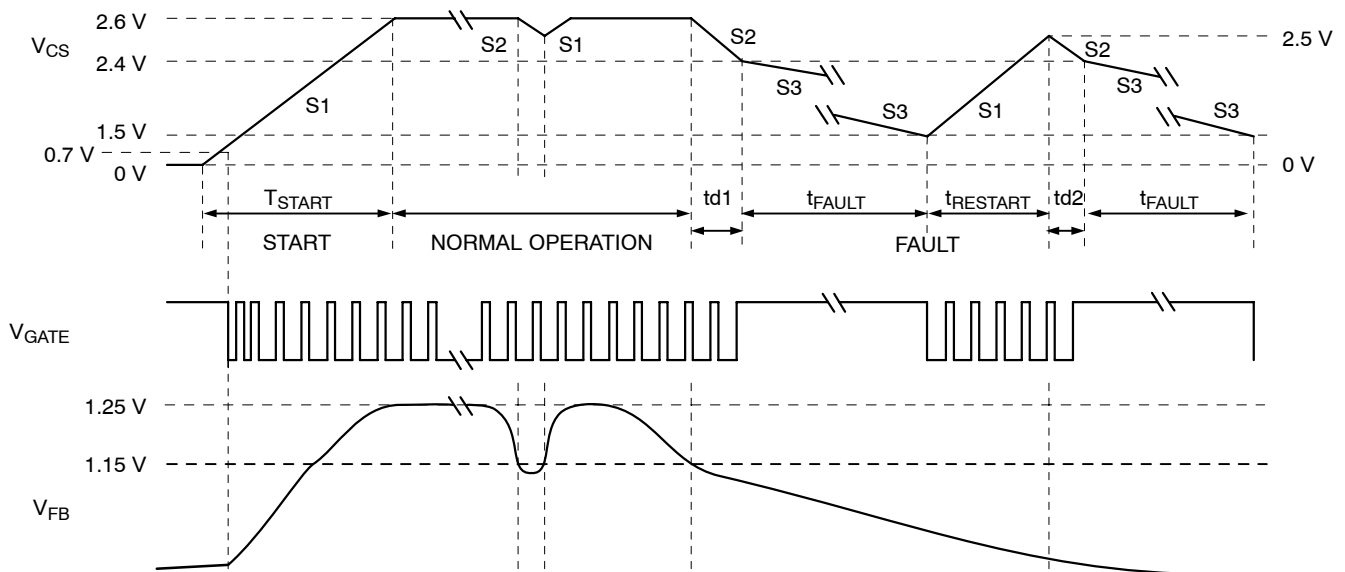


Figure 3. Voltage on Start Capacitor (V_{GS}), the Gate (V_{GATE}), and in the Feedback Loop (V_{FB}), During Startup, Normal and Fault Conditions

Buck Regulator Operation

A block diagram of a typical buck regulator is shown in Figure 4. If we assume that the output transistor is initially off, and the system is in discontinuous operation, the inductor current I_L is zero and the output voltage is at its nominal value. The current drawn by the load is supplied by the output capacitor C_O . When the voltage across C_O drops below the threshold established by the feedback resistors R_1

and R_2 and the reference voltage V_{REF} , the power transistor Q_1 switches on and current flows through the inductor to the output. The inductor current rises at a rate determined by $(V_{IN} - V_{OUT})/L$. The duty cycle (or “on” time) for the CS51031 is limited to 80%. If output voltage remains higher than nominal during the entire C_{OSC} change time, the Q_1 does not turn on, skipping the pulse.

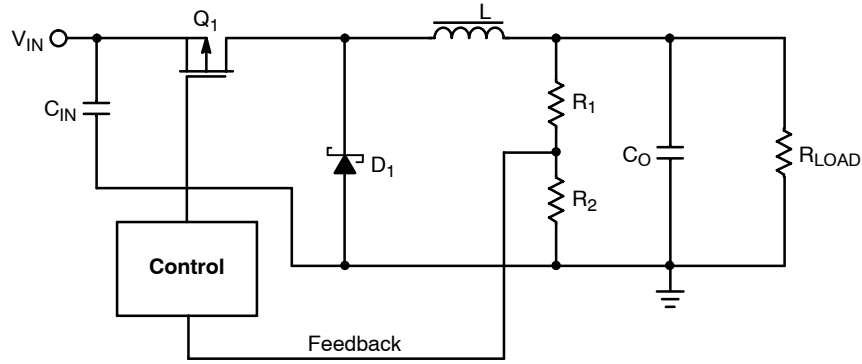


Figure 4. Buck Regulator Block Diagram

APPLICATIONS INFORMATION

CS51031 DESIGN EXAMPLE

Specifications 12 V to 5.0 V, 3.0 A Buck Controller

- $V_{IN} = 12\text{ V} \pm 20\%$ (i.e. 14.4 V max, 12 V nom, 9.6 V min)
- $V_{OUT} = 5.0\text{ V} \pm 2\%$
- $I_{OUT} = 0.3\text{ A to } 3.0\text{ A}$
- Output ripple voltage < 50 mV max
- Efficiency > 80%
- $f_{SW} = 200\text{ kHz}$

1) Duty Cycle Estimates

Since the maximum duty cycle D , of the CS51031 is limited to 80% min, it is necessary to estimate the duty cycle for the various input conditions over the complete operating range.

The duty cycle for a buck regulator operating in a continuous conduction mode is given by:

$$D = \frac{V_{OUT} + V_F}{V_{IN} - V_{SAT}}$$

where:

$V_{SAT} = R_{DS(ON)} \times I_{OUT\text{ max}}$ and $R_{DS(ON)}$ is the value at $T_J 100^\circ\text{C}$.

If $V_F = 0.60\text{ V}$ and $V_{SAT} = 0.60\text{ V}$ then the above equation becomes:

$$D_{MAX} = \frac{5.6}{9.0} = 0.62$$

$$D_{MIN} = \frac{5.6}{13.8} = 0.40$$

2) Switching Frequency and On and Off Time Calculations

Given that $f_{SW} = 200\text{ kHz}$ and $D_{MAX} = 0.80$

$$T = \frac{1.0}{f_{SW}} = 5.0\text{ }\mu\text{s}$$

$$T_{ON(max)} = T \times D_{MAX} = 5.0\text{ }\mu\text{s} \times 0.62 \cong 3.0\text{ }\mu\text{s}$$

$$T_{ON(min)} = T \times D_{MIN} = 5.0\text{ }\mu\text{s} \times 0.40 \cong 2.0\text{ }\mu\text{s}$$

$$T_{OFF(max)} = T_{ON(min)} = 5.0\text{ }\mu\text{s} - 2.0\text{ }\mu\text{s} = 3.0\text{ }\mu\text{s}$$

3) Oscillator Capacitor Selection

The switching frequency is set by C_{OSC} , whose value is given by:

$$C_{OSC}\text{ in pF} = \frac{95 \times 10 + 6}{f_{SW} \left(1 + \frac{f_{SW}}{3 \times 10^6} - \left(\frac{30 \times 10^3}{f_{SW}} \right)^2 \right)}$$

4) Inductor Selection

The inductor value is chosen for continuous mode operation down to 0.3 Amps.

The ripple current $\Delta I = 2 \times I_{OUTmin} = 2 \times 0.3 \text{ A} = 0.6 \text{ A}$.

$$L_{min} = \frac{(V_{OUT} + V_D) \times T_{OFF(max)}}{\Delta I} = \frac{5.6 \text{ V} \times 3.0 \mu\text{s}}{0.6 \text{ A}} = 28 \mu\text{H}$$

This is the minimum value of inductor to keep the ripple current < 0.6 A during normal operation.

A smaller inductor will result in larger ripple current. Ripple current at a minimum off time is:

$$\Delta I = \frac{(V_{OUT} + V_F) \times T_{OFF(min)}}{L_{MIN}} = \frac{5.6 \text{ V} \times 2.0 \mu\text{s}}{28 \mu\text{H}} = 0.4 \text{ A}$$

The core must not saturate with the maximum expected current, here given by:

$$I_{MAX} = I_{OUT} + \Delta I/2 = 3.0 \text{ A} + 0.4 \text{ A}/2 = 3.2 \text{ A}$$

5) Output Capacitor

The output capacitor and the inductor form a low pass filter. The output capacitor should have a low ESL and ESR. Low impedance aluminum electrolytic, tantalum or organic semiconductor capacitors are a good choice for an output capacitor. Low impedance aluminum are less expensive. Solid tantalum chip capacitors are available from a number of suppliers and are the best choice for surface mount applications.

The output capacitor limits the output ripple voltage. The CS51031 needs a maximum of 20 mV of output ripple for the feedback comparator to change state. If we assume that all the inductor ripple current flows through the output capacitor and that it is an ideal capacitor (i.e. zero ESR), the minimum capacitance needed to limit the output ripple to 50 mV peak-to-peak is given by:

$$C = \frac{\Delta I}{8.0 \times f_{SW} \times \Delta V} = \frac{0.6 \text{ A}}{8.0 \times (200 \times 10^3 \text{ Hz}) \times (50 \times 10^{-3} \text{ V})} = 7.5 \mu\text{F}$$

The minimum ESR needed to limit the output voltage ripple to 50 mV peak-to-peak is:

$$ESR = \frac{\Delta V}{\Delta I} = \frac{50 \times 10^{-3}}{0.6 \text{ A}} = 83 \text{ m}\Omega$$

The output capacitor should be chosen so that its ESR is less than 83 mΩ.

During the minimum off time, the ripple current is 0.4 A and the output voltage ripple will be:

$$\Delta V = ESR \times \Delta I = 83 \text{ m}\Omega \times 0.4 = 33 \text{ mV}$$

6) V_{FB} Divider

$$V_{OUT} = 1.25 \text{ V} \left(\frac{R1 + R2}{R2} \right) = 1.25 \text{ V} \left(\frac{R1}{R2} + 1.0 \right)$$

The input bias current to the comparator is 4.0 μA. The resistor divider current should be considerably higher than this to ensure that there is sufficient bias current. If we choose the divider current to be at least 250 times the bias current this permits a divider current of 1.0 mA and simplifies the calculations.

$$\frac{5.0 \text{ V}}{1.0 \text{ mA}} = R1 + R2 = 5.0 \text{ K}\Omega$$

Let $R2 = 1.0 \text{ K}$

Rearranging the divider equation gives:

$$R1 = R2 \left(\frac{V_{OUT}}{1.25} - 1.0 \right) = 1.0 \text{ k}\Omega \left(\frac{5.0 \text{ V}}{1.25} - 1.0 \right) = 3.0 \text{ k}\Omega$$

7) Divider Bypass Capacitor C_{RR}

Since the feedback resistors divide the output voltage by a factor of 4.0, i.e. $5.0 \text{ V}/1.25 \text{ V} = 4.0$, it follows that the output ripple is also divided by four. This would require that the output ripple be at least 60 mV ($4.0 \times 15 \text{ mV}$) to trip the feedback comparator. We use a capacitor C_{RR} to act as an AC short.

The ripple voltage frequency is equal to the switching frequency so we choose $C_{RR} = 1.0 \text{ nF}$.

8) Soft-Start and Fault Timing Capacitor CS

CS performs several important functions. First it provides a delay time for load transients so that the IC does not enter a fault mode every time the load changes abruptly. Secondly it disables the fault circuitry during startup, it also provides Soft-Start by clamping the reference voltage during startup, allowing it to rise slowly, and, finally it controls the hiccup short circuit protection circuitry. This reduces the duty cycle to approximately 0.035 during short circuit conditions.

An important consideration in calculating CS is that its voltage does not reach 2.5 V (the voltage at which the fault detect circuitry is enabled) before V_{FB} reaches 1.15 V otherwise the power supply will never start.

If the V_{FB} pin reaches 1.15 V, the fault timing comparator will discharge CS and the supply will not start. For the V_{FB} voltage to reach 1.15 V the output voltage must be at least $4 \times 1.15 = 4.6 \text{ V}$.

If we choose an arbitrary startup time of 900 μs, the value of CS is:

$$t_{Startup} = \frac{CS \times 2.5 \text{ V}}{I_{Charge}}$$

$$CS_{min} = \frac{900 \mu\text{s} \times 264 \mu\text{A}}{2.5 \text{ V}} = 950 \text{ nF} \approx 0.1 \mu\text{F}$$

The fault time is the sum of the slow discharge time the fast discharge time and the recharge time. It is dominated by the slow discharge time.

The first parameter is the slow discharge time, it is the time for the CS capacitor to discharge from 2.4 V to 1.5 V and is given by:

$$t_{\text{SlowDischarge}}(t) = \frac{CS \times (2.4 \text{ V} - 1.5 \text{ V})}{I_{\text{Discharge}}}$$

where $I_{\text{Discharge}}$ is 6.0 μA typical.

$$t_{\text{SlowDischarge}}(t) = CS \times 1.5 \times 10^5$$

The fast discharge time occurs when a fault is first detected. The CS capacitor is discharged from 2.5 V to 2.4 V.

$$t_{\text{FastDischarge}}(t) = \frac{CS \times (2.5 \text{ V} - 2.4 \text{ V})}{I_{\text{FastDischarge}}}$$

where $I_{\text{FastDischarge}}$ is 66 μA typical.

$$t_{\text{FastDischarge}}(t) = CS \times 1515$$

The recharge time is the time for CS to charge from 1.5 V to 2.5 V.

$$t_{\text{Charge}}(t) = \frac{CS \times (2.5 \text{ V} - 1.5 \text{ V})}{I_{\text{Charge}}}$$

where I_{Charge} is 264 μA typical.

$$t_{\text{Charge}}(t) = CS \times 3787$$

The fault time is given by:

$$t_{\text{Fault}} = CS \times (3787 + 1515 + 1.5 \times 10^5)$$

$$t_{\text{Fault}} = CS \times (1.55 \times 10^5)$$

For this circuit

$$t_{\text{Fault}} = 0.1 \times 10^{-6} \times 1.55 \times 10^5 = 15.5 \mu\text{s}$$

A larger value of CS will increase the fault time out time but will also increase the Soft-Start time.

9) Input Capacitor

The input capacitor reduces the peak currents drawn from the input supply and reduces the noise and ripple voltage on

the V_{CC} and V_C pins. This capacitor must also ensure that the V_{CC} remains above the UVLO voltage in the event of an output short circuit. A low ESR capacitor of at least 100 μF is good. A ceramic surface mount capacitor should also be connected between V_{CC} and ground to filter high frequency noise.

10) MOSFET Selection

The CS51031 drives a P-Channel MOSFET. The V_{GATE} pin swings from GND to V_C . The type of P-Ch FET used depends on the operating conditions but for input voltages below 7.0 V a logic level FET should be used.

A P-Ch FET with a continuous drain current (I_D) rating greater than the maximum output current is required.

The Gate-to-Source voltage V_{GS} and the Drain-to-Source Breakdown Voltage should be chosen based on the input supply voltage.

The power dissipation due to the conduction losses is given by:

$$P_D = I_{\text{OUT}}^2 \times R_{\text{DS(ON)}} \times D$$

where

$R_{\text{DS(ON)}}$ is the value at $T_J = 100^\circ\text{C}$

The power dissipation of the P-Ch FET due to the switching losses is given by:

$$P_D = 0.5 \times V_{\text{IN}} \times I_{\text{OUT}} \times (t_r) \times f_{\text{SW}}$$

where t_r = Rise Time.

11) Diode Selection

The flyback or catch diode should be a Schottky diode because of its fast switching ability and low forward voltage drop. The current rating must be at least equal to the maximum output current. The breakdown voltage should be at least 20 V for this 12 V application.

The diode power dissipation is given by:

$$P_D = I_{\text{OUT}} \times V_D \times (1.0 - D_{\text{min}})$$

CS51031

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping [†]
CS51031YD8	-40°C < T _A < 85°C	SOIC-8	95 Units/Rail
CS51031YDR8		SOIC-8	2500 Tape & Reel
CS51031GD8	0°C < T _A < 70°C	SOIC-8	95 Units/Rail
CS51031GD8G		SOIC-8 (Pb-Free)	95 Units/Rail
CS51031GDR8		SOIC-8	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE THERMAL DATA

Parameter		SOIC-8	Unit
R _{θJC}	Typical	45	°C/W
R _{θJA}	Typical	165	°C/W

CS51033

Fast P-Ch FET Buck Controller

The CS51033 is a switching controller for use in DC-DC converters. It can be used in the buck topology with a minimum number of external components. The CS51033 consists of a 1.0 A power driver for controlling the gate of a discrete P-Channel transistor, fixed frequency oscillator, short circuit protection timer, programmable Soft-Start, precision reference, fast output voltage monitoring comparator, and output stage driver logic with latch.

The high frequency oscillator allows the use of small inductors and output capacitors, minimizing PC board area and systems cost. The programmable Soft-Start reduces current surges at start up. The short circuit protection timer significantly reduces the P-Ch FET duty cycle to approximately 1/30 of its normal cycle during short circuit conditions.

Features

- Pb-Free Package is Available
- 1.0 A Totem Pole Output Driver
- High Speed Oscillator (700 kHz max)
- No Stability Compensation Required
- Lossless Short Circuit Protection
- 2.0% Precision Reference
- Programmable Soft-Start
- Wide Ambient Temperature Range:
 - ♦ Industrial Grade: -40°C to 85°C
 - ♦ Commercial Grade: 0°C to 70°C



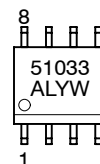
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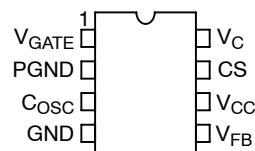
**SOIC-8
D SUFFIX
CASE 751**

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 47 of this data sheet.

CS51033

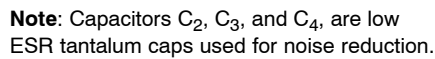


Figure 1. Typical Application Diagram

MAXIMUM RATINGS

Rating		Value	Unit
Power Supply Voltage, V_{CC}		5.0	V
Driver Supply Voltage, V_C		20	V
Driver Output Voltage, V_{GATE}		20	V
C_{OSC} , CS, V_{FB} (Logic Pins)		5.0	V
Peak Output Current		1.0	A
Steady State Output Current		200	mA
Operating Junction Temperature, T_J		150	°C
Storage Temperature Range, T_S		−65 to 150	°C
ESD (Human Body Model)		2.0	kV
Package Thermal Resistance:	Junction-to-Case, $R_{\theta JC}$ Junction-to-Ambient, $R_{\theta JA}$	45 165	°C/W °C/W
Lead Temperature Soldering:	Reflow (SMD styles only) (Note 4)	230 peak	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

4. 60 sec. max above 183°C.

ELECTRICAL CHARACTERISTICS (Specifications apply for $3.135 \leq V_{CC} \leq 3.465$, $3.0 \text{ V} \leq V_C \leq 16 \text{ V}$;Industrial Grade: $-40^\circ\text{C} < T_A < 85^\circ\text{C}$; $-40^\circ\text{C} < T_J < 125^\circ\text{C}$; Commercial Grade: $0^\circ\text{C} < T_A < 70^\circ\text{C}$; $0^\circ\text{C} < T_J < 125^\circ\text{C}$, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Oscillator $V_{FB} = 1.2 \text{ V}$					
Frequency	$C_{OSC} = 470 \text{ pF}$	160	200	240	kHz
Charge Current	$1.4 \text{ V} < V_{COSC} < 2.0 \text{ V}$	–	110	–	μA
Discharge Current	$2.7 \text{ V} > V_{COSC} > 2.0 \text{ V}$	–	660	–	μA
Maximum Duty Cycle	$1 - (t_{OFF}/t_{ON})$	80.0	83.3	–	%

Short Circuit Timer $V_{FB} = 1.0 \text{ V}$; $CS = 0.1 \mu\text{F}$; $V_{COSC} = 2.0 \text{ V}$					
Charge Current	$1.0 \text{ V} < V_{CS} < 2.0 \text{ V}$	175	264	325	μA
Fast Discharge Current	$2.55 \text{ V} > V_{CS} > 2.4 \text{ V}$	40	66	80	μA
Slow Discharge Current	$2.4 \text{ V} > V_{CS} > 1.5 \text{ V}$	4.0	6.0	10	μA
Start Fault Inhibit Time	–	0.70	0.85	1.40	ms
Valid Fault Time	$2.6 \text{ V} > V_{CS} > 2.4 \text{ V}$	0.2	0.3	0.45	ms
GATE Inhibit Time	$2.4 \text{ V} > V_{CS} > 1.5 \text{ V}$	9.0	15	23	ms
Duty Cycle	–	2.5	3.1	4.6	%

CS Comparator $V_{FB} = 1.0 \text{ V}$					
Fault Enable CS Voltage	–	–	2.5	–	V
Max CS Voltage	$V_{FB} = 1.5 \text{ V}$	–	2.6	–	V
Fault Detect Voltage	V_{CS} when GATE goes high	–	2.4	–	V
Fault Inhibit Voltage	Minimum V_{CS}	–	1.5	–	V
Hold Off Release Voltage	$V_{FB} = 0 \text{ V}$	0.4	0.7	1.0	V
Regulator Threshold Voltage Clamp	$V_{CS} = 1.5 \text{ V}$	0.725	0.866	1.035	V

V_{FB} Comparators $V_{COSC} = V_{CS} = 2.0 \text{ V}$					
Regulator Threshold Voltage	$T_J = 25^\circ\text{C}$ (Note 5)	1.225	1.250	1.275	V
	$T_J = -40$ to 125°C	1.210	1.250	1.290	V
Fault Threshold Voltage	$T_J = 25^\circ\text{C}$ (Note 5)	1.12	1.15	1.17	V
	$T_J = -40$ to 125°C	1.10	1.15	1.19	V
Threshold Line Regulation	$3.135 \text{ V} \leq V_{CC} \leq 3.465$	–	6.0	15	mV
Input Bias Current	$V_{FB} = 0 \text{ V}$	–	1.0	4.0	μA
Voltage Tracking	(Regulator Threshold – Fault Threshold Voltage)	70	100	120	mV
Input Hysteresis Voltage	–	–	4.0	20	mV

Power Stage $V_C = 10 \text{ V}$; $V_{FB} = 1.2 \text{ V}$					
GATE DC Low Saturation Voltage	$V_{COSC} = 1.0 \text{ V}$; 200 mA Sink	–	1.2	1.5	V
GATE DC High Saturation Voltage	$V_{COSC} = 2.7 \text{ V}$; 200 mA Source; $V_C = V_{GATE}$	–	1.5	2.1	V
Rise Time	$C_{GATE} = 1.0 \text{ nF}$; $1.5 \text{ V} < V_{GATE} < 9.0 \text{ V}$	–	25	60	ns
Fall Time	$C_{GATE} = 1.0 \text{ nF}$; $9.0 \text{ V} > V_{GATE} > 1.5 \text{ V}$	–	25	60	ns

Current Drain					
I_{CC}	$3.135 \text{ V} < V_{CC} < 3.465 \text{ V}$, Gate switching	–	3.5	6.0	mA
I_C	$3.0 \text{ V} < V_C < 16 \text{ V}$, Gate non-switching	–	2.7	4.0	mA

5. Guaranteed by design, not 100% tested in production.

PACKAGE PIN DESCRIPTION

Pin Number	Pin Symbol	Function
1	V _{GATE}	Driver pin to gate of external P-Ch FET.
2	PGND	Output power stage ground connection.
3	C _{OSC}	Oscillator frequency programming capacitor.
4	GND	Logic ground.
5	V _{FB}	Feedback voltage input.
6	V _{CC}	Logic supply voltage.
7	CS	Soft-Start and fault timing capacitor.
8	V _C	Driver supply voltage.

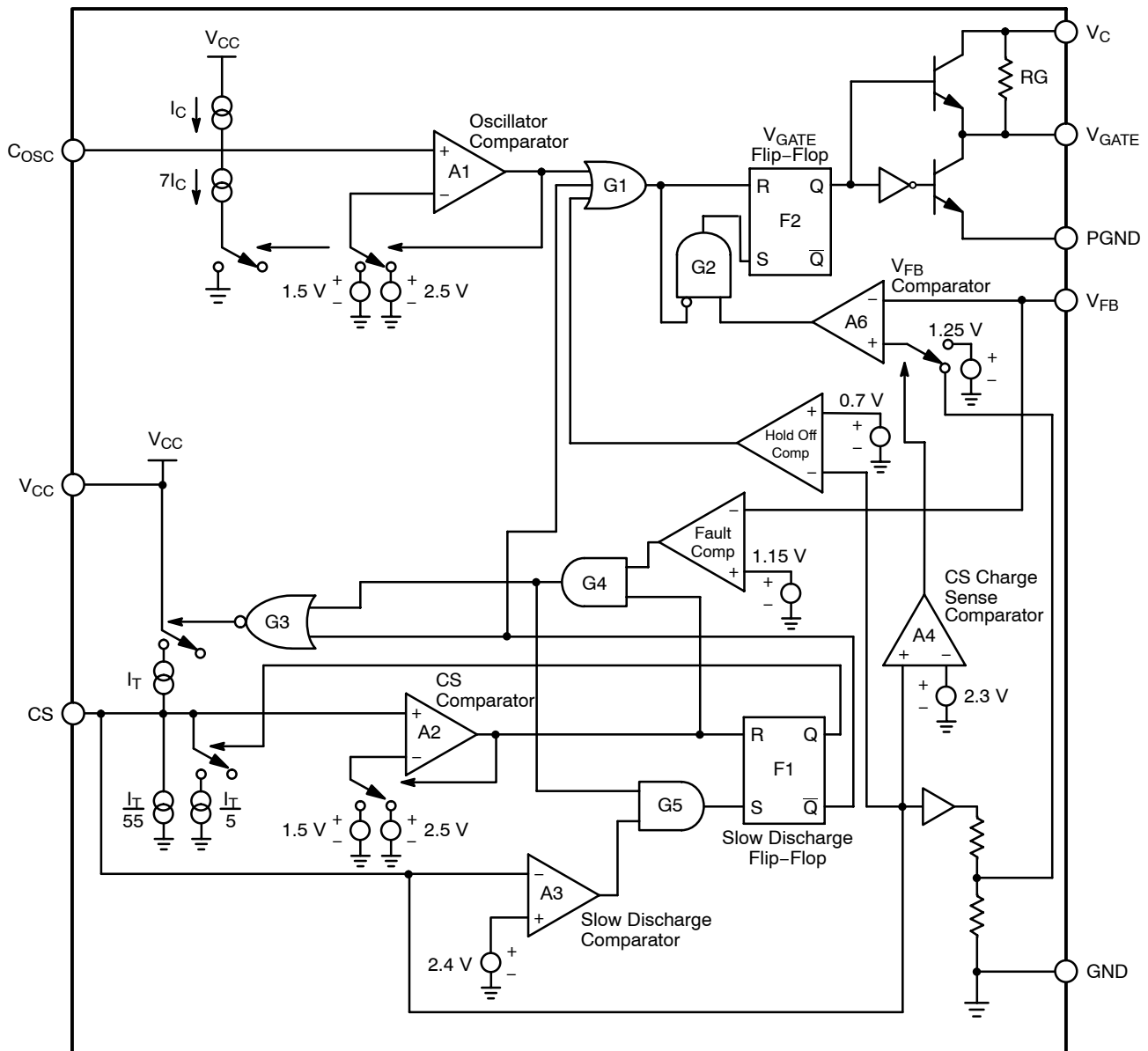


Figure 2. Block Diagram

CIRCUIT DESCRIPTION

THEORY OF OPERATION

Control Scheme

The CS51033 monitors the output voltage to determine when to turn on the P–Ch FET. If V_{FB} falls below the internal reference voltage of 1.25 V during the oscillator's charge cycle, the P–Ch FET is turned on and remains on for the duration of the charge time. The P–Ch FET gets turned off and remains off during the oscillator's discharge cycle time with the maximum duty cycle to 80%. It requires 7.0 mV typical, and 20 mV maximum ripple on the V_{FB} pin to operate. This method of control does not require any loop stability compensation.

Startup

The CS51033 has an externally programmable Soft–Start feature that allows the output voltage to come up slowly, preventing voltage overshoot on the output.

At startup, the voltage on all pins is zero. As V_{CC} rises, the V_C voltage along with the internal resistor R_G keeps the P–Ch FET off. As V_{CC} and V_C continue to rise, the oscillator capacitor (C_{OSC}) and the Soft–Start/Fault Timing capacitor (CS) charges via internal current sources. C_{OSC} gets charged by the current source I_C and CS gets charged by the I_T source combination described by:

$$I_{CS} = I_T - \left(\frac{I_T}{55} + \frac{I_T}{5} \right)$$

The internal Holdoff Comparator ensures that the external P–Ch FET is off until $V_{CS} > 0.7$ V, preventing the GATE flip–flop (F2) from being set. This allows the oscillator to reach its operating frequency before enabling the drive output. Soft–Start is obtained by clamping the V_{FB} comparator's (A6) reference input to approximately 1/2 of the voltage at the CS pin during startup, permitting the

control loop and the output voltage to slowly increase. Once the CS pin charges above the Holdoff Comparator trip point of 0.7 V, the low feedback to the V_{FB} Comparator sets the GATE flip–flop during C_{OSC} 's charge cycle. Once the GATE flip–flop is set, V_{GATE} goes low and turns on the P–Ch FET. When V_{CS} exceeds 2.4 V, the CS charge sense comparator (A4) sets the V_{FB} comparator reference to 1.25 V completing the startup cycle.

Lossless Short Circuit Protection

The CS51033 has “lossless” short circuit protection since there is no current sense resistor required. When the voltage at the CS pin (the fault timing capacitor voltage) reaches 2.5 V, the fault timing circuitry is enabled. During normal operation the CS voltage is 2.6 V. During a short circuit or a transient condition, the output voltage moves lower and the voltage at V_{FB} drops. If V_{FB} drops below 1.15 V, the output of the fault comparator goes high and the CS51033 goes into a fast discharge mode. The fault timing capacitor, CS, discharges to 2.4 V. If the V_{FB} voltage is still below 1.15 V when the CS pin reaches 2.4 V, a valid fault condition has been detected. The slow discharge comparator output goes high and enables gate G5 which sets the slow discharge flip–flop. The V_{GATE} flip–flop resets and the output switch is turned off. The fault timing capacitor is slowly discharged to 1.5 V. The CS51033 then enters a normal startup routine. If the fault is still present when the fault timing capacitor voltage reaches 2.5 V, the fast and slow discharge cycles repeat as shown in Figure 3.

If the V_{FB} voltage is above 1.15 V when CS reaches 2.4 V a fault condition is not detected, normal operation resumes and CS charges back to 2.6 V. This reduces the chance of erroneously detecting a load transient as a fault condition.

CS51033

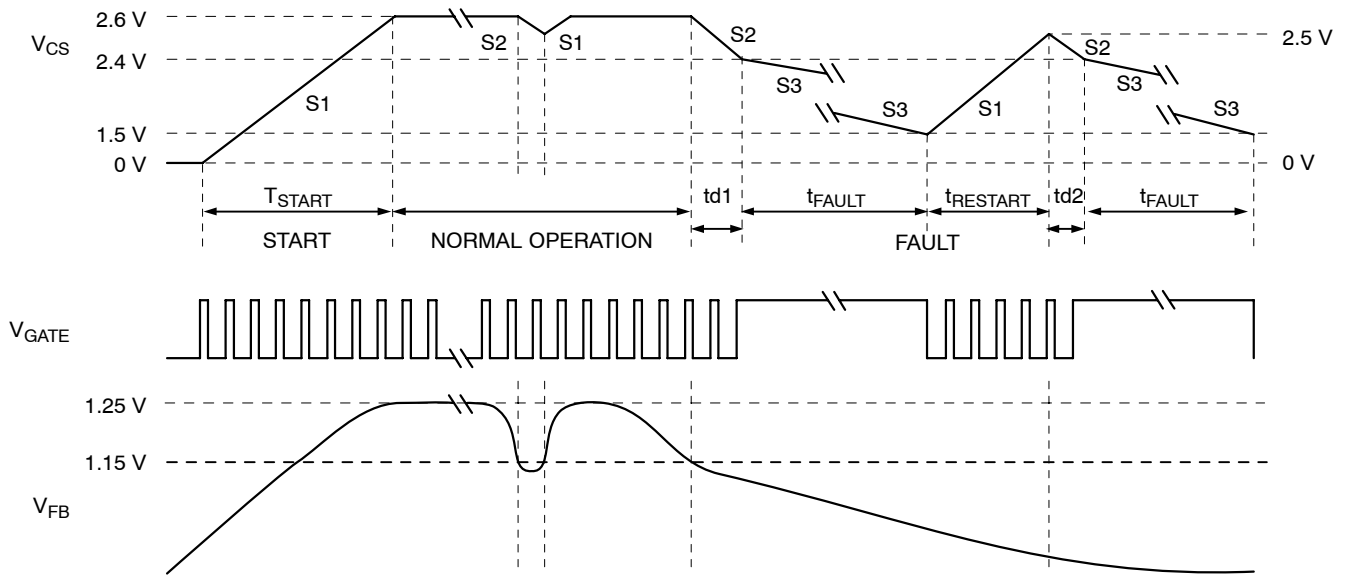


Figure 3. Voltage on Start Capacitor (V_{GS}), the Gate (V_{GATE}), and in the Feedback Loop (V_{FB}), During Startup, Normal and Fault Conditions

Buck Regulator Operation

A block diagram of a typical buck regulator is shown in Figure 4. If we assume that the output transistor is initially off, and the system is in discontinuous operation, the inductor current I_L is zero and the output voltage is at its nominal value. The current drawn by the load is supplied by the output capacitor C_O . When the voltage across C_O drops below the threshold established by the feedback resistors R_1

and R_2 and the reference voltage V_{REF} , the power transistor Q_1 switches on and current flows through the inductor to the output. The inductor current rises at a rate determined by $(V_{IN} - V_{OUT})/Load$. The duty cycle (or “on” time) for the CS51033 is limited to 80%. If output voltage remains higher than nominal during the entire C_{OSC} change time, the Q_1 does not turn on, skipping the pulse.

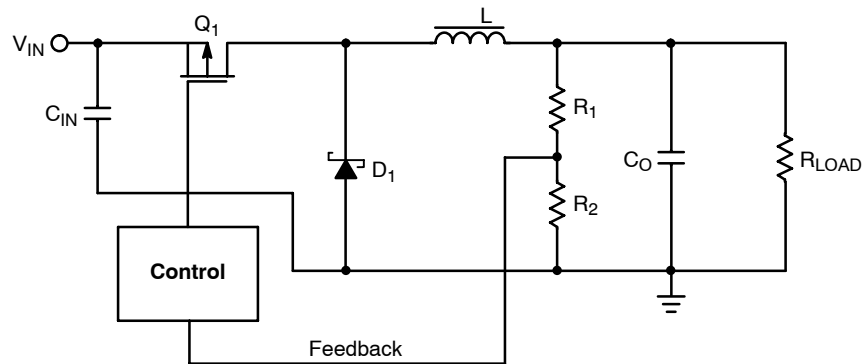


Figure 4. Buck Regulator Block Diagram

Charge Pump Circuit

(Refer to the CS51033 Application Diagram on page 40).

An external charge pump circuit is necessary when the V_C input voltage is below 5.0 V to ensure that there is sufficient gate drive voltage for the external FET. When V_{IN} is applied, capacitors C_1 and C_2 will be charged to a diodes drop below V_{IN} via diodes D_2 and D_4 , respectively. When the P-Ch

FET turns on, its drain voltage will be approximately equal to V_{IN} . Since the voltage across C_1 can not change instantaneously, D_2 is reverse biased and the anode voltage rises to approximately $2.0 \times 3.3 \text{ V} - V_{D2}$. C_1 transfers some of its stored charge C_2 via D_3 . After several cycles there is sufficient gate drive voltage.

APPLICATIONS INFORMATION

DESIGNING A POWER SUPPLY WITH THE CS51033

Specifications

- $V_{IN} = 3.3 \text{ V} \pm 10\%$ (i.e. 3.63 V max., 2.97 V min.)
- $V_{OUT} = 1.5 \text{ V} \pm 2.0\%$
- $I_{OUT} = 0.3 \text{ A to } 3.0 \text{ A}$
- Output ripple voltage < 33 mV.
- $F_{SW} = 200 \text{ kHz}$

1) Duty Cycle Estimates

Since the maximum duty cycle D, of the CS51033 is limited to 80% min., it is best to estimate the duty cycle for the various input conditions to see that the design will work over the complete operating range.

The duty cycle for a buck regulator operating in a continuous conduction mode is given by:

$$D = \frac{V_{OUT} + V_D}{V_{IN} - V_{SAT}}$$

where:

$$V_{SAT} = R_{DS(ON)} \times I_{OUT \text{ Max.}}$$

In this case we can assume that $V_D = 0.6 \text{ V}$ and $V_{SAT} = 0.6 \text{ V}$ so the equation reduces to:

$$D = \frac{V_{OUT}}{V_{IN}}$$

From this, the maximum duty cycle D_{MAX} is 53%, this occurs when V_{IN} is at its minimum while the minimum duty cycle D_{MIN} is 0.35%.

2) Switching Frequency and On and Off Time Calculations

$F_{SW} = 200 \text{ kHz}$. The switching frequency is determined by C_{OSC} , whose value is determined by:

$$C_{OSC} = \frac{95}{F_{SW} \times \left(1 - \left(\frac{F_{SW}}{3 \times 10^6}\right) - \left(\frac{30 \times 10^3}{F_{SW}}\right)^2\right)} \approx 470 \text{ pF}$$

$$T = \frac{1.0}{F_{SW}} = 5.0 \mu\text{s}$$

$$T_{ON(MAX)} = 5.0 \mu\text{s} \times 0.53 = 2.65 \mu\text{s}$$

$$T_{ON(MIN)} = 5.0 \mu\text{s} \times 0.35 = 1.75 \mu\text{s}$$

$$T_{OFF(MAX)} = 5.0 \mu\text{s} - 0.7 \mu\text{s} = 4.3 \mu\text{s}$$

3) Inductor Selection

Pick the inductor value to maintain continuous mode operation down to 0.3 Amps.

The ripple current $\Delta I = 2 \times I_{OUT(MIN)} = 2 \times 0.3 \text{ A} = 0.6 \text{ A}$.

$$L_{MIN} = \frac{V_{OUT} + V_D \times T_{OFF(MAX)}}{\Delta I} = \frac{2.1 \text{ V} \times 4.3 \mu\text{s}}{0.6 \text{ A}} \approx 15 \mu\text{H}$$

The CS51033 will operate with almost any value of inductor. With larger inductors the ripple current is reduced

and the regulator will remain in a continuous conduction mode for lower values of load current. A smaller inductor will result in larger ripple current. The core must not saturate with the maximum expected current, here given by:

$$I_{MAX} = \frac{I_{OUT} + \Delta I}{2.0} = 3.0 \text{ A} + 0.6 \text{ A}/2.0 = 3.3 \text{ A}$$

4) Output Capacitor

The output capacitor limits the output ripple voltage. The CS51033 needs a maximum of 15 mV of output ripple for the feedback comparator to change state. If we assume that all the inductor ripple current flows through the output capacitor and that it is an ideal capacitor (i.e. zero ESR), the minimum capacitance needed to limit the output ripple to 50 mV peak-to-peak is given by:

$$C_O = \frac{\Delta I}{8.0 \times F_{SW} \times \Delta V}$$

$$= \frac{0.6 \text{ A}}{8.0 \times (200 \times 10^3 \text{ Hz}) \times (33 \times 10^{-3} \text{ V})} \approx 11.4 \mu\text{F}$$

The minimum ESR needed to limit the output voltage ripple to 50 mV peak-to-peak is:

$$ESR = \frac{\Delta V}{\Delta I} = \frac{50 \times 10^{-3}}{0.6 \text{ A}} = 55 \text{ m}\Omega$$

The output capacitor should be chosen so that its ESR is at least half of the calculated value and the capacitance is at least ten times the calculated value. It is often advisable to use several capacitors in parallel to reduce ESR.

Low impedance aluminum electrolytic, tantalum or organic semiconductor capacitors are a good choice for an output capacitor. Low impedance aluminum are the cheapest but are not available in surface mount at present. Solid tantalum chip capacitors are available from a number of suppliers and offer the best choice for surface mount applications. The capacitor working voltage should be greater than the output voltage in all cases.

5) V_{FB} Divider

$$V_{OUT} = 1.25 \text{ V} \left(\frac{R_1 + R_2}{R_2} \right) = 1.25 \text{ V} \left(\frac{R_1}{R_2} + 1.0 \right)$$

The input bias current to the comparator is 4.0 μA . The resistor divider current should be considerably higher than this to ensure that there is sufficient bias current. If we choose the divider current to be at least 250 times the bias current this gives a divider current of 1.0 mA and simplifies the calculations.

$$\frac{1.5 \text{ V}}{1.0 \text{ mA}} = R_1 + R_2 = 1.5 \text{ k}\Omega$$

Let $R_2 = 1.0 \text{ k}$

Rearranging the divider equation gives:

$$R_1 = R_2 \left(\frac{V_{OUT}}{1.25} - 1.0 \right) = 1.0 \text{ k}\Omega \left(\frac{1.5 \text{ V}}{1.25} - 1.0 \right) = 200 \Omega$$

6) Divider Bypass Capacitor C_{RR}

Since the feedback resistors divide the output voltage by a factor of 4.0, i.e. $5.0\text{ V}/1.25\text{ V} = 4.0$, it follows that the output ripple is also divided by four. This would require that the output ripple be at least 60 mV ($4.0 \times 15\text{ mV}$) to trip the feedback comparator. We use a capacitor C_{RR} to act as an AC short so that the output ripple is not attenuated by the divider network. The ripple voltage frequency is equal to the switching frequency so we choose C_{RR} so that:

$$X_C = \frac{1.0}{2\pi fC}$$

is negligible at the switching frequency.

In this case F_{SW} is 200 kHz if we allow $X_C = 3.0\ \Omega$ then:

$$C = \frac{1.0}{2\pi f3} \approx 0.265\ \mu\text{F}$$

7) Soft-Start and Fault Timing Capacitor CS

CS performs several important functions. First it provides a dead time for load transients so that the IC does not enter a fault mode every time the load changes abruptly. Secondly it disables the fault circuitry during startup, it also provides Soft-Start by clamping the reference voltage during startup to rise slowly and finally it controls the hiccup short circuit protection circuitry. This function reduces the P-Ch FET's duty cycle to 2.0% of the CS period.

The most important consideration in calculating CS is that it's voltage does not reach 2.5 V (the voltage at which the fault detect circuitry is enabled) before V_{FB} reaches 1.15 V otherwise the power supply will never start.

If the V_{FB} pin reaches 1.15 V , the fault timing comparator will discharge CS and the supply will not start. For the V_{FB} voltage to reach 1.15 V the output voltage must be at least $4 \times 1.15 = 4.6\text{ V}$.

If we choose an arbitrary startup time of $200\ \mu\text{s}$, we calculate the value of CS from:

$$T = \frac{CS \times 2.5\text{ V}}{I_{CHARGE}}$$

$$CS(\text{MIN}) = \frac{200\ \mu\text{s} \times 264\ \mu\text{A}}{2.5\text{ V}} = 0.02\ \mu\text{F}$$

Use $0.1\ \mu\text{F}$.

The fault time out time is the sum of the slow discharge time the fast discharge time and the recharge time and is obviously dominated by the slow discharge time.

The first parameter is the slow discharge time, it is the time for the CS capacitor to discharge from 2.4 V to 1.5 V and is given by:

$$T_{\text{SLOWDISCHARGE}} = \frac{CS \times (2.4\text{ V} - 1.5\text{ V})}{I_{\text{DISCHARGE}}}$$

where $I_{\text{DISCHARGE}}$ is $6.0\ \mu\text{A}$ typical.

$$T_{\text{SLOWDISCHARGE}} = CS \times 1.5\text{ V} \times 10^5$$

The fast discharge time occurs when a fault is first detected. The CS capacitor is discharged from 2.5 V to 2.4 V .

$$T_{\text{FASTDISCHARGE}} = \frac{CS \times (2.5\text{ V} - 2.4\text{ V})}{I_{\text{FASTDISCHARGE}}}$$

where $I_{\text{FASTDISCHARGE}}$ is $66\ \mu\text{A}$ typical.

$$T_{\text{FASTDISCHARGE}} = CS \times 1515$$

The recharge time is the time for CS to charge from 1.5 V to 2.5 V .

$$T_{\text{CHARGE}} = \frac{CS \times (2.5\text{ V} - 1.5\text{ V})}{I_{\text{CHARGE}}}$$

where I_{CHARGE} is $264\ \mu\text{A}$ typical.

$$T_{\text{CHARGE}} = CS \times 3787$$

The fault time out time is given by:

$$T_{\text{FAULT}} = CS \times (3787 + 1515 + 1.5 \times 10^5)$$

$$T_{\text{FAULT}} = CS \times (1.55 \times 10^5)$$

For this circuit

$$T_{\text{FAULT}} = 0.1 \times 10^{-6} \times 1.55 \times 10^5 = 0.0155$$

A larger value of CS will increase the fault time out time but will also increase the Soft-Start time.

8) Input Capacitor

The input capacitor reduces the peak currents drawn from the input supply and reduces the noise and ripple voltage on the V_{CC} and V_C pins. This capacitor must also ensure that the V_{CC} remains above the UVLO voltage in the event of an output short circuit. C_{IN} should be a low ESR capacitor of at least $100\ \mu\text{F}$. A ceramic surface mount capacitor should also be connected between V_{CC} and ground to prevent spikes.

9) MOSFET Selection

The CS51033 drives a P-Channel MOSFET. The V_{GATE} pin swings from GND to V_C . The type of P-Ch FET used depends on the operating conditions but for input voltages below 7.0 V a logic level FET should be used.

Choose a P-Ch FET with a continuous drain current (I_D) rating greater than the maximum output current. $R_{DS(ON)}$ should be less than

$$R_{DS} < = \frac{0.6\text{ V}}{I_{OUT(\text{MAX})}} 167\text{ m}\Omega$$

The Gate-to-Source voltage V_{GS} and the Drain-to-Source Breakdown Voltage should be chosen based on the input supply voltage.

The power dissipation due to the conduction losses is given by:

$$P_D = I_{OUT}^2 \times R_{DS(ON)} \times D$$

The power dissipation due to the switching losses is given by:

$$P_D = 0.5 \times V_{IN} \times I_{OUT} \times (T_{Rf} + T_F) \times F_{SW}$$

where T_R = Rise Time and T_F = Fall Time.

CS51033

10) Diode Selection

The flyback or catch diode should be a Schottky diode because of its fast switching ability and low forward voltage drop. The current rating must be at least equal to the

maximum output current. The breakdown voltage should be at least 20 V for this 12 V application.

The diode power dissipation is given by:

$$P_D = I_{OUT} \times V_D \times (1.0 - D_{MIN})$$

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping [†]
CS51033YD8	-40°C < T _A < 85°C	SOIC-8	95 Units/Rail
CS51033YDR8			2500 Tape & Reel
CS51033YDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel
CS51033GD8	0°C < T _A < 70°C	SOIC-8	95 Units/Rail
CS51033GDR8			2500 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

CS51411, CS51412, CS51413, CS51414

1.5 A, 260 kHz and 520 kHz, Low Voltage Buck Regulators with External Bias or Synchronization Capability

The CS5141X products are 1.5 A buck regulator ICs. These devices are fixed-frequency operating at 260 kHz and 520 kHz. The regulators use the V^2 ™ control architecture to provide unmatched transient response, the best overall regulation and the simplest loop compensation for today's high-speed logic. These products accommodate input voltages from 4.5 V to 40 V.

The CS51411 and CS51413 contain synchronization circuitry. The CS51412 and CS51414 have the option of powering the controller from an external 3.3 V to 6.0 V supply in order to improve efficiency, especially in high input voltage, light load conditions.

The on-chip NPN transistor is capable of providing a minimum of 1.5 A of output current, and is biased by an external “boost” capacitor to ensure saturation, thus minimizing on-chip power dissipation. Protection circuitry includes thermal shutdown, cycle-by-cycle current limiting and frequency foldback. The CS51411 and CS51413 are functionally pin-compatible with the LT1375. The CS51412 and CS51414 are functionally pin-compatible with the LT1376.

Features

- V^2 Architecture Provides Ultrafast Transient Response, Improved Regulation and Simplified Design
- 2.0% Error Amp Reference Voltage Tolerance
- Switch Frequency Decrease of 4:1 in Short Circuit Conditions Reduces Short Circuit Power Dissipation
- BOOST Lead Allows “Bootstrapped” Operation to Maximize Efficiency
- Sync Function for Parallel Supply Operation or Noise Minimization
- Shutdown Lead Provides Power-Down Option
- 85 μ A Quiescent Current During Power-Down
- Thermal Shutdown
- Soft-Start
- Pin-Compatible with LT1375 and LT1376
- Pb-Free Packages are Available



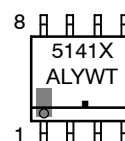
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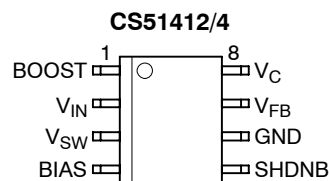
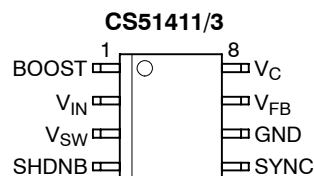
SOIC-8
D SUFFIX
CASE 751

MARKING DIAGRAM



X	= 1, 2, 3 or 4
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
T	= Temperature Range, E or G
▪	= Pb-Free Indicator

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 62 of this data sheet.

CS51411, CS51412, CS51413, CS51414

PRODUCT SELECTION GUIDE

Part Number	Frequency	Temperature Range	Bias/Sync
CS51411E	260 kHz	-40°C to 85°C	Sync
CS51411G	260 kHz	0°C to 70°C	Sync
CS51412E	260 kHz	-40°C to 85°C	Bias
CS51412G	260 kHz	0°C to 70°C	Bias
CS51413E	520 kHz	-40°C to 85°C	Sync
CS51413G	520 kHz	0°C to 70°C	Sync
CS51414E	520 kHz	-40°C to 85°C	Bias
CS51414G	520 kHz	0°C to 70°C	Bias

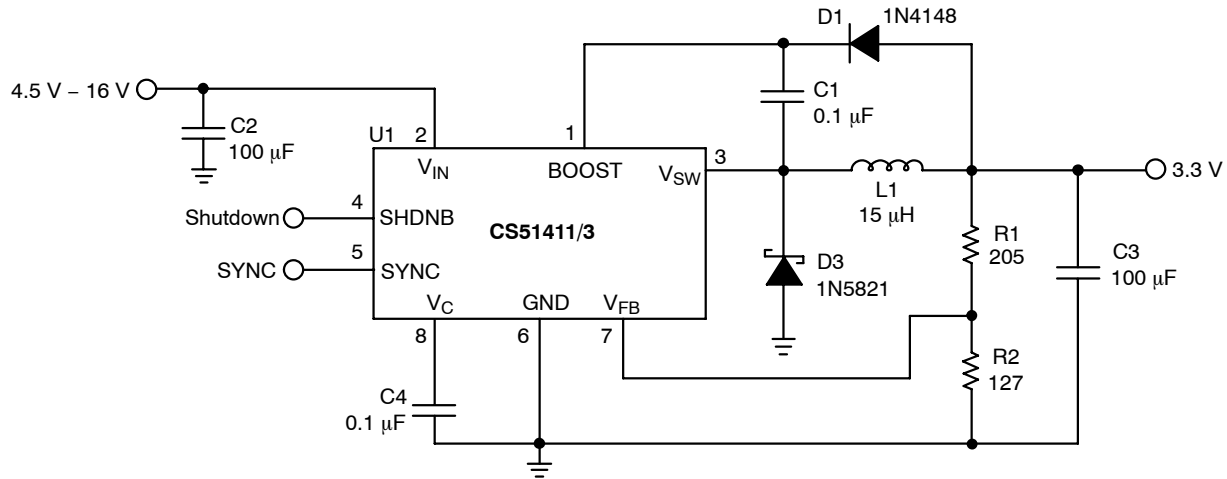


Figure 1. Application Diagram, 4.5 V - 16 V to 3.3 V @ 1.0 A Converter

MAXIMUM RATINGS

Rating	Value	Unit
Operating Junction Temperature Range, T_J	-40 to 150	°C
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1)	230 peak
Storage Temperature Range, T_S	-65 to +150	°C
ESD Damage Threshold (Human Body Model)	2.0	kV

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. 60 second maximum above 183°C.

CS51411, CS51412, CS51413, CS51414

MAXIMUM RATINGS

Pin Name	V _{Max}	V _{MIN}	I _{SOURCE}	I _{SINK}
V _{IN}	40 V	-0.3 V	N/A	4.0 A
BOOST	40 V	-0.3 V	N/A	100 mA
V _{SW}	40 V	-0.6 V/-1.0 V, t < 50 ns	4.0 A	10 mA
V _C	7.0 V	-0.3 V	1.0 mA	1.0 mA
SHDNB	7.0 V	-0.3 V	1.0 mA	1.0 mA
SYNC	7.0 V	-0.3 V	1.0 mA	1.0 mA
BIAS	7.0 V	-0.3 V	1.0 mA	50 mA
V _{FB}	7.0 V	-0.3 V	1.0 mA	1.0 mA
GND	7.0 V	-0.3 V	50 mA	1.0 mA

ELECTRICAL CHARACTERISTICS (-40°C < T_J < 125°C (CS51411E/2E/3E/4E); -40°C < T_A < 85°C (CS51411E/2E/3E/4E); 0°C < T_A < 70°C (CS51411G/2G/3G/4G), 4.5 V < V_{IN} < 40 V; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit

Oscillator

Operating Frequency	CS51411/CS51412	224	260	296	kHz
Operating Frequency	CS51413/CS51414	446	520	594	kHz
Frequency Line Regulation	-	-	0.05	0.15	%/V
Maximum Duty Cycle	-	85	90	95	%
V _{FB} Frequency Foldback Threshold	-	0.29	0.32	0.36	V

PWM Comparator

Slope Compensation Voltage	CS51411/CS51412, Fix V _{FB} , ΔV _C /ΔT _{ON} CS51413/CS51414	8.0 25	17 50	26 75	mV/μs mV/μs
Minimum Output Pulse Width	CS51411/CS51412, V _{FB} to V _{SW} CS51413/CS51414, V _{FB} to V _{SW}	- -	150 -	300 230	ns ns

Power Switch

Current Limit	V _{FB} > 0.36 V	1.6	2.3	3.0	A
Foldback Current	V _{FB} < 0.29 V	0.9	1.5	2.1	A
Saturation Voltage	I _{OUT} = 1.5 A, V _{BOOST} = V _{IN} + 2.5 V	0.4	0.7	1.0	V
Current Limit Delay	(Note 2)	-	120	160	ns

Error Amplifier

Internal Reference Voltage	-	1.244	1.270	1.296	V
Reference PSRR	(Note 2)	-	40	-	dB
FB Input Bias Current	-	-	0.02	0.1	μA
Output Source Current	V _C = 1.270 V, V _{FB} = 1.0 V	15	25	35	μA
Output Sink Current	V _C = 1.270 V, V _{FB} = 2.0 V	15	25	35	μA
Output High Voltage	V _{FB} = 1.0 V	1.39	1.46	1.53	V
Output Low Voltage	V _{FB} = 2.0 V	5.0	20	60	mV
Unity Gain Bandwidth	(Note 2)	-	500	-	kHz
Open Loop Amplifier Gain	(Note 2)	-	70	-	dB
Amplifier Transconductance	(Note 2)	-	6.4	-	mA/V

2. Guaranteed by design, not 100% tested in production.

CS51411, CS51412, CS51413, CS51414

ELECTRICAL CHARACTERISTICS (continued) ($-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$ (CS51411E/2E/3E/4E); $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ (CS51411E/2E/3E/4E); $0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$ (CS51411G/2G/3G/4G), $4.5\text{ V} < V_{IN} < 40\text{ V}$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Sync					
Sync Frequency Range	CS51411/CS51412	305	–	470	kHz
Sync Frequency Range	CS51413/CS51414	575	–	880	kHz
Sync Pin Bias Current	$V_{SYNC} = 0\text{ V}$ $V_{SYNC} = 5.0\text{ V}$	– 250	0.1 360	0.2 460	μA μA
Sync Threshold Voltage	–	1.0	1.5	1.9	V

Shutdown

Shutdown Threshold Voltage	–	1.0	1.3	1.6	V
Shutdown Pin Bias Current	$V_{SHDNB} = 0\text{ V}$	0.14	5.00	35	μA

Thermal Shutdown

Overtemperature Trip Point	(Note 3)	175	185	195	$^{\circ}\text{C}$
Thermal Shutdown Hysteresis	(Note 3)	–	42	–	$^{\circ}\text{C}$

General

Quiescent Current	$I_{SW} = 0\text{ A}$	3.0	4.0	6.25	mA
Shutdown Quiescent Current	$V_{SHDNB} = 0\text{ V}$	8.0	20	85	μA
Boost Operating Current	$V_{BOOST} - V_{SW} = 2.5\text{ V}$	6.0	15	40	mA/A
Minimum Boost Voltage	(Note 3)	–	–	2.5	V
Startup Voltage	–	2.2	3.3	4.4	V
Minimum Output Current	–	–	7.0	12	mA

3. Guaranteed by design, not 100% tested in production.

PACKAGE PIN DESCRIPTION

Package Pin #	Pin Symbol	Function
1	BOOST	The BOOST pin provides additional drive voltage to the on-chip NPN power transistor. The resulting decrease in switch on voltage increases efficiency.
2	V_{IN}	This pin is the main power input to the IC.
3	V_{SW}	This is the connection to the emitter of the on-chip NPN power transistor and serves as the switch output to the inductor. This pin may be subjected to negative voltages during switch off-time. A catch diode is required to clamp the pin voltage in normal operation. This node can stand -1.0 V for less than 50 ns during switch node flyback.
4 (CS51412/CS51414)	BIAS	The BIAS pin connects to the on-chip power rail and allows the IC to run most of its internal circuitry from the regulated output or another low voltage supply to improve efficiency. The BIAS pin is left floating if this feature is not used.
5 (CS51411/CS51413)	SYNC	This pin provides the synchronization input.
5 (CS51412/CS51414) 4 (CS51411/CS51413)	SHDNB	The shutdown pin is active low and TTL compatible. The IC goes into sleep mode, drawing less than $85\text{ }\mu\text{A}$ when the pin voltage is pulled below 1.0 V . This pin should be left floating in normal position.
6	GND	Power return connection for the IC.
7	V_{FB}	The FB pin provides input to the inverting input of the error amplifier. If V_{FB} is lower than 0.29 V , the oscillator frequency is divided by four, and current limit folds back to about 1 A . These features protect the IC under severe overcurrent or short circuit conditions.
8	V_C	The V_C pin provides a connection point to the output of the error amplifier and input to the PWM comparator. Driving of this pin should be avoided because on-chip test circuitry becomes active whenever current exceeding 0.5 mA is forced into the IC.

CS51411, CS51412, CS51413, CS51414

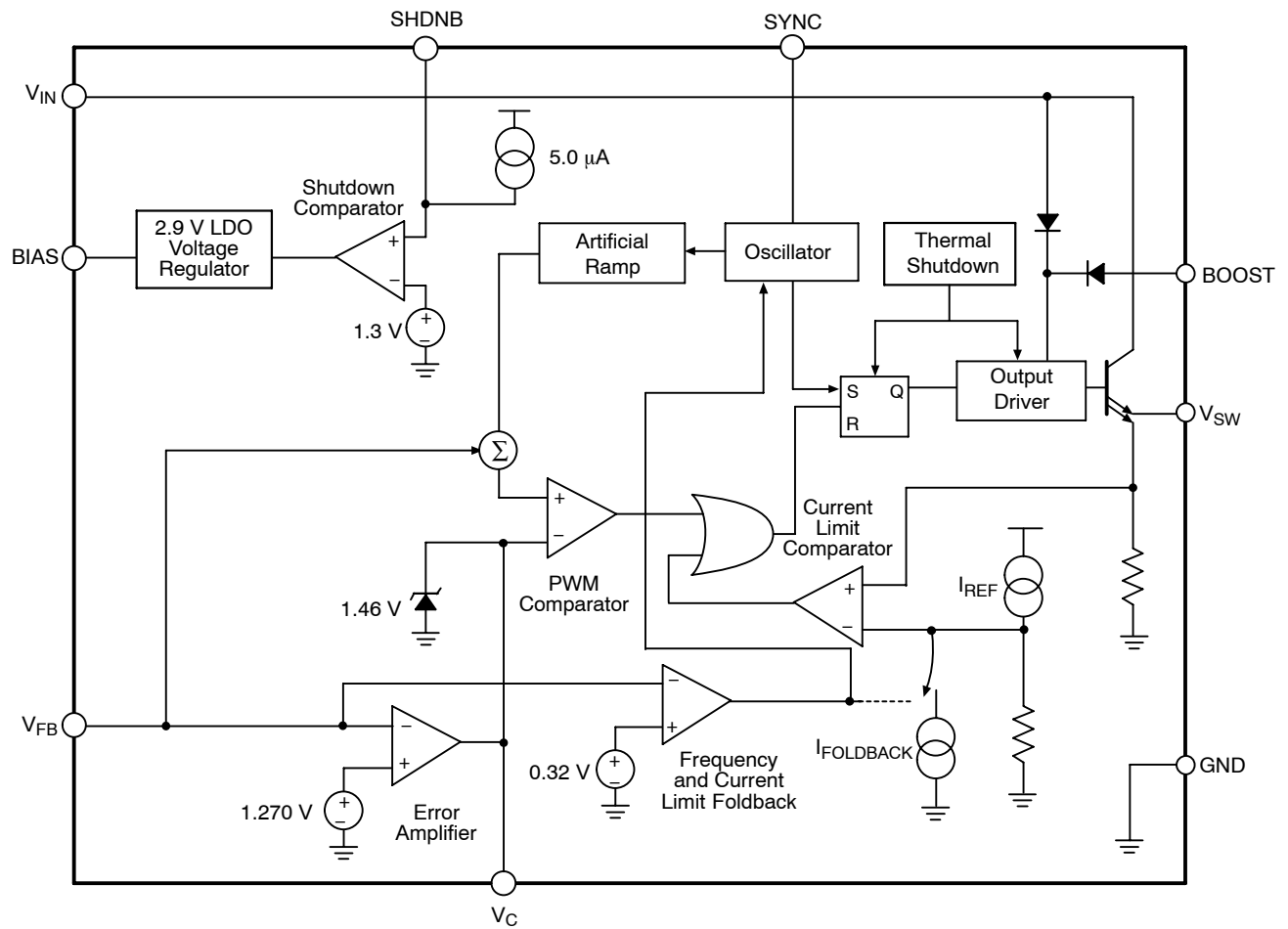


Figure 2. Block Diagram

APPLICATIONS INFORMATION

THEORY OF OPERATION

V² Control

The CS5141X family of buck regulators provides leading edge technology, a high level of integration and high operating frequencies allowing the layout of a switchmode power supply in a very small board area. These devices are based on the proprietary V² control architecture. V² control uses the output voltage and its ripple as the ramp signal, providing an ease of use not generally associated with voltage or current mode control. Improved line regulation, load regulation and very fast transient response are also major advantages.

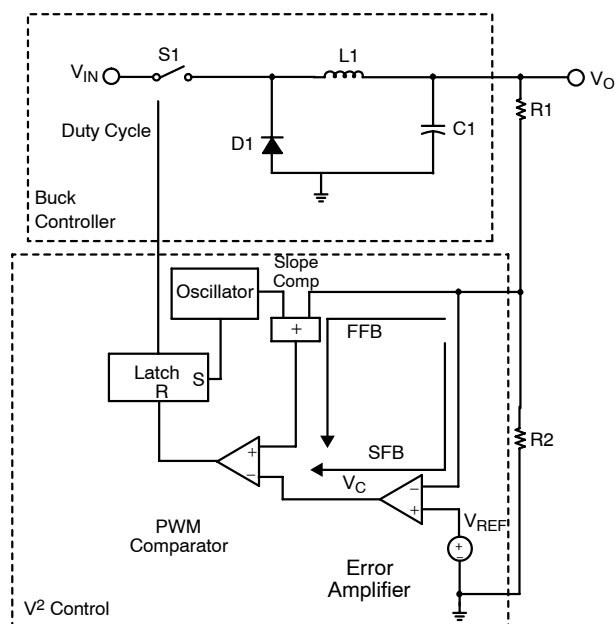


Figure 3. Buck Converter with V² Control.

As shown in Figure 3, there are two voltage feedback paths in V² control, namely Fast Feedback (FFB) and Slow Feedback (SFB). In FFB path, the feedback voltage connects directly to the PWM comparator. This feedback path carries the ramp signal as well as the output DC voltage. Artificial ramp derived from oscillator is added to the feedback signal to improve stability. The other feedback path SFB connects the feedback voltage to the error amplifier whose output V_C feeds to the other input of the PWM comparator. In a constant frequency mode, the oscillator signal sets the output latch and turns on the switch S1. This starts a new switch cycle. The ramp signal, composed of both artificial ramp and output ripple, eventually comes across the V_C voltage, and consequently resets the latch to turn off the switch. The switch S1 will turn on again at the beginning of the next switch cycle. In a buck converter, the output ripple is determined by the ripple current of the inductor L1 and the ESR (equivalent series resistor) of the output capacitor C1.

The slope compensation signal is a fixed voltage ramp provided by the oscillator. Adding this signal eliminates subharmonic oscillation associated with the operation at duty cycle greater than 50%. The artificial ramp also ensures the proper PWM function when the output ripple voltage is inadequate. The slope compensation signal is properly sized to serve its purposes without sacrificing the transient response speed.

Underload and line transient, not only the ramp signal changes, but more significantly the DC component of the feedback voltage varies proportionally to the output voltage. FFB path connects both signals directly to the PWM comparator. This allows instant modulation of the duty cycle to counteract any output voltage deviations. The transient response time is independent of the error amplifier bandwidth. This eliminates the delay associated with error amplifier and greatly improves the transient response time. The error amplifier is used here to ensure excellent DC accuracy.

Error Amplifier

The CS5141X has a transconductance error amplifier, whose noninverting input is connected to an Internal Reference Voltage generated from the on-chip regulator. The inverting input connects to the V_{FB} pin. The output of the error amplifier is made available at the V_C pin. A typical frequency compensation requires only a 0.1 μF capacitor connected between the V_C pin and ground, as shown in Figure 1. This capacitor and error amplifier's output resistance (approximately 8.0 MΩ) create a low frequency pole to limit the bandwidth. Since V² control does not require a high bandwidth error amplifier, the frequency compensation is greatly simplified.

The V_C pin is clamped below Output High Voltage. This allows the regulator to recover quickly from overcurrent or short circuit conditions.

Oscillator and Sync Feature (CS51411 and CS51413 only)

The on-chip oscillator is trimmed at the factory and requires no external components for frequency control. The high switching frequency allows smaller external components to be used, resulting in a board area and cost savings. The tight frequency tolerance simplifies magnetic components selection. The switching frequency is reduced to 25% of the nominal value when the V_{FB} pin voltage is below Frequency Foldback Threshold. In short circuit or overload conditions, this reduces the power dissipation of the IC and external components.

An external clock signal can sync CS51411/CS51414 to a higher frequency. The rising edge of the sync pulse turns on the power switch to start a new switching cycle, as shown in Figure 4. There is approximately 0.5 μs delay between the rising edge of the sync pulse and rising edge of the V_{sw} pin voltage. The sync threshold is TTL logic compatible, and duty cycle of the sync pulses can vary from 10% to 90%. The

frequency foldback feature is disabled during the sync mode.

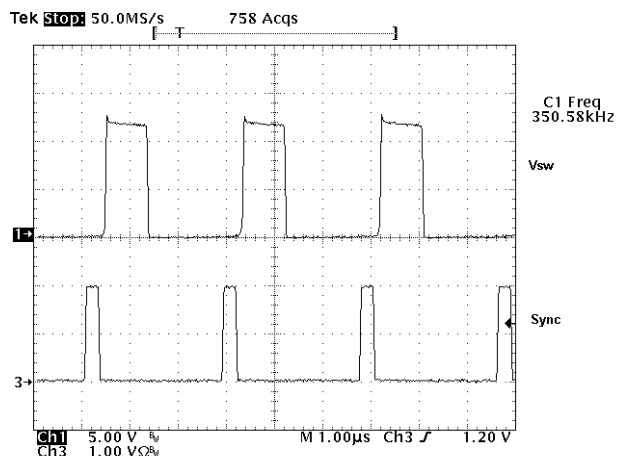


Figure 4. A CS51411 Buck Regulator is Synced by an External 350 kHz Pulse Signal

Power Switch and Current Limit

The collector of the built-in NPN power switch is connected to the V_{IN} pin, and the emitter to the V_{SW} pin. When the switch turns on, the V_{SW} voltage is equal to the V_{IN} minus switch Saturation Voltage. In the buck regulator, the V_{SW} voltage swings to one diode drop below ground when the power switch turns off, and the inductor current is commutated to the catch diode. Due to the presence of high pulsed current, the traces connecting the V_{SW} pin, inductor and diode should be kept as short as possible to minimize the noise and radiation. For the same reason, the input capacitor should be placed close to the V_{IN} pin and the anode of the diode.

The saturation voltage of the power switch is dependent on the switching current, as shown in Figure 5.

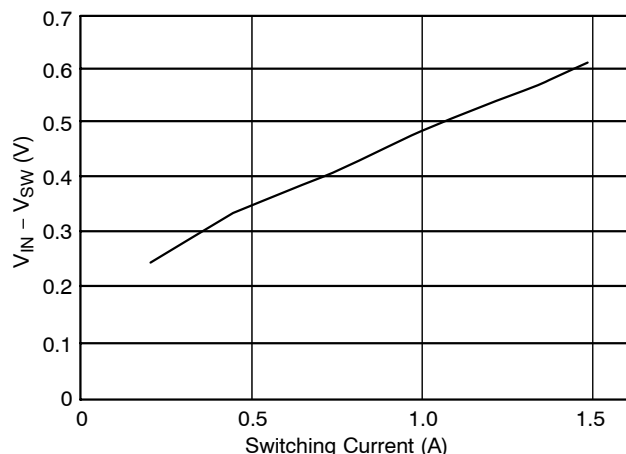


Figure 5. The Saturation Voltage of the Power Switch Increases with the Conducting Current

Members of the CS5141X family contain pulse-by-pulse current limiting to protect the power switch and external components. When the peak of the switching current reaches the Current Limit, the power switch turns off after the

Current Limit Delay. The switch will not turn on until the next switching cycle. The current limit threshold is independent of switching duty cycle. The maximum load current, given by the following formula under continuous conduction mode, is less than the Current Limit due to the ripple current.

$$I_{O(MAX)} = I_{LIM} - \frac{V_O(V_{IN} - V_O)}{2(L)(V_{IN})(f_s)}$$

where:

- f_s = switching frequency,
- I_{LIM} = current limit threshold,
- V_O = output voltage,
- V_{IN} = input voltage,
- L = inductor value.

When the regulator runs undercurrent limit, the subharmonic oscillation may cause low frequency oscillation, as shown in Figure 6. Similar to current mode control, this oscillation occurs at the duty cycle greater than 50% and can be alleviated by using a larger inductor value. The current limit threshold is reduced to Foldback Current when the FB pin falls below Foldback Threshold. This feature protects the IC and external components under the power up or overload conditions.

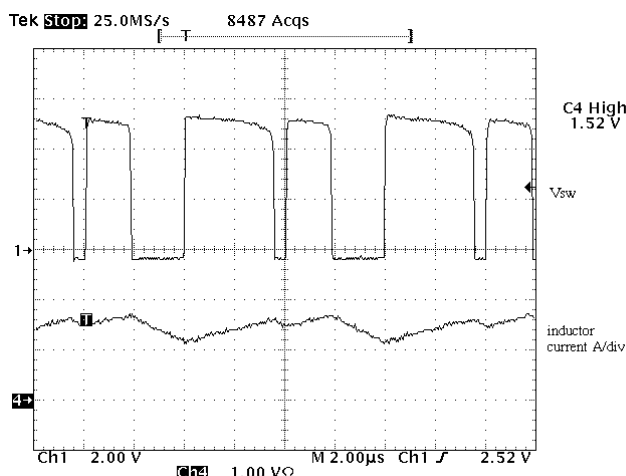


Figure 6. The Regulator in Current Limit

BOOST Pin

The BOOST pin provides base driving current for the power switch. A voltage higher than V_{IN} provides required headroom to turn on the power switch. This in turn reduces IC power dissipation and improves overall system efficiency. The BOOST pin can be connected to an external boost-strapping circuit which typically uses a 0.1 μ F capacitor and a 1N914 or 1N4148 diode, as shown in Figure 1. When the power switch is turned on, the voltage on the BOOST pin is equal to

$$V_{BOOST} = V_{IN} + V_O - V_F$$

where:

- V_F = diode forward voltage.

The anode of the diode can be connected to any DC voltage other than the regulated output voltage. However, the maximum voltage on the BOOST pin shall not exceed 40 V.

As shown in Figure 7, the BOOST pin current includes a constant 7.0 mA predriver current and base current proportional to switch conducting current. A detailed discussion of this current is conducted in Thermal Consideration section. A 0.1 μ F capacitor is usually adequate for maintaining the Boost pin voltage during the on time.

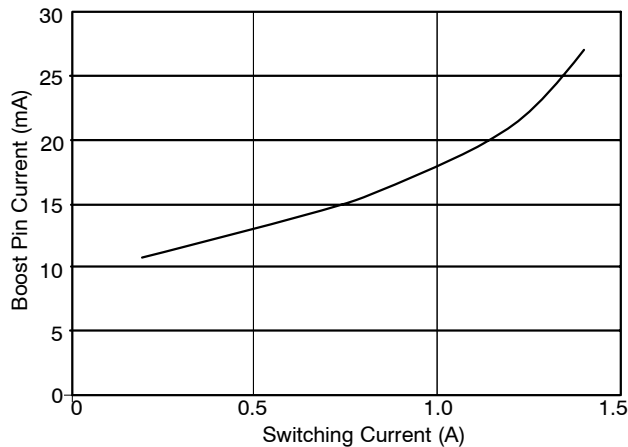


Figure 7. The Boost Pin Current Includes 7.0 mA Predriver Current and Base Current when the Switch is Turned On. The Beta Decline of the Power Switch Further Increases the Base Current at High Switching Current

BIAS Pin (CS51412 and CS51414 Only)

The BIAS pin allows a secondary power supply to bias the control circuitry of the IC. The BIAS pin voltage should be between 3.3 V and 6.0 V. If the BIAS pin voltage falls below that range, use a diode to prevent current drain from the BIAS pin. Powering the IC with a voltage lower than the regulator's input voltage reduces the IC power dissipation and improves energy transfer efficiency.

Shutdown

The internal power switch will not turn on until the V_{IN} pin rises above the Startup Voltage. This ensures no switching until adequate supply voltage is provided to the IC.

The IC enters a sleep mode when the SHDNB pin is pulled below Shutdown Threshold Voltage. In the sleep mode, the power switch keeps open and the supply current reduces to Shutdown Quiescent Current. This pin has internal pull-up current. So when this pin is not used, leave the SHDNB pin open.

Startup

During power up, the regulator tends to quickly charge up the output capacitors to reach voltage regulation. This gives rise to an excessive in-rush current which can be detrimental to the inductor, IC and catch diode. In V^2 control, the

compensation capacitor provides Soft-Start with no need for extra pin or circuitry. During the power up, the Output Source Current of the error amplifier charges the compensation capacitor which forces V_C pin and thus output voltage ramp up gradually. The Soft-Start duration can be calculated by

$$T_{SS} = \frac{V_C \times C_{COMP}}{I_{SOURCE}}$$

where:

V_C = V_C pin steady-state voltage, which is approximately equal to error amplifier's reference voltage.

C_{COMP} = Compensation capacitor connected to the V_C pin

I_{SOURCE} = Output Source Current of the error amplifier.

Using a 0.1 μ F C_{COMP} , the calculation shows a T_{SS} over 5.0 ms which is adequate to avoid any current stresses. Figure 8 shows the gradual rise of the V_C , V_O and envelope of the V_{SW} during power up. There is no voltage overshoot after the output voltage reaches the regulation. If the supply voltage rises slower than the V_C pin, output voltage may overshoot.

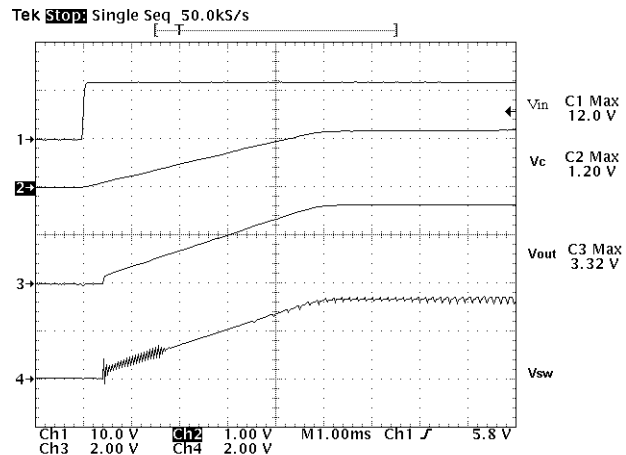


Figure 8. The Power Up Transition of CS5141X Regulator

Short Circuit

When the V_{FB} pin voltage drops below Foldback Threshold, the regulator reduces the peak current limit by 40% and switching frequency to 1/4 of the nominal frequency. These features are designed to protect the IC and external components during overload or short circuit conditions. In those conditions, peak switching current is clamped to the current limit threshold. The reduced switching frequency significantly increases the ripple current, and thus lowers the DC current. The short circuit can cause the minimum duty cycle to be limited by Minimum Output Pulse Width. The foldback frequency reduces the minimum duty cycle by extending the switching cycle. This protects the IC from overheating, and also limits the power that can be transferred to the output. The current limit foldback effectively reduces the current stress on the inductor and diode. When the output is shorted, the DC

current of the inductor and diode can approach the current limit threshold. Therefore, reducing the current limit by 40% can result in an equal percentage drop of the inductor and diode current. The short circuit waveforms are captured in Figure 9, and the benefit of the foldback frequency and current limit is self-evident.

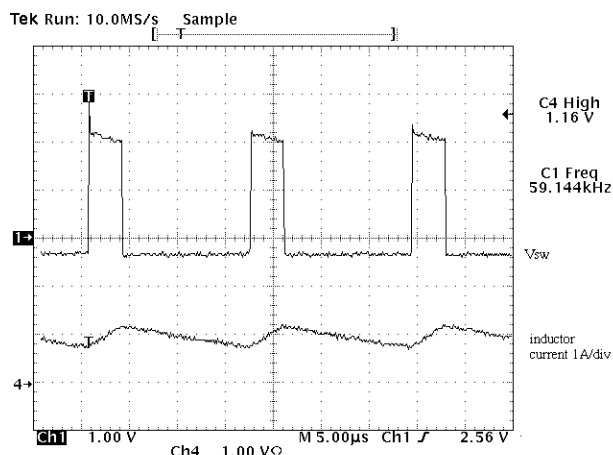


Figure 9. In Short Circuit, the Foldback Current and Foldback Frequency Limit the Switching Current to Protect the IC, Inductor and Catch Diode

Thermal Considerations

A calculation of the power dissipation of the IC is always necessary prior to the adoption of the regulator. The current drawn by the IC includes quiescent current, predriver current, and power switch base current. The quiescent current drives the low power circuits in the IC, which include comparators, error amplifier and other logic blocks. Therefore, this current is independent of the switching current and generates power equal to

$$W_Q = V_{IN} \times I_Q$$

where:

I_Q = quiescent current.

The predriver current is used to turn on/off the power switch and is approximately equal to 12 mA in worst case. During steady state operation, the IC draws this current from the Boost pin when the power switch is on and then receives it from the V_{IN} pin when the switch is off. The predriver current always returns to the V_{SW} pin. Since the predriver current goes out to the regulator's output even when the power switch is turned off, a minimum load is required to prevent overvoltage in light load conditions. If the Boost pin voltage is equal to $V_{IN} + V_O$ when the switch is on, the power dissipation due to predriver current can be calculated by

$$W_{DRV} = 12 \text{ mA} \times (V_{IN} - V_O + \frac{V_O^2}{V_{IN}})$$

The base current of a bipolar transistor is equal to collector current divided by beta of the device. Beta of 60 is used here to estimate the base current. The Boost pin provides the base

current when the transistor needs to be on. The power dissipated by the IC due to this current is

$$W_{BASE} = \frac{V_O^2}{V_{IN}} \times \frac{I_S}{60}$$

where:

I_S = DC switching current.

When the power switch turns on, the saturation voltage and conduction current contribute to the power loss of a non-ideal switch. The power loss can be quantified as

$$W_{SAT} = \frac{V_O}{V_{IN}} \times I_S \times V_{SAT}$$

where:

V_{SAT} = saturation voltage of the power switch which is shown in Figure 5.

The switching loss occurs when the switch experiences both high current and voltage during each switch transition. This regulator has a 30 ns turn-off time and associated power loss is equal to

$$W_S = \frac{I_S \times V_{IN}}{2} \times 30 \text{ ns} \times f_S$$

The turn-on time is much shorter and thus turn-on loss is not considered here.

The total power dissipated by the IC is sum of all the above

$$W_{IC} = W_Q + W_{DRV} + W_{BASE} + W_{SAT} + W_S$$

The IC junction temperature can be calculated from the ambient temperature, IC power dissipation and thermal resistance of the package. The equation is shown as follows,

$$T_J = W_{IC} \times R_{\theta JA} + T_A$$

The maximum IC junction temperature shall not exceed 125°C to guarantee proper operation and avoid any damages to the IC.

Using the BIAS Pin

The efficiency savings in using the BIAS pin is most notable at low load and high input voltage as will be explained below.

Figure 10 will help to understand the increase in efficiency when the BIAS pin is used. The circuitry shown is not the actual implementation, but is useful in the explanation.

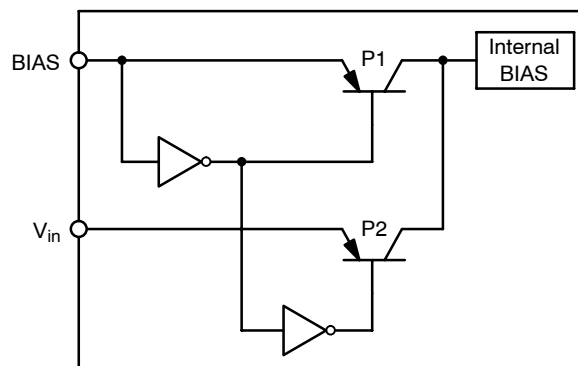


Figure 10.

Internal bias to the IC can be supplied via the V_{in} pin or the BIAS pin. When the BIAS pin is low, the logic turns P2 on and current is routed to the internal bias circuitry from the V_{in} pin. Conversely, when the BIAS pin is high, the logic turns P1 on and current is routed to the internal bias circuitry from the BIAS pin.

Here is an example of the power savings:

The input voltage range for V_{in} is 4.5 V to 40 V. The input voltage range for BIAS is 3.3 V to 6 V. The quiescent current specification is 3 mA (min), 4 mA (typ), and 6.25 mA (max).

Using a typical battery voltage of 14 V and the typical quiescent current number of 4 mA, the power would be:

$$P = V \times I = 14 \times 4e-3 = 56 \text{ mW}$$

We'll assume the BIAS pin is connected to an external regulator at 5 V instead of the output voltage. The BIAS pin would normally be connected to the output voltage, but adding an added switching regulator efficiency number here would cloud this example. Now the internal BIAS circuitry is being powered via 5 V. The resulting on chip power being dissipated is:

$$P = V \times I = 5 \times 4e-3 = 21 \text{ mW}$$

The power savings is 35 mW.

Now, to demonstrate more notable savings using the maximum battery input voltage of 40 V, the maximum quiescent current of 6.25 mA, and the lowest allowed BIAS voltage for proper operation of 3.3 V;

Powered from V_{in} :

$$P = 40 \times 6.25e-3 = 250 \text{ mW}$$

Powered from the BIAS pin:

$$P = 3.3 \times 6.25e-3 = 21 \text{ mW}$$

The power savings is 229 mW.

Minimum Load Requirement

As pointed out in the previous section, a minimum load is required for this regulator due to the predriver current feeding the output. Placing a resistor equal to V_O divided by 12 mA should prevent any voltage overshoot at light load conditions. Alternatively, the feedback resistors can be valued properly to consume 12 mA current.

COMPONENT SELECTION

Input Capacitor

In a buck converter, the input capacitor witnesses pulsed current with an amplitude equal to the load current. This pulsed current and the ESR of the input capacitors determine the V_{IN} ripple voltage, which is shown in Figure 11. For V_{IN} ripple, low ESR is a critical requirement for the input capacitor selection. The pulsed input current possesses a significant AC component, which is absorbed by the input capacitors. The RMS current of the input capacitor can be calculated using:

$$I_{RMS} = I_O \sqrt{D(1-D)}$$

where:

D = switching duty cycle which is equal to V_O/V_{IN} .

I_O = load current.

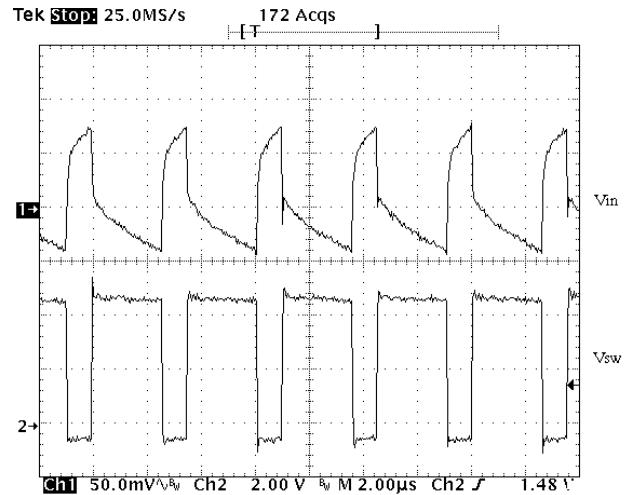


Figure 11. Input Voltage Ripple in a Buck Converter

To calculate the RMS current, multiply the load current with the constant given by Figure 12 at each duty cycle. It is a common practice to select the input capacitor with an RMS current rating more than half the maximum load current. If multiple capacitors are paralleled, the RMS current for each capacitor should be the total current divided by the number of capacitors.

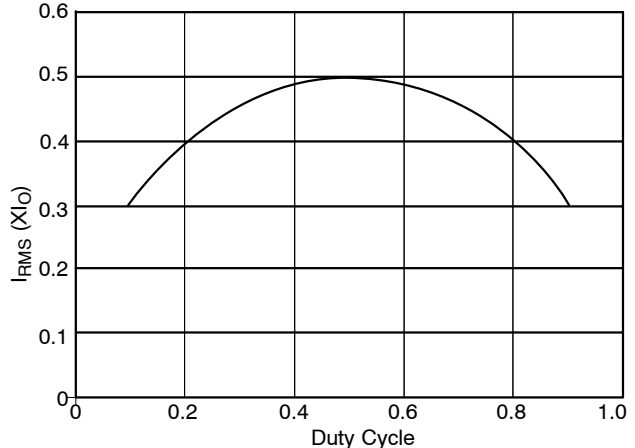


Figure 12. Input Capacitor RMS Current can be Calculated by Multiplying Y Value with Maximum Load Current at any Duty Cycle

Selecting the capacitor type is determined by each design's constraint and emphasis. The aluminum electrolytic capacitors are widely available at lowest cost. Their ESR and Equivalent Series Inductor (ESL) are relatively high. Multiple capacitors are usually paralleled to achieve lower ESR. In addition, electrolytic capacitors usually need to be paralleled with a ceramic capacitor for filtering high frequency noises. The OS-CON are solid aluminum electrolytic capacitors, and therefore has a much lower ESR. Recently, the price of the OS-CON capacitors

has dropped significantly so that it is now feasible to use them for some low cost designs. Electrolytic capacitors are physically large, and not used in applications where the size, and especially height is the major concern.

Ceramic capacitors are now available in values over 10 μF . Since the ceramic capacitor has low ESR and ESL, a single ceramic capacitor can be adequate for both low frequency and high frequency noises. The disadvantage of ceramic capacitors are their high cost. Solid tantalum capacitors can have low ESR and small size. However, the reliability of the tantalum capacitor is always a concern in the application where the capacitor may experience surge current.

Output Capacitor

In a buck converter, the requirements on the output capacitor are not as critical as those on the input capacitor. The current to the output capacitor comes from the inductor and thus is triangular. In most applications, this makes the RMS ripple current not an issue in selecting output capacitors.

The output ripple voltage is the sum of a triangular wave caused by ripple current flowing through ESR, and a square wave due to ESL. Capacitive reactance is assumed to be small compared to ESR and ESL. The peak-to-peak ripple current of the inductor is:

$$I_P - P = \frac{V_O(V_{IN} - V_O)}{(V_{IN})(L)(f_s)}$$

$V_{\text{RIPPLE(ESR)}}$, the output ripple due to the ESR, is equal to the product of I_{P-P} and ESR. The voltage developed across the ESL is proportional to the di/dt of the output capacitor. It is realized that the di/dt of the output capacitor is the same as the di/dt of the inductor current. Therefore, when the switch turns on, the di/dt is equal to $(V_{IN} - V_O)/L$, and it becomes V_O/L when the switch turns off. The total ripple voltage induced by ESL can then be derived from

$$V_{\text{RIPPLE(ESL)}} = \text{ESL} \left(\frac{V_{IN}}{L} \right) + \text{ESL} \left(\frac{V_{IN} - V_O}{L} \right) = \text{ESL} \left(\frac{V_{IN}}{L} \right)$$

The total output ripple is the sum of the $V_{\text{RIPPLE(ESR)}}$ and $V_{\text{RIPPLE(ESL)}}$.

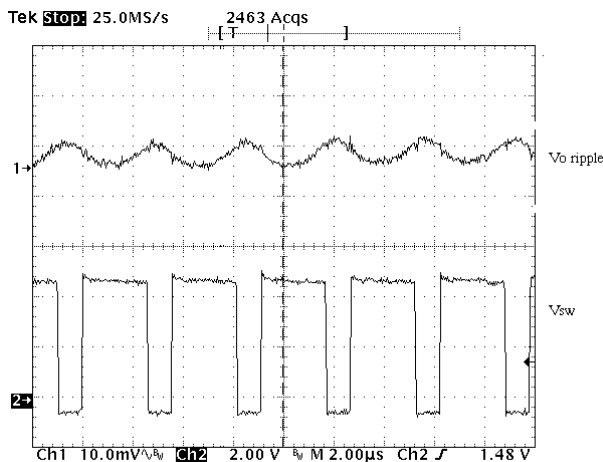


Figure 13. The Output Voltage Ripple Using Two 10 μF Ceramic Capacitors in Parallel

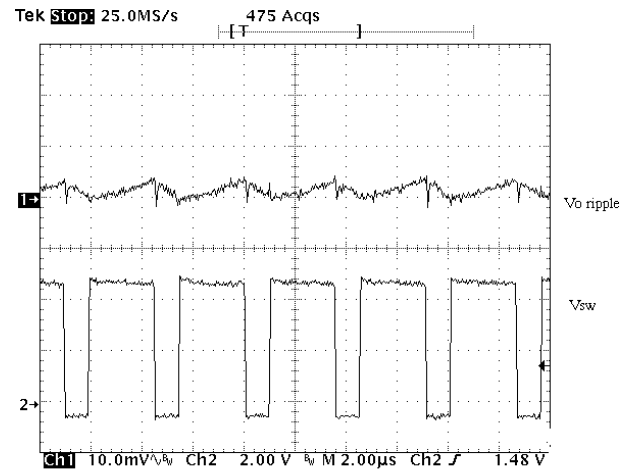


Figure 14. The Output Voltage Ripple Using One 100 μF POSCAP Capacitor

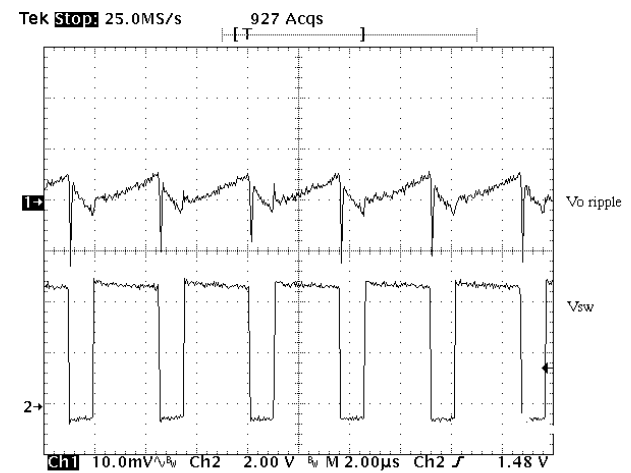


Figure 15. The Output Voltage Ripple Using One 100 μF OS-CON

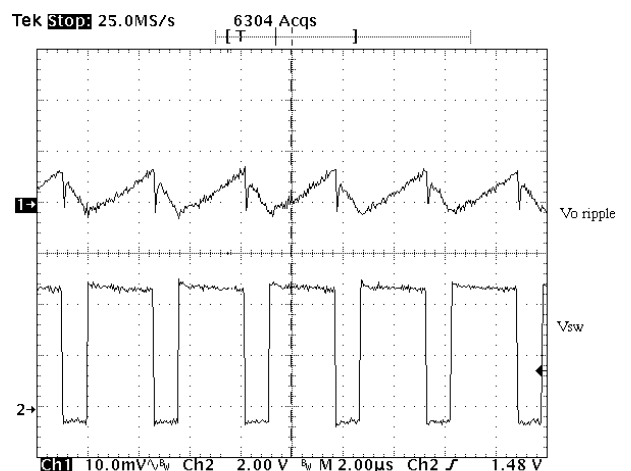


Figure 16. The Output Voltage Ripple Using One 100 μF Tantalum Capacitor

Figure 13 to Figure 16 show the output ripple of a 5.0 V to 3.3 V/500 mA regulator using 22 μ H inductor and various capacitor types. At the switching frequency, the low ESR and ESL make the ceramic capacitors behave capacitively as shown in Figure 13. Additional paralleled ceramic capacitors will further reduce the ripple voltage, but inevitably increase the cost. “POSCAP”, manufactured by SANYO, is a solid electrolytic capacitor. The anode is sintered tantalum and the cathode is a highly conductive polymerized organic semiconductor. TPC series, featuring low ESR and low profile, is used in the measurement of Figure 14. It is shown that POSCAP presents a good balance of capacitance and ESR, compared with a ceramic capacitor. In this application, the low ESR generates less than 5.0 mV of ripple and the ESL is almost unnoticeable. The ESL of the through-hole OS-CON capacitor give rise to the inductive impedance. It is evident from Figure 15 which shows the step rise of the output ripple on the switch turn-on and large spike on the switch turn-off. The ESL prevents the output capacitor from quickly charging up the parasitic capacitor of the inductor when the switch node is pulled below ground through the catch diode conduction. This results in the spike associated with the falling edge of the switch node. The D package tantalum capacitor used in Figure 16 has the same footprint as the POSCAP, but doubles the height. The ESR of the tantalum capacitor is apparently higher than the POSCAP. The electrolytic and tantalum capacitors provide a low-cost solution with compromised performance. The reliability of the tantalum capacitor is not a serious concern for output filtering because the output capacitor is usually free of surge current and voltage.

Diode Selection

The diode in the buck converter provides the inductor current path when the power switch turns off. The peak reverse voltage is equal to the maximum input voltage. The peak conducting current is clamped by the current limit of the IC. The average current can be calculated from:

$$I_{D(AVG)} = \frac{I_O(V_{IN} - V_O)}{V_{IN}}$$

The worse case of the diode average current occurs during maximum load current and maximum input voltage. For the diode to survive the short circuit condition, the current rating of the diode should be equal to the Foldback Current Limit. See Table 1 for Schottky diodes from ON Semiconductor which are suggested for CS5141X regulator.

Inductor Selection

When choosing inductors, one might have to consider maximum load current, core and copper losses, component height, output ripple, EMI, saturation and cost. Lower inductor values are chosen to reduce the physical size of the inductor. Higher value cuts down the ripple current, core losses and allows more output current. For most applications, the inductor value falls in the range between 2.2 μ H and 22 μ H. The saturation current ratings of the inductor shall not exceed the $I_{L(PK)}$, calculated according to

$$I_{L(PK)} = I_O + \frac{V_O(V_{IN} - V_O)}{2(f_S)(L)(V_{IN})}$$

The DC current through the inductor is equal to the load current. The worse case occurs during maximum load current. Check the vendor's spec to adjust the inductor value undercurrent loading. Inductors can lose over 50% of inductance when it nears saturation.

The core materials have a significant effect on inductor performance. The ferrite core has benefits of small physical size, and very low power dissipation. But be careful not to operate these inductors too far beyond their maximum ratings for peak current, as this will saturate the core. Powered Iron cores are low cost and have a more gradual saturation curve. The cores with an open magnetic path, such as rod or barrel, tend to generate high magnetic field radiation. However, they are usually cheap and small. The cores providing a close magnetic loop, such as pot-core and toroid, generate low electro-magnetic interference (EMI).

There are many magnetic component vendors providing standard product lines suitable for CS5141X. Table 2 lists three vendors, their products and contact information.

CS51411, CS51412, CS51413, CS51414

Table 1.

Part Number	V _{BREAKDOWN} (V)	I _{AVERAGE} (A)	V _F (V) @ I _{AVERAGE}	Package
1N5817	20	1.0	0.45	Axial Lead
1N5818	30	1.0	0.55	Axial Lead
1N5819	40	1.0	0.6	Axial Lead
MBR0520	20	0.5	0.385	SOD-123
MBR0530	30	0.5	0.43	SOD-123
MBR0540	40	0.5	0.53	SOD-123
MBRS120	20	1.0	0.55	SMB
MBRS130	30	1.0	0.395	SMB
MBRS140	40	1.0	0.6	SMB

Table 2.

Vendor	Product Family	Web Site	Telephone
Coiltronics	UNI-Pac1/2: SMT, barrel THIN-PAC: SMT, toroid, low profile CTX: Leaded, toroid	www.coiltronics.com	(516) 241-7876
Coilcraft	DO1608: SMT, barrel DS/DT 1608: SMT, barrel, magnetically shielded DO3316: SMT, barrel DS/DT 3316: SMT, barrel, magnetically shielded DO3308: SMT, barrel, low profile	www.coilcraft.com	(800) 322-2645
Pulse	–	www.pulseeng.com	(619) 674-8100

CS51411, CS51412, CS51413, CS51414

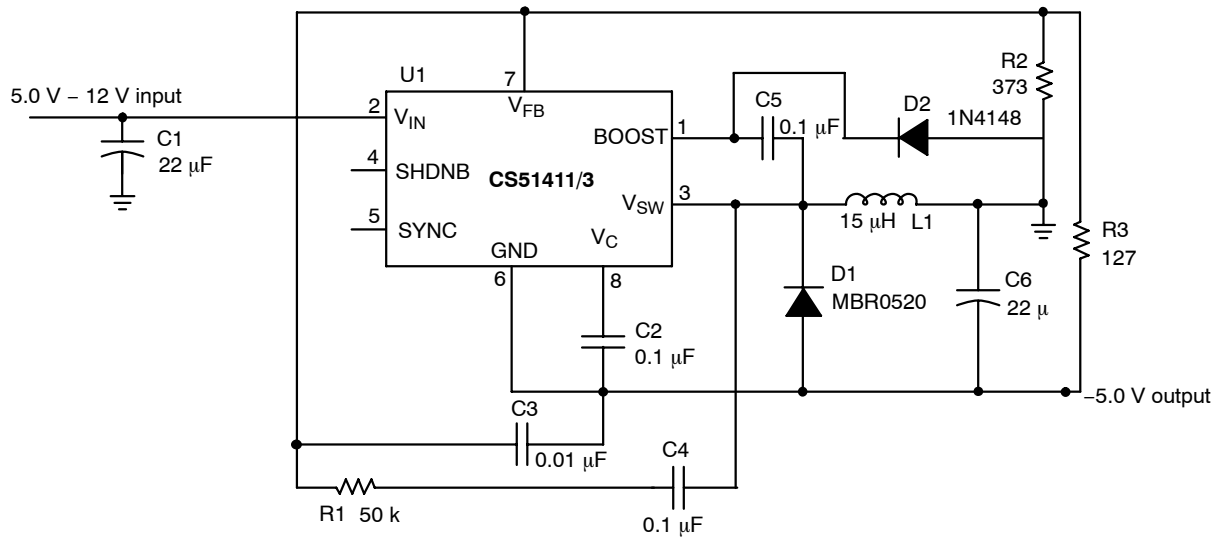


Figure 17. Additional Application Diagram, 5.0 V – 12 V to –5.0 V/400 mA Inverting Converter

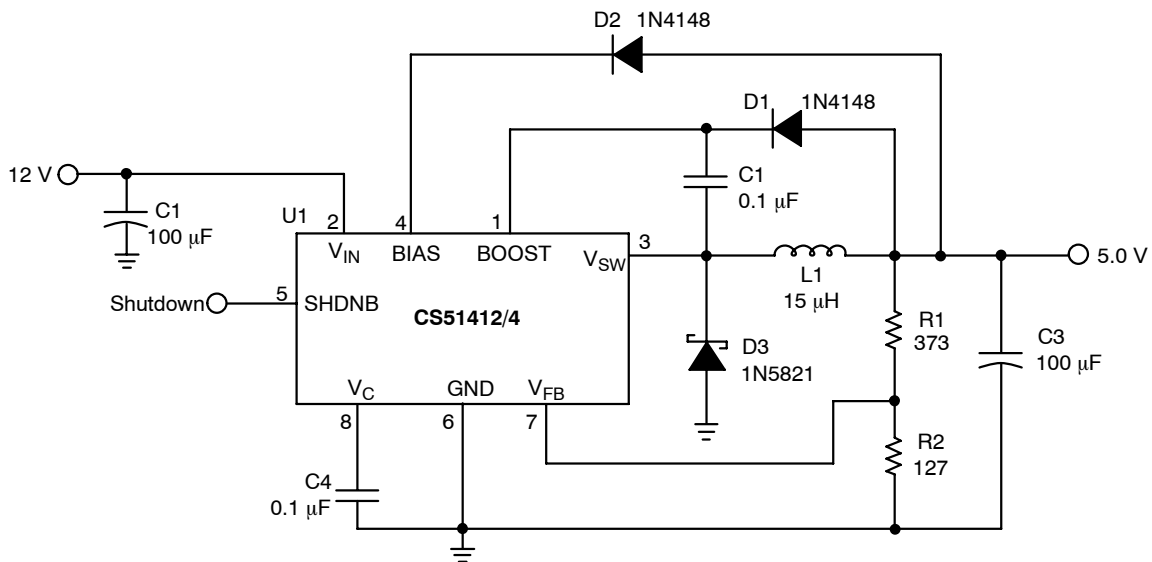


Figure 18. Additional Application Diagram, 12 V to 5.0 V/1.0 A Buck Converter using the BIAS Pin

CS51411, CS51412, CS51413, CS51414

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping [†]
CS51411ED8	-40°C < T _A < 85°C	SOIC-8	95 Units/Rail
CS51411EDR8			2500 Tape & Reel
CS51411EDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel
CS51412ED8		SOIC-8	95 Units/Rail
CS51412ED8G		SOIC-8 (Pb-Free)	95 Units/Rail
CS51412EDR8		SOIC-8	2500 Tape & Reel
CS51413ED8			95 Units/Rail
CS51413EDR8			2500 Tape & Reel
CS51413EDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel
CS51414ED8		SOIC-8	95 Units/Rail
CS51414EDR8			2500 Tape & Reel
CS51411GD8	0°C < T _A < 70°C	SOIC-8	95 Units/Rail
CS51411GDR8			2500 Tape & Reel
CS51411GDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel
CS51412GD8		SOIC-8	95 Units/Rail
CS51412GDR8			2500 Tape & Reel
CS51413GD8			95 Units/Rail
CS51413GDR8		SOIC-8 (Pb-Free)	2500 Tape & Reel
CS51413GDR8G			2500 Tape & Reel
CS51414GD8		SOIC-8	95 Units/Rail
CS51414GDR8			2500 Tape & Reel
CS51414GDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE THERMAL DATA

Parameter		SOIC-8	Unit
R _{θJC}	Typical	45	°C/W
R _{θJA}	Typical	165	°C/W

CS5171, CS5172, CS5173, CS5174

1.5 A 280 kHz/560 kHz Boost Regulators

The CS5171/2/3/4 products are 280 kHz/560 kHz switching regulators with a high efficiency, 1.5 A integrated switch. These parts operate over a wide input voltage range, from 2.7 V to 30 V. The flexibility of the design allows the chips to operate in most power supply configurations, including boost, flyback, forward, inverting, and SEPIC. The ICs utilize current mode architecture, which allows excellent load and line regulation, as well as a practical means for limiting current. Combining high frequency operation with a highly integrated regulator circuit results in an extremely compact power supply solution. The circuit design includes provisions for features such as frequency synchronization, shutdown, and feedback controls for either positive or negative voltage regulation. These parts are pin-to-pin compatible with LT1372/1373.

Part Number	Frequency	Feedback Voltage Polarity
CS5171	280 kHz	positive
CS5172	280 kHz	negative
CS5173	560 kHz	positive
CS5174	560 kHz	negative

Features

- Pb-Free Packages are Available
- Integrated Power Switch: 1.5 A Guaranteed
- Wide Input Range: 2.7 V to 30 V
- High Frequency Allows for Small Components
- Minimum External Components
- Easy External Synchronization
- Built in Overcurrent Protection
- Frequency Foldback Reduces Component Stress During an Overcurrent Condition
- Thermal Shutdown with Hysteresis
- Regulates Either Positive or Negative Output Voltages
- Shut Down Current: 50 μ A Maximum
- Pin-to-Pin Compatible with LT1372/1373
- Wide Temperature Range
 - ♦ Industrial Grade: -40°C to 125°C
 - ♦ Commercial Grade: 0°C to 125°C



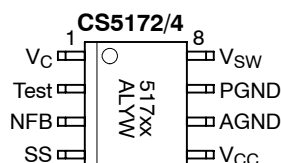
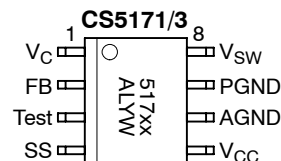
ON Semiconductor®

<http://onsemi.com>



SOIC-8
D SUFFIX
CASE 751

PIN CONNECTIONS AND MARKING DIAGRAM



x = 1, 2, 3, or 4
x = E, G
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 79 of this data sheet.

CS5171, CS5172, CS5173, CS5174

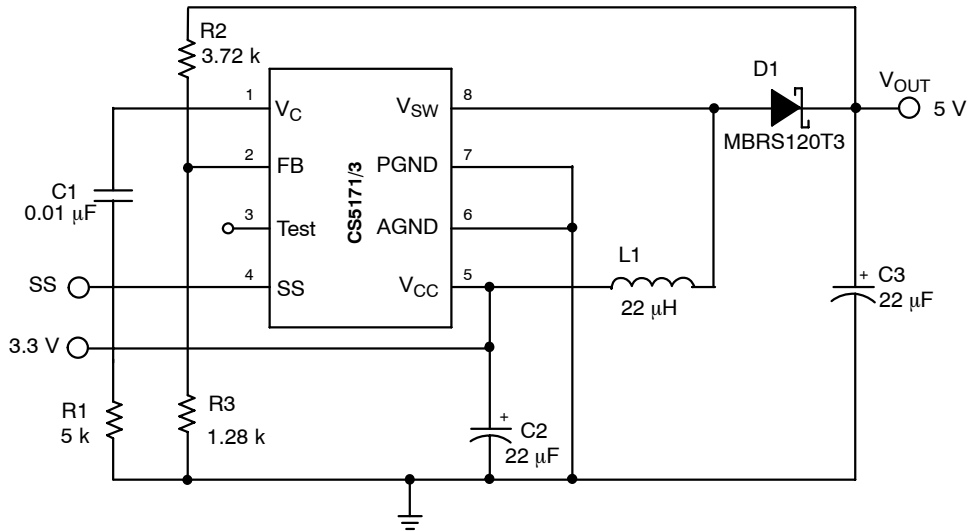


Figure 1. Applications Diagram

MAXIMUM RATINGS

Rating	Value	Unit
Junction Temperature Range, T _J	−40 to +150	°C
Storage Temperature Range, T _{STORAGE}	−65 to +150	°C
Package Thermal Resistance: Junction-to-Case, R _{θJC} Junction-to-Ambient, R _{θJA}	45 165	°C/W °C/W
Lead Temperature Soldering: Reflow (Note 1)	230 Peak	°C
ESD, Human Body Model	1.2	kV

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. 60 second maximum above 183°C.

MAXIMUM RATINGS

Pin Name	Pin Symbol	V _{MAX}	V _{MIN}	I _{SOURCE}	I _{SINK}
IC Power Input	V _{CC}	30 V	−0.3 V	N/A	200 mA
Shutdown/Sync	SS	30 V	−0.3 V	1.0 mA	1.0 mA
Loop Compensation	V _C	6.0 V	−0.3 V	10 mA	10 mA
Voltage Feedback Input	FB (CS5171/3 only)	10 V	−0.3 V	1.0 mA	1.0 mA
Negative Feedback Input (transient, 10 ms)	NFB (CS5172/4 only)	−10 V	10 V	1.0 mA	1.0 mA
Test Pin	Test	6.0 V	−0.3 V	1.0 mA	1.0 mA
Power Ground	PGND	0.3 V	−0.3 V	4 A	10 mA
Analog Ground	AGND	0 V	0 V	N/A	10 mA
Switch Input	V _{SW}	40 V	−0.3 V	10 mA	3.0 A

CS5171, CS5172, CS5173, CS5174

ELECTRICAL CHARACTERISTICS (2.7 V < V_{CC} < 30 V; Industrial Grade: -40°C < T_J < 125°C;
Commercial Grade: 0°C < T_J < 125°C; For all CS5171/2/3/4 specifications unless otherwise stated.)

Characteristic	Test Conditions	Min	Typ	Max	Unit

Positive and Negative Error Amplifiers

FB Reference Voltage (CS5171/3 only)	V _C tied to FB; measure at FB	1.246	1.276	1.300	V
NFB Reference Voltage (CS5172/4 only)	V _C = 1.25 V	-2.55	-2.45	-2.35	V
FB Input Current (CS5171/3 only)	FB = V _{REF}	-1.0	0.1	1.0	μA
NFB Input Current (CS5172/4 only)	NFB = NV _{REF}	-16	-10	-5.0	μA
FB Reference Voltage Line Regulation (CS5171/3 only)	V _C = FB	-	0.01	0.03	%/V
NFB Reference Voltage Line Regulation (CS5172/4 only)	V _C = 1.25 V	-	0.01	0.05	%/V
Positive Error Amp Transconductance	I _{VC} = ± 25 μA	300	550	800	μMho
Negative Error Amp Transconductance	I _{VC} = ± 5 μA	115	160	225	μMho
Positive Error Amp Gain	(Note 2)	200	500	-	V/V
Negative Error Amp Gain	(Note 2)	100	180	320	V/V
V _C Source Current	FB = 1.0 V or NFB = -1.9 V, V _C = 1.25 V	25	50	90	μA
V _C Sink Current	FB = 1.5 V or NFB = -3.1 V, V _C = 1.25 V	200	625	1500	μA
V _C High Clamp Voltage	FB = 1.0 V or NFB = -1.9 V; V _C sources 25 μA	1.5	1.7	1.9	V
V _C Low Clamp Voltage	FB = 1.5 V or NFB = -3.1 V, V _C sinks 25 μA	0.25	0.50	0.65	V
V _C Threshold	Reduce V _C from 1.5 V until switching stops	0.75	1.05	1.30	V

Oscillator

Base Operating Frequency	CS5171/2, FB = 1 V or NFB = -1.9 V	230	280	310	kHz
Reduced Operating Frequency	CS5171/2, FB = 0 V or NFB = 0 V	30	52	120	kHz
Maximum Duty Cycle	CS5171/2	90	94	-	%
Base Operating Frequency	CS5173/4, FB = 1 V or NFB = -1.9 V	460	560	620	kHz
Reduced Operating Frequency	CS5173/4, FB = 0 V or NFB = 0 V	60	104	160	kHz
Maximum Duty Cycle	CS5173/4	82	90	-	%
NFB Frequency Shift Threshold	Frequency drops to reduced operating frequency	-0.80	-0.65	-0.50	V
FB Frequency Shift Threshold	Frequency drops to reduced operating frequency	0.36	0.40	0.44	V

Sync/ Shutdown

Sync Range	CS5171/2	320	-	500	kHz
Sync Range	CS5173/4	640	-	1000	kHz
Sync Pulse Transition Threshold	Rise time = 20 ns	2.5	-	-	V
SS Bias Current	SS = 0 V SS = 3.0 V	-15 -	-3.0 3.0	- 8.0	μA μA
Shutdown Threshold	-	0.50	0.85	1.20	V
Shutdown Delay	2.7 V ≤ V _{CC} ≤ 12 V 12 V < V _{CC} ≤ 30 V	12 12	80 36	350 200	μs μs

2. Guaranteed by design, not 100% tested in production.

CS5171, CS5172, CS5173, CS5174

ELECTRICAL CHARACTERISTICS (continued) (2.7 V < V_{CC} < 30 V; Industrial Grade: -40°C < T_J < 125°C;
Commercial Grade: 0°C < T_J < 125°C; For all CS5171/2/3/4 specifications unless otherwise stated.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Power Switch					
Switch Saturation Voltage	I _{SWITCH} = 1.5 A, (Note 3)	–	0.8	1.4	V
	I _{SWITCH} = 1.0 A, 0°C ≤ T _J ≤ 85°C	–	0.55	–	V
	I _{SWITCH} = 1.0 A, -40°C ≤ T _J ≤ 0°C	–	0.75	–	V
	I _{SWITCH} = 10 mA	–	0.09	0.45	V
Switch Current Limit	50% duty cycle, Note 3	1.6	1.9	2.4	A
	80% duty cycle, Note 3	1.5	1.7	2.2	A
Minimum Pulse Width	FB = 0 V or NFB = 0 V, I _{SW} = 4.0 A, (Note 3)	200	250	300	ns
ΔI _{CC} / ΔI _{VSW}	2.7 V ≤ V _{CC} ≤ 12 V, 10 mA ≤ I _{SW} ≤ 1.0 A	–	10	30	mA/A
	12 V < V _{CC} ≤ 30 V, 10 mA ≤ I _{SW} ≤ 1.0 A	–	–	100	mA/A
	2.7 V ≤ V _{CC} ≤ 12 V, 10 mA ≤ I _{SW} ≤ 1.5 A, (Note 3)	–	17	30	mA/A
	12 V < V _{CC} ≤ 30 V, 10 mA ≤ I _{SW} ≤ 1.5 A, (Note 3)	–	–	100	mA/A
Switch Leakage	V _{SW} = 40 V, V _{CC} = 0V	–	2.0	100	μA

General

Operating Current	I _{SW} = 0	–	5.5	8.0	mA
Shutdown Mode Current	V _C < 0.8 V, SS = 0 V, 2.7 V ≤ V _{CC} ≤ 12 V	–	12	60	μA
	V _C < 0.8 V, SS = 0 V, 12 V ≤ V _{CC} ≤ 30 V	–	–	100	μA
Minimum Operation Input Voltage	V _{SW} switching, maximum I _{SW} = 10 mA	–	2.45	2.70	V
Thermal Shutdown	(Note 3)	150	180	210	°C
Thermal Hysteresis	(Note 3)	–	25	–	°C

3. Guaranteed by design, not 100% tested in production.

PACKAGE PIN DESCRIPTION

Package Pin #	Pin Symbol	Function
1	V _C	Loop compensation pin. The V _C pin is the output of the error amplifier and is used for loop compensation, current limit and soft start. Loop compensation can be implemented by a simple RC network as shown in the application diagram on page 64 as R1 and C1.
2 (CS5171/3 only)	FB	Positive regulator feedback pin. This pin senses a positive output voltage and is referenced to 1.276 V. When the voltage at this pin falls below 0.4 V, chip switching frequency reduces to 20% of the nominal frequency.
2 (CS5172/4) 3 (CS5171/3)	Test	These pins are connected to internal test logic and should either be left floating or tied to ground. Connection to a voltage between 2 V and 6 V shuts down the internal oscillator and leaves the power switch running.
3 (CS5172/4)	NFB	Negative feedback pin. This pin senses a negative output voltage and is referenced to -2.5 V. When the voltage at this pin goes above -0.65 V, chip switching frequency reduces to 20% of the nominal frequency.
4	SS	Synchronization and shutdown pin. This pin may be used to synchronize the part to nearly twice the base frequency. A TTL low will shut the part down and put it into low current mode. If synchronization is not used, this pin should be either tied high or left floating for normal operation.
5	V _{CC}	Input power supply pin. This pin supplies power to the part and should have a bypass capacitor connected to AGND.
6	AGND	Analog ground. This pin provides a clean ground for the controller circuitry and should not be in the path of large currents. The output voltage sensing resistors should be connected to this ground pin. This pin is connected to the IC substrate.
7	PGND	Power ground. This pin is the ground connection for the emitter of the power switching transistor. Connection to a good ground plane is essential.
8	V _{SW}	High current switch pin. This pin connects internally to the collector of the power switch. The open voltage across the power switch can be as high as 40 V. To minimize radiation, use a trace as short as practical.

CS5171, CS5172, CS5173, CS5174

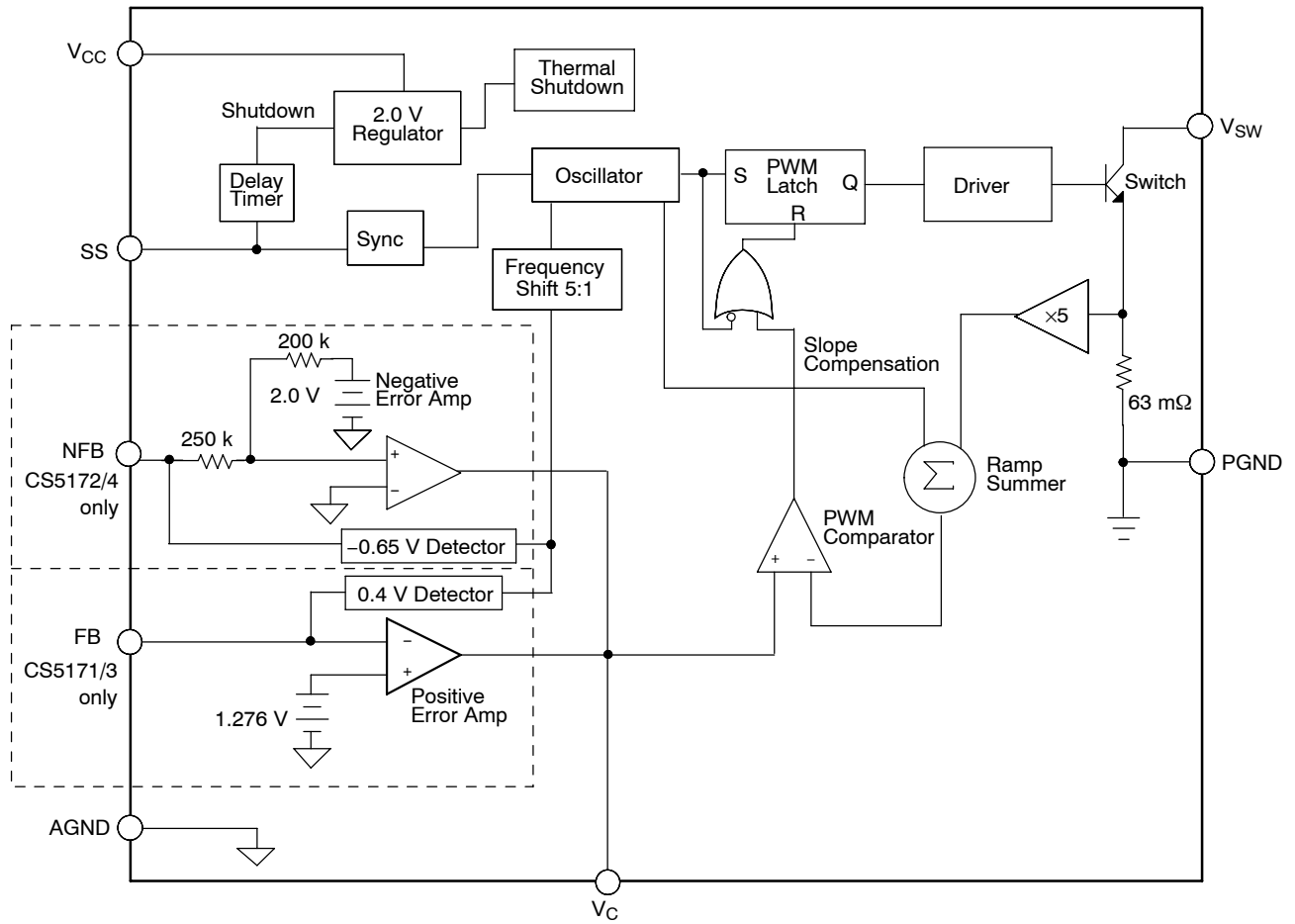


Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

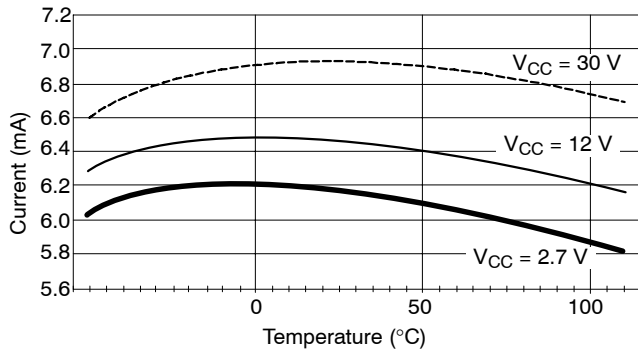


Figure 3. I_{CC} (No Switching) vs. Temperature

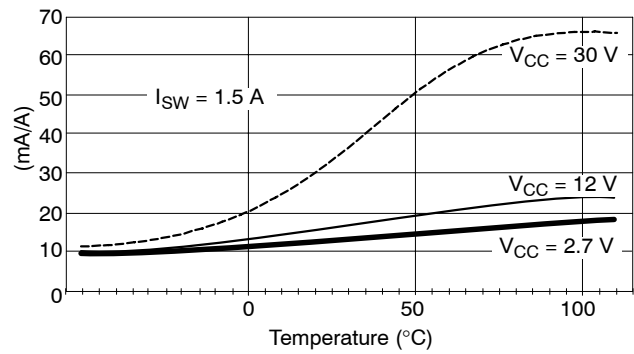


Figure 4. $\Delta I_{CC} / \Delta V_{SW}$ vs. Temperature

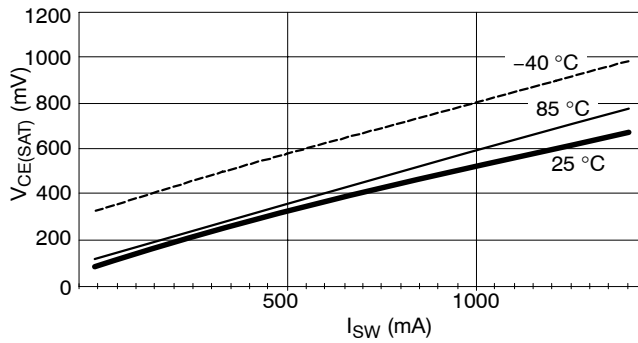


Figure 5. V_{CE(SAT)} vs. I_{SW}

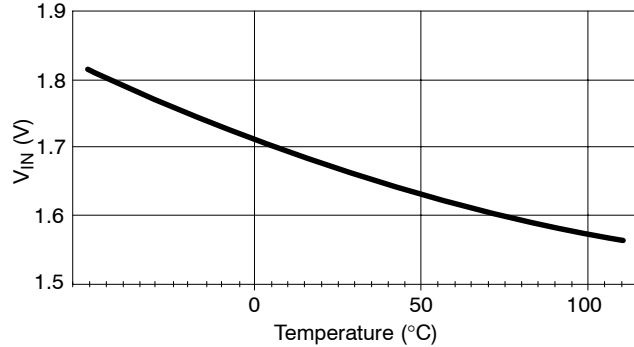


Figure 6. Minimum Input Voltage vs. Temperature

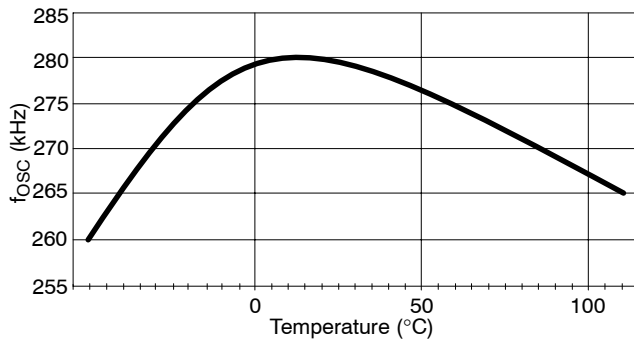


Figure 7. Switching Frequency vs. Temperature (CS5171/2 only)

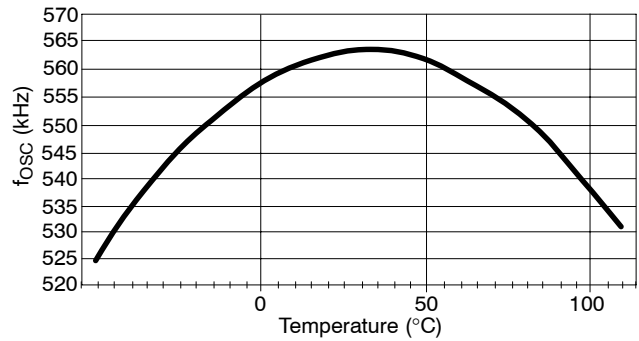


Figure 8. Switching Frequency vs. Temperature (CS5173/4 only)

TYPICAL PERFORMANCE CHARACTERISTICS

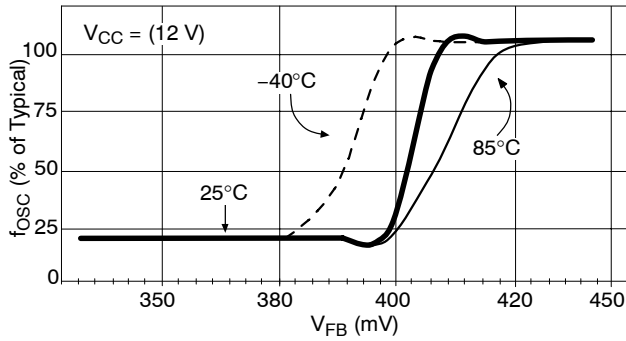


Figure 9. Switching Frequency vs. V_{FB}
(CS5171/3 only)

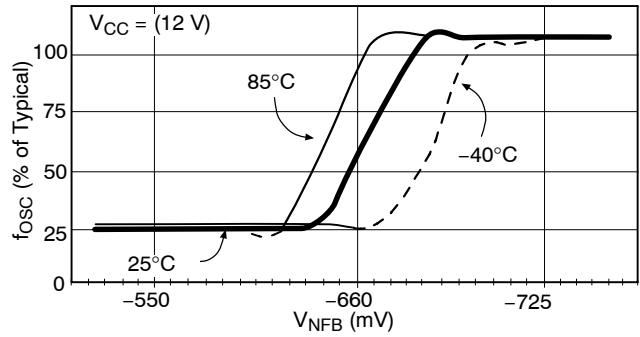


Figure 10. Switching Frequency vs. V_{NFB}
(CS5172/4 only)

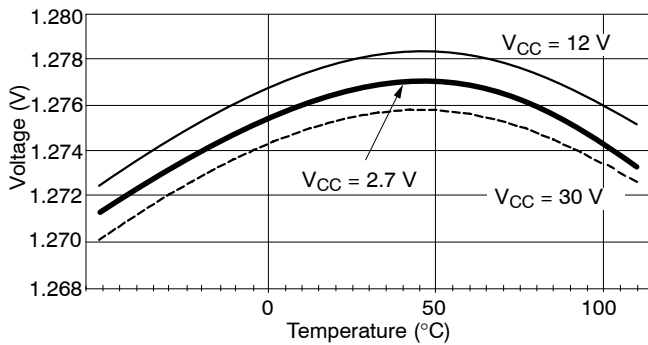


Figure 11. Reference Voltage vs. Temperature
(CS5171/3 only)

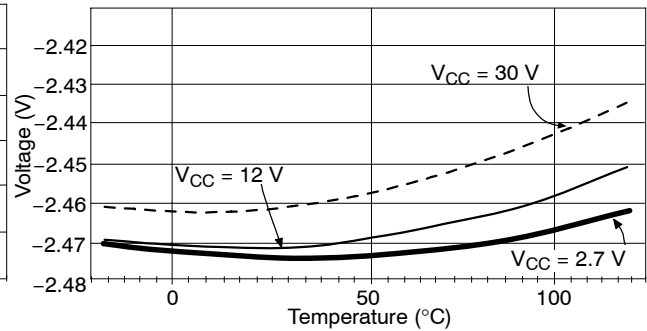


Figure 12. Reference Voltage vs. Temperature
(CS5172/4 only)

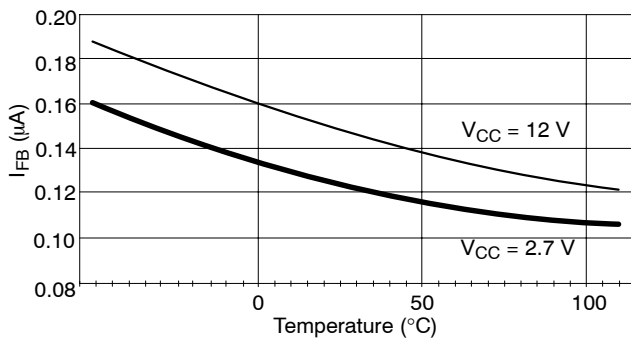


Figure 13. I_{FB} vs. Temperature (CS5171/3 only)

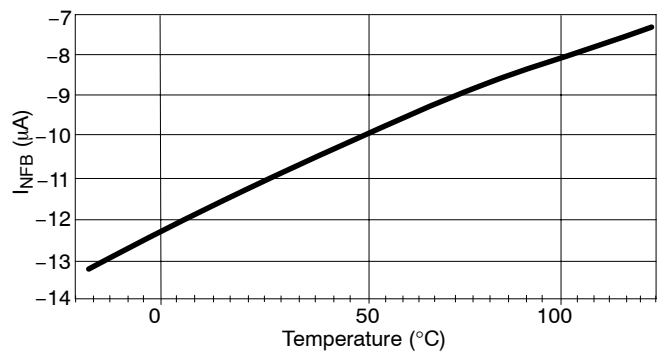


Figure 14. I_{NFB} vs. Temperature (CS5172/4 only)

TYPICAL PERFORMANCE CHARACTERISTICS

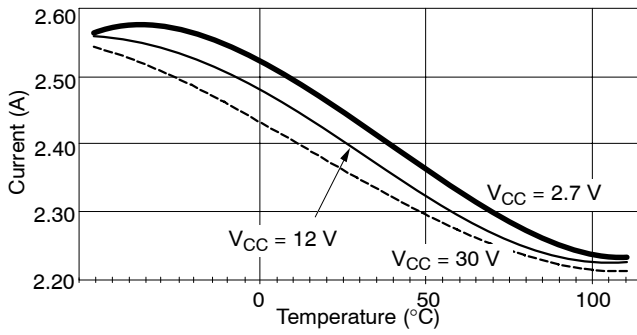


Figure 15. Current Limit vs. Temperature

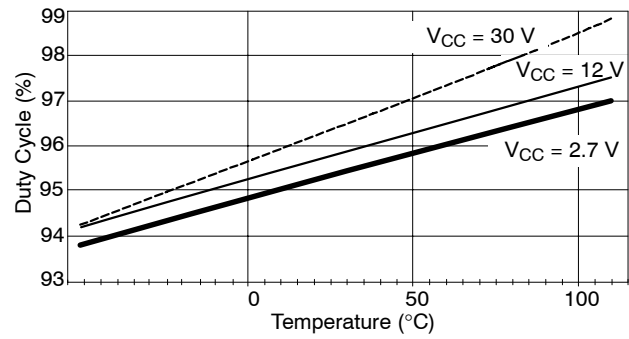


Figure 16. Maximum Duty Cycle vs. Temperature

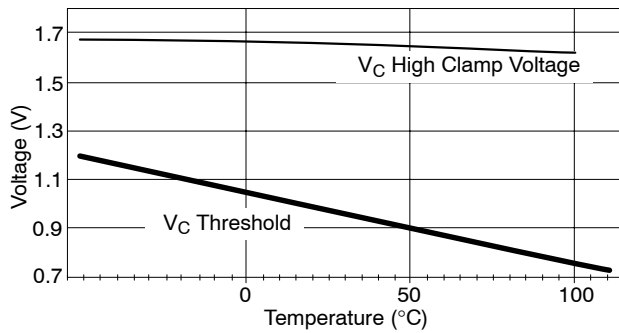


Figure 17. V_C Threshold and High Clamp Voltage vs. Temperature

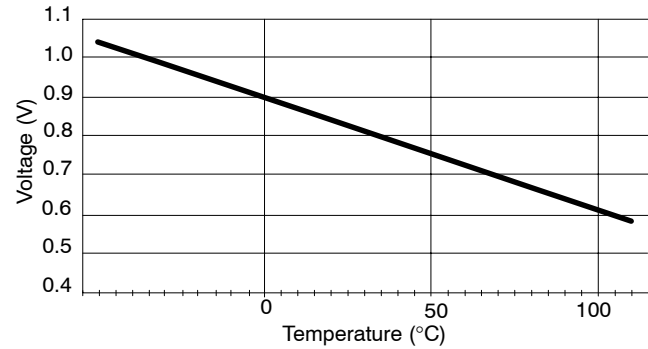


Figure 18. Shutdown Threshold vs. Temperature

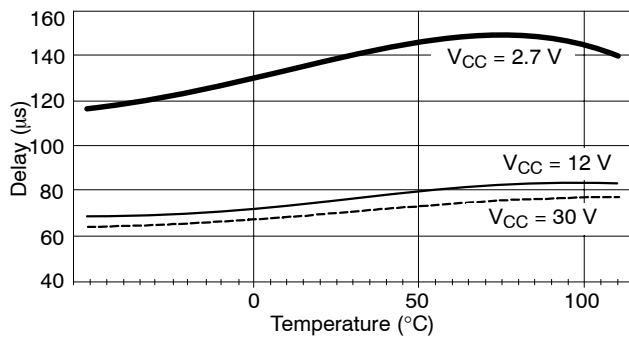


Figure 19. Shutdown Delay vs. Temperature

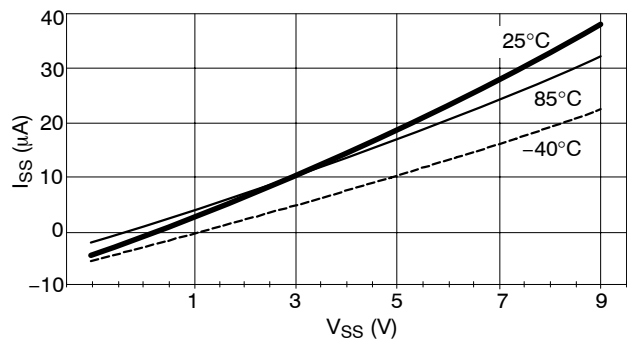


Figure 20. I_{SS} vs. V_{SS}

TYPICAL PERFORMANCE CHARACTERISTICS

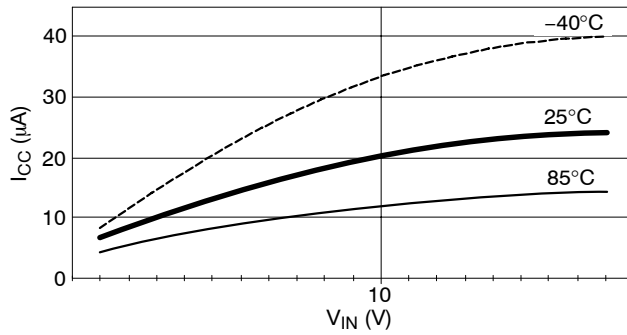


Figure 21. I_{CC} vs. V_{IN} During Shutdown

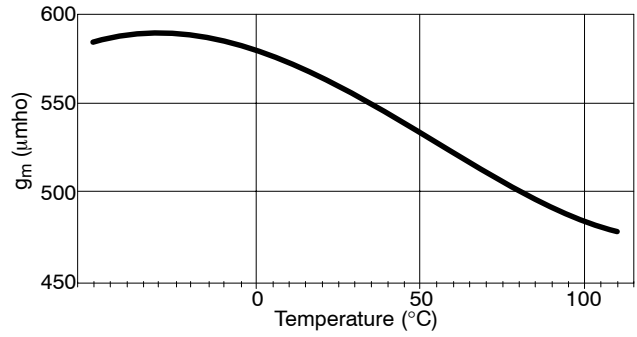


Figure 22. Error Amplifier Transconductance vs. Temperature (CS5171/3 only)

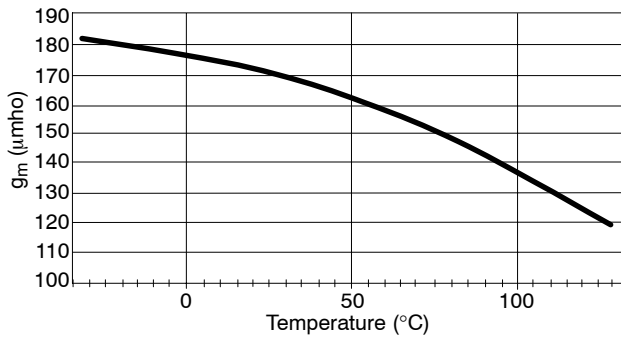


Figure 23. Negative Error Amplifier Transconductance vs. Temperature (CS5172/4 only)

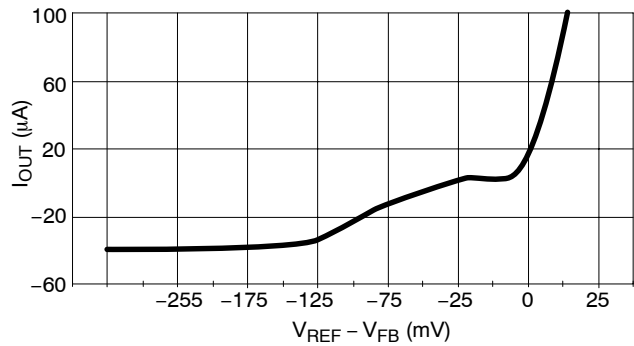


Figure 24. Error Amplifier I_{OUT} vs. V_{FB} (CS5171/3 only)

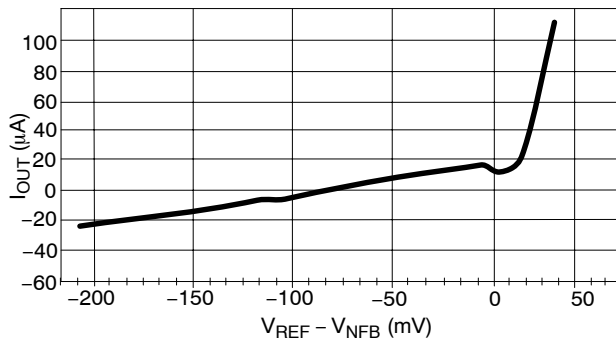


Figure 25. Error Amplifier I_{OUT} vs. V_{NFB} (CS5172/4 only)

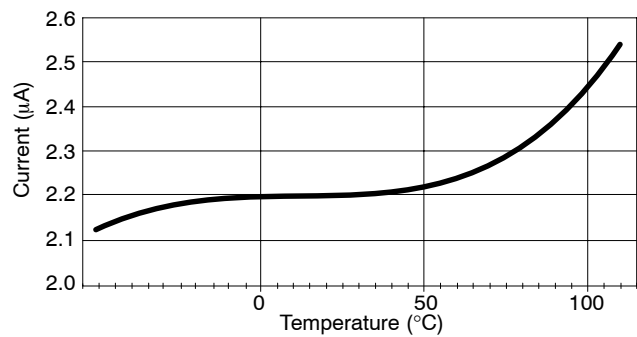


Figure 26. Switch Leakage vs. Temperature

APPLICATIONS INFORMATION

THEORY OF OPERATION

Current Mode Control

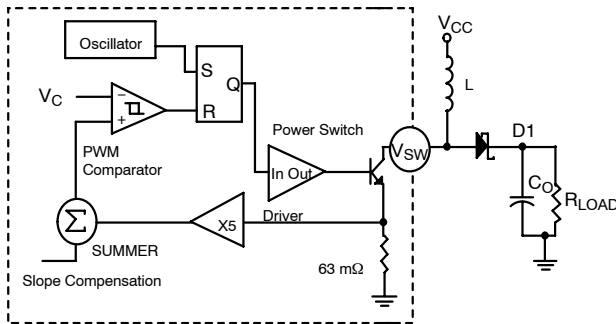


Figure 27. Current Mode Control Scheme

The CS517x family incorporates a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on-time of the power switch. The oscillator is used as a fixed-frequency clock to ensure a constant operational frequency. The resulting control scheme features several advantages over conventional voltage mode control. First, derived directly from the inductor, the ramp signal responds immediately to line voltage changes. This eliminates the delay caused by the output filter and error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse-by-pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This allows both a simpler compensation and a higher gain-bandwidth over a comparable voltage mode circuit.

Without discrediting its apparent merits, current mode control comes with its own peculiar problems, mainly, subharmonic oscillation at duty cycles over 50%. The CS517x family solves this problem by adopting a slope compensation scheme in which a fixed ramp generated by the oscillator is added to the current ramp. A proper slope rate is provided to improve circuit stability without sacrificing the advantages of current mode control.

Oscillator and Shutdown

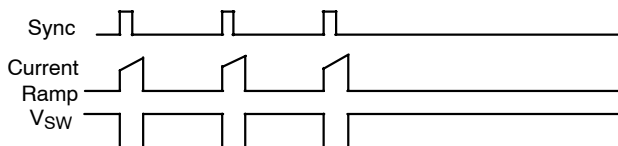


Figure 28. Timing Diagram of Sync and Shutdown

The oscillator is trimmed to guarantee an 18% frequency accuracy. The output of the oscillator turns on the power switch at a frequency of 280 kHz (CS5171/2) or 560 kHz (CS5173/4), as shown in Figure 27. The power switch is turned off by the output of the PWM Comparator.

A TTL-compatible sync input at the SS pin is capable of syncing up to 1.8 times the base oscillator frequency. As shown in Figure 28, in order to sync to a higher frequency, a positive transition turns on the power switch before the output of the oscillator goes high, thereby resetting the oscillator. The sync operation allows multiple power supplies to operate at the same frequency.

A sustained logic low at the SS pin will shut down the IC and reduce the supply current.

An additional feature includes frequency shift to 20% of the nominal frequency when either the NFB or FB pins trigger the threshold. During power up, overload, or short circuit conditions, the minimum switch on-time is limited by the PWM comparator minimum pulse width. Extra switch off-time reduces the minimum duty cycle to protect external components and the IC itself.

As previously mentioned, this block also produces a ramp for the slope compensation to improve regulator stability.

Error Amplifier

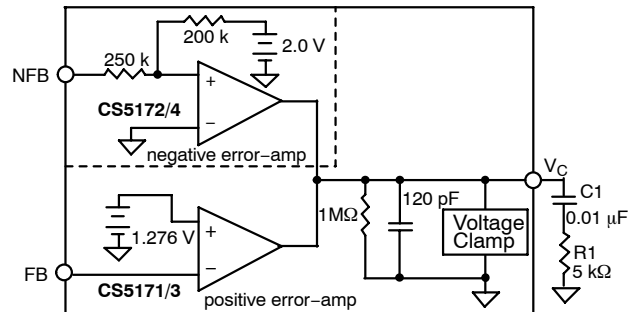


Figure 29. Error Amplifier Equivalent Circuit

For CS5172/4, the NFB pin is internally referenced to -2.5 V with approximately a 250 kΩ input impedance. For CS5171/3, the FB pin is directly connected to the inverting input of the positive error amplifier, whose non-inverting input is fed by the 1.276 V reference. Both amplifiers are transconductance amplifiers with a high output impedance of approximately 1 MΩ, as shown in Figure 29. The V_C pin is connected to the output of the error amplifiers and is internally clamped between 0.5 V and 1.7 V. A typical connection at the V_C pin includes a capacitor in series with a resistor to ground, forming a pole/zero for loop compensation.

An external shunt can be connected between the V_C pin and ground to reduce its clamp voltage. Consequently, the current limit of the internal power transistor current is reduced from its nominal value.

Switch Driver and Power Switch

The switch driver receives a control signal from the logic section to drive the output power switch. The switch is grounded through emitter resistors (63 mΩ total) to the PGND pin. PGND is not connected to the IC substrate so that switching noise can be isolated from the analog ground. The peak switching current is clamped by an internal circuit. The clamp current is guaranteed to be greater than 1.5 A and varies with duty cycle due to slope compensation. The power switch can withstand a maximum voltage of 40 V on the collector (V_{SW} pin). The saturation voltage of the switch is typically less than 1 V to minimize power dissipation.

Short Circuit Condition

When a short circuit condition happens in a boost circuit, the inductor current will increase during the whole switching cycle, causing excessive current to be drawn from the input power supply. Since control ICs don't have the means to limit load current, an external current limit circuit (such as a fuse or relay) has to be implemented to protect the load, power supply and ICs.

In other topologies, the frequency shift built into the IC prevents damage to the chip and external components. This feature reduces the minimum duty cycle and allows the transformer secondary to absorb excess energy before the switch turns back on.

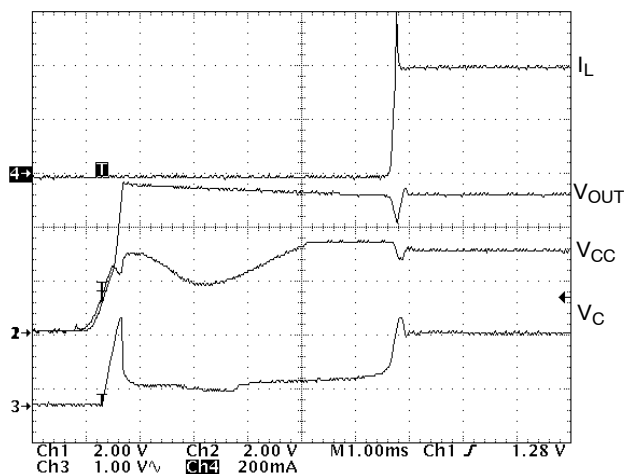


Figure 30. Startup Waveforms of Circuit Shown in the Application Diagram. Load = 400 mA.

The CS517x can be activated by either connecting the V_{CC} pin to a voltage source or by enabling the SS pin. Startup waveforms shown in Figure 30 are measured in the boost converter demonstrated in the Application Diagram on the page 64 of this document. Recorded after the input voltage is turned on, this waveform shows the various phases during the power up transition.

When the V_{CC} voltage is below the minimum supply voltage, the V_{SW} pin is in high impedance. Therefore, current conducts directly from the input power source to the output through the inductor and diode. Once V_{CC} reaches

approximately 1.5 V, the internal power switch briefly turns on. This is a part of the CS517x's normal operation. The turn-on of the power switch accounts for the initial current swing.

When the V_C pin voltage rises above the threshold, the internal power switch starts to switch and a voltage pulse can be seen at the V_{SW} pin. Detecting a low output voltage at the FB pin, the built-in frequency shift feature reduces the switching frequency to a fraction of its nominal value, reducing the minimum duty cycle, which is otherwise limited by the minimum on-time of the switch. The peak current during this phase is clamped by the internal current limit.

When the FB pin voltage rises above 0.4 V, the frequency increases to its nominal value, and the peak current begins to decrease as the output approaches the regulation voltage. The overshoot of the output voltage is prevented by the active pull-on, by which the sink current of the error amplifier is increased once an overvoltage condition is detected. The overvoltage condition is defined as when the FB pin voltage is 50 mV greater than the reference voltage.

COMPONENT SELECTION

Frequency Compensation

The goal of frequency compensation is to achieve desirable transient response and DC regulation while ensuring the stability of the system. A typical compensation network, as shown in Figure 31, provides a frequency response of two poles and one zero. This frequency response is further illustrated in the Bode plot shown in Figure 32.

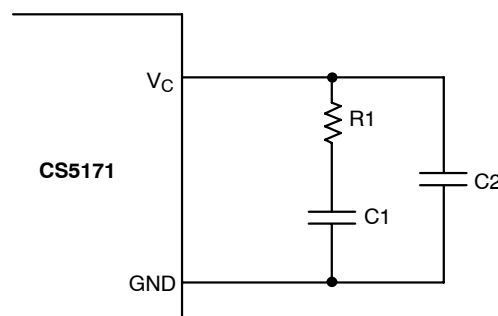


Figure 31. A Typical Compensation Network

The high DC gain in Figure 32 is desirable for achieving DC accuracy over line and load variations. The DC gain of a transconductance error amplifier can be calculated as follows:

$$\text{Gain}_{\text{DC}} = G_M \times R_O$$

where:

G_M = error amplifier transconductance;

R_O = error amplifier output resistance $\approx 1 \text{ M}\Omega$.

The low frequency pole, f_{P1} , is determined by the error amplifier output resistance and C1 as:

$$f_{P1} = \frac{1}{2\pi C1 R_O}$$

The first zero generated by C1 and R1 is:

$$f_{Z1} = \frac{1}{2\pi C1R1}$$

The phase lead provided by this zero ensures that the loop has at least a 45° phase margin at the crossover frequency. Therefore, this zero should be placed close to the pole generated in the power stage which can be identified at frequency:

$$f_P = \frac{1}{2\pi C_{O}R_{LOAD}}$$

where:

C_O = equivalent output capacitance of the error amplifier
 $\approx 120\text{pF}$;

R_{LOAD} = load resistance.

The high frequency pole, f_{P2} , can be placed at the output filter's ESR zero or at half the switching frequency. Placing the pole at this frequency will cut down on switching noise. The frequency of this pole is determined by the value of C2 and R1:

$$f_{P2} = \frac{1}{2\pi C2R1}$$

One simple method to ensure adequate phase margin is to design the frequency response with a -20 dB per decade slope, until unity-gain crossover. The crossover frequency should be selected at the midpoint between f_{Z1} and f_{P2} where the phase margin is maximized.

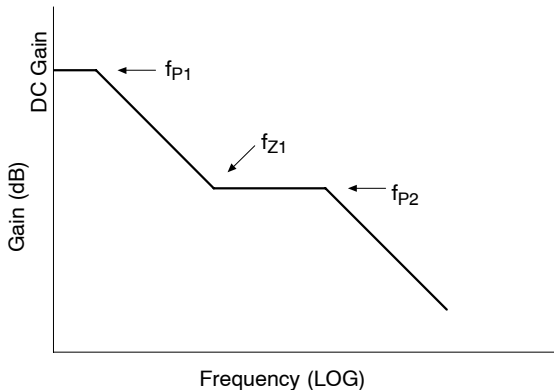


Figure 32. Bode Plot of the Compensation Network Shown in Figure 31

Negative Voltage Feedback

Since the negative error amplifier has finite input impedance as shown in Figure 33, its induced error has to be considered. If a voltage divider is used to scale down the negative output voltage for the NFB pin, the equation for calculating output voltage is:

$$-V_{OUT} = \left(\frac{-2.5 (R1 + R2)}{R2} \right) - 10 \mu A \times R1$$

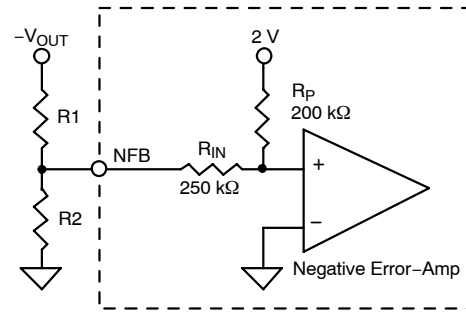


Figure 33. Negative Error Amplifier and NFB Pin

It is shown that if R1 is less than 10 k, the deviation from the design target will be less than 0.1 V. If the tolerances of the negative voltage reference and NFB pin input current are considered, the possible offset of the output V_{OFFSET} varies in the range of:

$$\left(\frac{-0.05 (R1 + R2)}{R2} \right) - (15 \mu A \times R1) \leq V_{OFFSET} \leq \left(\frac{0.05 (R1 + R2)}{R2} \right) - (5 \mu A \times R1)$$

V_{SW} Voltage Limit

In the boost topology, V_{SW} pin maximum voltage is set by the maximum output voltage plus the output diode forward voltage. The diode forward voltage is typically 0.5 V for Schottky diodes and 0.8 V for ultrafast recovery diodes

$$V_{SW(MAX)} = V_{OUT(MAX)} + V_F$$

where:

V_F = output diode forward voltage.

In the flyback topology, peak V_{SW} voltage is governed by:

$$V_{SW(MAX)} = V_{CC(MAX)} + (V_{OUT} + V_F) \times N$$

where:

N = transformer turns ratio, primary over secondary.

When the power switch turns off, there exists a voltage spike superimposed on top of the steady-state voltage. Usually this voltage spike is caused by transformer leakage inductance charging stray capacitance between the V_{SW} and PGND pins. To prevent the voltage at the V_{SW} pin from exceeding the maximum rating, a transient voltage suppressor in series with a diode is paralleled with the primary windings. Another method of clamping switch voltage is to connect a transient voltage suppressor between the V_{SW} pin and ground.

Magnetic Component Selection

When choosing a magnetic component, one must consider factors such as peak current, core and ferrite material, output voltage ripple, EMI, temperature range, physical size and cost. In boost circuits, the average inductor current is the product of output current and voltage gain (V_{OUT}/V_{CC}), assuming 100% energy transfer efficiency. In continuous conduction mode, inductor ripple current is

$$I_{RIPPLE} = \frac{V_{CC}(V_{OUT} - V_{CC})}{(f)(L)(V_{OUT})}$$

where:

$f = 280 \text{ kHz}$ for CS5171/2 and 560 kHz for CS5173/4.

The peak inductor current is equal to average current plus half of the ripple current, which should not cause inductor saturation. The above equation can also be referenced when selecting the value of the inductor based on the tolerance of the ripple current in the circuits. Small ripple current provides the benefits of small input capacitors and greater output current capability. A core geometry like a rod or barrel is prone to generating high magnetic field radiation, but is relatively cheap and small. Other core geometries, such as toroids, provide a closed magnetic loop to prevent EMI.

Input Capacitor Selection

In boost circuits, the inductor becomes part of the input filter, as shown in Figure 35. In continuous mode, the input current waveform is triangular and does not contain a large pulsed current, as shown in Figure 34. This reduces the requirements imposed on the input capacitor selection. During continuous conduction mode, the peak to peak inductor ripple current is given in the previous section. As we can see from Figure 34, the product of the inductor current ripple and the input capacitor's effective series resistance (ESR) determine the V_{CC} ripple. In most applications, input capacitors in the range of $10 \mu\text{F}$ to $100 \mu\text{F}$ with an ESR less than 0.3Ω work well up to a full 1.5 A switch current.

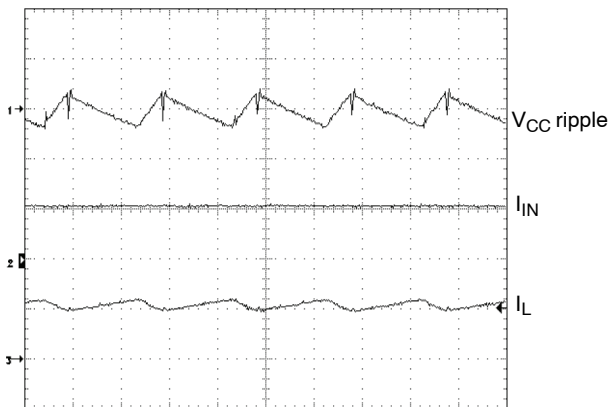


Figure 34. Boost Input Voltage and Current Ripple Waveforms

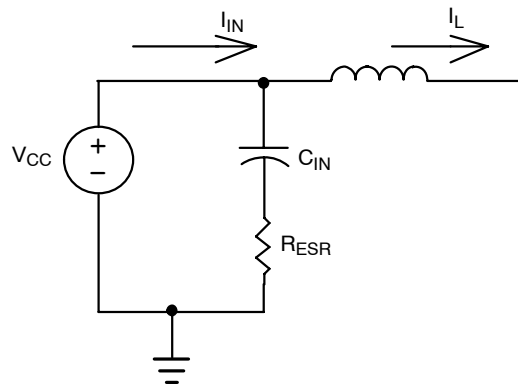


Figure 35. Boost Circuit Effective Input Filter

The situation is different in a flyback circuit. The input current is discontinuous and a significant pulsed current is seen by the input capacitors. Therefore, there are two requirements for capacitors in a flyback regulator: energy storage and filtering. To maintain a stable voltage supply to the chip, a storage capacitor larger than $20 \mu\text{F}$ with low ESR is required. To reduce the noise generated by the inductor, insert a $1.0 \mu\text{F}$ ceramic capacitor between V_{CC} and ground as close as possible to the chip.

Output Capacitor Selection

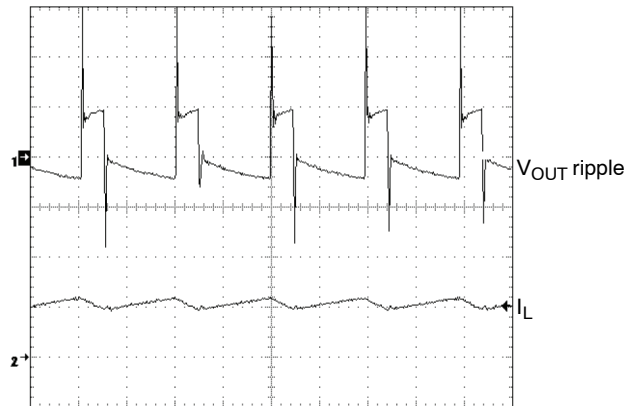


Figure 36. Typical Output Voltage Ripple

By examining the waveforms shown in Figure 36, we can see that the output voltage ripple comes from two major sources, namely capacitor ESR and the charging/discharging of the output capacitor. In boost circuits, when the power switch turns off, I_L flows into the output capacitor causing an instant $\Delta V = I_{IN} \times \text{ESR}$. At the same time, current $I_L - I_{OUT}$ charges the capacitor and increases the output voltage gradually. When the power switch is turned on, I_L is shunted to ground and I_{OUT} discharges the output capacitor. When the I_L ripple is small enough, I_L can be treated as a constant and is equal to input current I_{IN} .

Summing up, the output voltage peak–peak ripple can be calculated by:

$$V_{OUT(RIPPLE)} = \frac{(I_{IN} - I_{OUT})(1 - D)}{(C_{OUT})(f)} + \frac{I_{OUT}D}{(C_{OUT})(f)} + I_{IN} \times ESR$$

The equation can be expressed more conveniently in terms of V_{CC} , V_{OUT} and I_{OUT} for design purposes as follows:

$$V_{OUT(RIPPLE)} = \frac{I_{OUT}(V_{OUT} - V_{CC})}{(C_{OUT})(f)} \times \frac{1}{(C_{OUT})(f)} + \frac{(I_{OUT})(V_{OUT})(ESR)}{V_{CC}}$$

The capacitor RMS ripple current is:

$$I_{RIPPLE} = \sqrt{(I_{IN} - I_{OUT})^2(1 - D) + (I_{OUT})^2(D)}$$

$$= I_{OUT} \sqrt{\frac{V_{OUT} - V_{CC}}{V_{CC}}}$$

Although the above equations apply only for boost circuits, similar equations can be derived for flyback circuits.

Reducing the Current Limit

In some applications, the designer may prefer a lower limit on the switch current than 1.5 A. An external shunt can be connected between the V_C pin and ground to reduce its clamp voltage. Consequently, the current limit of the internal power transistor current is reduced from its nominal value.

The voltage on the V_C pin can be evaluated with the equation

$$V_C = I_{SW}R_EA_V$$

where:

$R_E = .063\Omega$, the value of the internal emitter resistor;

$A_V = 5 \text{ V/V}$, the gain of the current sense amplifier.

Since R_E and A_V cannot be changed by the end user, the only available method for limiting switch current below 1.5 A is to clamp the V_C pin at a lower voltage. If the maximum switch or inductor current is substituted into the equation above, the desired clamp voltage will result.

A simple diode clamp, as shown in Figure 37, clamps the V_C voltage to a diode drop above the voltage on resistor R_3 .

Unfortunately, such a simple circuit is not generally acceptable if V_{IN} is loosely regulated.

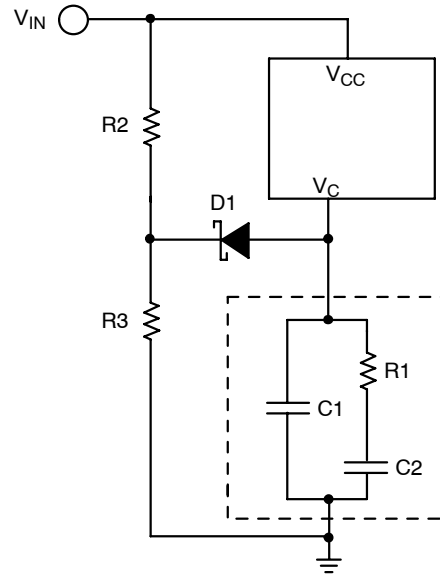


Figure 37. Current Limiting using a Diode Clamp

Another solution to the current limiting problem is to externally measure the current through the switch using a sense resistor. Such a circuit is illustrated in Figure 38.

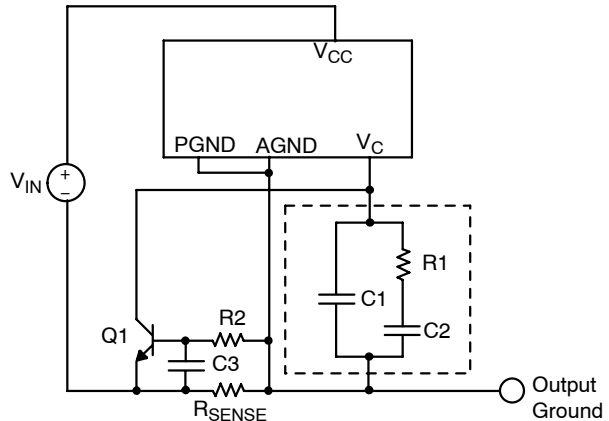


Figure 38. Current Limiting using a Current Sense Resistor

The switch current is limited to

$$I_{SWITCH(PEAK)} = \frac{V_{BE(Q1)}}{R_{SENSE}}$$

where:

$V_{BE(Q1)}$ is the base–emitter voltage drop of $Q1$, typically 0.65 V.

The improved circuit does not require a regulated voltage to operate properly. Unfortunately, a price must be paid for this convenience in the overall efficiency of the circuit. The designer should note that the input and output grounds are no longer common. Also, the addition of the current sense resistor, R_{SENSE} , results in a considerable power loss which increases with the duty cycle. Resistor R2 and capacitor C3 form a low-pass filter to remove noise.

Subharmonic Oscillation

Subharmonic oscillation (SHM) is a problem found in current-mode control systems, where instability results when duty cycle exceeds 50%. SHM only occurs in switching regulators with a continuous inductor current. This instability is not harmful to the converter and usually does not affect the output voltage regulation. SHM will increase the radiated EM noise from the converter and can cause, under certain circumstances, the inductor to emit high-frequency audible noise.

SHM is an easily remedied problem. The rising slope of the inductor current is supplemented with internal “slope compensation” to prevent any duty cycle instability from carrying through to the next switching cycle. In the CS517x family, slope compensation is added during the entire switch on-time, typically in the amount of 180 mA/μs.

In some cases, SHM can rear its ugly head despite the presence of the onboard slope compensation. The simple cure to this problem is more slope compensation to avoid the unwanted oscillation. In that case, an external circuit, shown in Figure 39, can be added to increase the amount of slope compensation used. This circuit requires only a few components and is “tacked on” to the compensation network.

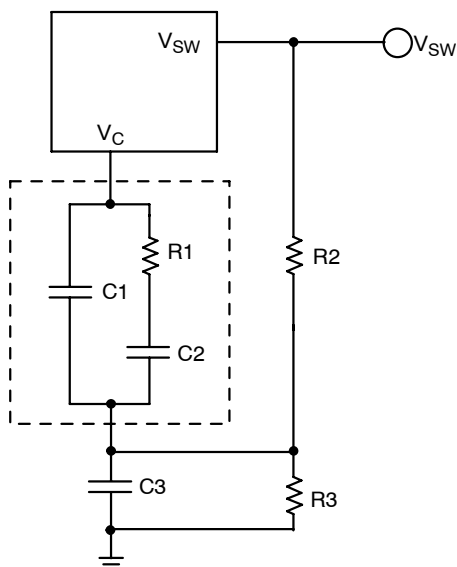


Figure 39. Technique for Increasing Slope Compensation

The dashed box contains the normal compensation circuitry to limit the bandwidth of the error amplifier. Resistors R2 and R3 form a voltage divider off of the V_{SW} pin. In normal operation, V_{SW} looks similar to a square wave, and is dependent on the converter topology. Formulas for calculating V_{SW} in the boost and flyback topologies are given in the section “ V_{SW} Voltage Limit.” The voltage on V_{SW} charges capacitor C3 when the switch is off, causing the voltage at the V_C pin to shift upwards. When the switch turns on, C3 discharges through R3, producing a negative slope at the V_C pin. This negative slope provides the slope compensation.

The amount of slope compensation added by this circuit is

$$\frac{\Delta I}{\Delta T} = V_{SW} \left(\frac{R_3}{R_2 + R_3} \right) \left(1 - e^{\frac{-(1-D)}{R_3 C_3 f_{SW}}} \right) \left(\frac{f_{SW}}{(1-D) R_E A_V} \right)$$

where:

$\Delta I/\Delta T$ = the amount of slope compensation added (A/s);

V_{SW} = the voltage at the switch node when the transistor is turned off (V);

f_{SW} = the switching frequency, typically 280 kHz (CS5171/3) or 560 kHz (CS5172/4) (Hz);

D = the duty cycle;

$R_E = 0.063 \Omega$, the value of the internal emitter resistor;

$A_V = 5 \text{ V/V}$, the gain of the current sense amplifier.

In selecting appropriate values for the slope compensation network, the designer is advised to choose a convenient capacitor, then select values for R2 and R3 such that the amount of slope compensation added is 100 mA/μs. Then R2 may be increased or decreased as necessary. Of course, the series combination of R2 and R3 should be large enough to avoid drawing excessive current from V_{SW} . Additionally, to ensure that the control loop stability is *improved*, the time constant formed by the additional components should be chosen such that

$$R_3 C_3 < \frac{1-D}{f_{SW}}$$

Finally, it is worth mentioning that the added slope compensation is a tradeoff between duty cycle stability and transient response. The more slope compensation a designer adds, the slower the transient response will be, due to the external circuitry interfering with the proper operation of the error amplifier.

Soft-Start

Through the addition of an external circuit, a Soft-Start function can be added to the CS5171/2/3/4 family of components. Soft-Start circuitry prevents the V_C pin from slamming high during startup, thereby inhibiting the inductor current from rising at a high slope.

This circuit, shown in Figure 40, requires a minimum number of components and allows the Soft-Start circuitry to activate any time the SS pin is used to restart the converter.

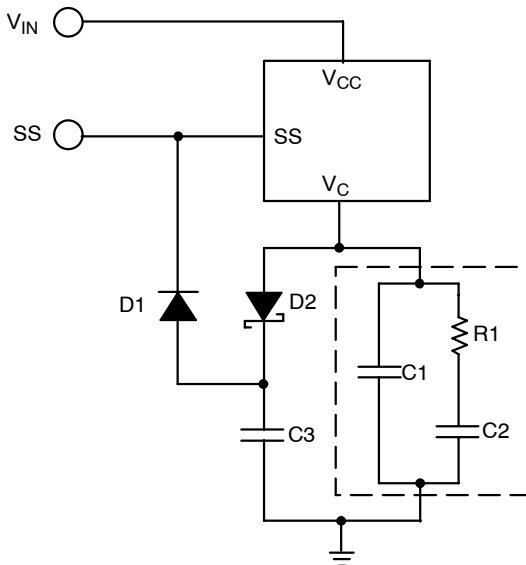


Figure 40. Soft Start

Resistor R1 and capacitors C1 and C2 form the compensation network. At turn on, the voltage at the V_C pin starts to come up, charging capacitor C3 through Schottky diode D2, clamping the voltage at the V_C pin such that switching begins when V_C reaches the V_C threshold, typically 1.05 V (refer to graphs for detail over temperature).
 $V_C = V_F(D2) + V_{C3}$

Therefore, C3 slows the startup of the circuit by limiting the voltage on the V_C pin. The Soft-Start time increases with the size of C3.

Diode D1 discharges C3 when SS is low. If the shutdown function is not used with this part, the cathode of D1 should be connected to V_{IN}.

Calculating Junction Temperature

To ensure safe operation of the CS5171/2/3/4, the designer must calculate the on-chip power dissipation and determine its expected junction temperature. Internal thermal protection circuitry will turn the part off once the junction temperature exceeds 180°C ± 30°. However, repeated operation at such high temperatures will ensure a reduced operating life.

Calculation of the junction temperature is an imprecise but simple task. First, the power losses must be quantified. There are three major sources of power loss on the CS517x:

- biasing of internal control circuitry, P_{BIAS}
- switch driver, P_{DRIVER}
- switch saturation, P_{SAT}

The internal control circuitry, including the oscillator and linear regulator, requires a small amount of power even

when the switch is turned off. The specifications section of this datasheet reveals that the typical operating current, I_O, due to this circuitry is 5.5 mA. Additional guidance can be found in the graph of operating current vs. temperature. This graph shows that I_O is strongly dependent on input voltage, V_{IN}, and temperature. Then

$$P_{BIAS} = V_{IN} I_O$$

Since the onboard switch is an NPN transistor, the base drive current must be factored in as well. This current is drawn from the V_{IN} pin, in addition to the control circuitry current. The base drive current is listed in the specifications as ΔI_{CC}/ΔI_{SW}, or switch transconductance. As before, the designer will find additional guidance in the graphs. With that information, the designer can calculate

$$P_{DRIVER} = V_{IN} I_{SW} \times \frac{I_{CC}}{\Delta I_{SW}} \times D$$

where:

I_{SW} = the current through the switch;

D = the duty cycle or percentage of switch on-time.

I_{SW} and D are dependent on the type of converter. In a boost converter,

$$I_{SW(AVG)} \approx I_{LOAD} \times D \times \frac{1}{\text{Efficiency}}$$

$$D \approx \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

In a flyback converter,

$$I_{SW(AVG)} \approx \frac{V_{OUT} I_{LOAD}}{V_{IN}} \times \frac{1}{\text{Efficiency}}$$

$$D \approx \frac{V_{OUT}}{V_{OUT} + \frac{N_S}{N_P} V_{IN}}$$

The switch saturation voltage, V_{(CE)SAT}, is the last major source of on-chip power loss. V_{(CE)SAT} is the collector-emitter voltage of the internal NPN transistor when it is driven into saturation by its base drive current. The value for V_{(CE)SAT} can be obtained from the specifications or from the graphs, as “Switch Saturation Voltage.” Thus,

$$P_{SAT} \approx V_{(CE)SAT} I_{SW} \times D$$

Finally, the total on-chip power losses are

$$P_D = P_{BIAS} + P_{DRIVER} + P_{SAT}$$

Power dissipation in a semiconductor device results in the generation of heat in the junctions at the surface of the chip. This heat is transferred to the surface of the IC package, but a thermal gradient exists due to the resistive properties of the package molding compound. The magnitude of the thermal gradient is expressed in manufacturers’ data sheets as θ_{JA}, or junction-to-ambient thermal resistance. The on-chip junction temperature can be calculated if θ_{JA}, the air temperature near the surface of the IC, and the on-chip power dissipation are known.

CS5171, CS5172, CS5173, CS5174

$$T_J = T_A + (P_D \theta_{JA})$$

where:

T_J = IC or FET junction temperature (°C);

T_A = ambient temperature (°C);

P_D = power dissipated by part in question (W);

θ_{JA} = junction-to-ambient thermal resistance (°C/W).

For the CS517x, θ_{JA} = 165°C/W.

Once the designer has calculated T_J , the question of whether the CS517x can be used in an application is settled. If T_J exceeds 150°C, the absolute maximum allowable junction temperature, the CS517x is not suitable for that application.

If T_J approaches 150°C, the designer should consider possible means of reducing the junction temperature. Perhaps another converter topology could be selected to reduce the switch current. Increasing the airflow across the surface of the chip might be considered to reduce T_A .

Circuit Layout Guidelines

In any switching power supply, circuit layout is very important for proper operation. Rapidly switching currents combined with trace inductance generates voltage

transitions that can cause problems. Therefore the following guidelines should be followed in the layout.

1. In boost circuits, high AC current circulates within the loop composed of the diode, output capacitor, and on-chip power transistor. The length of associated traces and leads should be kept as short as possible. In the flyback circuit, high AC current loops exist on both sides of the transformer. On the primary side, the loop consists of the input capacitor, transformer, and on-chip power transistor, while the transformer, rectifier diodes, and output capacitors form another loop on the secondary side. Just as in the boost circuit, all traces and leads containing large AC currents should be kept short.
2. Separate the low current signal grounds from the power grounds. Use single point grounding or ground plane construction for the best results.
3. Locate the voltage feedback resistors as near the IC as possible to keep the sensitive feedback wiring short. Connect feedback resistors to the low current analog ground.

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping [†]
CS5171ED8	-40°C < T_J < 125°C	SOIC-8	95 Units/Rail
CS5171EDR8			2500 Tape & Reel
CS5172ED8			95 Units/Rail
CS5172EDR8			2500 Tape & Reel
CS5173ED8			95 Units/Rail
CS5173EDR8			2500 Tape & Reel
CS5173EDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel
CS5174ED8		SOIC-8	95 Units/Rail
CS5174EDR8			2500 Tape & Reel
CS5171GD8	0°C < T_J < 125°C	SOIC-8 (Pb-Free)	95 Units/Rail
CS5171GDR8			2500 Tape & Reel
CS5171GDR8G			2500 Tape & Reel
CS5172GD8		SOIC-8	95 Units/Rail
CS5172GDR8			2500 Tape & Reel
CS5173GD8			95 Units/Rail
CS5173GDR8			2500 Tape & Reel
CS5174GD8			95 Units/Rail
CS5174GDR8			2500 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

CS5171, CS5172, CS5173, CS5174

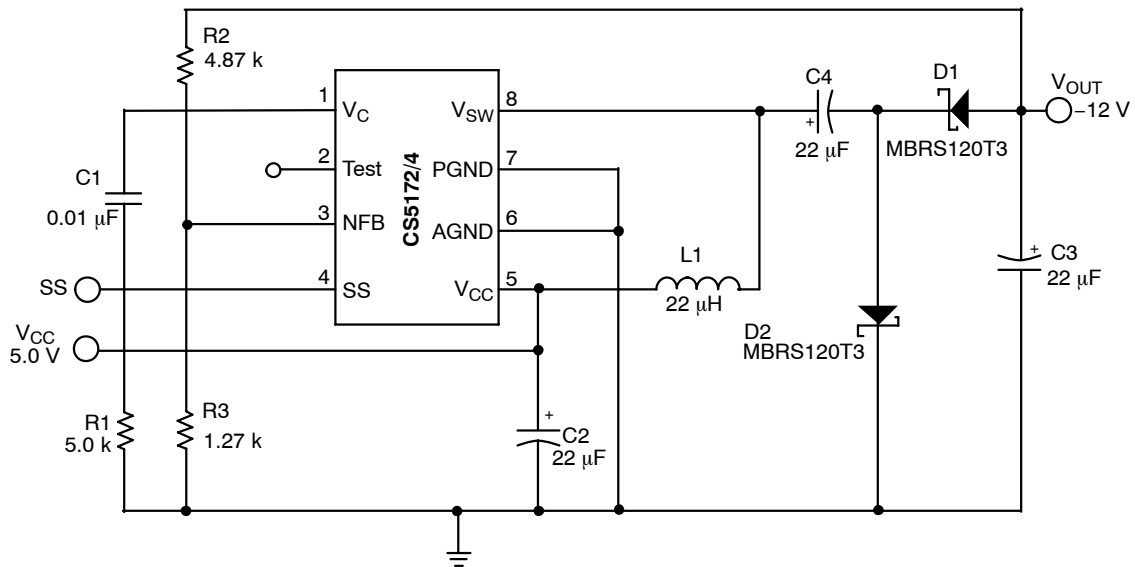


Figure 41. Additional Application Diagram, 5.0 V to -12 V/ 75 mA Inverting Converter

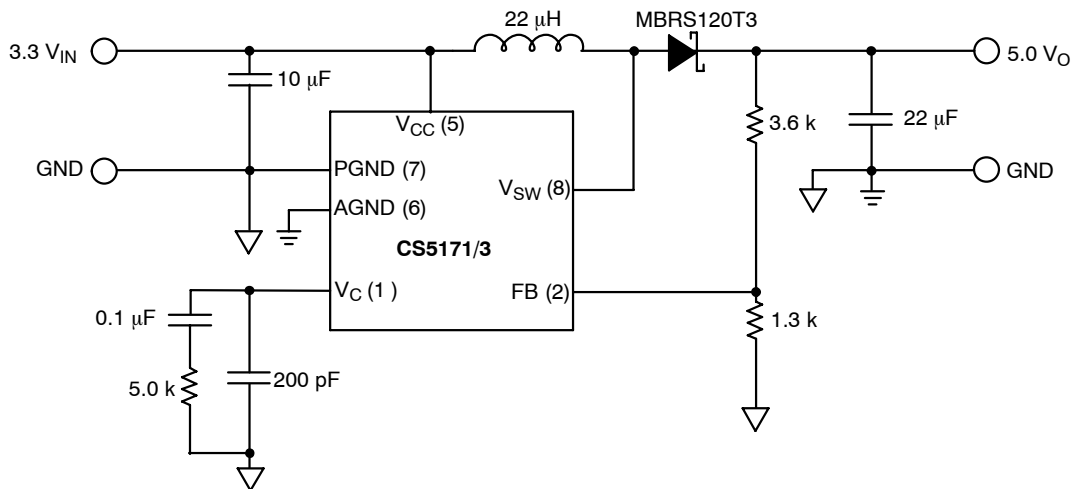


Figure 42. Additional Application Diagram, 3.3 V Input, 5.0 V/ 400 mA Output Boost Converter

CS5171, CS5172, CS5173, CS5174

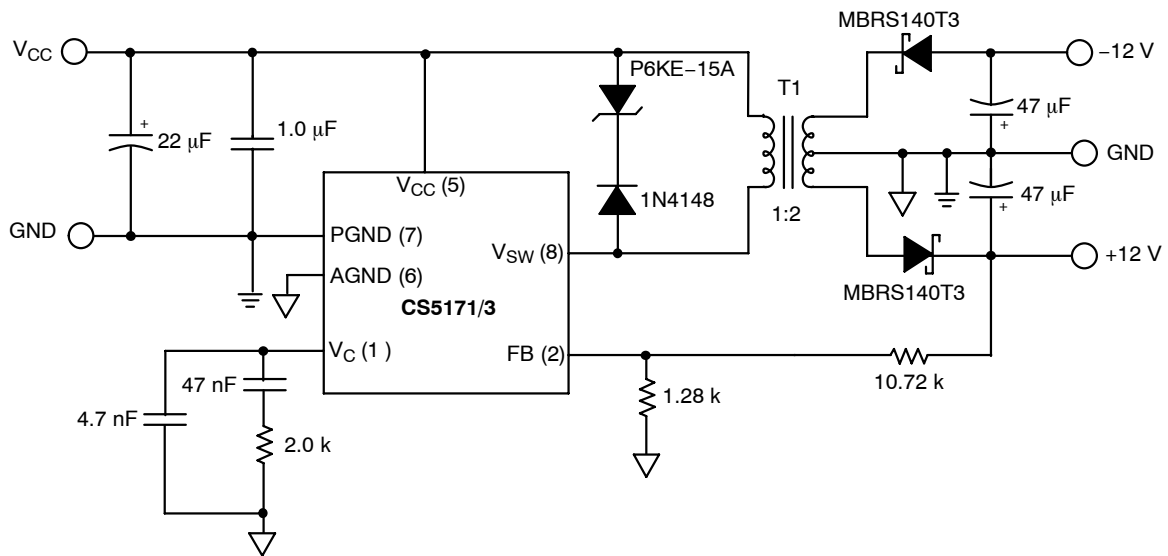


Figure 43. Additional Application Diagram, 2.7 to 13 V Input, ± 12 V/ 200 mA Output Flyback Converter

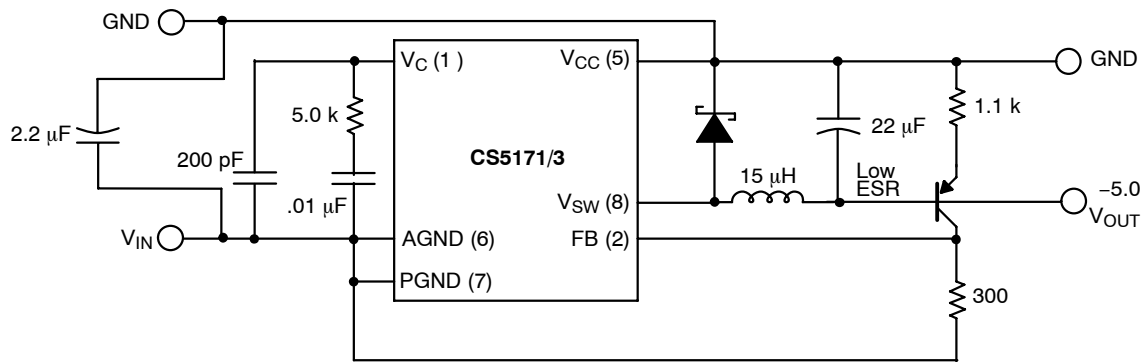


Figure 44. Additional Application Diagram, -9.0 V to -28 V Input, -5.0 V/700 mA Output Inverted Buck Converter

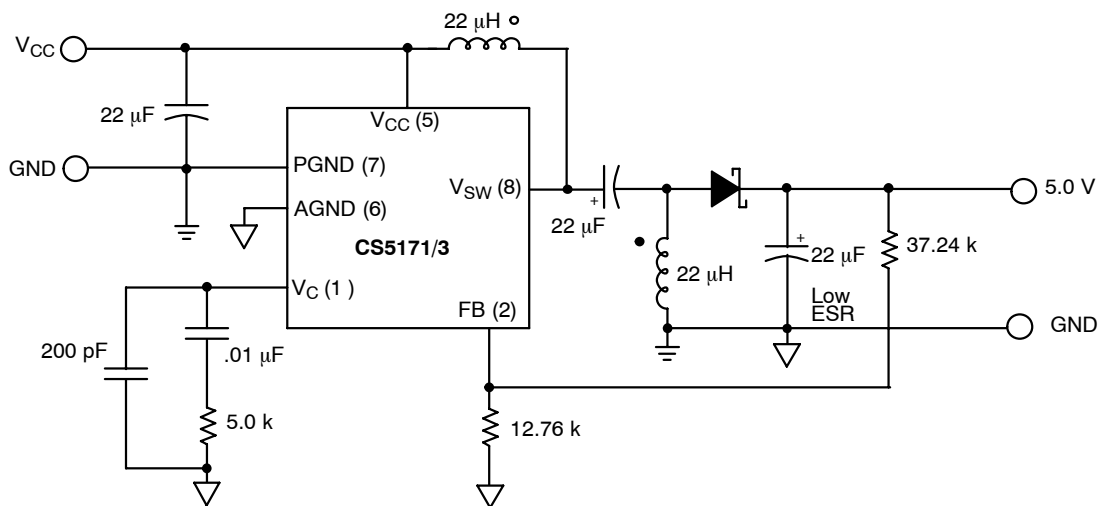


Figure 45. Additional Application Diagram, 2.7 V to 28 V Input, 5.0 V Output SEPIC Converter

CS5171, CS5172, CS5173, CS5174

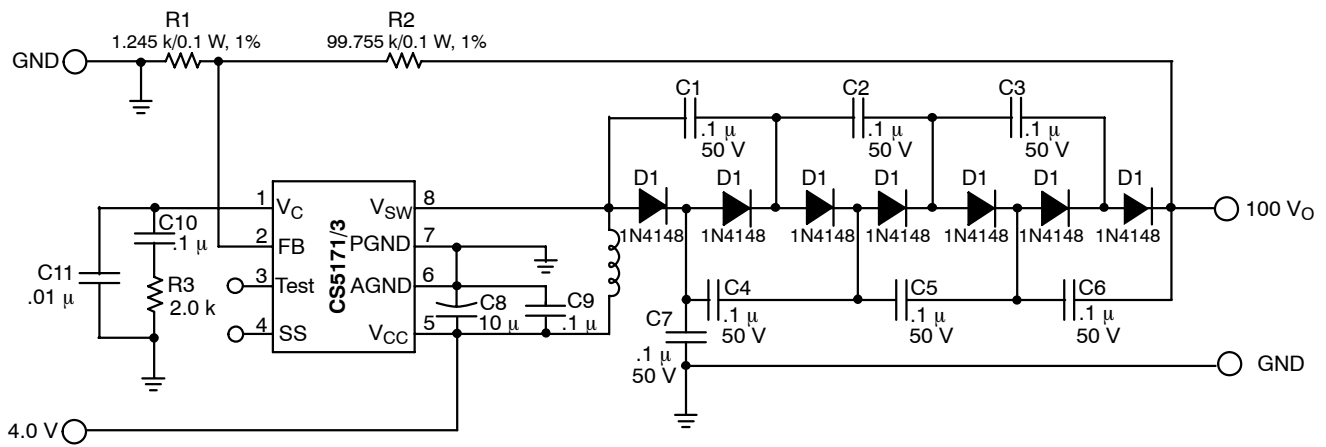


Figure 46. Additional Application Diagram, 4.0 V Input, 100 V / 10 mA Output Boost Converter with Output Voltage Multiplier

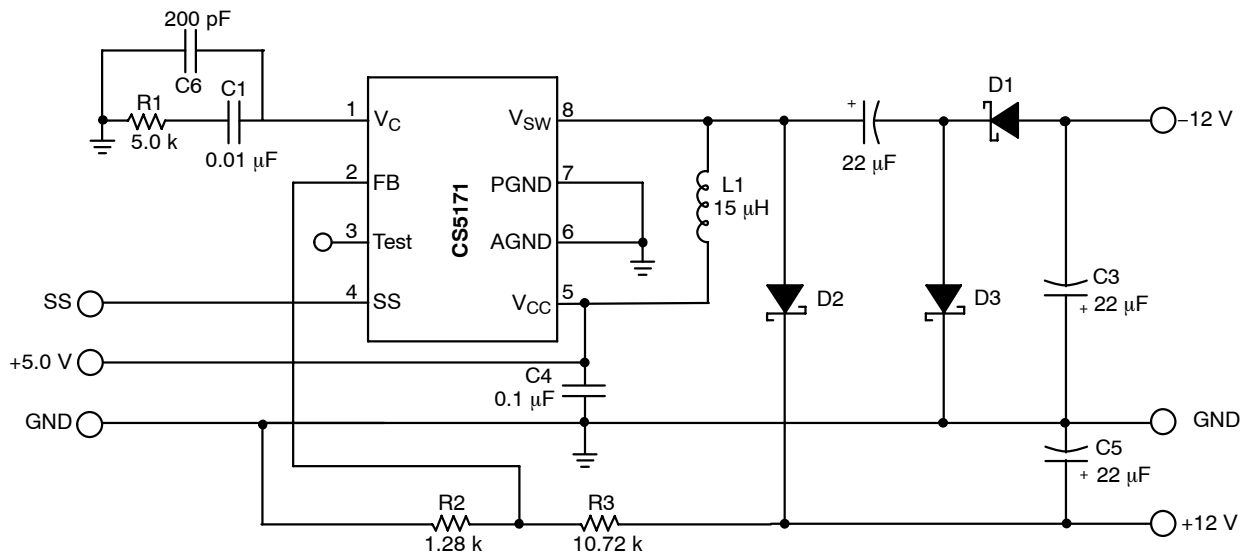


Figure 47. Additional Application Diagram, 5.0 V Input, ± 12 V Output Dual Boost Converter

CS5211

Low Voltage Synchronous Buck Controller

The CS5211 is a low voltage synchronous buck controller. It contains all required circuitry for a synchronous buck converter using external N-Channel MOSFETs. High current internal gate drivers are capable of driving high gate capacitance of low $R_{DS(on)}$ NFETs for better efficiency. The V^2 ™ control architecture is used to achieve unmatched transient response, the best overall regulation and the simplest loop compensation. The CS5211 is in a 14-pin package to allow the designer added flexibility.

The CS5211 provides overcurrent protection, undervoltage lockout, Soft Start and built in adaptive nonoverlap. The CS5211 also provides adjustable fixed frequency range of 150 kHz to 750 kHz. This gives the designer more flexibility to make efficiency and component size compromises. The CS5211 will operate over a 4.5 V to 14 V range using either single or dual input voltage.

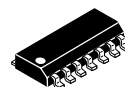
Features

- Switching Regulator Controller
 - N-Channel Synchronous Buck Design
 - V^2 Control Topology
 - 200 ns Transient Response
 - Programmable Fixed Frequency of 150 kHz–750 kHz
 - 1.0 V 1.5% Internal Reference
 - Lossless Inductor Sensing Overcurrent Protection
 - Hiccup Mode Short Circuit Protection
 - Programmable Soft Start
 - 40 ns GATE Rise and Fall Times (3.3 nF Load)
 - 70 ns Adaptive FET Nonoverlap Time
 - Differential Remote Sense Capability
- System Power Management
 - 5.0 V or 12 V Operation
 - Undervoltage Lockout
 - On/Off Control Through Use of the COMP Pin



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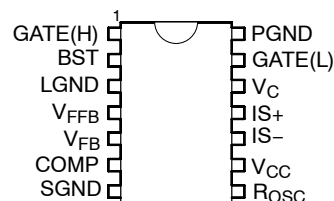
**SOIC-14
D SUFFIX
CASE 751A**

MARKING DIAGRAM



x = E or G
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 96 of this data sheet.

CS5211

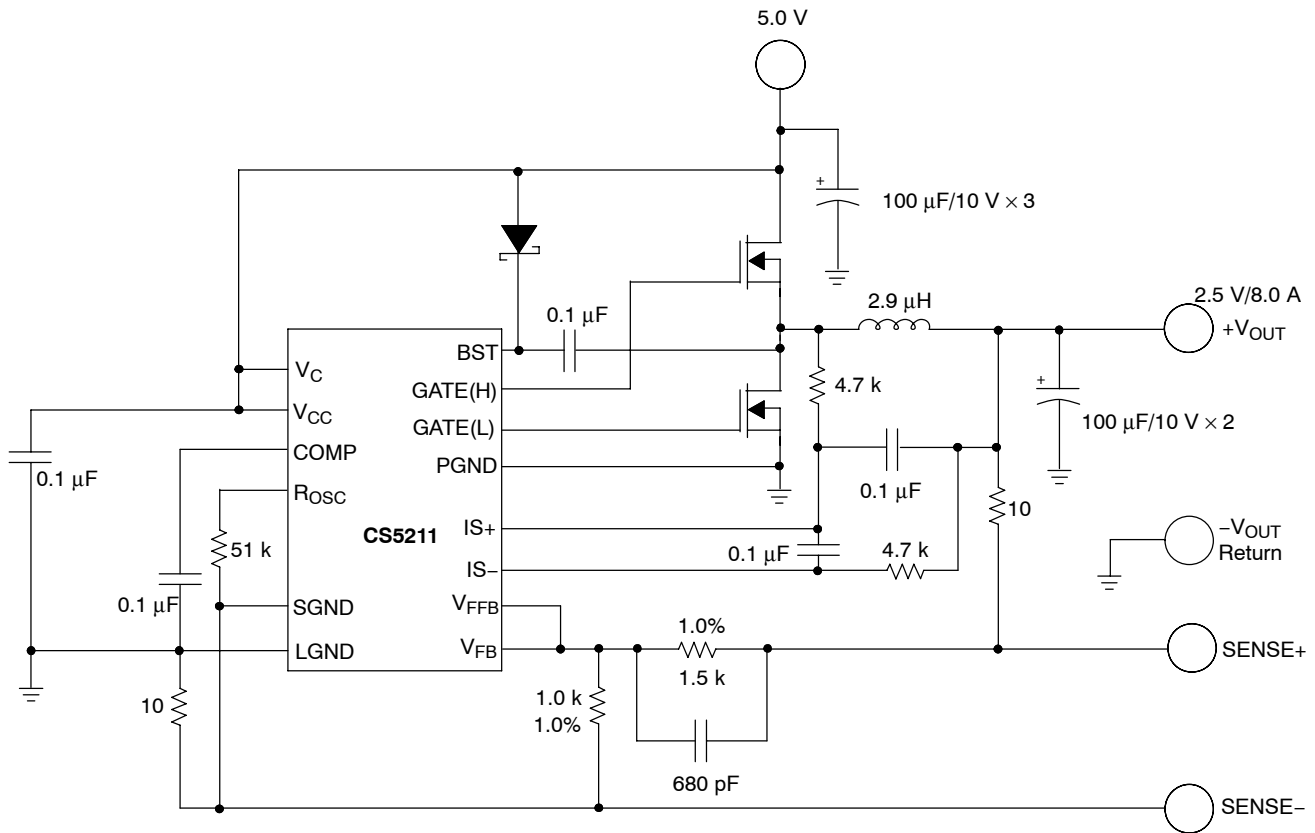


Figure 1. Application Diagram, 5.0 V to 2.5 V/8.0 A Converter with Differential Remote Sense

MAXIMUM RATINGS*

Rating	Value	Unit
Operating Junction Temperature, T_J	150	°C
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1)	230 peak	°C
Storage Temperature Range, T_S	-65 to +150	°C
Package Thermal Resistance: Junction-to-Case, $R_{\theta JC}$ Junction-to-Ambient, $R_{\theta JA}$	30 125	°C/W °C/W
ESD Susceptibility (Human Body Model)	2.0	kV
JEDEC Moisture Sensitivity	1.0	-

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

MAXIMUM RATINGS

Pin Name	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
IC Power Input	V_{CC}	16 V	-0.3 V	N/A	50 mA DC
Power input for the low side driver	V_C	16 V	-0.3 V	N/A	1.5 A Peak, 200 mA DC
Power Supply input for the high side driver	BST	20 V	-0.3 V	N/A	1.5 A Peak, 200 mA DC
Compensation Capacitor	COMP	6.0 V	-0.3 V	1.0 mA	1.0 mA
Voltage Feedback Input	V_{FB}	6.0 V	-0.3 V	1.0 mA	1.0 mA
Oscillator Resistor	R_{OSC}	6.0 V	-0.3 V	1.0 mA	1.0 mA

MAXIMUM RATINGS (continued)

Pin Name	Pin Symbol	V _{MAX}	V _{MIN}	I _{SOURCE}	I _{SINK}
Fast Feedback Input	V _{FFB}	6.0 V	–0.3 V	1.0 mA	1.0 mA
High-Side FET Driver	GATE(H)	20 V	–0.3 V –2.0 V for 50 ns	1.5 A Peak 200 mA DC	1.5 A Peak 200 mA DC
Low-Side FET Driver	GATE(L)	16 V	–0.3 V –2.0 V for 50 ns	1.5 A Peak 200 mA DC	1.5 A Peak 200 mA DC
Positive Current Sense	IS+	6.0 V	–0.3 V	1.0 mA	1.0 mA
Negative Current Sense	IS–	6.0 V	–0.3 V	1.0 mA	1.0 mA
Power Ground	PGND	0.3 V	–0.3 V	1.5 A Peak, 200 mA DC	N/A
Logic Ground	LGND	0 V	0 V	100 mA	N/A
Sense Ground	SGND	0.3 V	–0.3 V	1.0 mA	1.0 mA

ELECTRICAL CHARACTERISTICS (–40°C < T_A < 85°C; –40°C < T_J < 125°C; 4.5 V < V_{CC}, V_C < 14 V;
7.0 V < BST < 20 V; C_{GATE(H)} = C_{GATE(L)} = 3.3 nF; R_{OSC} = 51 k; C_{COMP} = 0.1 μF, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Error Amplifier					
V _{FB} Bias Current	V _{FB} = 0 V	–	0.1	1.0	μA
COMP Source Current	V _{FB} = 0.8 V	15	30	60	μA
COMP SINK Current	V _{FB} = 1.2 V	15	30	60	μA
Open Loop Gain	–	–	98	–	dB
Unity Gain Bandwidth	C = 0.1 μF	–	50	–	kHz
PSRR @ 1.0 kHz	–	–	70	–	dB
Output Transconductance	–	–	32	–	mmho
Output Impedance	–	–	2.5	–	MΩ
Reference Voltage	–0.1 V < SGND < 0.1 V, COMP = V _{FB} , Measure V _{FB} to SGND	0.977	0.992	1.007	V
COMP Max Voltage	V _{FB} = 0.8 V	2.5	3.0	–	V
COMP Min Voltage	V _{FB} = 1.2 V	–	0.1	0.2	V

GATE(H) and GATE(L)

High Voltage (AC)	GATE(L), GATE(H) 0.5 nF < C _{GATE(H)} = C _{GATE(L)} < 10 nF	V _C – 0.5 BST – 0.5	–	–	V
Low Voltage (AC)	GATE(L) or GATE(H) 0.5 nF < C _{GATE(H)} ; C _{GATE(L)} < 10 nF	–	–	0.5	V
Rise Time	V _C = BST = 10 V, Measure: 1.0 V < GATE(L) < 9.0 V, 1.0 V < GATE(H) < 9.0 V	–	40	80	ns
Fall Time	V _C = BST = 10 V, Measure: 1.0 V < GATE(L) < 9.0 V, 1.0 V < GATE(H) < 9.0 V	–	40	80	ns
GATE(H) to GATE(L) Delay	GATE(H) < 2.0 V, GATE(L) > 2.0 V	40	70	110	ns
GATE(L) to GATE(H) Delay	GATE(L) < 2.0 V, GATE(H) > 2.0 V	40	70	110	ns
GATE(H)/(L) Pull-Down	Resistance to PGND	20	50	115	KΩ

2. Guaranteed by design. Not tested in production.

CS5211

ELECTRICAL CHARACTERISTICS (continued) ($-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$; $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$; $4.5\text{ V} < V_{CC}$, $V_C < 14\text{ V}$; $7.0\text{ V} < \text{BST} < 20\text{ V}$; $C_{\text{GATE(H)}} = C_{\text{GATE(L)}} = 3.3\text{ nF}$; $R_{\text{OSC}} = 51\text{ k}$; $C_{\text{COMP}} = 0.1\text{ }\mu\text{F}$, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit

Overcurrent Protection

OVC Comparator Offset Voltage	$0\text{ V} < \text{IS+} < V_{CC}$, $0\text{ V} < \text{IS-} < V_{CC}$	54	60	66	mV
IS+ Bias Current	$0\text{ V} < \text{IS+} < V_{CC}$	-1.0	0.1	1.0	μA
IS- Bias Current	$0\text{ V} < \text{IS-} < V_{CC}$	-1.0	0.1	1.0	μA
COMP Discharge Threshold	–	0.20	0.25	0.30	V
COMP Discharge Current in OVC Fault Mode	COMP = 1.0 V	2.0	5.0	8.0	μA

PWM Comparator

Transient Response	COMP = 0 – 1.5 V, V_{FFB} , 20 mV overdrive	–	100	200	ns
PWM Comparator Offset	$V_{\text{FB}} = V_{\text{FFB}} = 0\text{ V}$; Increase COMP until GATE(H) starts switching	0.425	0.475	0.525	V
Artificial Ramp	Duty Cycle = 90%	40	70	100	mV
V_{FFB} Bias Current	$V_{\text{FFB}} = 0\text{ V}$	–	0.1	1.0	μA
V_{FFB} Input Range	Note 3.	–	–	1.1	V
Minimum Pulse Width	–	–	–	200	ns

Oscillator

Switching Frequency	$R_{\text{OSC}} = 18\text{ k}$	600	750	900	kHz
Switching Frequency	$R_{\text{OSC}} = 51\text{ k}$	240	300	360	kHz
Switching Frequency	$R_{\text{OSC}} = 115\text{ k}\Omega$	120	150	180	kHz
R_{OSC} Voltage	–	1.21	1.25	1.29	V

General Electrical Specifications

V_{CC} Supply Current	COMP = 0 V (no switching)	–	5.0	8.0	mA
BST/ V_C Supply Current	COMP = 0 V (no switching)	–	2.0	3.0	mA
Start Threshold	GATE(H) Switching, COMP Charging	3.90	4.05	4.20	V
Stop Threshold	GATE(H) Not Switching, COMP Not Charging	3.75	3.90	4.05	V
Hysteresis	Start–Stop	100	150	200	mV
Sense Ground Current	Note 3.	–	0.15	1.00	mA

3. Recommended maximum operating voltage between the three grounds is 200 mV.

PACKAGE PIN DESCRIPTION

PIN NO.	PIN SYMBOL	FUNCTION
1	GATE(H)	High Side Switch FET driver pin. Capable of delivering peak currents of 1.0 A.
2	BST	Power supply input for the high side driver.
3	LGND	Reference ground. All control circuits are referenced to this pin. IC substrate connection.
4	V _{FFB}	Input for the PWM comparator.
5	V _{FB}	Error amplifier input.
6	COMP	Error Amp output. PWM Comparator reference input. A capacitor to LGND provides error amp compensation.
7	SGND	Internal reference is connected to this ground. Connect directly at the load for ground remote sensing.
8	R _{OSC}	A resistor from this pin to SGND sets switching frequency.
9	V _{CC}	Input Power Supply Pin. It supplies power to control circuitry. A 0.1 μ F Decoupling cap is recommended.
10	IS-	Negative input for overcurrent comparator.
11	IS+	Positive input for overcurrent comparator.
12	V _C	Power supply input for the low side driver.
13	GATE(L)	Low Side Synchronous FET driver pin. Capable of delivering peak currents of 1.0 A.
14	PGND	High Current ground for the GATE(H) and GATE(L) pins.

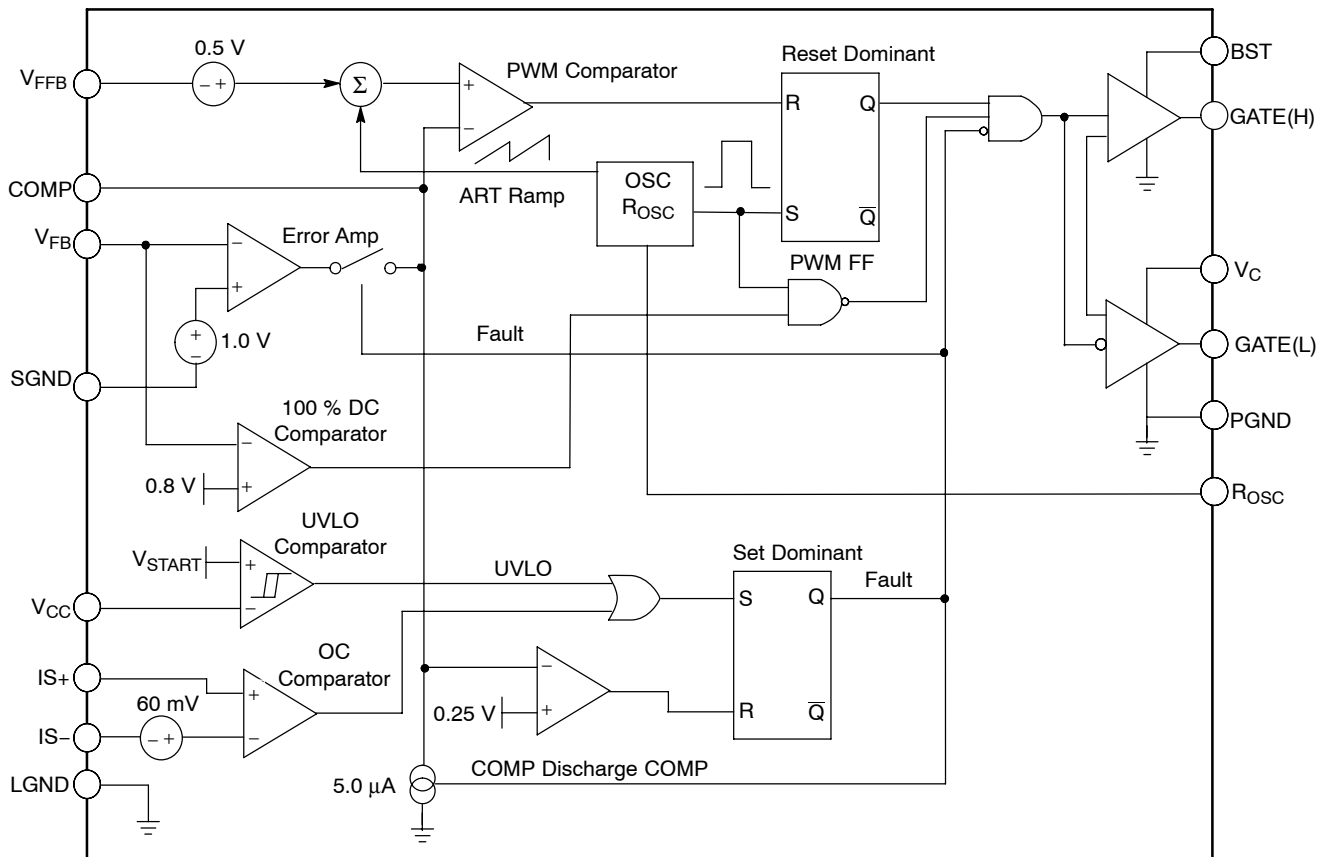


Figure 2. Block Diagram

THEORY OF OPERATION

V² Control Method

The V² method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variations in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.

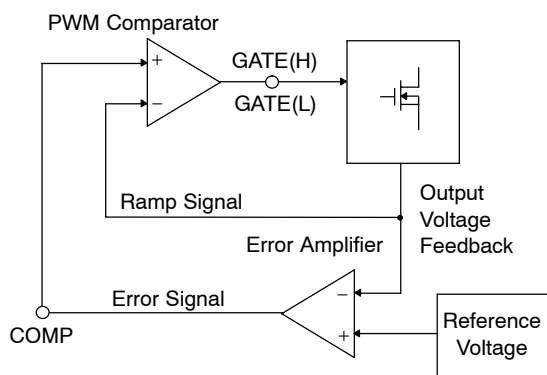


Figure 3. V² Control Block Diagram

The V² control method is illustrated in Figure 3. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of the change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to 0% or 100% duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the V² control scheme to compensate the duty cycle. Since the change in the inductor current modifies the ramp signal, as in current mode control, the V² control scheme has the same advantages in line transient response.

A change in load current will have an effect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this “slow” feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulations are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The V² method of control maintains a fixed error signal for both line and load variations, since both line and load affect the ramp signal.

Constant Frequency Operation

The CS5211 uses a constant frequency, trailing edge modulation architecture for generating PWM signal. During normal operation, the oscillator generates a narrow pulse at the beginning of each switching cycle to turn on the main switch. The main switch will be turned off when the ramp signal intersects with the output of the error amplifier (COMP pin voltage). Therefore, the switch duty cycle can be modified to regulate the output voltage to the desired value as line and load conditions change.

The major advantage of constant frequency operation is that the component selections, especially the magnetic component design, become very easy. The oscillator frequency of CS5211 is programmable from 150 kHz to 750 kHz using an external resistor connected from the ROSC pin to ground.

Startup

If there are no fault conditions and the fault latch is reset, the error amplifier will start charging the COMP pin capacitor after the CS5211 is powered up. The output of the error amplifier (COMP voltage) will ramp up linearly. The COMP capacitance and the source current of the error amplifier determine the slew rate of COMP voltage. The output of the error amplifier is connected internally to the inverting input of the PWM comparator and it is compared with the V_{FFB} pin voltage plus 0.5 V offset at the non-inverting input of the PWM comparator. Since V_{FFB} voltage is zero before the startup, the PWM comparator output will stay high until the COMP pin voltage hits 0.5 V. There is no switching action while the PWM comparator output is high.

After the COMP voltage exceeds the 0.5 V offset, the output of PWM comparator toggles and releases the PWM latch. The narrow pulse generated by the oscillator at the beginning of the next oscillator cycle will set the latch so that the main switch can be turned on and the regulator output voltage ramps up. When the output voltage achieves a level set by the COMP voltage, the main switch will be turned off. The V² control loop will adjust the main switch duty cycle as required to ensure the regulator output voltage tracks the

COMP voltage. Since the COMP voltage increases gradually, the soft start can be achieved. The start-up period ends when the output voltage reaches the level set by the external resistor divider.

Output Enable

Since there can be no switching until the COMP pin exceeds the 0.5 V offset built into the PWM comparator, the COMP pin can also be used for an enable function. Hold the COMP pin below 0.4 V with an open collector circuit to disable the output. When the COMP pin is released to enable startup, the user must ensure there is no leakage current from the enable circuit into COMP. During normal operation the COMP output is driven with only 5.0 μ A to 30 μ A internally.

Hiccup Mode Overcurrent Protection

Under normal load conditions, the voltage across the IS+ and IS- pins is less than the 60 mV overcurrent threshold. If the threshold is exceeded, the overcurrent fault latch is set, the high side gate driver is forced low, and the COMP pin is discharged with 5.0 μ A. There is no switching until the COMP voltage drops below a 0.25 V threshold. Then, the fault latch is cleared and a soft start is initiated. The low effective duty cycle during hiccup overcurrent greatly reduces component stress for an extended fault.

Inductor Current Sensing

Besides using a current sense resistor to sense inductor current, CS5211 provides the users with the possibility of using lossless inductor sensing technique. This sensing technique utilizes the Equivalent Series Resistance (ESR) of the inductor to sense the current. The output current is sensed through an RC network in parallel with the inductor as shown in Figure 4. The voltage across the small capacitor is then fed to the OC comparator.

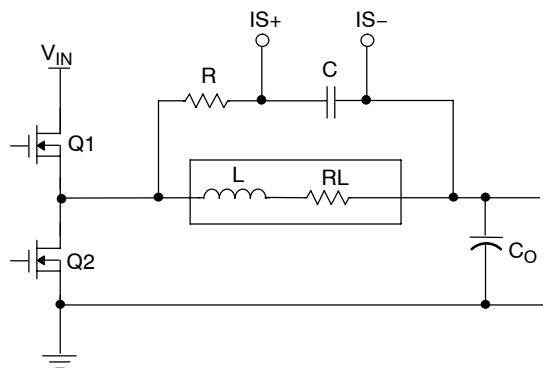


Figure 4. Inductor Current Sensing

If the values of R and C are chosen such that:

$$\frac{L}{R_L} = RC$$

Then the voltage across the capacitor C will be:

$$V_C = R_L I_L$$

Therefore, if the time constant of the RC network is equal to that of the inductor, the voltage across the capacitor is proportional to the inductor current by a factor of the inductor ESR. In practice, the user should ensure that under all component tolerances, the RC time constant is larger than the L/R time constant. This will keep the high frequency gain for $V_C(s)/I_L(s)$ less than the low frequency gain, and avoid unnecessary OCP tripping during short duration overcurrent situations.

Compared with conventional resistor sensing, the inductor ESR current sensing technique is lossless, but is not as accurate due to variation in the ESR from inductor to inductor and over temperature. For typical inductor ESR, the 0.39%/°C positive temperature coefficient will reduce the current limit at high temperature, and will help prevent thermal runaway, but will force an increased design target at room temperature. This technique can be more accurate than using a PCB trace, since PCB copper thickness can vary 10–20%, compared to 1% variation in wire diameter thickness typical of inductors.

Remote Voltage Sensing

The CS5211 has the capability to sense the voltage when the load is located far away from the regulator. The SGND pin is dedicated to the differential remote sensing. The negative remote sense line is connected to SGND pin directly, while the positive remote sense line is usually connected to the top of the feedback voltage divider. To prevent overvoltage condition caused by open remote sense lines, the divider should also be locally connected to the output of the regulator through a low value resistor. That resistor is used to compensate for the voltage drop across the output power cables.

APPLICATIONS INFORMATION

APPLICATIONS AND COMPONENT SELECTION

Inductor Component Selection

The output inductor may be the most critical component in the converter because it will directly effect the choice of other components and dictate both the steady-state and transient performance of the converter. When selecting an inductor the designer must consider factors such as DC current, peak current, output voltage ripple, core material, magnetic saturation, temperature, physical size, and cost (usually the primary concern).

In general, the output inductance value should be as low and physically small as possible to provide the best transient response and minimum cost. If a large inductance value is used, the converter will not respond quickly to rapid changes in the load current. On the other hand, too low an inductance value will result in very large ripple currents in the power components (MOSFETs, capacitors, etc) resulting in increased dissipation and lower converter efficiency. Also, increased ripple currents will force the designer to use higher rated MOSFETs, oversize the thermal solution, and use more, higher rated input and output capacitors – the converter cost will be adversely effected.

One method of calculating an output inductor value is to size the inductor to produce a specified maximum ripple current in the inductor. Lower ripple currents will result in less core and MOSFET losses and higher converter efficiency. The following equation may be used to calculate the minimum inductor value to produce a given maximum ripple current ($\alpha \cdot I_{O,MAX}$). The inductor value calculated by this equation is a minimum because values less than this will produce more ripple current than desired. Conversely, higher inductor values will result in less than the maximum ripple current.

$$L_{MIN} = (V_{in} - V_{out}) \cdot V_{out} / (\alpha \cdot I_{O,MAX} \cdot V_{in} \cdot f_{SW})$$

α is the ripple current as a percentage of the maximum output current ($\alpha = 0.15$ for $\pm 15\%$, $\alpha = 0.25$ for $\pm 25\%$, etc) and f_{SW} is the switching frequency. If the minimum inductor value is used, the inductor current will swing $\pm \alpha/2\%$ about I_{out} . Therefore, the inductor must be designed or selected such that it will not saturate with a peak current of $(1 + \alpha/2) \cdot I_{O,MAX}$.

Power dissipation in the inductor can now be calculated from the RMS current level. The RMS of the AC component of the inductor is given by the following relationship:

$$I_{AC} = \frac{I_{PP}}{\sqrt{12}}$$

where $I_{PP} = \alpha \cdot I_{O,MAX}$.

The total I_{RMS} of the current will be calculated from:

$$I_{RMS} = \sqrt{I_{OUT}^2 + I_{AC}^2}$$

The power dissipation for the inductor can be determined from:

$$P = I_{RMS}^2 \times R_L$$

Input Capacitor Selection and Considerations

The input capacitor is used to reduce the current surges caused by conduction of current of the top pass transistor charging the PWM inductor.

The input current is pulsing at the switching frequency going from 0 to peak current in the inductor. The duty factor will be a function of the ratio of the input to output voltage and of the efficiency.

$$DF = \frac{V_O}{V_I} \times \frac{1}{\text{Eff}}$$

The RMS value of the ripple into the input capacitors can now be calculated:

$$I_{IN(RMS)} = I_{OUT} \sqrt{DF - DF^2}$$

The input RMS is maximum at 50% DF, so selection of the possible duty factor closest to 50% will give the worst case dissipation in the capacitors. The power dissipation of the input capacitors can be calculated by multiplying the square of the RMS current by the ESR of the capacitor.

Output Capacitor

The output capacitor filters output inductor ripple current and provides low impedance for load current changes. The effect of the capacitance for handling the power supply induced ripple will be discussed here. Effects of load transient behavior can be considered separately.

The principle consideration for the output capacitor is the ripple current induced by the switches through the inductor. This ripple current was calculated as I_{AC} in the above discussion of the inductor. This ripple component will induce heating in the capacitor by a factor of the RMS current squared multiplied by the ESR of the output capacitor section. It will also create output ripple voltage.

The ripple voltage will be a vector summation of the ripple current times the ESR of the capacitor, plus the ripple current integrating in the capacitor, and the rate of change in current times the total series inductance of the capacitor and connections.

The inductor ripple current acting against the ESR of the output capacitor is the major contributor to the output ripple voltage. This fact can be used as a criterion to select the output capacitor.

$$V_{PP} = I_{PP} \times C_{ESR}$$

The power dissipation in the output capacitor can be calculated from:

$$P = I_{AC}^2 \times C_{ESR}$$

where:

I_{AC} = AC RMS of the inductor

C_{ESR} = Effective series resistance of the output capacitor network.

MOSFET & Heatsink Selection

Power dissipation, package size, and thermal solution drive MOSFET selection. To adequately size the heat sink,

the design must first predict the MOSFET power dissipation. Once the dissipation is known, the heat sink thermal impedance can be calculated to prevent the specified maximum case or junction temperatures from being exceeded at the highest ambient temperature. Power dissipation has two primary contributors: conduction losses and switching losses. The control or upper MOSFET will display both switching and conduction losses. The synchronous or lower MOSFET will exhibit only conduction losses because it switches into nearly zero voltage. However, the body diode in the synchronous MOSFET will suffer diode losses during the non-overlap time of the gate drivers.

For the upper or control MOSFET, the power dissipation can be approximated from:

$$\begin{aligned} P_{D,CONTROL} = & (I_{RMS,CNTL}^2 \cdot R_{DS(on)}) \\ & + (I_{Lo,MAX} \cdot Q_{switch}/I_g \cdot V_{IN} \cdot f_{SW}) \\ & + (Q_{oss}/2 \cdot V_{IN} \cdot f_{SW}) + (V_{IN} \cdot Q_{RR} \cdot f_{SW}) \end{aligned}$$

The first term represents the conduction or IR losses when the MOSFET is ON while the second term represents the switching losses. The third term is the losses associated with the *control and synchronous* MOSFET output charge when the control MOSFET turns ON. The output losses are caused by both the control and synchronous MOSFET but are dissipated only in the control FET. The fourth term is the loss due to the reverse recovery time of the body diode in the *synchronous* MOSFET. The first two terms are usually adequate to predict the majority of the losses.

Where $I_{RMS,CNTL}$ is the RMS value of the trapezoidal current in the control MOSFET:

$$I_{RMS,CNTL} = \sqrt{D} \cdot [(I_{Lo,MAX}^2 + I_{Lo,MAX} \cdot I_{Lo,MIN} + I_{Lo,MIN}^2)/3]^{1/2}$$

$I_{Lo,MAX}$ is the maximum output inductor current:

$$I_{Lo,MAX} = I_{O,MAX}/2 + \Delta I_{Lo}/2$$

$I_{Lo,MIN}$ is the minimum output inductor current:

$$I_{Lo,MIN} = I_{O,MAX}/2 - \Delta I_{Lo}/2$$

$I_{O,MAX}$ is the maximum converter output current.

D is the duty cycle of the converter:

$$D = V_{OUT}/V_{IN}$$

ΔI_{Lo} is the peak-to-peak ripple current in the output inductor of value Lo :

$$\Delta I_{Lo} = (V_{IN} - V_{OUT}) \cdot D/(Lo \cdot f_{SW})$$

$R_{DS(on)}$ is the ON resistance of the MOSFET at the applied gate drive voltage.

Q_{switch} is the post gate threshold portion of the gate-to-source charge plus the gate-to-drain charge. This may be specified in the data sheet or approximated from the gate-charge curve as shown in the Figure 5.

$$Q_{switch} = Q_{gs2} + Q_{gd}$$

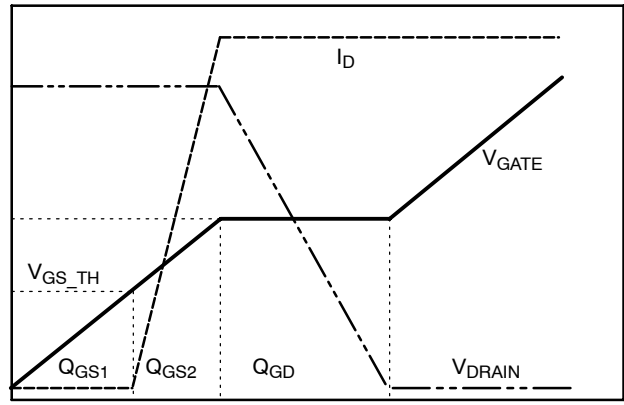


Figure 5. MOSFET Switching Characteristics

I_g is the output current from the gate driver IC.

V_{IN} is the input voltage to the converter.

f_{sw} is the switching frequency of the converter.

Q_G is the MOSFET total gate charge to obtain $R_{DS(on)}$.

Commonly specified in the data sheet.

V_g is the gate drive voltage.

Q_{RR} is the reverse recovery charge of the *lower* MOSFET.

Q_{oss} is the MOSFET output charge specified in the data sheet.

For the lower or synchronous MOSFET, the power dissipation can be approximated from:

$$\begin{aligned} P_{D,SYNCH} = & (I_{RMS,SYNCH}^2 \cdot R_{DS(on)}) \\ & + (V_{fdiode} \cdot I_{O,MAX}/2 \cdot t_{nonoverlap} \cdot f_{SW}) \end{aligned}$$

The first term represents the conduction or IR losses when the MOSFET is ON and the second term represents the diode losses that occur during the gate non-overlap time.

All terms were defined in the previous discussion for the control MOSFET with the exception of:

$$I_{RMS,SYNCH} = \sqrt{1-D} \cdot [(I_{Lo,MAX}^2 + I_{Lo,MAX} \cdot I_{Lo,MIN} + I_{Lo,MIN}^2)/3]^{1/2}$$

where:

V_{fdiode} is the forward voltage of the MOSFET's intrinsic diode at the converter output current.

$t_{nonoverlap}$ is the non-overlap time between the upper and lower gate drivers to prevent cross conduction. This time is usually specified in the data sheet for the control IC.

When the MOSFET power dissipations are known, the designer can calculate the required thermal impedance to maintain a specified junction temperature at the worst case ambient operating temperature

$$\theta_T < (T_J - T_A)/P_D$$

where;

θ_T is the total thermal impedance ($\theta_{JC} + \theta_{SA}$).

θ_{JC} is the junction-to-case thermal impedance of the MOSFET.

θ_{SA} is the sink-to-ambient thermal impedance of the heatsink assuming direct mounting of the MOSFET (no thermal “pad” is used).

T_J is the specified maximum allowed junction temperature.

T_A is the worst case ambient operating temperature.

For TO-220 and TO-263 packages, standard FR-4 copper clad circuit boards will have approximate thermal resistances (θ_{SA}) as shown below:

Pad Size (in ² /mm ²)	Single-Sided 1 oz. Copper
0.5/323	60–65°C/W
0.75/484	55–60°C/W
1.0/645	50–55°C/W
1.5/968	45–50°C/W
2.0/1290	38–42°C/W
2.5/1612	33–37°C/W

As with any power design, proper laboratory testing should be performed to insure the design will dissipate the required power under worst case operating conditions. Variables considered during testing should include maximum ambient temperature, minimum airflow, maximum input voltage, maximum loading, and component variations (i.e. worst case MOSFET $R_{DS(on)}$). Also, the inductors and capacitors share the MOSFET’s heatsinks and will add heat and raise the temperature of the circuit board and MOSFET. For any new design, its advisable to have as much heatsink area as possible – all too often new designs are found to be too hot and require re-design to add heatsinking.

Compensation Capacitor Selection

The nominal output current capability of the error amp is 30 μ A. This current charging the capacitor on the COMP pin is used as soft start for the converter. The COMP pin is going to ramp up to a voltage level that is within 70 mV of what V_{FFB} is going to be when in regulation. This is the voltage that will determine the soft start. Therefore, the COMP capacitor can be established by the following relationship:

$$C = 30 \mu A \times \frac{\text{soft start}}{V_{FFB(REG)}}$$

where:

soft start = output ramp-up time

$V_{FFB(REG)}$ = V_{FFB} voltage when in regulation

30 μ A = COMP output current, typ.

The COMP output current range is given in the data sheet and will affect the ramp-up time. The value of the capacitor on the COMP pin will have an effect on the loop response and the transient response of the converter. Transient response can be enhanced by the addition of a parallel combination of a resistor and capacitor between the COMP pin and the comp capacitor.

Rosc Selection

The switching frequency is programmed by selecting the resistor connected between the R_{OSC} pin and SGND (pin 7). The grounded side of this resistor should be directly connected to the SGND pin, without any other currents flowing between the bottom of the resistor and the pin. Also, avoid running any noisy signals under the resistor, since injected noise could cause frequency jitter. The graph in Figure 6 shows the required resistance to program the frequency. Below 500 kHz, the following formula is accurate:

$$R = 17544/f_{SW} - 4 \text{ k}\Omega$$

where f_{SW} is the switching frequency in kHz.

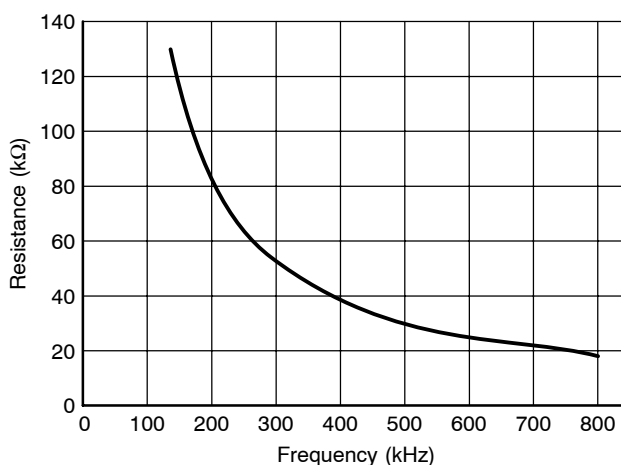


Figure 6. Frequency vs. R_{OSC}

Differential Remote Sense Operation

The ability to implement fully differential remote sense is provided by the CS5211. The positive remote sense is implemented by bringing the output remote sense connection to the positive load connection. A low value resistor is connected from V_{out} to the feedback point at the regulator to provide feedback in the instance when the remote sense point is not connected.

The negative remote sense connection is provided by connecting the SGND of the CS5211 to the negative of the load return. Again, a low value resistor should be connected between SGND and LGND at the regulator to provide feedback in the instance when the remote sense point is not connected. The maximum voltage differential between the three grounds for this part is 200 mV.

Feedback Divider Selection

The feedback voltage measured at V_{FB} during normal regulation will be 1.0 V. This voltage is compared to an internal 1.0 V reference and is used to regulate the output voltage. The bias current into the error amplifier is 1.0 μ A max, so select the resistor values so that this current does not add an excessive offset voltage.

V_{FFB} Feedback Selection

To take full advantage of the V² control scheme, a small amount of output ripple must be fed back to the V_{FFB} pin, typically 50 mV. For most application, this requirement is simple to achieve and the V_{FFB} can be connected directly to the V_{FB} pin. There are some application that have to meet stringent load transient requirements. One of the key factor in achieving tight dynamic voltage regulation is low ESR. Low ESR at the regulator output results in low output voltage ripple. This situation could result in increase noise sensitivity and a potential for loop instability. In applications where the output ripple is not sufficient, the performance of the CS5211 can be improved by adding a fixed amount external ramp compensation to the V_{FFB} pin. Refer to Figure 7, the amount of ramp at the V_{FFB} pin depends on the switch node Voltage, Feedback Voltage, R1 and C2.

$$V_{\text{ramp}} = (V_{\text{sw}} - V_{\text{FB}}) \times t_{\text{on}} / (R1 \times C2)$$

where:

V_{ramp} = amount of ramp needed;

V_{sw} = switch node voltage;

V_{FB} = voltage feedback, 1 V;

t_{on} = switch on-time.

To minimize the lost in efficiency R1 resistance should be large, typically 100 k or larger. With R1 chosen, C2 can be determined by the following;

$$C2 = (V_{\text{sw}} - V_{\text{FB}}) \times t_{\text{on}} / (R1 \times V_{\text{ramp}})$$

C1 is used as a bypass capacitor and its value should be equal to or greater than C2.

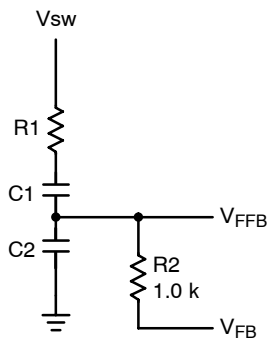


Figure 7. Small RC Filter Providing the Proper Voltage Ramp at the Beginning of Each On-Time Cycle

Maximum Frequency Operation

The minimum pulse width may limit the maximum operating frequency. The duty factor, given by the output/input voltage ratio, multiplied by the period determines the pulse width during normal operation. This pulse width must be greater than 200 ns, or duty cycle jitter could become excessive. For low pulse widths below 300 ns, external slope compensation should be added to the V_{FFB}

pin to increase the PWM ramp signal and improve stability. 50 mV of added ramp at the V_{FFB} pin is typically enough.

Current Sense Component Selection

The current limit threshold is set by sensing a 60 mV voltage differential between the IS+ and IS- pins. Referring to Figure 8, the time constant of the R2,C1 filter should be set larger than the L/R1 time constant under worst case tolerances, to prevent overshoot in the sensed voltage and tripping the current limit too low. Resistor R3 of value equal to R2 is added for bias current cancellation. R2 and R3 should not be made too large, to reduce errors from bias current offsets. For typical L/R time constants, a 0.1 μF capacitor for C1 will allow R2 to be between 1.0 k and 10 kΩ.

The current limit without R4 and R5, which are optional, is given by 60 mV/R1, where R1 is the internal resistance of the inductor, obtained from the manufacturer. The addition of R5 can be used to decrease the current limit to a value given by:

$$I_{\text{LIM}} = (60 \text{ mV} - (V_{\text{OUT}} \times R3 / (R3 + R5))) / R1$$

where V_{OUT} is the output voltage.

Similarly, omitting R5 and adding R4 will increase the current limit to a value given by:

$$I_{\text{LIM}} = 60 \text{ mV} / R1 \times (1 + R2 / R4)$$

Essentially, R4 or R5 are used to increase or decrease the inductor voltage drop which corresponds to 60 mV at the IS+ and IS- pins.

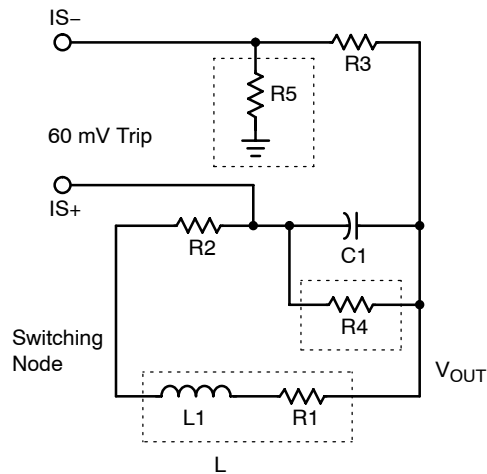


Figure 8. Current Limit

Boost Component Selection for Upper FET Gate Drive

The boost (BST) pin provides for application of a higher voltage to drive the upper FET. This voltage may be provided by a fixed higher voltage or it may be generated with a boost capacitor and charging diode, as shown in Figure 10. The voltage in the boost configuration would be the summation of the voltage from the charging diode and

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the output voltage swing. Care must be taken to keep the peak voltage with respect to ground less than 20 V peak. The

capacitor should be large enough to drive the capacitance of the top FET.

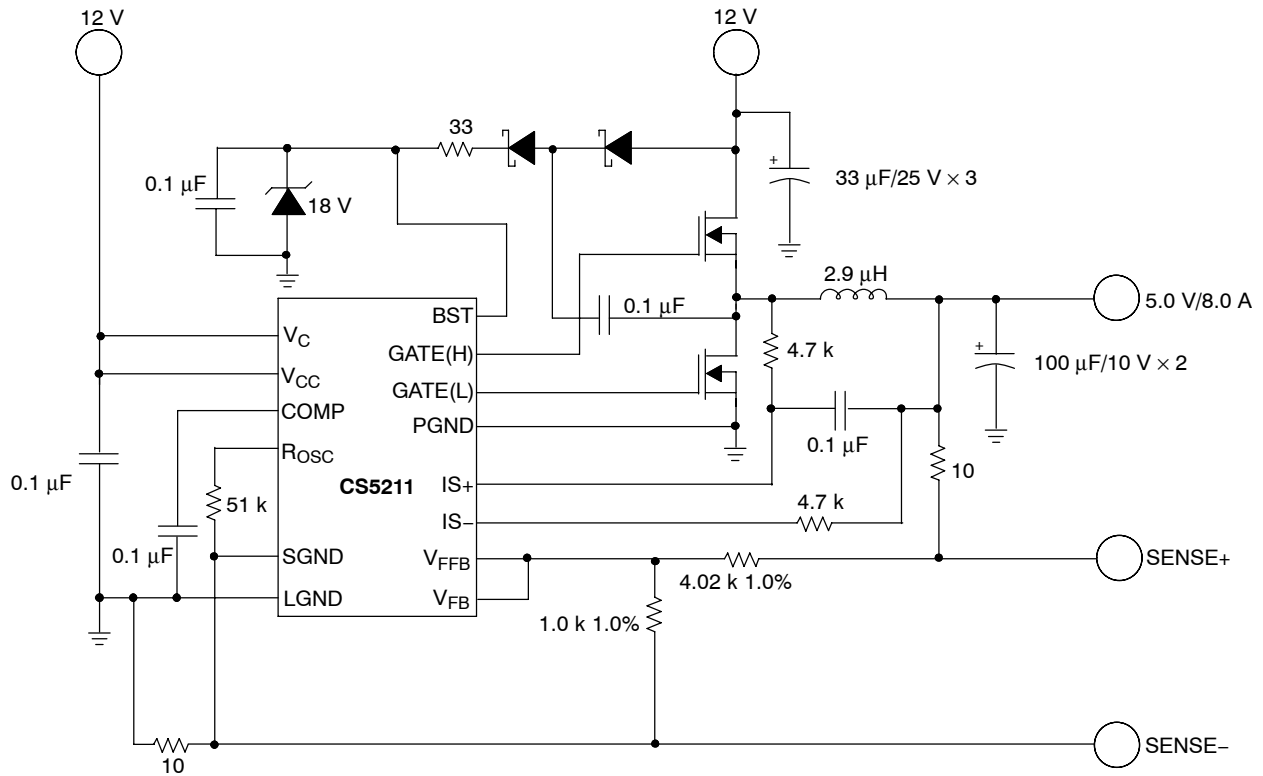


Figure 9. Additional Application Diagram, 12 V to 5.0 V/8.0 A Converter with Differential Remote Sense

CS5211

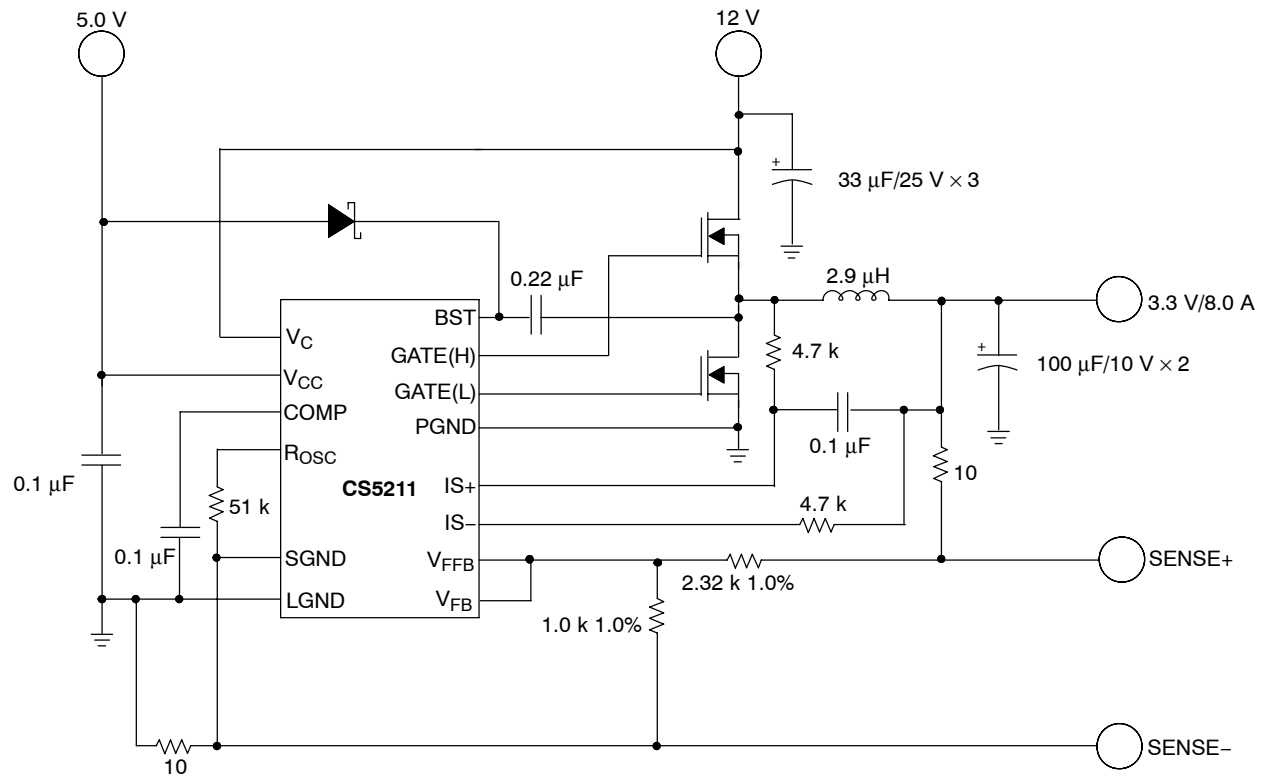


Figure 10. Additional Application Diagram, 12 V to 5.0 V Bias to 3.3 V/8.0 A Converter with Differential Remote Sense

CS5211

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping
CS5211ED14	$-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$	SO-14	55 Units/Rail
CS5211EDR14		SO-14	2500 Tape & Reel
CS5211GD14	$0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$	SO-14	55 Units/Rail
CS5211GDR14		SO-14	2500 Tape & Reel

CS5212

Low Voltage Synchronous Buck Controller

The CS5212 is a low voltage synchronous buck controller. It contains all required circuitry for a synchronous buck converter using external N-Channel MOSFETs. High current internal gate drivers are capable of driving high gate capacitance of low $R_{DS(on)}$ NFETs for better efficiency. The V^2 ™ control architecture is used to achieve unmatched transient response, the best overall regulation and the simplest loop compensation.

Additionally, the CS5212 provides overcurrent protection, undervoltage lockout, soft start, built-in adaptive non-overlap, and an adjustable fixed frequency range of 150 kHz to 750 kHz, which gives the designer more flexibility to make efficiency and component size trade offs. The CS5212 will also operate over a 3.1 V to 7.0 V range using either single or dual input voltage.

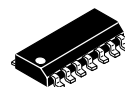
Features

- Switching Regulator Controller
 - N-Channel Synchronous Buck Design
 - V^2 Control Topology
 - 200 ns Transient Response
 - Programmable Fixed Frequency of 150 kHz–750 kHz
 - 1.0 V 1.5% Internal Reference
 - Lossless Inductor Sensing Overcurrent Protection
 - Hiccup Mode Short Circuit Protection
 - Programmable Soft Start
 - 40 ns GATE Rise and Fall Times (3.3 nF Load)
 - 70 ns Adaptive FET Nonoverlap Time
 - Differential Remote Sense Capability
 - Available in Industrial and Commercial Temperature Grades
- System Power Management
 - 3.3 V Operation
 - Undervoltage Lockout
 - On/Off Control Through Use of the COMP Pin



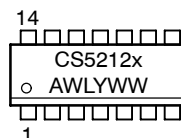
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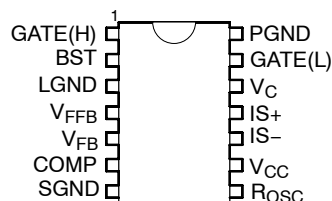
**SOIC-14
D SUFFIX
CASE 751A**

MARKING DIAGRAM



x = E or G
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 109 of this data sheet.

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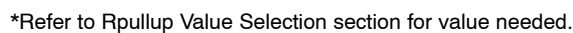


Figure 11. Application Diagram, 3.3 V to 1.5 V/8.0 A Converter with Differential Remote Sense

MAXIMUM RATINGS*

Rating	Value	Unit
Operating Junction Temperature, T _J	150	°C
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1) 230 peak	°C
Storage Temperature Range, T _S	–65 to +150	°C
Package Thermal Resistance: Junction–to–Case, R _{θJC} Junction–to–Ambient, R _{θJA}	30 125	°C/W °C/W
ESD Susceptibility: Human Body Model Machine Model	2.0 200	kV V
JEDEC Moisture Sensitivity	1	–

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

MAXIMUM RATINGS

Pin Name	Pin Symbol	V _{MAX}	V _{MIN}	I _{SOURCE}	I _{SINK}
IC Power Input	V _{CC}	6.0 V	−0.3 V	N/A	50 mA DC
Power input for the low side driver	V _C	16 V	−0.3 V	N/A	1.5 A Peak, 200 mA DC
Power Supply input for the high side driver	BST	20 V	−0.3 V	N/A	1.5 A Peak, 200 mA DC
Compensation Capacitor	COMP	6.0 V	−0.3 V	1.0 mA	1.0 mA
Voltage Feedback Input	V _{FB}	6.0 V	−0.3 V	1.0 mA	1.0 mA
Oscillator Resistor	R _{OSC}	6.0 V	−0.3 V	1.0 mA	1.0 mA
Fast Feedback Input	V _{FFB}	6.0 V	−0.3 V	1.0 mA	1.0 mA
High-Side FET Driver	GATE(H)	20 V	−0.3 V −2.0 V for 50 ns	1.5 A Peak 200 mA DC	1.5 A Peak 200 mA DC
Low-Side FET Driver	GATE(L)	16 V	−0.3 V −2.0 V for 50 ns	1.5 A Peak 200 mA DC	1.5 A Peak 200 mA DC
Positive Current Sense	IS+	6.0 V	−0.3 V	1.0 mA	1.0 mA
Negative Current Sense	IS−	6.0 V	−0.3 V	1.0 mA	1.0 mA
Power Ground	PGND	0.3 V	−0.3 V	1.5 A Peak, 200 mA DC	N/A
Logic Ground	LGND	0 V	0 V	100 mA	N/A
Sense Ground	SGND	0.3 V	−0.3 V	1.0 mA	1.0 mA

ELECTRICAL CHARACTERISTICS (−40°C < T_A < 85°C (CS5212E); 0°C < T_A < 70°C (CS5212G); −40°C < T_J < 125°C; 3.1 V < V_{CC} < 3.5 V; 3.1 V < V_C < 7.0 V; 4.5 V < BST < 20 V; C_{GATE(H)} = C_{GATE(L)} = 3.3 nF; R_{OSC} = 51 k; C_{COMP} = 0.1 μF, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Error Amplifier					
V _{FB} Bias Current	V _{FB} = 0 V	–	0.1	1.0	μA
COMP Source Current	V _{FB} = 0.8 V	15	30	60	μA
COMP SINK Current	V _{FB} = 1.2 V	15	30	60	μA
Open Loop Gain	–	–	98	–	dB
Unity Gain Bandwidth	C = 0.1 μF	–	50	–	kHz
PSRR @ 1.0 kHz	–	–	70	–	dB
Output Transconductance	–	–	32	–	mmho
Output Impedance	–	–	2.5	–	MΩ
Reference Voltage	−0.1 V < SGND < 0.1 V, COMP = V _{FB} , Measure V _{FB} to SGND	0.977	0.992	1.007	V
COMP Max Voltage	V _{FB} = 0.8 V	2.5	3.0	–	V
COMP Min Voltage	V _{FB} = 1.2 V	–	0.1	0.2	V

GATE(H) and GATE(L)

High Voltage (AC)	GATE(L) GATE(H) 0.5 nF < C _{GATE(H)} = C _{GATE(L)} < 10 nF. Note 2.	V _C − 0.5 BST − 0.5	– –	– –	V V
Low Voltage (AC)	GATE(L) or GATE(H) 0.5 nF < C _{GATE(H)} ; C _{GATE(L)} < 10 nF. Note 2.	–	–	0.5	V

2. GBD.

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ELECTRICAL CHARACTERISTICS (continued) ($-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ (CS5212E); $0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$ (CS5212G); $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$; $3.1\text{ V} < V_{CC} < 3.5\text{ V}$; $3.1\text{ V} < V_C < 7.0\text{ V}$; $4.5\text{ V} < BST < 20\text{ V}$; $C_{GATE(H)} = C_{GATE(L)} = 3.3\text{ nF}$; $R_{OSC} = 51\text{ k}$; $C_{COMP} = 0.1\text{ }\mu\text{F}$, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
GATE(H) and GATE(L)					
Rise Time	$V_C = BST = 7.0\text{ V}$, Measure: $0.7\text{ V} < \text{GATE(L)} < 6.3\text{ V}$, $0.7\text{ V} < \text{GATE(H)} < 6.3\text{ V}$	–	40	80	ns
Fall Time	$V_C = BST = 7.0\text{ V}$, Measure: $0.7\text{ V} < \text{GATE(L)} < 6.3\text{ V}$, $0.7\text{ V} < \text{GATE(H)} < 6.3\text{ V}$	–	40	80	ns
GATE(H) to GATE(L) Delay	$\text{GATE(H)} < 2.0\text{ V}$, $\text{GATE(L)} > 2.0\text{ V}$	40	70	110	ns
GATE(L) to GATE(H) Delay	$\text{GATE(L)} < 2.0\text{ V}$, $\text{GATE(H)} > 2.0\text{ V}$	40	70	110	ns
GATE(H)/(L) Pull-Down	Resistance to PGND	20	50	115	K Ω

Overcurrent Protection

OVC Comparator Offset Voltage	$0\text{ V} < \text{IS+} < V_{CC}$, $0\text{ V} < \text{IS-} < V_{CC}$	54	60	66	mV
IS+ Bias Current	$0\text{ V} < \text{IS+} < V_{CC}$	–1.0	0.1	1.0	μA
IS- Bias Current	$0\text{ V} < \text{IS-} < V_{CC}$	–1.0	0.1	1.0	μA
COMP Discharge Threshold	–	0.20	0.25	0.30	V
COMP Discharge Current in OVC Fault Mode	COMP = 1.0 V	2.0	5.0	8.0	μA

PWM Comparator

Transient Response	COMP = 0 – 1.5 V, V_{FFB} , 20 mV overdrive	–	100	200	ns
PWM Comparator Offset	$V_{FB} = V_{FFB} = 0\text{ V}$; Increase COMP until GATE(H) starts switching	0.35	0.40	0.45	V
Artificial Ramp	Duty Cycle = 90%	40	70	100	mV
V_{FFB} Bias Current	$V_{FFB} = 0\text{ V}$	–	0.1	1.0	μA
V_{FFB} Input Range	Note 3.	–	–	1.1	V
Minimum Pulse Width	–	–	–	200	ns

Oscillator

Switching Frequency	$R_{OSC} = 18\text{ k}$	600	750	900	kHz
Switching Frequency	$R_{OSC} = 51\text{ k}$	240	300	360	kHz
Switching Frequency	$R_{OSC} = 115\text{ k}$	120	150	180	kHz
R_{OSC} Voltage	–	1.21	1.25	1.29	V

General Electrical Specifications

V_{CC} Supply Current	COMP = 0 V (no switching)	–	5.0	8.0	mA
BST/ V_C Supply Current	COMP = 0 V (no switching)	–	2.0	3.0	mA
Start Threshold	GATE(H) Switching, COMP Charging	2.7	2.8	2.9	V
Stop Threshold	GATE(H) Not Switching, COMP Not Charging	2.6	2.7	2.8	V
Hysteresis	Start-Stop	75	100	125	mV
Sense Ground Current	Note 4.	–	0.15	1.00	mA

3. GBD.

4. Recommended maximum operating voltage between the three grounds is 200 mV.

PACKAGE PIN DESCRIPTION

PIN NO.	PIN SYMBOL	FUNCTION
1	GATE(H)	High Side Switch FET driver pin. Capable of delivering peak currents of 1.0 A.
2	BST	Power supply input for the high side driver.
3	LGND	Reference ground. All control circuits are referenced to this pin. IC substrate connection.
4	V _{FFB}	Input for the PWM comparator.
5	V _{FB}	Error amplifier input.
6	COMP	Error Amp output. PWM Comparator reference input. A capacitor to LGND provides error amp compensation.
7	SGND	Internal reference is connected to this ground. Connect directly at the load for ground remote sensing.
8	R _{OSC}	A resistor from this pin to SGND sets switching frequency.
9	V _{CC}	Input Power Supply Pin. It supplies power to control circuitry. A 0.1 μ F Decoupling cap is recommended.
10	IS ₋	Negative input for overcurrent comparator.
11	IS ₊	Positive input for overcurrent comparator.
12	V _C	Power supply input for the low side driver.
13	GATE(L)	Low Side Synchronous FET driver pin. Capable of delivering peak currents of 1.0 A.
14	PGND	High Current ground for the GATE(H) and GATE(L) pins.

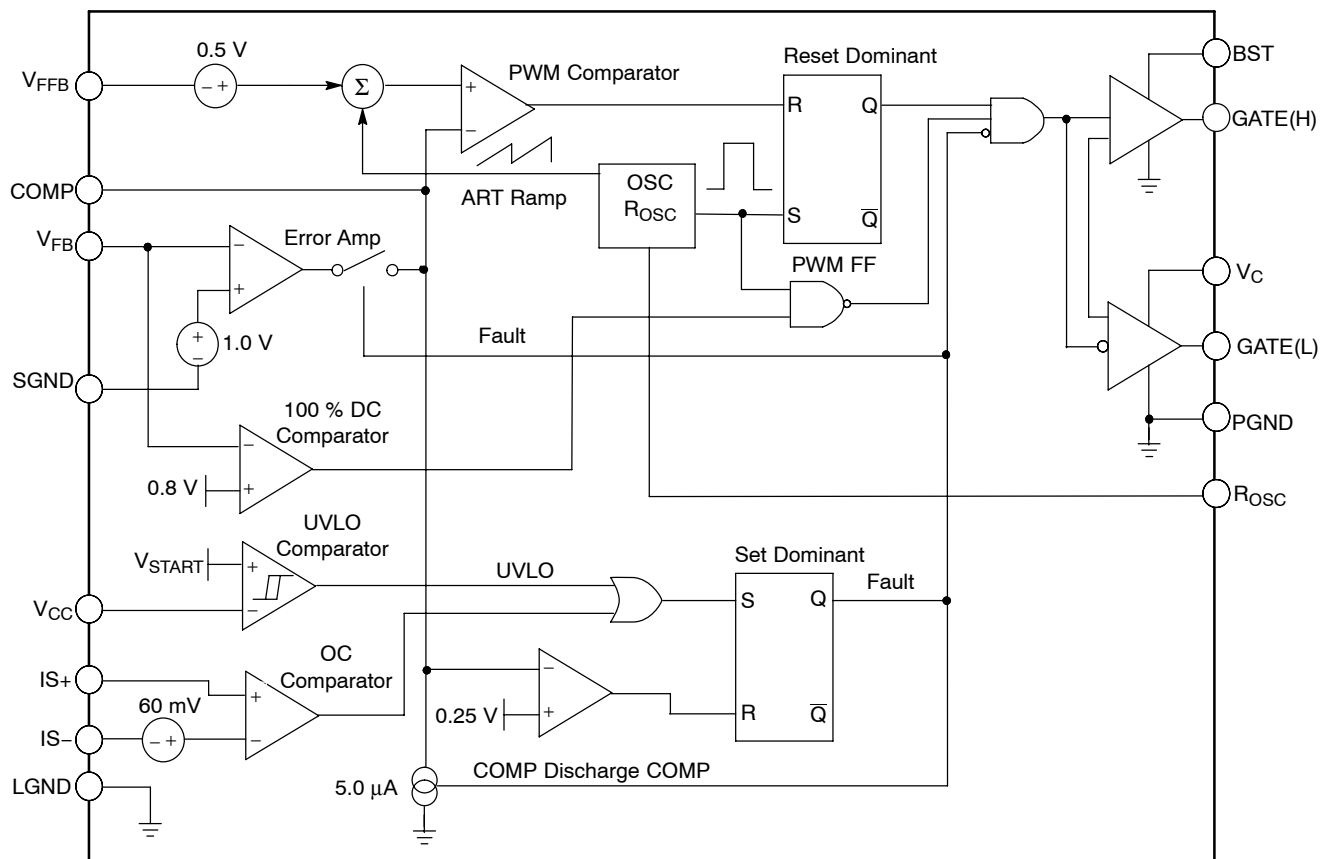


Figure 12. Block Diagram

THEORY OF OPERATION

The CS5212 is a synchronous, programmable fixed-frequency, low-voltage buck controller using the V^2 control method. It also provides overcurrent protection, undervoltage lockout, soft start and built-in adaptive non-overlap.

 V^2 Control Method

The V^2 method of control uses a ramp signal generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variations in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.

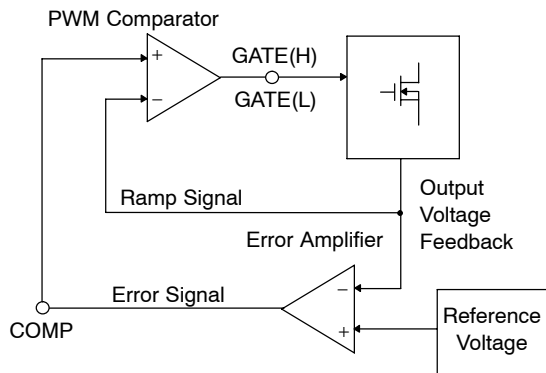


Figure 13. V^2 Control Block Diagram

As illustrated in Figure 13, the output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of the change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to 0% or 100% duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the V^2 control scheme to compensate the duty cycle. Since the change in the inductor current modifies the ramp signal, as in current mode control, the V^2 control scheme has the same advantages in line transient response.

A change in load current will have an effect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, compared to traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this “slow” feedback loop is to provide DC accuracy. Noise immunity is significantly improved, because the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulations are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The V^2 method of control maintains a fixed error signal for both line and load variations, since both line and load affect the ramp signal.

Constant Frequency Operation

The CS5212 uses a constant frequency, trailing edge modulation architecture for generating PWM signal. During normal operation, the oscillator generates a narrow pulse at the beginning of each switching cycle to turn on the main switch. The main switch will be turned off when the ramp signal intersects with the output of the error amplifier (COMP pin voltage). Therefore, the switch duty cycle can be modified to regulate the output voltage to the desired value as line and load conditions change.

The major advantage of constant frequency operation is that the component selections, especially the magnetic component design, become very easy. The oscillator frequency of CS5212 is programmable from 150 kHz to 750 kHz using an external resistor connected from the R_{OSC} pin to ground.

Startup

If there are no fault conditions and the fault latch is reset, the error amplifier will start charging the COMP pin capacitor after the CS5212 is powered up. The output of the error amplifier (COMP voltage) will ramp up linearly. The COMP capacitance and the source current of the error amplifier determine the slew rate of COMP voltage. The output of the error amplifier is connected internally to the inverting input of the PWM comparator and it is compared with the V_{FFB} pin voltage plus 0.5 V offset at the non-inverting input of the PWM comparator. Since V_{FFB} voltage is zero before the startup, the PWM comparator output will stay high until the COMP pin voltage hits 0.5 V. There is no switching action while the PWM comparator output is high.

After the COMP voltage exceeds the 0.5 V offset, the output of PWM comparator toggles and releases the PWM latch. The narrow pulse generated by the oscillator at the beginning of the next oscillator cycle will set the latch so that the main switch can be turned on and the regulator output voltage ramps up. When the output voltage achieves a level set by the COMP voltage, the main switch will be turned off. The V^2 control loop will adjust the main switch duty cycle as required to ensure the regulator output voltage tracks the COMP voltage. Since the COMP voltage increases gradually, the soft start can be achieved. The start-up period ends when the output voltage reaches the level set by the external resistor divider.

Output Enable

Since there can be no switching until the COMP pin exceeds the 0.5 V offset built into the PWM comparator, the COMP pin can also be used for an enable function. Hold the COMP pin below 0.4 V with an open collector circuit to disable the output. When the COMP pin is released to enable startup, the user must ensure there is no leakage current from the enable circuit into COMP. During normal operation the COMP output is driven with only 5.0 μ A to 30 μ A internally.

Hiccup Mode Overcurrent Protection

Under normal load conditions, the voltage across the IS+ and IS- pins is less than the 60 mV overcurrent threshold. If the threshold is exceeded, the overcurrent fault latch is set, the high side gate driver is forced low, and the COMP pin is discharged with 5.0 μ A. There is no switching until the COMP voltage drops below a 0.25 V threshold. Then, the fault latch is cleared and a soft start is initiated. The low effective duty cycle during hiccup overcurrent greatly reduces component stress for an extended fault.

Inductor Current Sensing

Besides using a current sense resistor to sense inductor current, CS5212 provides the users with the possibility of using loss-less inductor sensing technique. This sensing technique utilizes the Equivalent Series Resistance (ESR) of the inductor to sense the current. The output current is sensed through an RC network in parallel with the inductor as shown in Figure 14. The voltage across the small capacitor is then fed to the OC comparator.

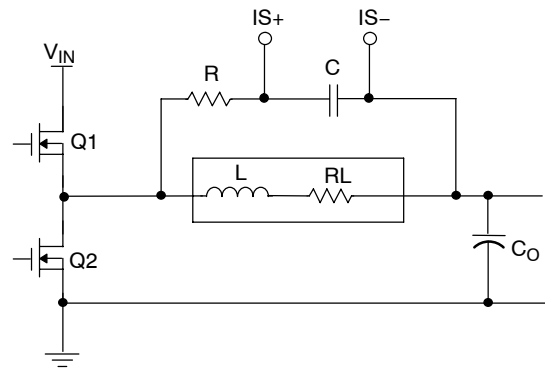


Figure 14. Inductor Current Sensing

If the values of R and C are chosen such that:

$$\frac{L}{R_L} = RC$$

Then the voltage across the capacitor C will be:

$$V_C = R_L I_L$$

Therefore, if the time constant of the RC network is equal to that of the inductor, the voltage across the capacitor is proportional to the inductor current by a factor of the inductor ESR. In practice, the user should ensure that under all component tolerances, the RC time constant is larger than the L/R time constant. This will keep the high frequency gain for $V_C(s)/I_L(s)$ less than the low frequency gain, and avoid unnecessary OCP tripping during short duration overcurrent situations.

Compared with conventional resistor sensing, the inductor ESR current sensing technique is lossless, but is not as accurate due to variation in the ESR from inductor to inductor and over temperature. For typical inductor ESR, the 0.39%/°C positive temperature coefficient will reduce the current limit at high temperature, and will help prevent thermal runaway, but will force an increased design target at room temperature. This technique can be more accurate than using a PCB trace, since PCB copper thickness can vary 10–20%, compared to 1% variation in wire diameter thickness typical of inductors.

Remote Voltage Sensing

The CS5212 has the capability to sense the voltage when the load is located far away from the regulator. The SGND pin is dedicated to the differential remote sensing. The negative remote sense line is connected to SGND pin directly, while the positive remote sense line is usually connected to the top of the feedback voltage divider. To prevent over-voltage condition caused by open remote sense lines, the divider should also be locally connected to the output of the regulator through a low value resistor. That resistor is used to compensate for the voltage drop across the output power cables.

APPLICATIONS INFORMATION

APPLICATIONS AND COMPONENT SELECTION

Inductor Component Selection

The output inductor may be the most critical component in the converter because it will directly effect the choice of other components and dictate both the steady-state and transient performance of the converter. When selecting an inductor the designer must consider factors such as DC current, peak current, output voltage ripple, core material, magnetic saturation, temperature, physical size, and cost (usually the primary concern).

In general, the output inductance value should be as low and physically small as possible to provide the best transient response and minimum cost. If a large inductance value is used, the converter will not respond quickly to rapid changes in the load current. On the other hand, too low an inductance value will result in very large ripple currents in the power components (MOSFETs, capacitors, etc) resulting in increased dissipation and lower converter efficiency. Also, increased ripple currents will force the designer to use higher rated MOSFETs, oversize the thermal solution, and use more, higher rated input and output capacitors – the converter cost will be adversely effected.

One method of calculating an output inductor value is to size the inductor to produce a specified maximum ripple current in the inductor. Lower ripple currents will result in less core and MOSFET losses and higher converter efficiency. The following equation may be used to calculate the minimum inductor value to produce a given maximum ripple current ($\alpha \cdot I_{O,MAX}$). The inductor value calculated by this equation is a minimum because values less than this will produce more ripple current than desired. Conversely, higher inductor values will result in less than the maximum ripple current.

$$L_{MIN} = (V_{in} - V_{out}) \cdot V_{out} / (\alpha \cdot I_{O,MAX} \cdot V_{in} \cdot f_{SW})$$

α is the ripple current as a percentage of the maximum output current ($\alpha = 0.15$ for $\pm 15\%$, $\alpha = 0.25$ for $\pm 25\%$, etc) and f_{SW} is the switching frequency. If the minimum inductor value is used, the inductor current will swing $\pm \alpha/2\%$ about I_{out} . Therefore, the inductor must be designed or selected such that it will not saturate with a peak current of $(1 + \alpha/2) \cdot I_{O,MAX}$.

Power dissipation in the inductor can now be calculated from the RMS current level. The RMS of the AC component of the inductor is given by the following relationship:

$$I_{AC} = \frac{I_{PP}}{\sqrt{12}}$$

where $I_{PP} = \alpha \cdot I_{O,MAX}$.

The total I_{RMS} of the current will be calculated from:

$$I_{RMS} = \sqrt{I_{OUT}^2 + I_{AC}^2}$$

The power dissipation for the inductor can be determined from:

$$P = I_{RMS}^2 \times R_L$$

Input Capacitor Selection and Considerations

The input capacitor is used to reduce the current surges caused by conduction of current of the top pass transistor charging the PWM inductor.

The input current is pulsing at the switching frequency going from 0 to peak current in the inductor. The duty factor will be a function of the ratio of the input to output voltage and of the efficiency.

$$DF = \frac{V_O}{V_I} \times \frac{1}{\text{Eff}}$$

The RMS value of the ripple into the input capacitors can now be calculated:

$$I_{IN(RMS)} = I_{OUT} \sqrt{DF - DF^2}$$

The input RMS is maximum at 50% DF, so selection of the possible duty factor closest to 50% will give the worst case dissipation in the capacitors. The power dissipation of the input capacitors can be calculated by multiplying the square of the RMS current by the ESR of the capacitor.

Output Capacitor

The output capacitor filters output inductor ripple current and provides low impedance for load current changes. The effect of the capacitance for handling the power supply induced ripple will be discussed here. Effects of load transient behavior can be considered separately.

The principle consideration for the output capacitor is the ripple current induced by the switches through the inductor. This ripple current was calculated as I_{AC} in the above discussion of the inductor. This ripple component will induce heating in the capacitor by a factor of the RMS current squared multiplied by the ESR of the output capacitor section. It will also create output ripple voltage.

The ripple voltage will be a vector summation of the ripple current times the ESR of the capacitor, plus the ripple current integrating in the capacitor, and the rate of change in current times the total series inductance of the capacitor and connections.

The inductor ripple current acting against the ESR of the output capacitor is the major contributor to the output ripple voltage. This fact can be used as a criterion to select the output capacitor.

$$V_{PP} = I_{PP} \times C_{ESR}$$

The power dissipation in the output capacitor can be calculated from:

$$P = I_{AC}^2 \times C_{ESR}$$

where:

I_{AC} = AC RMS of the inductor

C_{ESR} = Effective series resistance of the output capacitor network.

MOSFET & Heatsink Selection

Power dissipation, package size, and thermal solution drive MOSFET selection. To adequately size the heat sink,

the design must first predict the MOSFET power dissipation. Once the dissipation is known, the heat sink thermal impedance can be calculated to prevent the specified maximum case or junction temperatures from being exceeded at the highest ambient temperature. Power dissipation has two primary contributors: conduction losses and switching losses. The control or upper MOSFET will display both switching and conduction losses. The synchronous or lower MOSFET will exhibit only conduction losses because it switches into nearly zero voltage. However, the body diode in the synchronous MOSFET will suffer diode losses during the non-overlap time of the gate drivers.

For the upper or control MOSFET, the power dissipation can be approximated from:

$$\begin{aligned} P_{D,CONTROL} = & (I_{RMS,CNTL}^2 \cdot R_{DS(on)}) \\ & + (I_{Lo,MAX} \cdot Q_{switch}/I_g \cdot V_{IN} \cdot f_{SW}) \\ & + (Q_{oss}/2 \cdot V_{IN} \cdot f_{SW}) + (V_{IN} \cdot Q_{RR} \cdot f_{SW}) \end{aligned}$$

The first term represents the conduction or IR losses when the MOSFET is ON while the second term represents the switching losses. The third term is the losses associated with the *control and synchronous* MOSFET output charge when the control MOSFET turns ON. The output losses are caused by both the control and synchronous MOSFET but are dissipated only in the control FET. The fourth term is the loss due to the reverse recovery time of the body diode in the *synchronous* MOSFET. The first two terms are usually adequate to predict the majority of the losses.

Where $I_{RMS,CNTL}$ is the RMS value of the trapezoidal current in the control MOSFET:

$$I_{RMS,CNTL} = \sqrt{D} \cdot [(I_{Lo,MAX}^2 + I_{Lo,MAX} \cdot I_{Lo,MIN} + I_{Lo,MIN}^2)/3]^{1/2}$$

$I_{Lo,MAX}$ is the maximum output inductor current:

$$I_{Lo,MAX} = I_{O,MAX}/2 + \Delta I_{Lo}/2$$

$I_{Lo,MIN}$ is the minimum output inductor current:

$$I_{Lo,MIN} = I_{O,MAX}/2 - \Delta I_{Lo}/2$$

$I_{O,MAX}$ is the maximum converter output current.

D is the duty cycle of the converter:

$$D = V_{OUT}/V_{IN}$$

ΔI_{Lo} is the peak-to-peak ripple current in the output inductor of value Lo :

$$\Delta I_{Lo} = (V_{IN} - V_{OUT}) \cdot D/(Lo \cdot f_{SW})$$

$R_{DS(on)}$ is the ON resistance of the MOSFET at the applied gate drive voltage.

Q_{switch} is the post gate threshold portion of the gate-to-source charge plus the gate-to-drain charge. This may be specified in the data sheet or approximated from the gate-charge curve as shown in the Figure 15.

$$Q_{switch} = Q_{gs2} + Q_{gd}$$

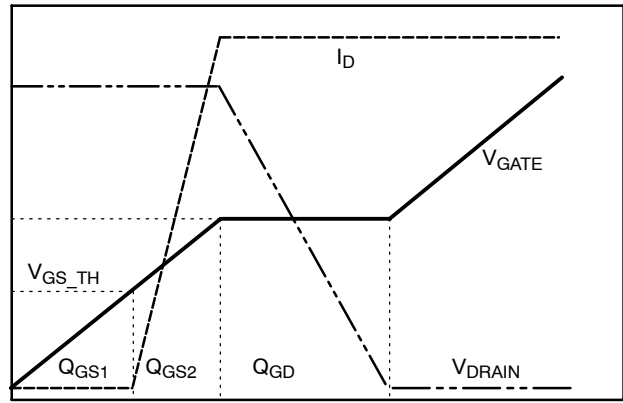


Figure 15. MOSFET Switching Characteristics

I_g is the output current from the gate driver IC.

V_{IN} is the input voltage to the converter.

f_{sw} is the switching frequency of the converter.

Q_G is the MOSFET total gate charge to obtain $R_{DS(on)}$.

Commonly specified in the data sheet.

V_g is the gate drive voltage.

Q_{RR} is the reverse recovery charge of the *lower* MOSFET.

Q_{oss} is the MOSFET output charge specified in the data sheet.

For the lower or synchronous MOSFET, the power dissipation can be approximated from:

$$\begin{aligned} P_{D,SYNCH} = & (I_{RMS,SYNCH}^2 \cdot R_{DS(on)}) \\ & + (V_{fdiode} \cdot I_{O,MAX}/2 \cdot t_{nonoverlap} \cdot f_{SW}) \end{aligned}$$

The first term represents the conduction or IR losses when the MOSFET is ON and the second term represents the diode losses that occur during the gate non-overlap time.

All terms were defined in the previous discussion for the control MOSFET with the exception of:

$$I_{RMS,SYNCH} = \sqrt{1-D} \cdot [(I_{Lo,MAX}^2 + I_{Lo,MAX} \cdot I_{Lo,MIN} + I_{Lo,MIN}^2)/3]^{1/2}$$

where:

V_{fdiode} is the forward voltage of the MOSFET's intrinsic diode at the converter output current.

$t_{nonoverlap}$ is the non-overlap time between the upper and lower gate drivers to prevent cross conduction. This time is usually specified in the data sheet for the control IC.

When the MOSFET power dissipations are known, the designer can calculate the required thermal impedance to maintain a specified junction temperature at the worst case ambient operating temperature

$$\theta_T < (T_J - T_A)/P_D$$

where;

θ_T is the total thermal impedance ($\theta_{JC} + \theta_{SA}$).

θ_{JC} is the junction-to-case thermal impedance of the MOSFET.

θ_{SA} is the sink-to-ambient thermal impedance of the heatsink assuming direct mounting of the MOSFET (no thermal “pad” is used).

T_J is the specified maximum allowed junction temperature.

T_A is the worst case ambient operating temperature.

For TO-220 and TO-263 packages, standard FR-4 copper clad circuit boards will have approximate thermal resistances (θ_{SA}) as shown below:

Pad Size (in ² /mm ²)	Single-Sided 1 oz. Copper
0.5/323	60–65°C/W
0.75/484	55–60°C/W
1.0/645	50–55°C/W
1.5/968	45–50°C/W
2.0/1290	38–42°C/W
2.5/1612	33–37°C/W

As with any power design, proper laboratory testing should be performed to insure the design will dissipate the required power under worst case operating conditions. Variables considered during testing should include maximum ambient temperature, minimum airflow, maximum input voltage, maximum loading, and component variations (i.e. worst case MOSFET $R_{DS(on)}$). Also, the inductors and capacitors share the MOSFET’s heatsinks and will add heat and raise the temperature of the circuit board and MOSFET. For any new design, its advisable to have as much heatsink area as possible – all too often new designs are found to be too hot and require re-design to add heatsinking.

Compensation Capacitor Selection

The nominal output current capability of the error amp is 30 μ A. This current charging the capacitor on the COMP pin is used as soft start for the converter. The COMP pin is going to ramp up to a voltage level that is within 70 mV of what V_{FFB} is going to be when in regulation. This is the voltage that will determine the soft start. Therefore, the COMP capacitor can be established by the following relationship:

$$C = 30 \mu A \times \frac{\text{soft start}}{V_{FFB(REG)}}$$

where:

soft start = output ramp-up time

$V_{FFB(REG)}$ = V_{FFB} voltage when in regulation

30 μ A = COMP output current, typ.

The COMP output current range is given in the data sheet and will affect the ramp-up time. The value of the capacitor on the COMP pin will have an effect on the loop response and the transient response of the converter. Transient response can be enhanced by the addition of a parallel combination of a resistor and capacitor between the COMP pin and the comp capacitor.

Rosc Selection

The switching frequency is programmed by selecting the resistor connected between the R_{OSC} pin and SGND (pin 7). The grounded side of this resistor should be directly connected to the SGND pin, without any other currents flowing between the bottom of the resistor and the pin. Also, avoid running any noisy signals under the resistor, since injected noise could cause frequency jitter. The graph in Figure 6 shows the required resistance to program the frequency. Below 500 kHz, the following formula is accurate:

$$R = 17544/f_{SW} - 4 \text{ k}\Omega$$

where f_{SW} is the switching frequency in kHz.

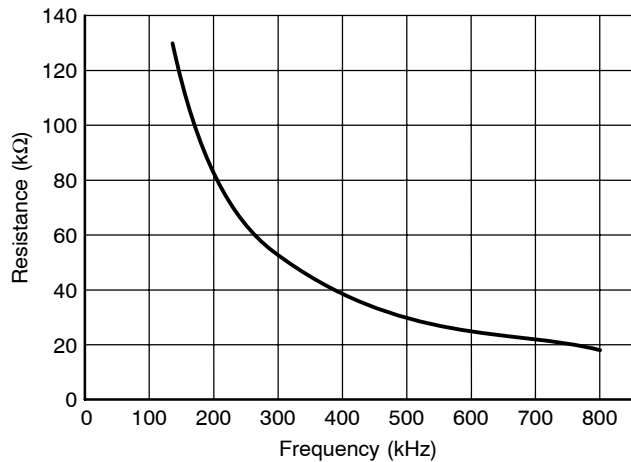


Figure 16. Frequency vs. R_{osc}

Differential Remote Sense Operation

The ability to implement fully differential remote sense is provided by the CS5212. The positive remote sense is implemented by bringing the output remote sense connection to the positive load connection. A low value resistor is connected from V_{out} to the feedback point at the regulator to provide feedback in the instance when the remote sense point is not connected.

The negative remote sense connection is provided by connecting the SGND of the CS5212 to the negative of the load return. Again, a low value resistor should be connected between SGND and LGND at the regulator to provide feedback in the instance when the remote sense point is not connected. The maximum voltage differential between the three grounds for this part is 200 mV.

Feedback Divider Selection

The feedback voltage measured at V_{FB} during normal regulation will be 1.0 V. This voltage is compared to an internal 1.0 V reference and is used to regulate the output voltage. The bias current into the error amplifier is 1.0 μ A max, so select the resistor values so that this current does not add an excessive offset voltage.

V_{FFB} Feedback Selection

To take full advantage of the V² control scheme, a small amount of output ripple must be fed back to the V_{FFB} pin, typically 50 mV. For most application, this requirement is simple to achieve and the V_{FFB} can be connected directly to the V_{FB} pin. There are some application that have to meet stringent load transient requirements. One of the key factor in achieving tight dynamic voltage regulation is low ESR. Low ESR at the regulator output results in low output voltage ripple. This situation could result in increase noise sensitivity and a potential for loop instability. In applications where the output ripple is not sufficient, the performance of the CS5212 can be improved by adding a fixed amount external ramp compensation to the V_{FFB} pin. Refer to Figure 17, the amount of ramp at the V_{FFB} pin depends on the switch node Voltage, Feedback Voltage, R1 and C2.

$$V_{\text{ramp}} = (V_{\text{sw}} - V_{\text{FB}}) \times t_{\text{on}} / (R1 \times C2)$$

where:

V_{ramp} = amount of ramp needed;

V_{sw} = switch node voltage;

V_{FB} = voltage feedback, 1 V;

t_{on} = switch on-time.

To minimize the lost in efficiency R1 resistance should be large, typically 100 k or larger. With R1 chosen, C2 can be determined by the following;

$$C2 = (V_{\text{sw}} - V_{\text{FB}}) \times t_{\text{on}} / (R1 \times V_{\text{ramp}})$$

C1 is used as a bypass capacitor and its value should be equal to or greater than C2.

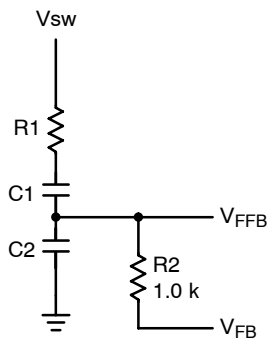


Figure 17. Small RC Filter Providing the Proper Voltage Ramp at the Beginning of Each On-Time Cycle

Maximum Frequency Operation

The minimum pulse width may limit the maximum operating frequency. The duty factor, given by the output/input voltage ratio, multiplied by the period determines the pulse width during normal operation. This pulse width must be greater than 200 ns, or duty cycle jitter could become excessive. For low pulse widths below 300 ns, external slope compensation should be added to the V_{FFB}

pin to increase the PWM ramp signal and improve stability. 50 mV of added ramp at the V_{FFB} pin is typically enough.

Current Sense Component Selection

The current limit threshold is set by sensing a 60 mV voltage differential between the IS+ and IS- pins. Referring to Figure 18, the time constant of the R2, C1 filter should be set larger than the L/R1 time constant under worst case tolerances, to prevent overshoot in the sensed voltage and tripping the current limit too low. Resistor R3 of value equal to R2 is added for bias current cancellation. R2 and R3 should not be made too large, to reduce errors from bias current offsets. For typical L/R time constants, a 0.1 μF capacitor for C1 will allow R2 to be between 1.0 k and 10 kΩ.

The current limit without R4 and R5, which are optional, is given by 60 mV/R1, where R1 is the internal resistance of the inductor, obtained from the manufacturer. The addition of R5 can be used to decrease the current limit to a value given by:

$$I_{\text{LIM}} = (60 \text{ mV} - (V_{\text{OUT}} \times R3 / (R3 + R5))) / R1$$

where V_{OUT} is the output voltage.

Similarly, omitting R5 and adding R4 will increase the current limit to a value given by:

$$I_{\text{LIM}} = 60 \text{ mV} / R1 \times (1 + R2 / R4)$$

Essentially, R4 or R5 are used to increase or decrease the inductor voltage drop which corresponds to 60 mV at the IS+ and IS- pins.

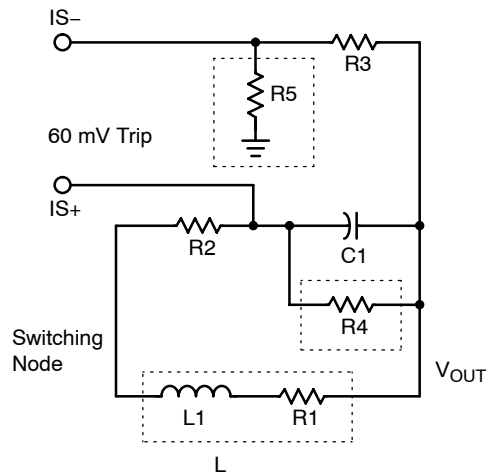


Figure 18. Current Limit

Boost Component Selection for Upper and Lower FET Gate Drive

The boost (BST) pin provides for application of a higher voltage to drive the upper FET. This voltage may be provided by a fixed higher voltage or it may be generated with a boost capacitor and charging diodes, as shown in Figure 11. The voltage in the boost configuration would be the summation of the voltage from the charging diodes and

the output voltage swing. Care must be taken to keep the peak voltage with respect to ground less than 20 V peak. The capacitor value should be ten times larger than the capacitance of the top FET. The boost circuit requires a modification to achieve startup. See Rpull-up Selection for boost circuit startup.

Rpull-up Value Selection for Boost Circuit Startup

The CS5212 application circuit incorporates a pull-up resistor, R7, into the boost circuitry. This resistor is essential to achieving startup of the boost circuit. At startup, the GATE(H) output may be limited to 0.8 V, due to internal Vbe drops. Until the boost circuitry charges up, the GATE(H) output cannot provide sufficient Vgs to turn on the MOSFET. A resistor from GATE(H) to BST allows bypassing of the GATE(H) driver until the boost circuitry is charged. The time constant, set by the pull-up resistor and

the Cin of the top MOSFET, must be fast enough to turn on the MOSFET during the switching period. The following equation is used to determine Rpull-up:

$$R_{\text{pull-up}} < \frac{1}{(C_{\text{in}} \times f_{\text{SW}})}$$

where f_{SW} is the switching frequency.

Choosing components according to this equation will insure that approximately 63% of the boost voltage will be applied to GATE(H) within one switching period. To start charge pumping, the control MOSFET must pull up the switching node above 0.6 V, two Schottky drops, which will allow V_C voltage to increase. Therefore, the voltage applied by GATE(H) must be 0.6 V greater than V_{th} of the top FET. Both high- and low-side switches must be sublogic level MOSFETs with R_{DS(on)} specified at 2.5 Vgs in order to ensure proper up.

CS5212

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping
CS5212ED14	$-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$	SO-14	55 Units/Rail
CS5212EDR14		SO-14	2500 Tape & Reel
CS5212GD14	$0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$	SO-14	55 Units/Rail
CS5212GDR14		SO-14	2500 Tape & Reel

LM2574

0.5 A, Adjustable Output Voltage, Step-Down Switching Regulator

The LM2574 series of regulators are monolithic integrated circuits ideally suited for easy and convenient design of a step-down switching regulator (buck converter). All circuits of this series are capable of driving a 0.5 A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3 V, 5.0 V, 12 V, 15 V, and an adjustable output version.

These regulators were designed to minimize the number of external components to simplify the power supply design. Standard series of inductors optimized for use with the LM2574 are offered by several different inductor manufacturers.

Since the LM2574 converter is a switch-mode power supply, its efficiency is significantly higher in comparison with popular three-terminal linear regulators, especially with higher input voltages. In most cases, the power dissipated by the LM2574 regulator is so low, that the copper traces on the printed circuit board are normally the only heatsink needed and no additional heatsinking is required.

The LM2574 features include a guaranteed $\pm 4\%$ tolerance on output voltage within specified input voltages and output load conditions, and $\pm 10\%$ on the oscillator frequency ($\pm 2\%$ over 0°C to $+125^\circ\text{C}$). External shutdown is included, featuring 60 μA (typical) standby current. The output switch includes cycle-by-cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

Features

- 3.3 V, 5.0 V, 12 V, 15 V, and Adjustable Output Versions
- Adjustable Version Output Voltage Range, 1.23 to 37 V $\pm 4\%$ max over Line and Load Conditions
- Guaranteed 0.5 A Output Current
- Wide Input Voltage Range: 4.75 to 40 V
- Requires Only 4 External Components
- 52 kHz Fixed Frequency Internal Oscillator
- TTL Shutdown Capability, Low Power Standby Mode
- High Efficiency
- Uses Readily Available Standard Inductors
- Thermal Shutdown and Current Limit Protection

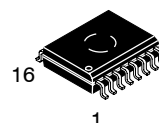
Applications

- Simple and High-Efficiency Step-Down (Buck) Regulators
- Efficient Pre-regulator for Linear Regulators
- On-Card Switching Regulators
- Positive to Negative Converters (Buck-Boost)
- Negative Step-Up Converters
- Power Supply for Battery Chargers

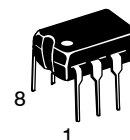


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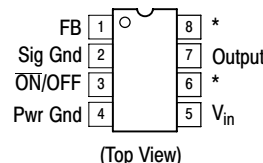
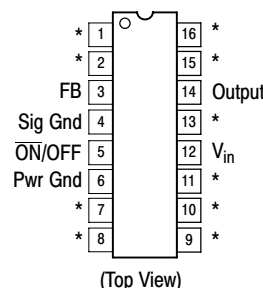


**SO-16W
DW SUFFIX
CASE 751G**



**PDIP-8
N SUFFIX
CASE 626**

PIN CONNECTIONS



* No internal connection, but should be soldered to PC board for best heat transfer.

ORDERING INFORMATION

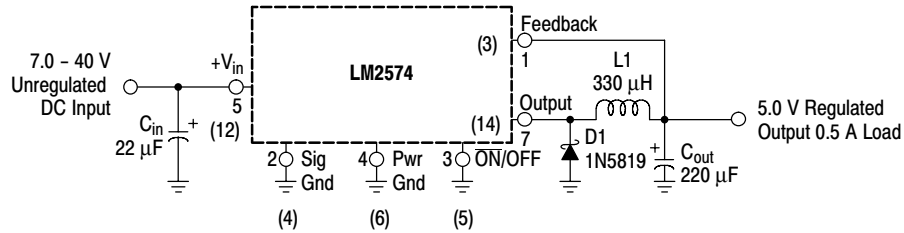
See detailed ordering and shipping information in the package dimensions section on page 133 of this data sheet.

DEVICE MARKING INFORMATION

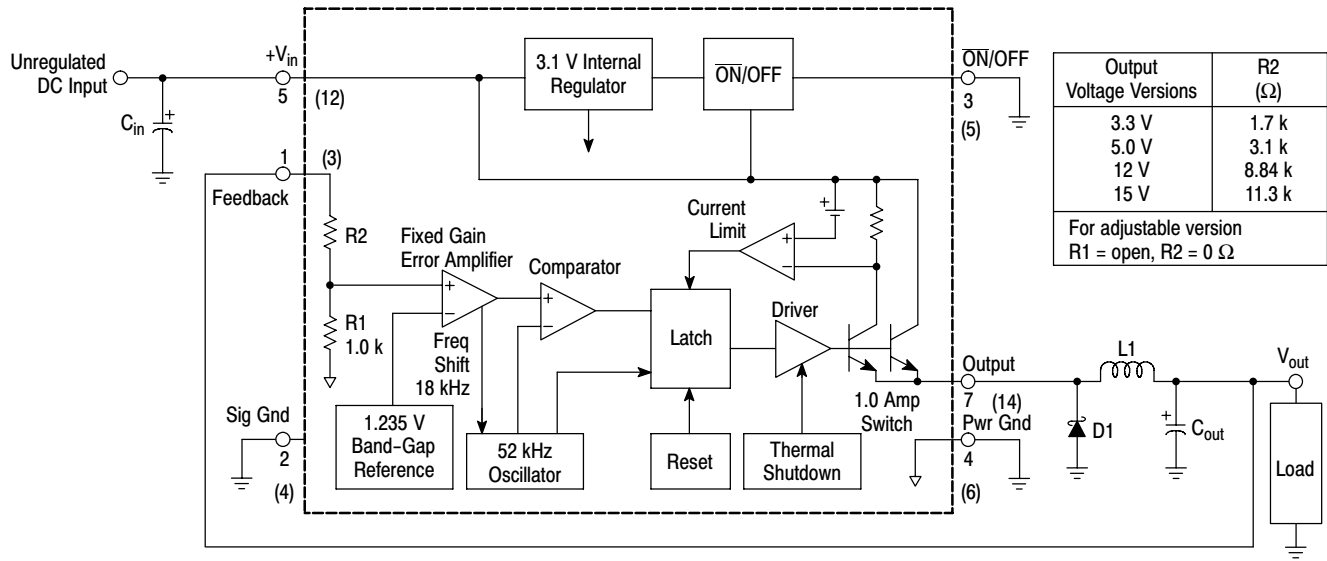
See general marking information in the device marking section on page 133 of this data sheet.

LM2574

Typical Application (Fixed Output Voltage Versions)



Representative Block Diagram and Typical Application



NOTE: Pin numbers in () are for the SO-16W package.

Figure 1. Block Diagram and Typical Application

ABSOLUTE MAXIMUM RATINGS (Absolute Maximum Ratings indicate limits beyond which damage to the device may occur).

Rating	Symbol	Value	Unit
Maximum Supply Voltage	V_{in}	45	V
ON/OFF Pin Input Voltage	–	$-0.3 \text{ V} \leq V \leq +V_{in}$	V
Output Voltage to Ground (Steady State)	–	-1.0	V
DW Suffix, Plastic Package Case 751G Max Power Dissipation Thermal Resistance, Junction-to-Air	P_D $R_{\theta JA}$	Internally Limited 145	W °C/W
N Suffix, Plastic Package Case 626 Max Power Dissipation Thermal Resistance, Junction-to-Ambient Thermal Resistance, Junction-to-Case	P_D $R_{\theta JA}$ $R_{\theta JC}$	Internally Limited 100 5.0	W °C/W °C/W
Storage Temperature Range	T_{stg}	-65°C to $+150^{\circ}\text{C}$	°C
Minimum ESD Rating (Human Body Model: $C = 100 \text{ pF}$, $R = 1.5 \text{ k}\Omega$)	–	2.0	kV
Lead Temperature (Soldering, 10 seconds)	–	260	°C
Maximum Junction Temperature	T_J	150	°C

NOTE: ESD data available upon request.

LM2574

OPERATING RATINGS (Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics).

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	-40 to +125	°C
Supply Voltage	V_{in}	40	V

SYSTEM PARAMETERS ([Note 1] Test Circuit Figure 16)

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $V_{in} = 12$ V for the 3.3 V, 5.0 V, and Adjustable version, $V_{in} = 25$ V for the 12 V version, $V_{in} = 30$ V for the 15 V version. $I_{Load} = 100$ mA. For typical values $T_J = 25^\circ\text{C}$, for min/max values T_J is the operating junction temperature range that applies [Note 2], unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit

LM2574-3.3 ([Note 1] Test Circuit Figure 16)

Output Voltage ($V_{in} = 12$ V, $I_{Load} = 100$ mA, $T_J = 25^\circ\text{C}$)	V_{out}	3.234	3.3	3.366	V
Output Voltage ($4.75 \text{ V} \leq V_{in} \leq 40$ V, $0.1 \text{ A} \leq I_{Load} \leq 0.5$ A) $T_J = 25^\circ\text{C}$ $T_J = -40$ to $+125^\circ\text{C}$	V_{out}	3.168 3.135	3.3 –	3.432 3.465	V
Efficiency ($V_{in} = 12$ V, $I_{Load} = 0.5$ A)	η	–	72	–	%

LM2574-5 ([Note 1] Test Circuit Figure 16)

Output Voltage ($V_{in} = 12$ V, $I_{Load} = 100$ mA, $T_J = 25^\circ\text{C}$)	V_{out}	4.9	5.0	5.1	V
Output Voltage ($7.0 \text{ V} \leq V_{in} \leq 40$ V, $0.1 \text{ A} \leq I_{Load} \leq 0.5$ A) $T_J = 25^\circ\text{C}$ $T_J = -40$ to $+125^\circ\text{C}$	V_{out}	4.8 4.75	5.0 –	5.2 5.25	V
Efficiency ($V_{in} = 12$ V, $I_{Load} = 0.5$ A)	η	–	77	–	%

LM2574-12 ([Note 1] Test Circuit Figure 16)

Output Voltage ($V_{in} = 25$ V, $I_{Load} = 100$ mA, $T_J = 25^\circ\text{C}$)	V_{out}	11.76	10	12.24	V
Output Voltage ($15 \text{ V} \leq V_{in} \leq 40$ V, $0.1 \text{ A} \leq I_{Load} \leq 0.5$ A) $T_J = 25^\circ\text{C}$ $T_J = -40$ to $+125^\circ\text{C}$	V_{out}	11.52 11.4	12 –	12.48 12.6	V
Efficiency ($V_{in} = 15$ V, $I_{Load} = 0.5$ A)	η	–	88	–	%

LM2574-15 ([Note 1] Test Circuit Figure 16)

Output Voltage ($V_{in} = 30$ V, $I_{Load} = 100$ mA, $T_J = 25^\circ\text{C}$)	V_{out}	14.7	15	15.3	V
Output Voltage ($18 \text{ V} < V_{in} < 40$ V, $0.1 \text{ A} < I_{Load} < 0.5$ A) $T_J = 25^\circ\text{C}$ $T_J = -40$ to $+125^\circ\text{C}$	V_{out}	14.4 14.25	15 –	15.6 15.75	V
Efficiency ($V_{in} = 18$ V, $I_{Load} = 0.5$ A)	η	–	88	–	%

LM2574 ADJUSTABLE VERSION ([Note 1] Test Circuit Figure 16)

Feedback Voltage $V_{in} = 12$ V, $I_{Load} = 100$ mA, $V_{out} = 5.0$ V, $T_J = 25^\circ\text{C}$	V_{FB}	1.217	1.23	1.243	V
Feedback Voltage $7.0 \text{ V} \leq V_{in} \leq 40$ V, $0.1 \text{ A} \leq I_{Load} \leq 0.5$ A, $V_{out} = 5.0$ V $T_J = 25^\circ\text{C}$ $T_J = -40$ to $+125^\circ\text{C}$	V_{FBT}	1.193 1.18	1.23 –	1.267 1.28	V
Efficiency ($V_{in} = 12$ V, $I_{Load} = 0.5$ A, $V_{out} = 5.0$ V)	η	–	77	–	%

- External components such as the catch diode, inductor, input and output capacitors can affect the switching regulator system performance. When the LM2574 is used as shown in the Figure 16 test circuit, the system performance will be as shown in the system parameters section of the Electrical Characteristics.
- Tested junction temperature range for the LM2574: $T_{low} = -40^\circ\text{C}$ $T_{high} = +125^\circ\text{C}$.

LM2574

SYSTEM PARAMETERS ([Note 3] Test Circuit Figure 16)

ELECTRICAL CHARACTERISTICS (continued) (Unless otherwise specified, $V_{in} = 12\text{ V}$ for the 3.3 V, 5.0 V, and Adjustable version, $V_{in} = 25\text{ V}$ for the 12 V version, $V_{in} = 30\text{ V}$ for the 15 V version. $I_{Load} = 100\text{ mA}$. For typical values $T_J = 25^\circ\text{C}$, for min/max values T_J is the operating junction temperature range that applies [Note 4], unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
ALL OUTPUT VOLTAGE VERSIONS					
Feedback Bias Current $V_{out} = 5.0\text{ V}$ (Adjustable Version Only) $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	I_b	– –	25 –	100 200	nA
Oscillator Frequency (Note 5) $T_J = 25^\circ\text{C}$ $T_J = 0\text{ to }+125^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	f_O	– 47 42	52 52 –	– 58 63	kHz
Saturation Voltage ($I_{out} = 0.5\text{ A}$, [Note 6]) $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	V_{sat}	– –	1.0 –	1.2 1.4	V
Max Duty Cycle (“on”) (Note 7)	DC	93	98	–	%
Current Limit Peak Current (Notes 5 and 6) $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	I_{CL}	0.7 0.65	1.0 –	1.6 1.8	A
Output Leakage Current (Notes 8 and 9), $T_J = 25^\circ\text{C}$ Output = 0 V Output = – 1.0 V	I_L	– –	0.6 10	2.0 30	mA
Quiescent Current (Note 8) $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	I_Q	– –	5.0 –	9.0 11	mA
Standby Quiescent Current ($\overline{\text{ON/OFF}}$ Pin = 5.0 V (“off”)) $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	I_{stby}	– –	60 –	200 400	μA
$\overline{\text{ON/OFF}}$ Pin Logic Input Level $V_{out} = 0\text{ V}$ $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$ Nominal Output Voltage $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	V_{IH} V_{IL}	2.2 2.4 – –	1.4 – 1.2 –	– – 1.0 0.8	V
$\overline{\text{ON/OFF}}$ P_{in} Input Current $\overline{\text{ON/OFF}}$ $P_{in} = 5.0\text{ V}$ (“off”), $T_J = 25^\circ\text{C}$ $\overline{\text{ON/OFF}}$ $P_{in} = 0\text{ V}$ (“on”), $T_J = 25^\circ\text{C}$	I_{IH} I_{IL}	– –	15 0	30 5.0	μA

- External components such as the catch diode, inductor, input and output capacitors can affect the switching regulator system performance. When the LM2574 is used as shown in the Figure 16 test circuit, the system performance will be as shown in the system parameters section of the Electrical Characteristics.
- Tested junction temperature range for the LM2574: $T_{low} = -40^\circ\text{C}$ $T_{high} = +125^\circ\text{C}$.
- The oscillator frequency reduces to approximately 18 kHz in the event of an output short or an overload which causes the regulated output voltage to drop approximately 40% from the nominal output voltage. This self protection feature lowers the average power dissipation of the IC by lowering the minimum duty cycle from 5% down to approximately 2%.
- Output (Pin 2) sourcing current. No diode, inductor or capacitor connected to the output pin.
- Feedback (Pin 4) removed from output and connected to 0 V.
- Feedback (Pin 4) removed from output and connected to 12 V for the Adjustable, 3.3 V, and 5.0 V versions, and 25 V for the 12 V and 15 V versions, to force the output transistor OFF.
- $V_{in} = 40\text{ V}$.

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 16)

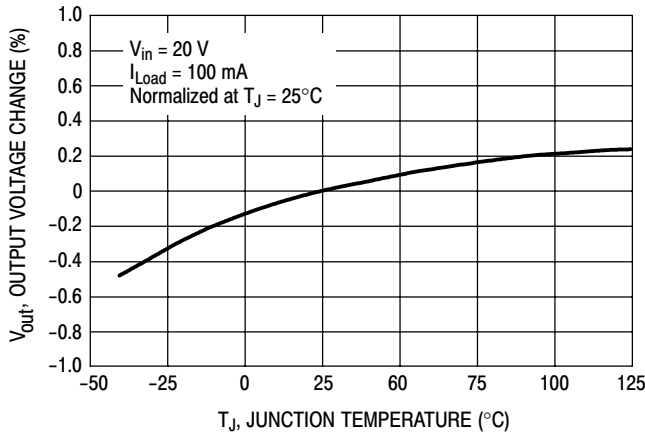


Figure 2. Normalized Output Voltage

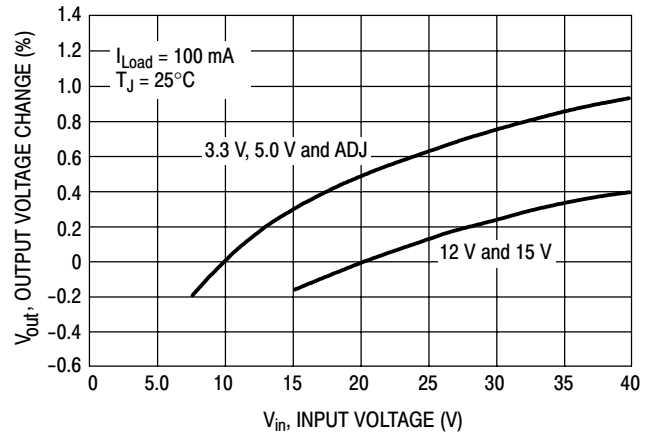


Figure 3. Line Regulation

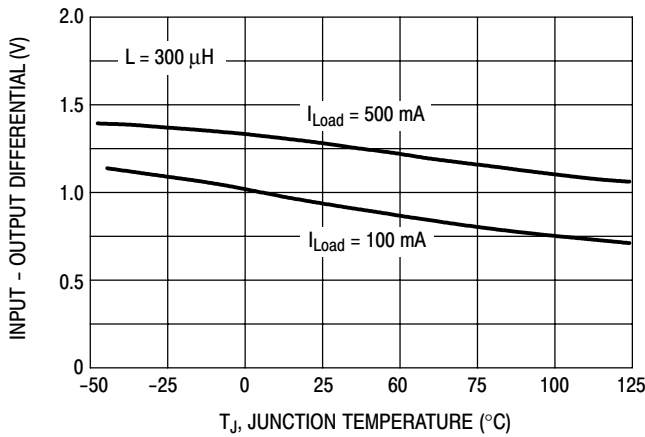


Figure 4. Dropout Voltage

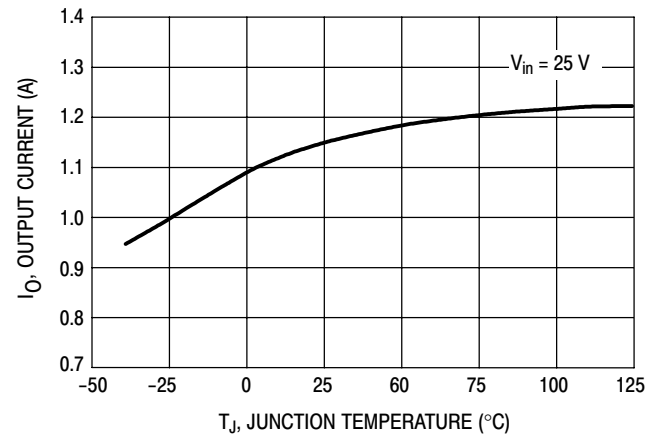


Figure 5. Current Limit

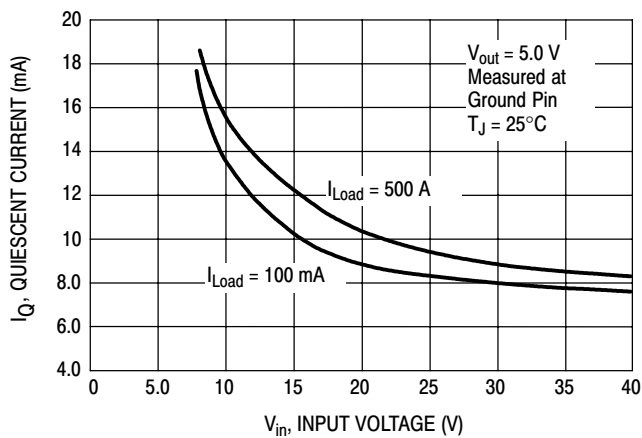


Figure 6. Quiescent Current

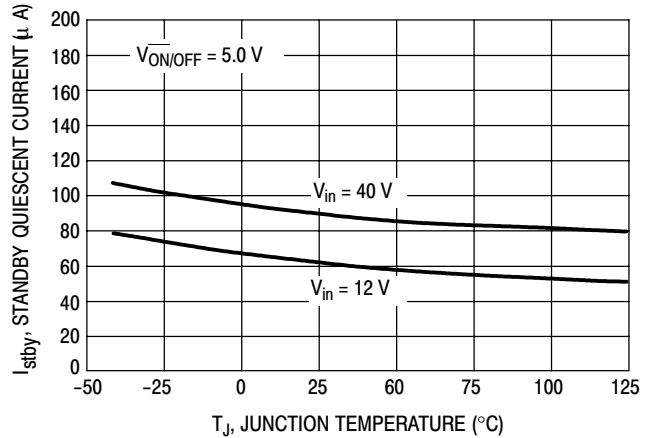


Figure 7. Standby Quiescent Current

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 16) (continued)

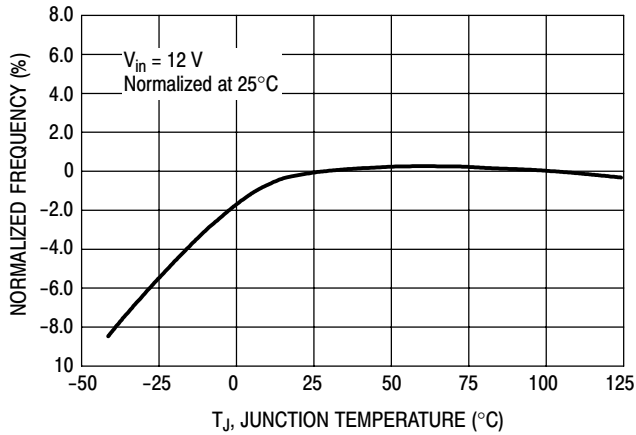


Figure 8. Oscillator Frequency

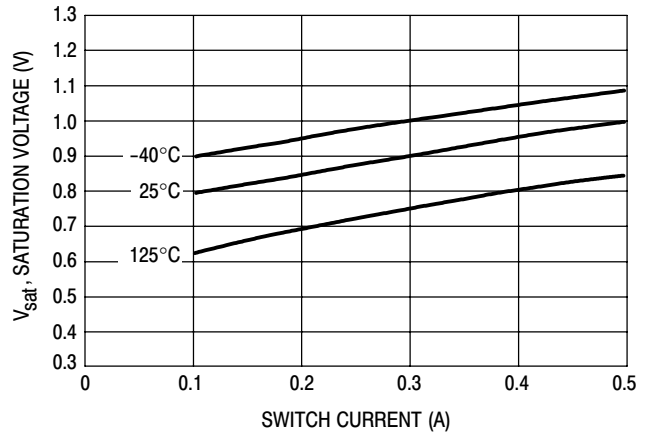


Figure 9. Switch Saturation Voltage

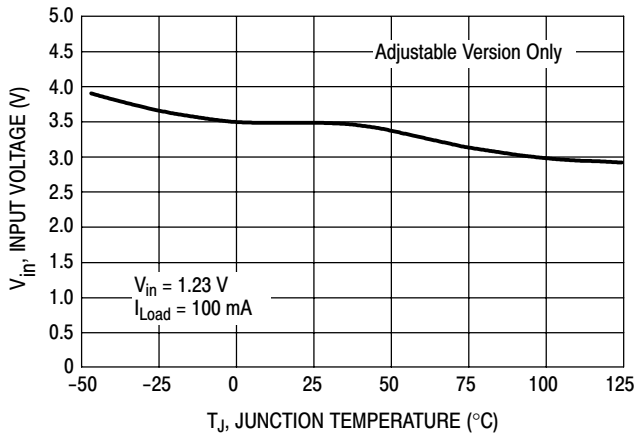


Figure 10. Minimum Operating Voltage

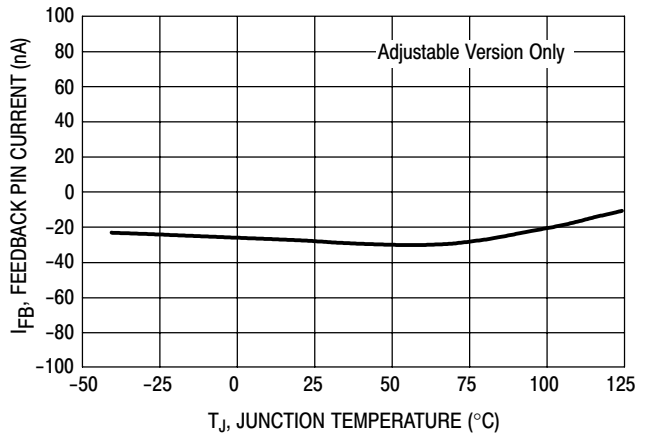
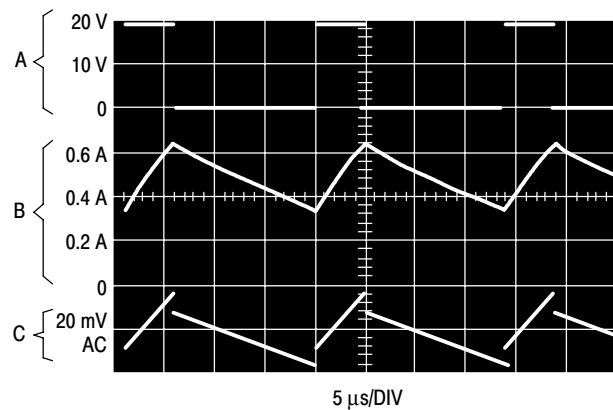
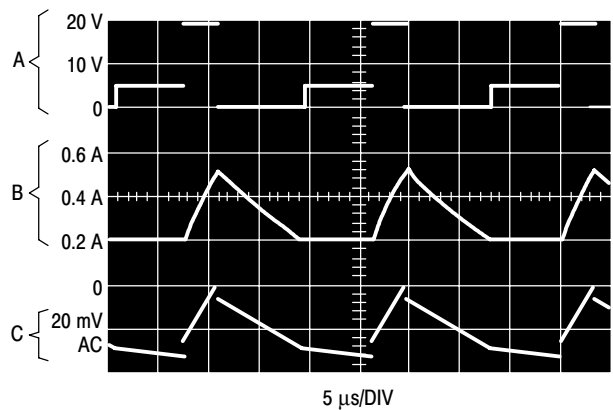


Figure 11. Feedback Pin Current



A: Output Pin Voltage, 10 V/DIV.
B: Inductor Current, 0.2 A/DIV.
C: Output Ripple Voltage, 20 mV/DIV, AC-Coupled

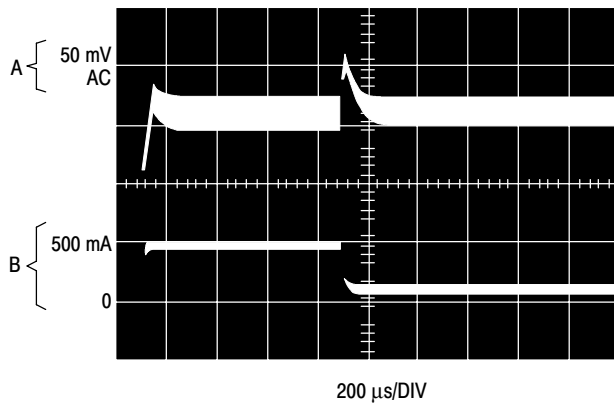
Figure 12. Continuous Mode Switching Waveforms
 $V_{out} = 5.0$ V, 500 mA Load Current, $L = 330$ μ H



A: Output Pin Voltage, 10 V/DIV.
B: Inductor Current, 0.2 A/DIV.
C: Output Ripple Voltage, 20 mV/DIV, AC-Coupled

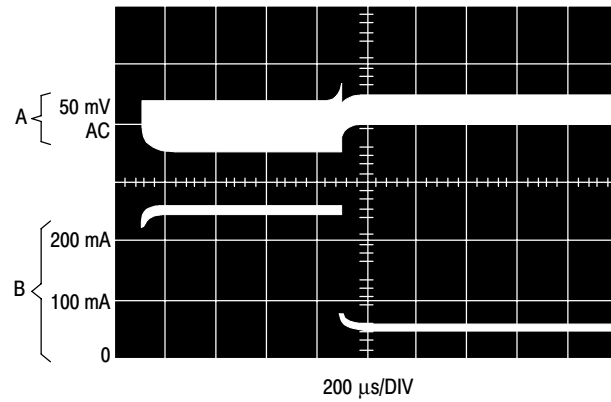
Figure 13. Discontinuous Mode Switching Waveforms
 $V_{out} = 5.0$ V, 100 mA Load Current, $L = 100$ μ H

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 16) (continued)



A: Output Voltage, 50 mV/DIV, AC Coupled
B: 100 mA to 500 mA Load Pulse

Figure 14. 500 mA Load Transient Response for Continuous Mode Operation, $L = 330 \mu\text{H}$, $C_{\text{out}} = 300 \mu\text{F}$

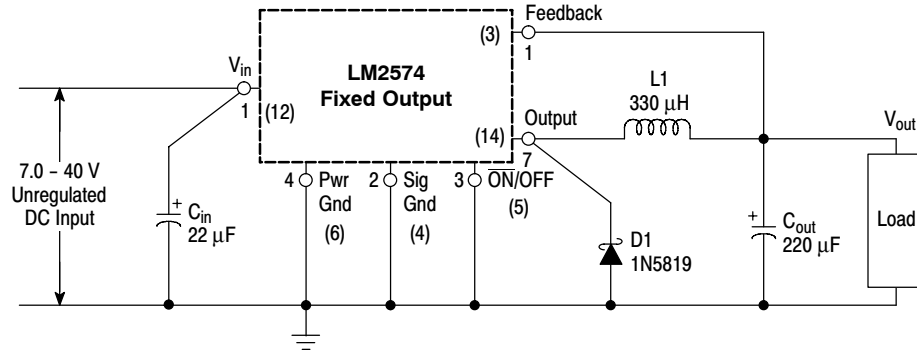


A: Output Voltage, 50 mV/DIV, AC Coupled
B: 50 mA to 250 mA Load Pulse

Figure 15. 250 mA Load Transient Response for Discontinuous Mode Operation, $L = 68 \mu\text{H}$, $C_{\text{out}} = 470 \mu\text{F}$

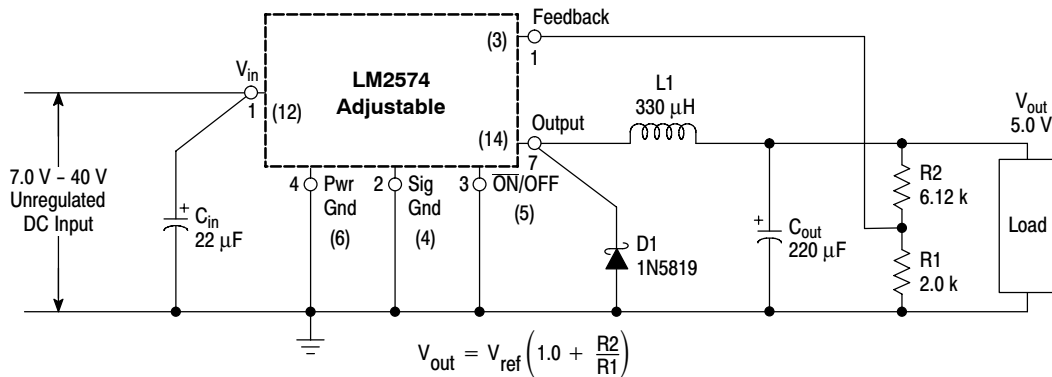
LM2574

Fixed Output Voltage Versions



- C_{in} - 22 μ F, 60 V, Aluminium Electrolytic
- C_{out} - 220 μ F, 25 V, Aluminium Electrolytic
- D1 - Schottky, 1N5819
- L1 - 330 μ H, (For 5.0 V_{in} , 3.3 V_{out} , use 100 μ H)
- R1 - 2.0 k, 0.1%
- R2 - 6.12 k, 0.1%

Adjustable Output Voltage Versions



$$V_{out} = V_{ref} \left(1.0 + \frac{R2}{R1} \right)$$

$$R2 = R1 \left(\frac{V_{out}}{V_{ref}} - 1.0 \right)$$

Where $V_{ref} = 1.23$ V, R1
between 1.0 k Ω and 5.0 k Ω

NOTE: Pin numbers in () are for the SO-16W package.

Figure 16. Test Circuit and Layout Guidelines

PCB LAYOUT GUIDELINES

As in any switching regulator, the layout of the printed circuit board is very important. Rapidly switching currents associated with wiring inductance, stray capacitance and parasitic inductance of the printed circuit board traces can generate voltage transients which can generate electromagnetic interferences (EMI) and affect the desired operation. As indicated in the Figure 16, to minimize inductance and ground loops, the length of the leads indicated by heavy lines should be kept as short as possible.

For best results, single-point grounding (as indicated) or ground plane construction should be used.

On the other hand, the PCB area connected to the Pin 7 (emitter of the internal switch) of the LM2574 should be kept to a minimum in order to minimize coupling to sensitive circuitry.

Another sensitive part of the circuit is the feedback. It is important to keep the sensitive feedback wiring short. To assure this, physically locate the programming resistors near to the regulator, when using the adjustable version of the LM2574 regulator.

PIN FUNCTION DESCRIPTION

Pin		Symbol	Description (Refer to Figure 1)
SO-16W	PDIP-8		
12	5	V_{in}	This pin is the positive input supply for the LM2574 step-down switching regulator. In order to minimize voltage transients and to supply the switching currents needed by the regulator, a suitable input bypass capacitor must be present (C_{in} in Figure 1).
14	7	Output	This is the emitter of the internal switch. The saturation voltage V_{sat} of this output switch is typically 1.0 V. It should be kept in mind that the PCB area connected to this pin should be kept to a minimum in order to minimize coupling to sensitive circuitry.
4	2	Sig Gnd	Circuit signal ground pin. See the information about the printed circuit board layout.
6	4	Pwr Gnd	Circuit power ground pin. See the information about the printed circuit board layout.
3	1	Feedback	This pin senses regulated output voltage to complete the feedback loop. The signal is divided by the internal resistor divider network R2, R1 and applied to the non-inverting input of the internal error amplifier. In the Adjustable version of the LM2574 switching regulator, this pin is the direct input of the error amplifier and the resistor network R2, R1 is connected externally to allow programming of the output voltage.
5	3	ON/OFF	It allows the switching regulator circuit to be shut down using logic level signals, thus dropping the total input supply current to approximately 80 μ A. The input threshold voltage is typically 1.5 V. Applying a voltage above this value (up to $+V_{in}$) shuts the regulator off. If the voltage applied to this pin is lower than 1.5 V or if this pin is left open, the regulator will be in the "on" condition.

DESIGN PROCEDURE

Buck Converter Basics

The LM2574 is a "Buck" or Step-Down Converter which is the most elementary forward-mode converter. Its basic schematic can be seen in Figure 17.

The operation of this regulator topology has two distinct time periods. The first one occurs when the series switch is on, the input voltage is connected to the input of the inductor.

The output of the inductor is the output voltage, and the rectifier (or catch diode) is reverse biased. During this period, since there is a constant voltage source connected across the inductor, the inductor current begins to linearly ramp upwards, as described by the following equation:

$$I_{L(on)} = \frac{(V_{in} - V_{out}) t_{on}}{L}$$

During this "on" period, energy is stored within the core material in the form of magnetic flux. If the inductor is properly designed, there is sufficient energy stored to carry the requirements of the load during the "off" period.

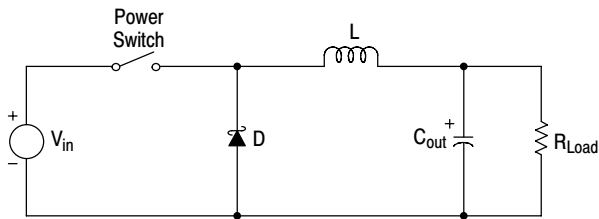


Figure 17. Basic Buck Converter

The next period is the "off" period of the power switch. When the power switch turns off, the voltage across the inductor reverses its polarity and is clamped at one diode voltage drop below ground by the catch diode. Current now flows through the catch diode thus maintaining the load

current loop. This removes the stored energy from the inductor. The inductor current during this time is:

$$I_{L(off)} = \frac{(V_{out} - V_D) t_{off}}{L}$$

This period ends when the power switch is once again turned on. Regulation of the converter is accomplished by varying the duty cycle of the power switch. It is possible to describe the duty cycle as follows:

$$d = \frac{t_{on}}{T}, \text{ where } T \text{ is the period of switching.}$$

For the buck converter with ideal components, the duty cycle can also be described as:

$$d = \frac{V_{out}}{V_{in}}$$

Figure 18 shows the buck converter idealized waveforms of the catch diode voltage and the inductor current.

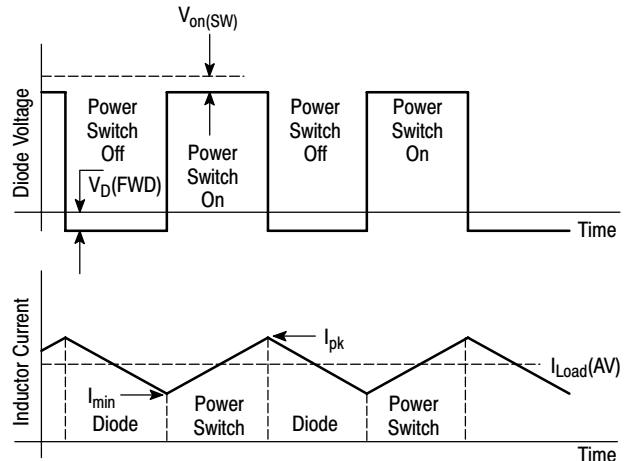


Figure 18. Buck Converter Idealized Waveforms

Procedure (Fixed Output Voltage Version) In order to simplify the switching regulator design, a step-by-step design procedure and example is provided.

Procedure	Example
Given Parameters: V_{out} = Regulated Output Voltage (3.3 V, 5.0 V, 12 V or 15 V) $V_{in(max)}$ = Maximum Input Voltage $I_{Load(max)}$ = Maximum Load Current	Given Parameters: V_{out} = 5.0 V $V_{in(max)}$ = 15 V $I_{Load(max)}$ = 0.4 A
1. Controller IC Selection According to the required input voltage, output voltage and current, select the appropriate type of the controller IC output voltage version.	1. Controller IC Selection According to the required input voltage, output voltage, current polarity and current value, use the LM2574-5 controller IC.
2. Input Capacitor Selection (C_{in}) To prevent large voltage transients from appearing at the input and for stable operation of the converter, an aluminium or tantalum electrolytic bypass capacitor is needed between the input pin + V_{in} and ground pin Gnd. This capacitor should be located close to the IC using short leads. This capacitor should have a low ESR (Equivalent Series Resistance) value.	2. Input Capacitor Selection (C_{in}) A 22 μ F, 25 V aluminium electrolytic capacitor located near to the input and ground pins provides sufficient bypassing.
3. Catch Diode Selection (D1) A. Since the diode maximum peak current exceeds the regulator maximum load current, the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design the diode should have a current rating equal to the maximum current limit of the LM2574 to be able to withstand a continuous output short. B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.	3. Catch Diode Selection (D1) A. For this example the current rating of the diode is 1.0 A. B. Use a 20 V 1N5817 Schottky diode, or any of the suggested fast recovery diodes shown in Table 1.
4. Inductor Selection (L1) A. According to the required working conditions, select the correct inductor value using the selection guide from Figures 19 to 23. B. From the appropriate inductor selection guide, identify the inductance region intersected by the Maximum Input Voltage line and the Maximum Load Current line. Each region is identified by an inductance value and an inductor code. C. Select an appropriate inductor from the several different manufacturers part numbers listed in Table 2. The designer must realize that the inductor current rating must be higher than the maximum peak current flowing through the inductor. This maximum peak current can be calculated as follows: $I_{p(max)} = I_{Load(max)} + \frac{(V_{in} - V_{out})t_{on}}{2L}$ where t_{on} is the "on" time of the power switch and $t_{on} = \frac{V_{out}}{V_{in}} \times \frac{1.0}{f_{osc}}$ For additional information about the inductor, see the inductor section in the "EXTERNAL COMPONENTS" section of this data sheet.	4. Inductor Selection (L1) A. Use the inductor selection guide shown in Figure 20. B. From the selection guide, the inductance area intersected by the 15 V line and 0.4 A line is 330. C. Inductor value required is 330 μ H. From Table 2, choose an inductor from any of the listed manufacturers.

Procedure (Fixed Output Voltage Version) (continued) In order to simplify the switching regulator design, a step-by-step design procedure and example is provided.

Procedure	Example
5. Output Capacitor Selection (C_{out}) A. Since the LM2574 is a forward-mode switching regulator with voltage mode control, its open loop 2-pole-1-zero frequency characteristic has the dominant pole-pair determined by the output capacitor and inductor values. For stable operation and an acceptable ripple voltage, (approximately 1% of the output voltage) a value between 100 μ F and 470 μ F is recommended. B. Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating at least 8.0 V is appropriate, and a 10 V or 16 V rating is recommended.	5. Output Capacitor Selection (C_{out}) A. $C_{out} = 100 \mu\text{F}$ to 470 μF standard aluminium electrolytic. B. Capacitor voltage rating = 20 V.

Procedure (Adjustable Output Version: LM2574-ADJ)

Procedure	Example
Given Parameters: V_{out} = Regulated Output Voltage $V_{in(max)}$ = Maximum DC Input Voltage $I_{Load(max)}$ = Maximum Load Current	Given Parameters: $V_{out} = 24 \text{ V}$ $V_{in(max)} = 40 \text{ V}$ $I_{Load(max)} = 0.4 \text{ A}$
1. Programming Output Voltage To select the right programming resistor R1 and R2 value (see Figure 2) use the following formula: $V_{out} = V_{ref} \left(1.0 + \frac{R2}{R1} \right) \quad \text{where } V_{ref} = 1.23 \text{ V}$ Resistor R1 can be between 1.0 k Ω and 5.0 k Ω . (For best temperature coefficient and stability with time, use 1% metal film resistors). $R2 = R1 \left(\frac{V_{out}}{V_{ref}} - 1.0 \right)$	1. Programming Output Voltage (selecting R1 and R2) Select R1 and R2 : $V_{out} = 1.23 \left(1.0 + \frac{R2}{R1} \right) \quad \text{Select } R1 = 1.0 \text{ k}\Omega$ $R2 = R1 \left(\frac{V_{out}}{V_{ref}} - 1.0 \right) = 1.0 \text{ k} \left(\frac{24 \text{ V}}{1.23 \text{ V}} - 1.0 \right)$ $R2 = 18.51 \text{ k}\Omega, \text{ choose a } 18.7 \text{ k}\Omega \text{ metal film resistor.}$
2. Input Capacitor Selection (C_{in}) To prevent large voltage transients from appearing at the input and for stable operation of the converter, an aluminium or tantalum electrolytic bypass capacitor is needed between the input pin + V_{in} and ground pin Gnd. This capacitor should be located close to the IC using short leads. This capacitor should have a low ESR (Equivalent Series Resistance) value. For additional information see input capacitor section in the "EXTERNAL COMPONENTS" section of this data sheet.	2. Input Capacitor Selection (C_{in}) A 22 μ F aluminium electrolytic capacitor located near the input and ground pin provides sufficient bypassing.
3. Catch Diode Selection (D1) A. Since the diode maximum peak current exceeds the regulator maximum load current the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design, the diode should have a current rating equal to the maximum current limit of the LM2574 to be able to withstand a continuous output short. B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.	3. Catch Diode Selection (D1) A. For this example, a 1.0 A current rating is adequate. B. Use a 50 V MBR150 Schottky diode or any suggested fast recovery diodes in Table 1.

Procedure (Adjustable Output Version: LM2574-ADJ)

Procedure	Example
4. Inductor Selection (L₁) A. Use the following formula to calculate the inductor Volt x microsecond [V x μs] constant: $E \times T = (V_{in} - V_{out}) \frac{V_{out}}{V_{in}} \times \frac{10^6}{F[\text{Hz}]} [V \times \mu\text{s}]$ B. Match the calculated E x T value with the corresponding number on the vertical axis of the Inductor Value Selection Guide shown in Figure 23. This E x T constant is a measure of the energy handling capability of an inductor and is dependent upon the type of core, the core area, the number of turns, and the duty cycle. C. Next step is to identify the inductance region intersected by the E x T value and the maximum load current value on the horizontal axis shown in Figure 27. D. From the inductor code, identify the inductor value. Then select an appropriate inductor from Table 2. The inductor chosen must be rated for a switching frequency of 52 kHz and for a current rating of 1.15 x I_{Load}. The inductor current rating can also be determined by calculating the inductor peak current: $I_{p(\text{max})} = I_{\text{Load}(\text{max})} + \frac{(V_{in} - V_{out})t_{on}}{2L}$ where t_{on} is the “on” time of the power switch and $t_{on} = \frac{V_{out}}{V_{in}} \times \frac{1.0}{f_{osc}}$ For additional information about the inductor, see the inductor section in the “External Components” section of this data sheet.	4. Inductor Selection (L₁) A. Calculate E x T [V x μs] constant : $E \times T = (40 - 24) \times \frac{24}{40} \times \frac{1000}{52} = 105 [V \times \mu\text{s}]$ B. E x T = 185 [V x μs] C. I_{Load(max)} = 0.4 A Inductance Region = 1000 D. Proper inductor value = 1000 μH Choose the inductor from Table 2.
5. Output Capacitor Selection (C_{out}) A. Since the LM2574 is a forward-mode switching regulator with voltage mode control, its open loop 2-pole-1-zero frequency characteristic has the dominant pole-pair determined by the output capacitor and inductor values. For stable operation, the capacitor must satisfy the following requirement: $C_{out} \geq 13,300 \frac{V_{in(\text{max})}}{V_{out} \times L[\mu\text{H}]} [\mu\text{F}]$ B. Capacitor values between 10 μF and 2000 μF will satisfy the loop requirements for stable operation. To achieve an acceptable output ripple voltage and transient response, the output capacitor may need to be several times larger than the above formula yields. C. Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating of at least 8.0 V is appropriate, and a 10 V or 16V rating is recommended.	5. Output Capacitor Selection (C_{out}) A. $C_{out} \geq 13,300 \times \frac{40}{24 \times 1000} = 22.2 \mu\text{F}$ To achieve an acceptable ripple voltage, select C_{out} = 100 μF electrolytic capacitor.

LM2574

LM2574 Series Buck Regulator Design Procedures (continued)

Indicator Value Selection Guide (For Continuous Mode Operation)

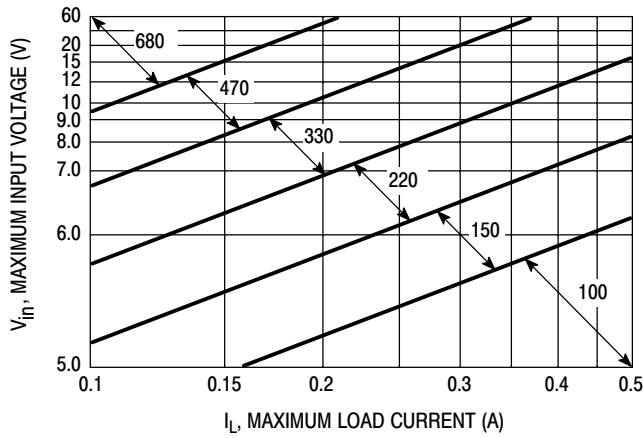


Figure 19. LM2574-3.3

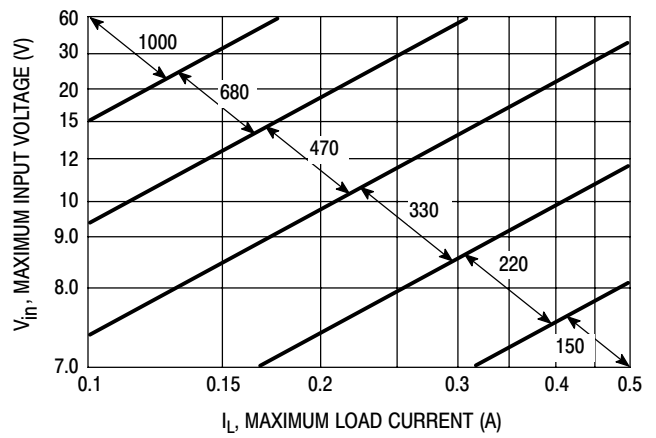


Figure 20. LM2574-5

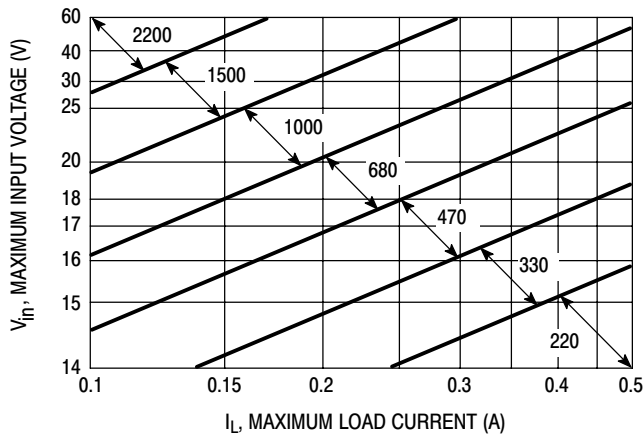


Figure 21. LM2574-12

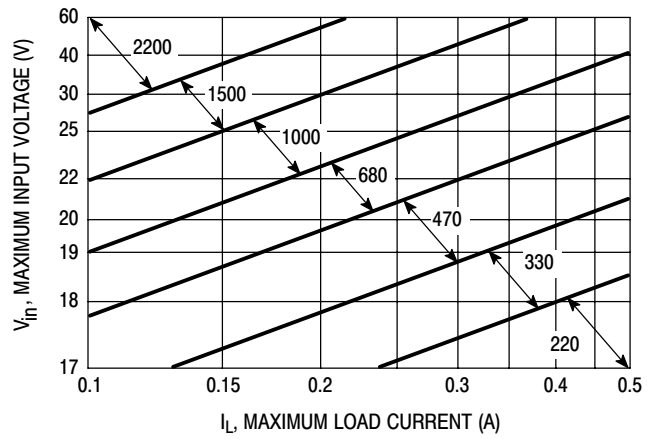


Figure 22. LM2574-15

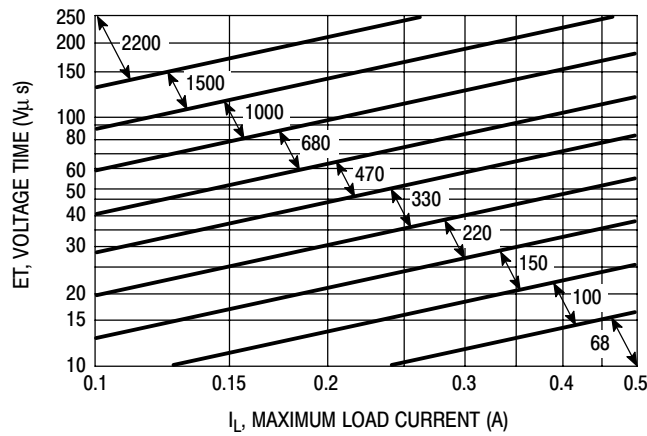


Figure 23. LM2574-ADJ

LM2574

Table 1. Diode Selection Guide gives an overview about through-hole diodes for an effective design. Device listed in bold are available from ON Semiconductor

V_R	1.0 Amp Diodes	
	Schottky	Fast Recovery
20 V	1N5817 MBR120P	MUR110 (rated to 100 V)
30 V	1N5818 MBR130P	
40 V	1N5819 MBR140P	
50 V	MBR150	
60 V	MBR160	

Table 2. Inductor Selection Guide

Inductor Value	Pulse Engineering	Tech 39	Renco	NPI
68 μ H	*	55 258 SN	RL-1284-68	NP5915
100 μ H	*	55 308 SN	RL-1284-100	NP5916
150 μ H	52625	55 356 SN	RL-1284-150	NP5917
220 μ H	52626	55 406 SN	RL-1284-220	NP5918/5919
330 μ H	52627	55 454 SN	RL-1284-330	NP5920/5921
470 μ H	52628	*	RL-1284-470	NP5922
680 μ H	52629	55 504 SN	RL-1284-680	NP5923
1000 μ H	52631	55 554 SN	RL-1284-1000	*
1500 μ H	*	*	RL-1284-1500	*
2200 μ H	*	*	RL-1284-2200	*

* : Contact Manufacturer

Table 3. Example of Several Inductor Manufacturers Phone/Fax Numbers

Pulse Engineering Inc.	Phone Fax	+ 1-619-674-8100 + 1-619-674-8262
Pulse Engineering Inc. Europe	Phone Fax	+ 353-9324-107 + 353-9324-459
Renco Electronics Inc.	Phone Fax	+ 1-516-645-5828 + 1-516-586-5562
Tech 39	Phone Fax	+ 33-1-4115-1681 + 33-1-4709-5051
NPI/APC	Phone Fax	+ 44-634-290-588

EXTERNAL COMPONENTS

Input Capacitor (C_{in})***The Input Capacitor Should Have a Low ESR***

For stable operation of the switch mode converter a low ESR (Equivalent Series Resistance) aluminium or solid tantalum bypass capacitor is needed between the input pin and the ground pin, to prevent large voltage transients from appearing at the input. It must be located near the regulator and use short leads. With most electrolytic capacitors, the capacitance value decreases and the ESR increases with lower temperatures. For reliable operation in temperatures below -25°C larger values of the input capacitor may be needed. Also paralleling a ceramic or solid tantalum capacitor will increase the regulator stability at cold temperatures.

RMS Current Rating of C_{in}

The important parameter of the input capacitor is the RMS current rating. Capacitors that are physically large and have large surface area will typically have higher RMS current ratings. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower voltage capacitor, and thus be able to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating. The consequences of operating an electrolytic capacitor beyond the RMS current rating is a shortened operating life. In order to assure maximum capacitor operating lifetime, the capacitor's RMS ripple current rating should be:

$$I_{rms} > 1.2 \times d \times I_{Load}$$

where d is the duty cycle, for a continuous mode buck regulator

$$d = \frac{t_{on}}{T} = \frac{V_{out}}{V_{in}}$$

and $d = \frac{t_{on}}{T} = \frac{|V_{out}|}{|V_{out}| + V_{in}}$ for a buck-boost regulator.

Output Capacitor (C_{out})

For low output ripple voltage and good stability, low ESR output capacitors are recommended. An output capacitor has two main functions: it filters the output and provides regulator loop stability. The ESR of the output capacitor and the peak-to-peak value of the inductor ripple current are the main factors contributing to the output ripple voltage value. Standard aluminium electrolytics could be adequate for some applications but for quality design, low ESR types are recommended.

An aluminium electrolytic capacitor's ESR value is related to many factors, such as the capacitance value, the voltage rating, the physical size and the type of construction. In most cases, the higher voltage electrolytic capacitors have lower ESR value. Often capacitors with much higher

voltage ratings may be needed to provide low ESR values, that are required for low output ripple voltage.

The Output Capacitor Requires an ESR Value that has an Upper and Lower Limit

As mentioned above, a low ESR value is needed for low output ripple voltage, typically 1% to 2% of the output voltage. But if the selected capacitor's ESR is extremely low (below 0.03Ω), there is a possibility of an unstable feedback loop, resulting in oscillation at the output. This situation can occur when a tantalum capacitor, that can have a very low ESR, is used as the only output capacitor.

At Low Temperatures, Put in Parallel Aluminium Electrolytic Capacitors with Tantalum Capacitors

Electrolytic capacitors are not recommended for temperatures below -25°C . The ESR rises dramatically at cold temperatures and typically rises 3 times at -25°C and as much as 10 times at -40°C . Solid tantalum capacitors have much better ESR spec at cold temperatures and are recommended for temperatures below -25°C . They can be also used in parallel with aluminium electrolytics. The value of the tantalum capacitor should be about 10% or 20% of the total capacitance. The output capacitor should have at least 50% higher RMS ripple current rating at 52 kHz than the peak-to-peak inductor ripple current.

Catch Diode***Locate the Catch Diode Close to the LM2574***

The LM2574 is a step-down buck converter, it requires a fast diode to provide a return path for the inductor current when the switch turns off. This diode must be located close to the LM2574 using short leads and short printed circuit traces to avoid EMI problems.

Use a Schottky or a Soft Switching Ultra-Fast Recovery Diode

Since the rectifier diodes are very significant source of losses within switching power supplies, choosing the rectifier that best fits into the converter design is an important process. Schottky diodes provide the best performance because of their fast switching speed and low forward voltage drop.

They provide the best efficiency especially in low output voltage applications (5.0 V and lower). Another choice could be Fast-Recovery, or Ultra-Fast Recovery diodes. It has to be noted, that some types of these diodes with an abrupt turnoff characteristic may cause instability or EMI troubles.

A fast-recovery diode with soft recovery characteristics can better fulfill some quality, low noise design requirements. Table 1 provides a list of suitable diodes for the LM2574 regulator. Standard 50/60 Hz rectifier diodes, such as the 1N4001 series or 1N5400 series are NOT suitable.

Inductor

The magnetic components are the cornerstone of all switching power supply designs. The style of the core and the winding technique used in the magnetic component's design have a great influence on the reliability of the overall power supply.

Using an improper or poorly designed inductor can cause high voltage spikes generated by the rate of transitions in current within the switching power supply, and the possibility of core saturation can arise during an abnormal operational mode. Voltage spikes can cause the semiconductors to enter avalanche breakdown and the part can instantly fail if enough energy is applied. It can also cause significant RFI (Radio Frequency Interference) and EMI (Electro-Magnetic Interference) problems.

Continuous and Discontinuous Mode of Operation

The LM2574 step-down converter can operate in both the continuous and the discontinuous modes of operation. The regulator works in the continuous mode when loads are relatively heavy, the current flows through the inductor continuously and never falls to zero. Under light load conditions, the circuit will be forced to the discontinuous mode when inductor current falls to zero for certain period of time (see Figure 24 and Figure 25). Each mode has distinctively different operating characteristics, which can affect the regulator performance and requirements. In many cases the preferred mode of operation is the continuous mode. It offers greater output power, lower peak currents in the switch, inductor and diode, and can have a lower output ripple voltage. On the other hand it does require larger inductor values to keep the inductor current flowing continuously, especially at low output load currents and/or high input voltages.

To simplify the inductor selection process, an inductor selection guide for the LM2574 regulator was added to this data sheet (Figures 19 through 23). This guide assumes that the regulator is operating in the continuous mode, and selects an inductor that will allow a peak-to-peak inductor ripple current to be a certain percentage of the maximum design load current. This percentage is allowed to change as different design load currents are selected. For light loads (less than approximately 0.2 A) it may be desirable to operate the regulator in the discontinuous mode, because the inductor value and size can be kept relatively low. Consequently, the percentage of inductor peak-to-peak

current increases. This discontinuous mode of operation is perfectly acceptable for this type of switching converter. Any buck regulator will be forced to enter discontinuous mode if the load current is light enough.

Selecting the Right Inductor Style

Some important considerations when selecting a core type are core material, cost, the output power of the power supply, the physical volume the inductor must fit within, and the amount of EMI (Electro-Magnetic Interference) shielding that the core must provide. There are many different styles of inductors available, such as pot core, E-core, toroid and bobbin core, as well as different core materials such as ferrites and powdered iron from different manufacturers.

For high quality design regulators the toroid core seems to be the best choice. Since the magnetic flux is contained within the core, it generates less EMI, reducing noise problems in sensitive circuits. The least expensive is the bobbin core type, which consists of wire wound on a ferrite rod core. This type of inductor generates more EMI due to the fact that its core is open, and the magnetic flux is not contained within the core.

When multiple switching regulators are located on the same printed circuit board, open core magnetics can cause interference between two or more of the regulator circuits, especially at high currents due to mutual coupling. A toroid, pot core or E-core (closed magnetic structure) should be used in such applications.

Do Not Operate an Inductor Beyond its Maximum Rated Current

Exceeding an inductor's maximum current rating may cause the inductor to overheat because of the copper wire losses, or the core may saturate. Core saturation occurs when the flux density is too high and consequently the cross sectional area of the core can no longer support additional lines of magnetic flux.

This causes the permeability of the core to drop, the inductance value decreases rapidly and the inductor begins to look mainly resistive. It has only the dc resistance of the winding. This can cause the switch current to rise very rapidly and force the LM2574 internal switch into cycle-by-cycle current limit, thus reducing the dc output load current. This can also result in overheating of the inductor and/or the LM2574. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.

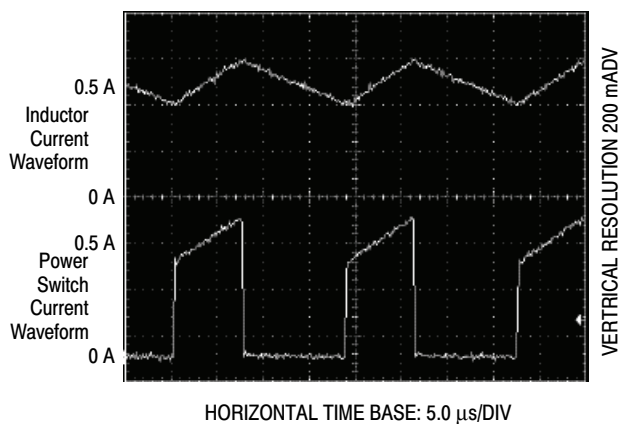


Figure 24. Continuous Mode Switching Current Waveforms

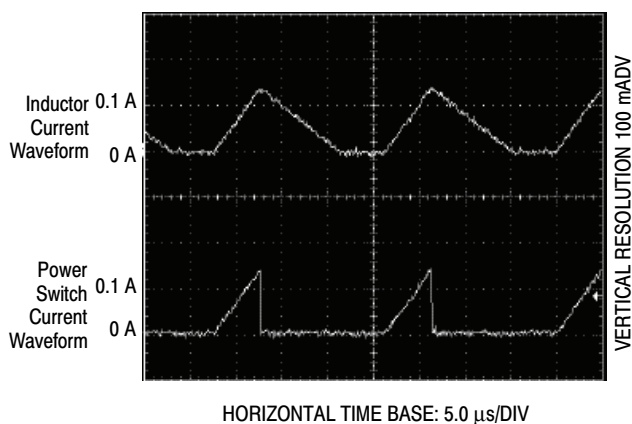


Figure 25. Continuous Mode Switching Current Waveforms

GENERAL RECOMMENDATIONS

Output Voltage Ripple and Transients

Source of the Output Ripple

Since the LM2574 is a switch mode power supply regulator, its output voltage, if left unfiltered, will contain a sawtooth ripple voltage at the switching frequency. The output ripple voltage value ranges from 0.5% to 3% of the output voltage. It is caused mainly by the inductor sawtooth ripple current multiplied by the ESR of the output capacitor.

Short Voltage Spikes and How to Reduce Them

The regulator output voltage may also contain short voltage spikes at the peaks of the sawtooth waveform (see Figure 26). These voltage spikes are present because of the fast switching action of the output switch, and the parasitic inductance of the output filter capacitor. There are some other important factors such as wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all these contribute to the amplitude of these spikes. To minimize these voltage spikes, low inductance capacitors should be used, and their lead lengths must be kept short. The importance of quality printed circuit board layout design should also be highlighted.

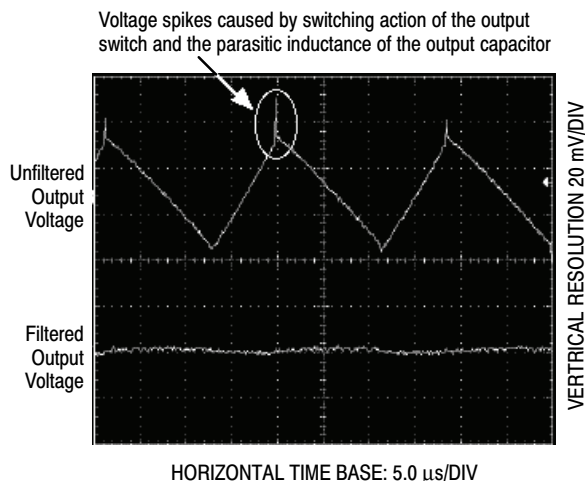


Figure 26. Output Ripple Voltage Waveforms

Minimizing the Output Ripple

In order to minimize the output ripple voltage it is possible to enlarge the inductance value of the inductor L1 and/or to use a larger value output capacitor. There is also another way to smooth the output by means of an additional LC filter (20 μ H, 100 μ F), that can be added to the output (see Figure 35) to further reduce the amount of output ripple and transients. With such a filter it is possible to reduce the output ripple voltage transients 10 times or more. Figure 26 shows the difference between filtered and unfiltered output waveforms of the regulator shown in Figure 34.

The upper waveform is from the normal unfiltered output of the converter, while the lower waveform shows the output ripple voltage filtered by an additional LC filter.

Heatsinking and Thermal Considerations

The LM2574 is available in both 8-pin DIP and SO-16L packages. When used in the typical application the copper lead frame conducts the majority of the heat from the die, through the leads, to the printed circuit copper. The copper and the board are the heatsink for this package and the other heat producing components, such as the catch diode and inductor.

For the best thermal performance, wide copper traces should be used and all ground and unused pins should be soldered to generous amounts of printed circuit board copper, such as a ground plane. Large areas of copper provide the best transfer of heat to the surrounding air. One exception to this is the output (switch) pin, which should not have large areas of copper in order to minimize coupling to sensitive circuitry.

Additional improvement in heat dissipation can be achieved even by using of double sided or multilayer boards which can provide even better heat path to the ambient. Using a socket for the 8-pin DIP package is not recommended because socket represents an additional thermal resistance, and as a result the junction temperature will be higher.

Since the current rating of the LM2574 is only 0.5 A, the total package power dissipation for this switcher is quite low, ranging from approximately 0.1 W up to 0.75 W under varying conditions. In a carefully engineered printed circuit board, the through-hole DIP package can easily dissipate up to 0.75 W, even at ambient temperatures of 60°C, and still keep the maximum junction temperature below 125°C.

Thermal Analysis and Design

The following procedure must be performed to determine the operating junction temperature. First determine:

1. $P_{D(max)}$ – maximum regulator power dissipation in the application.
2. $T_{A(max)}$ – maximum ambient temperature in the application.
3. $T_{J(max)}$ – maximum allowed junction temperature (125°C for the LM2574). For a conservative design, the maximum junction temperature should not exceed 110°C to assure safe operation. For every additional +10°C temperature rise that the junction must withstand, the estimated operating lifetime of the component is halved.
4. $R_{\theta JC}$ – package thermal resistance junction–case.
5. $R_{\theta JA}$ – package thermal resistance junction–ambient.

(Refer to Absolute Maximum Ratings on page 111 of this data sheet or $R_{\theta JC}$ and $R_{\theta JA}$ values).

The following formula is to calculate the approximate total power dissipated by the LM2574:

$$P_D = (V_{in} \times I_Q) + d \times I_{Load} \times V_{sat}$$

where d is the duty cycle and for buck converter

$$d = \frac{t_{on}}{T} = \frac{V_O}{V_{in}}$$

I_Q (quiescent current) and V_{sat} can be found in the LM2574 data sheet,

V_{in} is minimum input voltage applied,

V_O is the regulator output voltage,

I_{Load} is the load current.

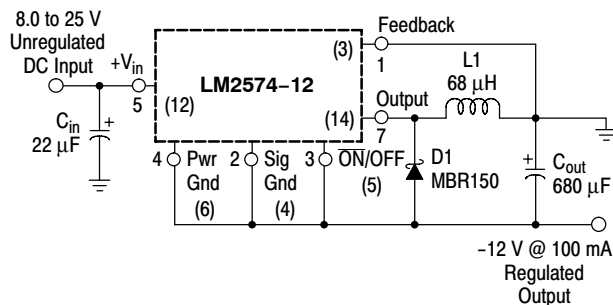


Figure 27. Inverting Buck-Boost Develops -12 V

The dynamic switching losses during turn-on and turn-off can be neglected if a proper type catch diode is used.

The junction temperature can be determined by the following expression:

$$T_J = (R_{\theta JA})(P_D) + T_A$$

where $(R_{\theta JA})(P_D)$ represents the junction temperature rise caused by the dissipated power and T_A is the maximum ambient temperature.

Some Aspects That can Influence Thermal Design

It should be noted that the package thermal resistance and the junction temperature rise numbers are all approximate, and there are many factors that will affect these numbers, such as PC board size, shape, thickness, physical position, location, board temperature, as well as whether the surrounding air is moving or still. At higher power levels the thermal resistance decreases due to the increased air current activity.

Other factors are trace width, total printed circuit copper area, copper thickness, single- or double-sided, multilayer board, the amount of solder on the board or even color of the traces.

The size, quantity and spacing of other components on the board can also influence its effectiveness to dissipate the heat. Some of them, like the catch diode or the inductor will generate some additional heat.

ADDITIONAL APPLICATIONS

Inverting Regulator

An inverting buck-boost regulator using the LM2574-12 is shown in Figure 27. This circuit converts a positive input voltage to a negative output voltage with a common ground by bootstrapping the regulators ground to the negative output voltage. By grounding the feedback pin, the regulator senses the inverted output voltage and regulates it.

In this example the LM2574-12 is used to generate a -12 V output. The maximum input voltage in this case cannot exceed 28 V because the maximum voltage appearing across the regulator is the absolute sum of the input and output voltages and this must be limited to a maximum of 40 V.

This circuit configuration is able to deliver approximately 0.1 A to the output when the input voltage is 8.0 V or higher. At lighter loads the minimum input voltage required drops to approximately 4.7 V, because the buck-boost regulator topology can produce an output voltage that, in its absolute value, is either greater or less than the input voltage.

Since the switch currents in this buck-boost configuration are higher than in the standard buck converter topology, the available output current is lower.

This type of buck-boost inverting regulator can also require a larger amount of startup input current, even for light loads. This may overload an input power source with a current limit less than 0.6 A.

Because of the relatively high startup currents required by this inverting regulator topology, the use of a delayed startup or an undervoltage lockout circuit is recommended.

While using a delayed startup arrangement, the input capacitor can charge up to a higher voltage before the switch-mode regulator begins to operate.

The high input current needed for startup is now partially supplied by the input capacitor C_{in} .

Design Recommendations:

The inverting regulator operates in a different manner than the buck converter and so a different design procedure has to be used to select the inductor L_1 or the output capacitor C_{out} .

The output capacitor values must be larger than what is normally required for buck converter designs. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of μF).

The recommended range of inductor values for the inverting converter design is between $68\ \mu\text{H}$ and $220\ \mu\text{H}$. To select an inductor with an appropriate current rating, the inductor peak current has to be calculated.

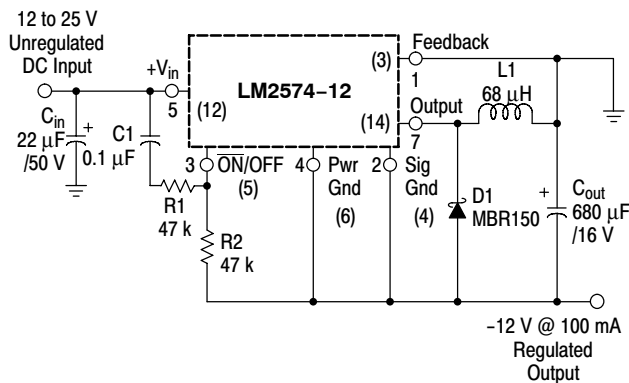


Figure 28. Inverting Buck-Boost Regulator with Delayed Startup

The following formula is used to obtain the peak inductor current:

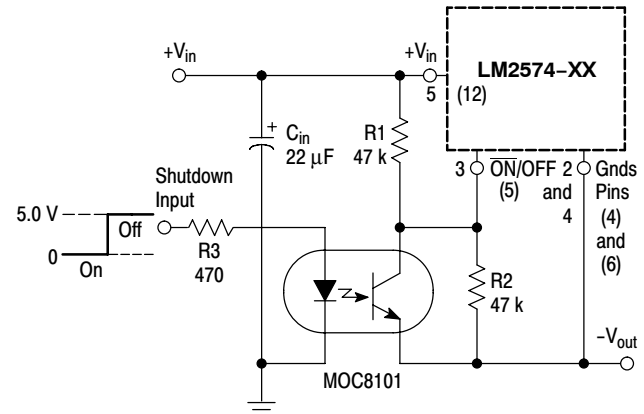
$$I_{\text{peak}} \approx \frac{I_{\text{Load}}(V_{\text{in}} + |V_{\text{O}}|)}{V_{\text{in}}} + \frac{V_{\text{in}} \times t_{\text{on}}}{2L_1}$$

where $t_{\text{on}} = \frac{|V_{\text{O}}|}{V_{\text{in}} + |V_{\text{O}}|} \times \frac{1.0}{f_{\text{osc}}}$, and $f_{\text{osc}} = 52\ \text{kHz}$.

Under normal continuous inductor current operating conditions, the worst case occurs when V_{in} is minimal.

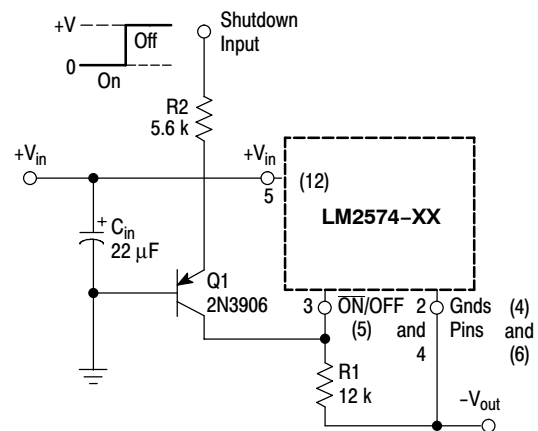
It has been already mentioned above, that in some situations, the delayed startup or the undervoltage lockout features could be very useful. A delayed startup circuit applied to a buck-boost converter is shown in Figure 28. Figure 34 in the “Undervoltage Lockout” section describes an undervoltage lockout feature for the same converter topology.

With the inverting configuration, the use of the $\overline{\text{ON/OFF}}$ pin requires some level shifting techniques. This is caused by the fact, that the ground pin of the converter IC is no longer at ground. Now, the $\overline{\text{ON/OFF}}$ pin threshold voltage (1.3 V approximately) has to be related to the negative output voltage level. There are many different possible shutdown methods, two of them are shown in Figures 29 and 30.



NOTE: This picture does not show the complete circuit.

Figure 29. Inverting Buck-Boost Regulator Shutdown Circuit Using an Optocoupler



NOTE: This picture does not show the complete circuit.

Figure 30. Inverting Buck-Boost Regulator Shutdown Circuit Using a PNP Transistor

Negative Boost Regulator

This example is a variation of the buck-boost topology and it is called negative boost regulator. This regulator experiences relatively high switch current, especially at low input voltages. The internal switch current limiting results in lower output load current capability.

LM2574

The circuit in Figure 31 shows the negative boost configuration. The input voltage in this application ranges from -5.0 to -12 V and provides a regulated -12 V output. If the input voltage is greater than -12 V, the output will rise above -12 V accordingly, but will not damage the regulator.

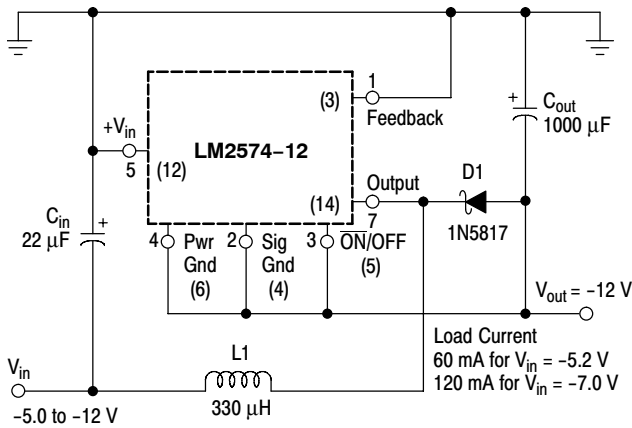


Figure 31. Negative Boost Regulator

Design Recommendations:

The same design rules as for the previous inverting buck-boost converter can be applied. The output capacitor C_{out} must be chosen larger than what would be required for a standard buck converter. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of μ F). The recommended range of inductor values for the negative boost regulator is the same as for inverting converter design.

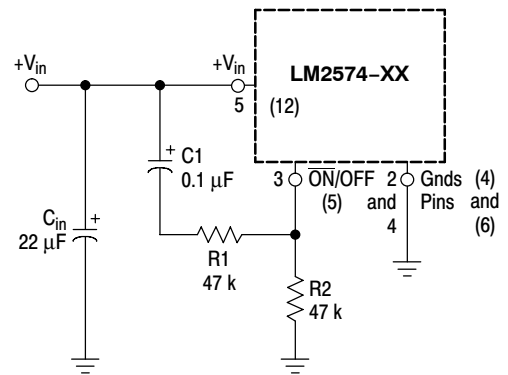
Another important point is that these negative boost converters cannot provide any current limiting load protection in the event of a short in the output so some other means, such as a fuse, may be necessary to provide the load protection.

Delayed Startup

There are some applications, like the inverting regulator already mentioned above, which require a higher amount of startup current. In such cases, if the input power source is limited, this delayed startup feature becomes very useful.

To provide a time delay between the time when the input voltage is applied and the time when the output voltage comes up, the circuit in Figure 32 can be used. As the input voltage is applied, the capacitor $C1$ charges up, and the voltage across the resistor $R2$ falls down. When the voltage on the $\overline{ON}/OFF$ pin falls below the threshold value 1.3 V, the regulator starts up. Resistor $R1$ is included to limit the maximum voltage applied to the $\overline{ON}/OFF$ pin. It reduces the power supply noise sensitivity, and also limits the capacitor $C1$ discharge current, but its use is not mandatory.

When a high 50 Hz or 60 Hz (100 Hz or 120 Hz respectively) ripple voltage exists, a long delay time can cause some problems by coupling the ripple into the $\overline{ON}/OFF$ pin, the regulator could be switched periodically on and off with the line (or double) frequency.



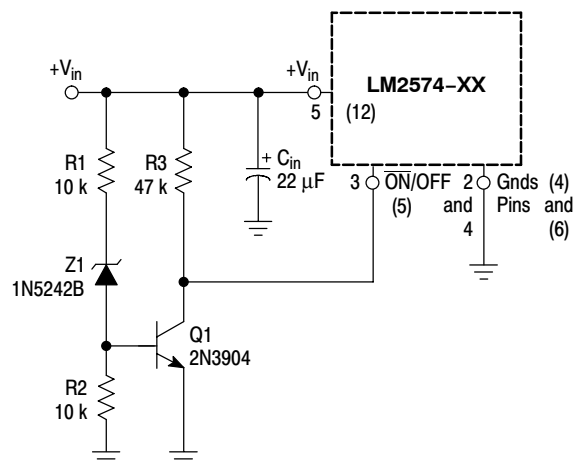
NOTE: This picture does not show the complete circuit.

Figure 32. Delayed Startup Circuitry

Undervoltage Lockout

Some applications require the regulator to remain off until the input voltage reaches a certain threshold level. Figure 33 shows an undervoltage lockout circuit applied to a buck regulator. A version of this circuit for buck-boost converter is shown in Figure 34. Resistor $R3$ pulls the $\overline{ON}/OFF$ pin high and keeps the regulator off until the input voltage reaches a predetermined threshold level, which is determined by the following expression:

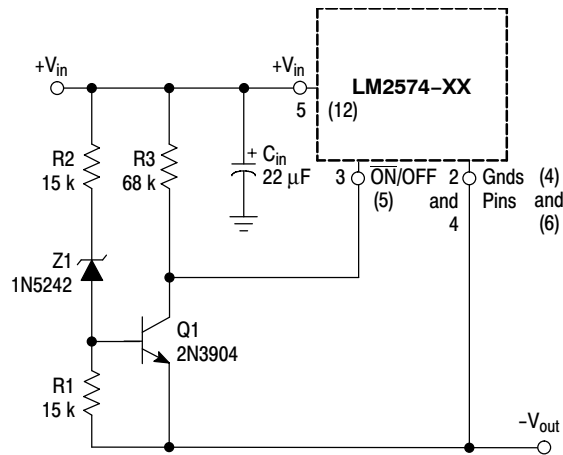
$$V_{th} \approx V_{Z1} + \left(1.0 + \frac{R2}{R1}\right)V_{BE}(Q1)$$



NOTE: This picture does not show the complete circuit.

Figure 33. Undervoltage Lockout Circuit for Buck Converter

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NOTE: This picture does not show the complete circuit (see Figure 27).

Figure 34. Undervoltage Lockout Circuit for Buck-Boost Converter

Adjustable Output, Low-Ripple Power Supply

A 0.5 A output current capability power supply that features an adjustable output voltage is shown in Figure 35.

This regulator delivers 0.5 A into 1.2 to 35 V output. The input voltage ranges from roughly 3.0 to 40 V. In order to achieve a 10 or more times reduction of output ripple, an additional L-C filter is included in this circuit.

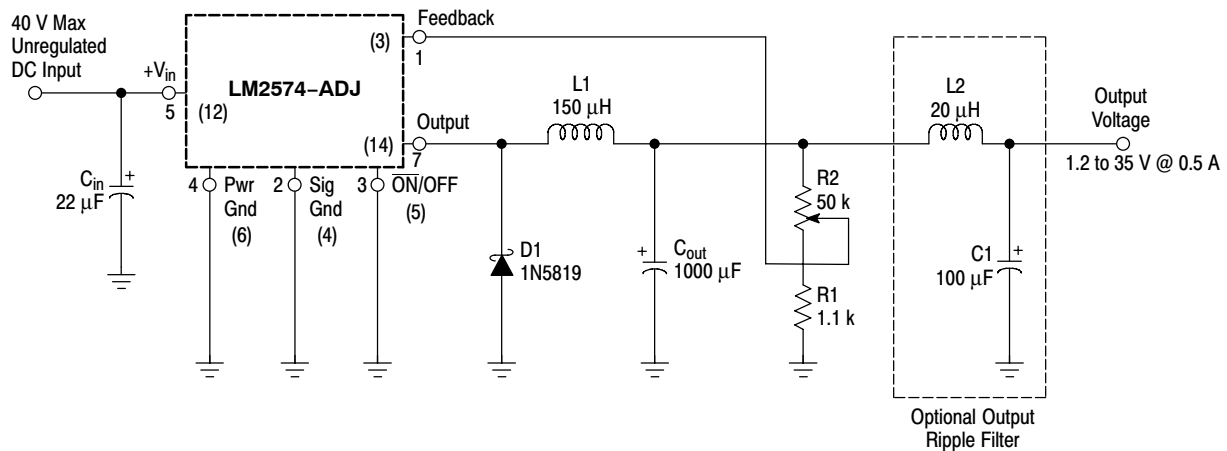


Figure 35. 1.2 to 35 V Adjustable 500 mA Power Supply with Low Output Ripple

LM2574

The LM2574-5 Step-Down Voltage Regulator with 5.0 V @ 0.5 A Output Power Capability. Typical Application With Through-Hole PC Board Layout

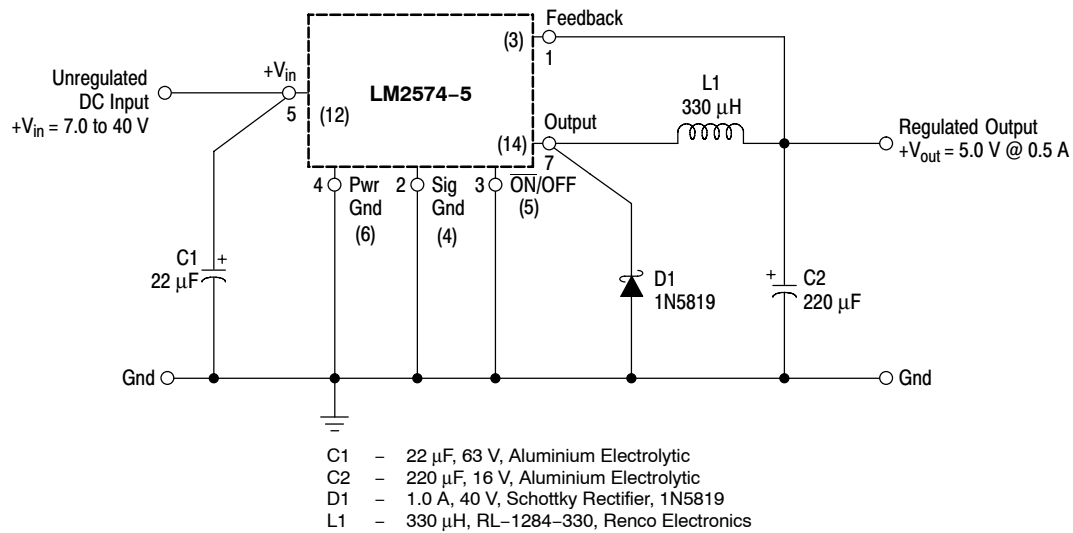


Figure 36. Schematic Diagram of the LM2574-5 Step-Down Converter

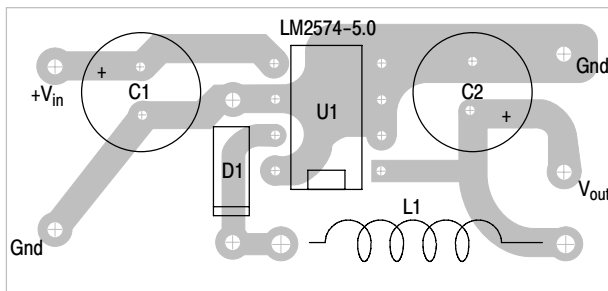


Figure 37. PC Board Layout Component Side

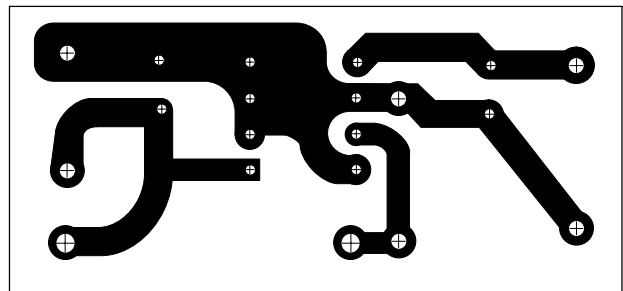


Figure 38. PC Board Layout Copper Side

LM2574

The LM2574-ADJ Step-Down Voltage Regulator with 5.0 V @ 0.5 A Output Power Capability Typical Application With Through-Hole PC Board Layout

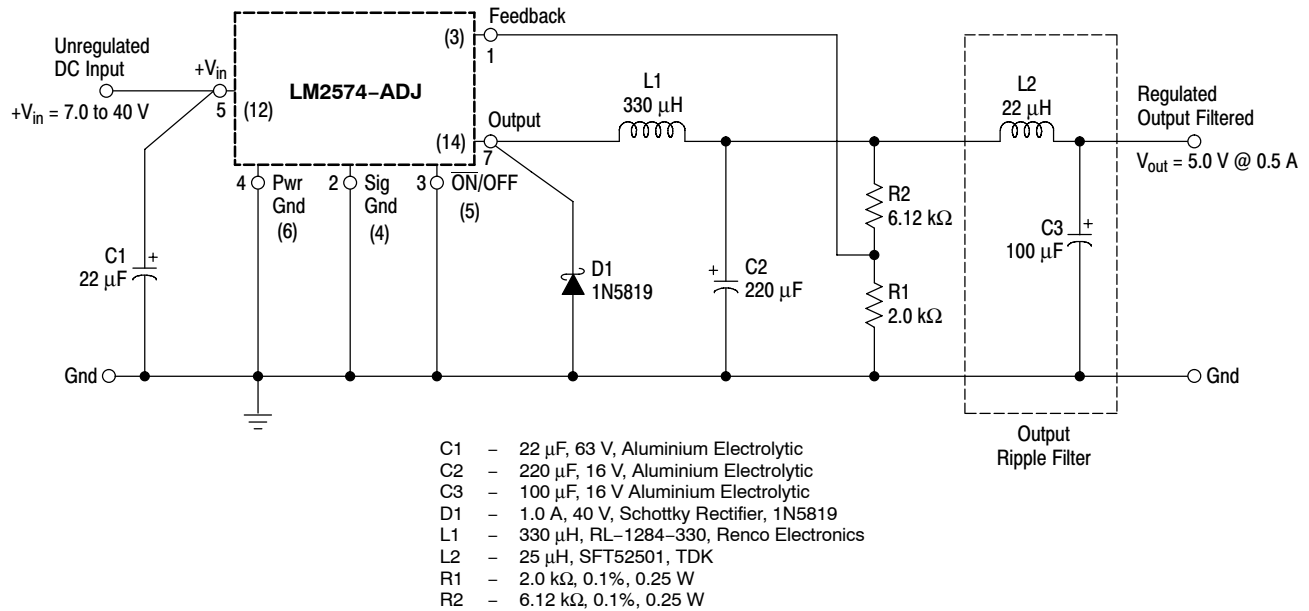
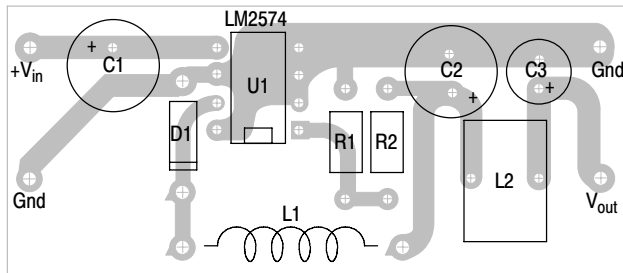
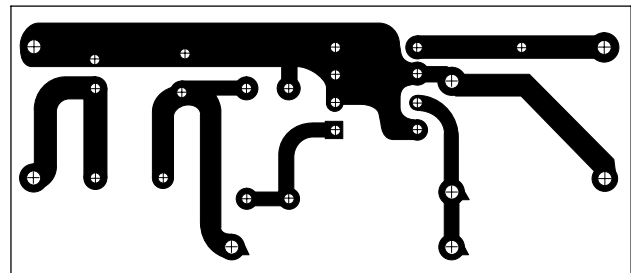


Figure 39. Schematic Diagram of the 5.0 V @ 0.5 A Step-Down Converter Using the LM2574-ADJ
(An additional LC filter is included to achieve low output ripple voltage)



NOTE: Not to scale.

Figure 40. PC Board Layout Component Side



NOTE: Not to scale.

Figure 41. PC Board Layout Copper Side

References

- Marty Brown "Practical Switching Power Supply Design", Academic Press, Inc., San Diego 1990
- Ray Ridley "High Frequency Magnetics Design", Ridley Engineering, Inc. 1995

LM2574

ORDERING INFORMATION

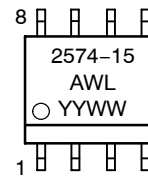
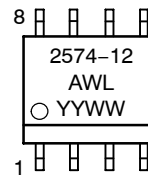
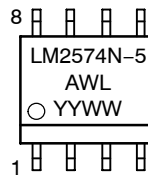
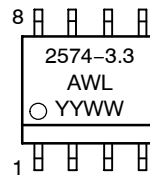
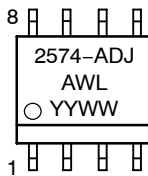
Device	Nominal Output Voltage	Operating Junction Temperature Range	Package	Shipping
LM2574DW-ADJ	1.23 V to 37 V	$T_J = -40^{\circ} \text{ to } +125^{\circ}\text{C}$	SO-16W	47 Units/Rail
LM2574DW-ADJR2			SO-16W	1000 Units/Tape & Reel
LM2574N-ADJ			PDIP-8	50 Units/Rail
LM2574N-3.3	3.3 V		PDIP-8	50 Units/Rail
LM2574N-5	5.0 V		PDIP-8	50 Units/Rail
LM2574N-12	12 V		PDIP-8	50 Units/Rail
LM2574N-15	15 V		PDIP-8	50 Units/Rail

MARKING DIAGRAMS

SO-16W
DW SUFFIX
CASE 751G



PDIP-8
N SUFFIX
CASE 626



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

LM2575

1.0 A, Adjustable Output Voltage, Step-Down Switching Regulator

The LM2575 series of regulators are monolithic integrated circuits ideally suited for easy and convenient design of a step-down switching regulator (buck converter). All circuits of this series are capable of driving a 1.0 A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3 V, 5.0 V, 12 V, 15 V, and an adjustable output version.

These regulators were designed to minimize the number of external components to simplify the power supply design. Standard series of inductors optimized for use with the LM2575 are offered by several different inductor manufacturers.

Since the LM2575 converter is a switch-mode power supply, its efficiency is significantly higher in comparison with popular three-terminal linear regulators, especially with higher input voltages. In many cases, the power dissipated by the LM2575 regulator is so low, that no heatsink is required or its size could be reduced dramatically.

The LM2575 features include a guaranteed $\pm 4\%$ tolerance on output voltage within specified input voltages and output load conditions, and $\pm 10\%$ on the oscillator frequency ($\pm 2\%$ over 0°C to 125°C). External shutdown is included, featuring 80 μA typical standby current. The output switch includes cycle-by-cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

Features

- 3.3 V, 5.0 V, 12 V, 15 V, and Adjustable Output Versions
- Adjustable Version Output Voltage Range of 1.23 V to 37 V $\pm 4\%$ Maximum Over Line and Load Conditions
- Guaranteed 1.0 A Output Current
- Wide Input Voltage Range: 4.75 V to 40 V
- Requires Only 4 External Components
- 52 kHz Fixed Frequency Internal Oscillator
- TTL Shutdown Capability, Low Power Standby Mode
- High Efficiency
- Uses Readily Available Standard Inductors
- Thermal Shutdown and Current Limit Protection
- Moisture Sensitivity Level (MSL) Equals 1
- Pb-Free Packages are Available

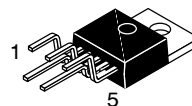
Applications

- Simple and High-Efficiency Step-Down (Buck) Regulators
- Efficient Pre-Regulator for Linear Regulators
- On-Card Switching Regulators
- Positive to Negative Converters (Buck-Boost)
- Negative Step-Up Converters
- Power Supply for Battery Chargers



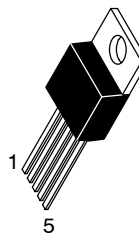
ON Semiconductor®

<http://onsemi.com>



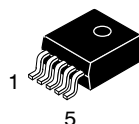
**TO-220
TV SUFFIX
CASE 314B**

Heatsink surface connected to Pin 3



**TO-220
T SUFFIX
CASE 314D**

Pin 1. V_{in}
2. Output
3. Ground
4. Feedback
5. ON/OFF



**D²PAK
D2T SUFFIX
CASE 936A**

Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 157 of this data sheet.

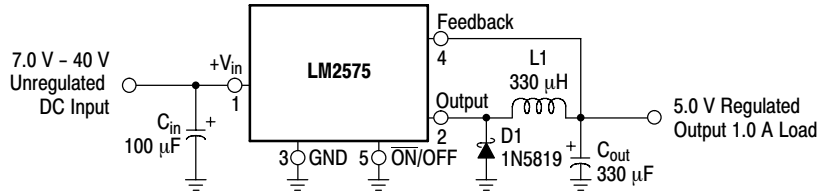
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DEVICE MARKING INFORMATION

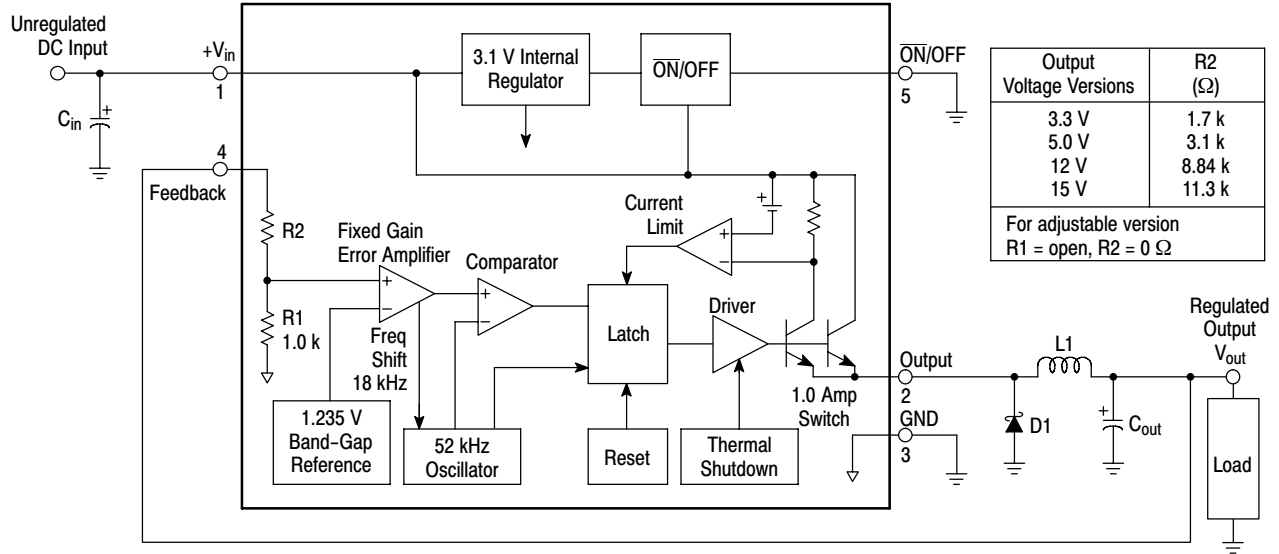
See general marking information in the device marking section on page 157 of this data sheet.

LM2575

Typical Application (Fixed Output Voltage Versions)



Representative Block Diagram and Typical Application



This device contains 162 active transistors.

Figure 1. Block Diagram and Typical Application

ABSOLUTE MAXIMUM RATINGS (Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.)

Rating	Symbol	Value	Unit
Maximum Supply Voltage	V _{in}	45	V
ON/OFF Pin Input Voltage	–	–0.3 V ≤ V ≤ +V _{in}	V
Output Voltage to Ground (Steady-State)	–	–1.0	V
Power Dissipation			
Case 314B and 314D (TO–220, 5–Lead)	P _D	Internally Limited	W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	65	°C/W
Thermal Resistance, Junction-to-Case	R _{θJC}	5.0	°C/W
Case 936A (D ² PAK)	P _D	Internally Limited	W
Thermal Resistance, Junction-to-Ambient (Figure 34)	R _{θJA}	70	°C/W
Thermal Resistance, Junction-to-Case	R _{θJC}	5.0	°C/W
Storage Temperature Range	T _{stg}	–65 to +150	°C
Minimum ESD Rating (Human Body Model: C = 100 pF, R = 1.5 kΩ)	–	3.0	kV
Lead Temperature (Soldering, 10 s)	–	260	°C
Maximum Junction Temperature	T _J	150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

LM2575

OPERATING RATINGS (Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	-40 to +125	°C
Supply Voltage	V_{in}	40	V

SYSTEM PARAMETERS ([Note 1] Test Circuit Figure 14)

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $V_{in} = 12$ V for the 3.3 V, 5.0 V, and Adjustable version, $V_{in} = 25$ V for the 12 V version, and $V_{in} = 30$ V for the 15 V version. $I_{Load} = 200$ mA. For typical values $T_J = 25^\circ\text{C}$, for min/max values T_J is the operating junction temperature range that applies [Note 2], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit

LM2575-3.3 (Note 1 Test Circuit Figure 14)

Output Voltage ($V_{in} = 12$ V, $I_{Load} = 0.2$ A, $T_J = 25^\circ\text{C}$)	V_{out}	3.234	3.3	3.366	V
Output Voltage (4.75 V $\leq V_{in} \leq 40$ V, 0.2 A $\leq I_{Load} \leq 1.0$ A) $T_J = 25^\circ\text{C}$ $T_J = -40$ to $+125^\circ\text{C}$	V_{out}	3.168 3.135	3.3 –	3.432 3.465	V
Efficiency ($V_{in} = 12$ V, $I_{Load} = 1.0$ A)	η	–	75	–	%

LM2575-5 ([Note 1] Test Circuit Figure 14)

Output Voltage ($V_{in} = 12$ V, $I_{Load} = 0.2$ A, $T_J = 25^\circ\text{C}$)	V_{out}	4.9	5.0	5.1	V
Output Voltage (8.0 V $\leq V_{in} \leq 40$ V, 0.2 A $\leq I_{Load} \leq 1.0$ A) $T_J = 25^\circ\text{C}$ $T_J = -40$ to $+125^\circ\text{C}$	V_{out}	4.8 4.75	5.0 –	5.2 5.25	V
Efficiency ($V_{in} = 12$ V, $I_{Load} = 1.0$ A)	η	–	77	–	%

LM2575-12 (Note 1 Test Circuit Figure 14)

Output Voltage ($V_{in} = 25$ V, $I_{Load} = 0.2$ A, $T_J = 25^\circ\text{C}$)	V_{out}	11.76	12	12.24	V
Output Voltage (15 V $\leq V_{in} \leq 40$ V, 0.2 A $\leq I_{Load} \leq 1.0$ A) $T_J = 25^\circ\text{C}$ $T_J = -40$ to $+125^\circ\text{C}$	V_{out}	11.52 11.4	12 –	12.48 12.6	V
Efficiency ($V_{in} = 15$ V, $I_{Load} = 1.0$ A)	η	–	88	–	%

LM2575-15 (Note 1 Test Circuit Figure 14)

Output Voltage ($V_{in} = 30$ V, $I_{Load} = 0.2$ A, $T_J = 25^\circ\text{C}$)	V_{out}	14.7	15	15.3	V
Output Voltage (18 V $\leq V_{in} \leq 40$ V, 0.2 A $\leq I_{Load} \leq 1.0$ A) $T_J = 25^\circ\text{C}$ $T_J = -40$ to $+125^\circ\text{C}$	V_{out}	14.4 14.25	15 –	15.6 15.75	V
Efficiency ($V_{in} = 18$ V, $I_{Load} = 1.0$ A)	η	–	88	–	%

LM2575 ADJUSTABLE VERSION (Note 1 Test Circuit Figure 14)

Feedback Voltage ($V_{in} = 12$ V, $I_{Load} = 0.2$ A, $V_{out} = 5.0$ V, $T_J = 25^\circ\text{C}$)	V_{FB}	1.217	1.23	1.243	V
Feedback Voltage (8.0 V $\leq V_{in} \leq 40$ V, 0.2 A $\leq I_{Load} \leq 1.0$ A, $V_{out} = 5.0$ V) $T_J = 25^\circ\text{C}$ $T_J = -40$ to $+125^\circ\text{C}$	V_{FB}	1.193 1.18	1.23 –	1.267 1.28	V
Efficiency ($V_{in} = 12$ V, $I_{Load} = 1.0$ A, $V_{out} = 5.0$ V)	η	–	77	–	%

- External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2575 is used as shown in the Figure 14 test circuit, system performance will be as shown in system parameters section.
- Tested junction temperature range for the LM2575: $T_{low} = -40^\circ\text{C}$ $T_{high} = +125^\circ\text{C}$

DEVICE PARAMETERS

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $V_{in} = 12\text{ V}$ for the 3.3 V, 5.0 V, and Adjustable version, $V_{in} = 25\text{ V}$ for the 12 V version, and $V_{in} = 30\text{ V}$ for the 15 V version. $I_{Load} = 200\text{ mA}$. For typical values $T_J = 25^\circ\text{C}$, for min/max values T_J is the operating junction temperature range that applies [Note 2], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
ALL OUTPUT VOLTAGE VERSIONS					
Feedback Bias Current ($V_{out} = 5.0\text{ V}$ Adjustable Version Only) $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	I_b	– –	25 –	100 200	nA
Oscillator Frequency Note 3 $T_J = 25^\circ\text{C}$ $T_J = 0\text{ to }+125^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	f_{osc}	– 47 42	52 – –	– 58 63	kHz
Saturation Voltage ($I_{out} = 1.0\text{ A}$ Note 4) $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	V_{sat}	– –	1.0 –	1.2 1.3	V
Max Duty Cycle ("on") Note 5	DC	94	98	–	%
Current Limit (Peak Current Notes 4 and 3) $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	I_{CL}	1.7 1.4	2.3 –	3.0 3.2	A
Output Leakage Current Notes 6 and 7, $T_J = 25^\circ\text{C}$ Output = 0 V Output = –1.0 V	I_L	– –	0.8 6.0	2.0 20	mA
Quiescent Current Note 6 $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	I_Q	– –	5.0 –	9.0 11	mA
Standby Quiescent Current ($\overline{\text{ON/OFF}}$ Pin = 5.0 V ("off")) $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	I_{stby}	– –	80 –	200 400	μA
$\overline{\text{ON/OFF}}$ Pin Logic Input Level (Test Circuit Figure 14) $V_{out} = 0\text{ V}$ $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$ $V_{out} = \text{Nominal Output Voltage}$ $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	V_{IH} V_{IL}	2.2 2.4 – –	1.4 – 1.2 –	– – 1.0 0.8	V
$\overline{\text{ON/OFF}}$ Pin Input Current (Test Circuit Figure 14) $\overline{\text{ON/OFF}}$ Pin = 5.0 V ("off"), $T_J = 25^\circ\text{C}$ $\overline{\text{ON/OFF}}$ Pin = 0 V ("on"), $T_J = 25^\circ\text{C}$	I_{IH} I_{IL}	– –	15 0	30 5.0	μA

- The oscillator frequency reduces to approximately 18 kHz in the event of an output short or an overload which causes the regulated output voltage to drop approximately 40% from the nominal output voltage. This self protection feature lowers the average dissipation of the IC by lowering the minimum duty cycle from 5% down to approximately 2%.
- Output (Pin 2) sourcing current. No diode, inductor or capacitor connected to output pin.
- Feedback (Pin 4) removed from output and connected to 0 V.
- Feedback (Pin 4) removed from output and connected to +12 V for the Adjustable, 3.3 V, and 5.0 V versions, and +25 V for the 12 V and 15 V versions, to force the output transistor "off".
- $V_{in} = 40\text{ V}$.

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 14)

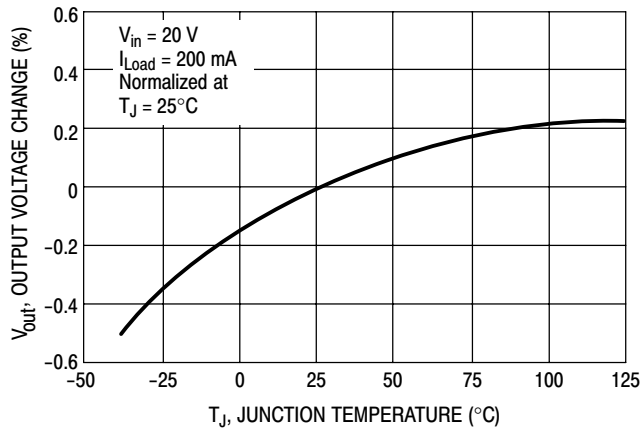


Figure 2. Normalized Output Voltage

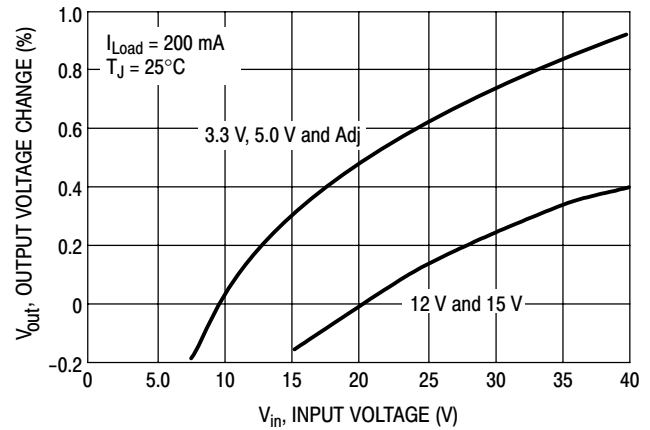


Figure 3. Line Regulation

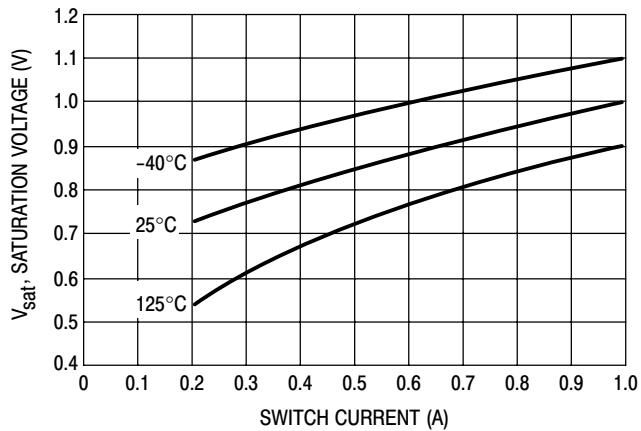


Figure 4. Switch Saturation Voltage

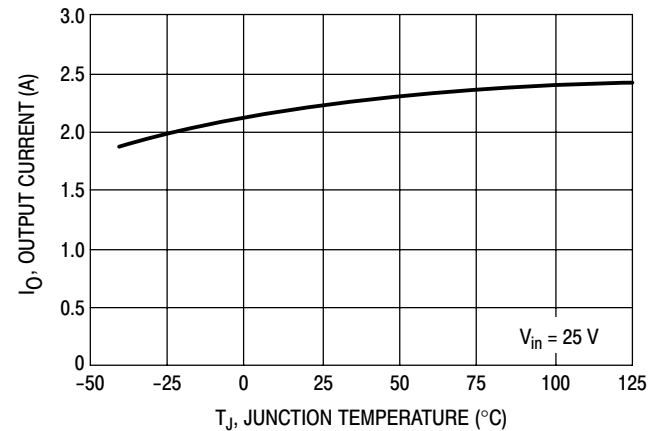


Figure 5. Current Limit

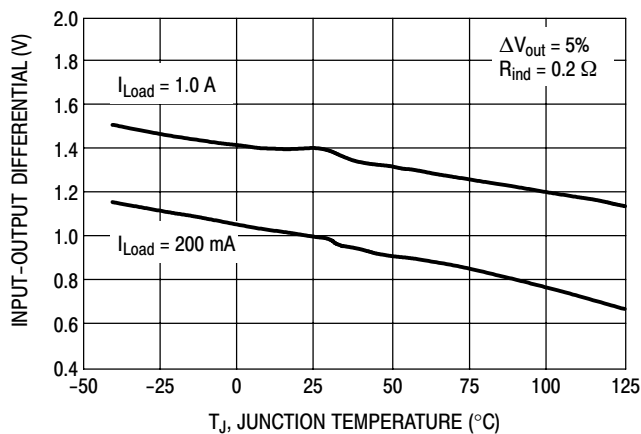


Figure 6. Dropout Voltage

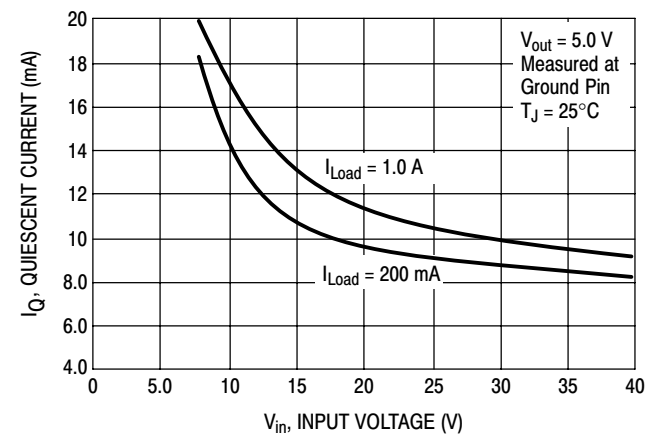


Figure 7. Quiescent Current

LM2575

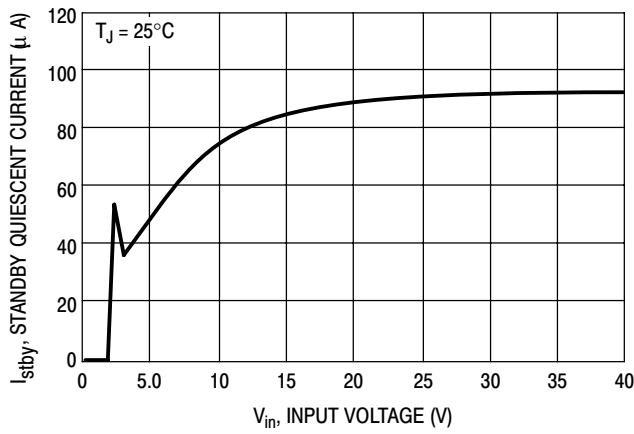


Figure 8. Standby Quiescent Current

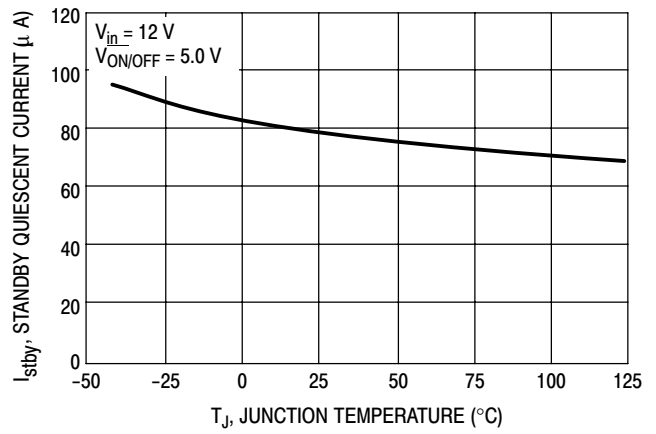


Figure 9. Standby Quiescent Current

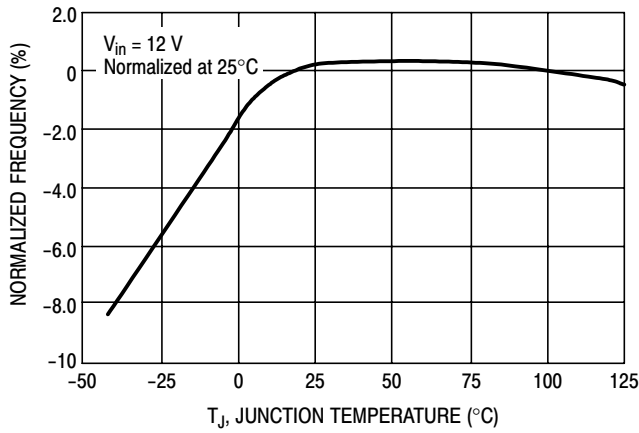


Figure 10. Oscillator Frequency

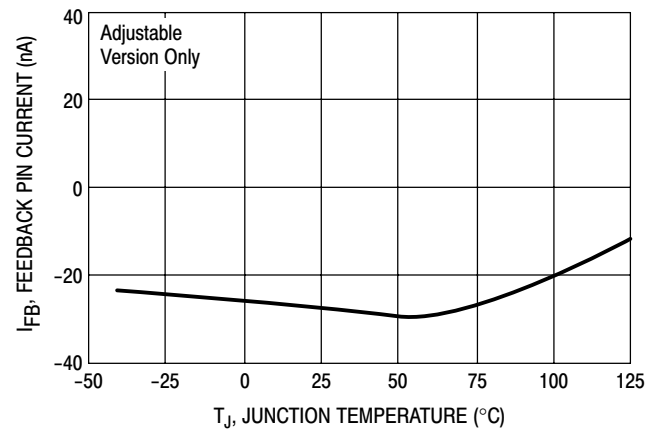


Figure 11. Feedback Pin Current

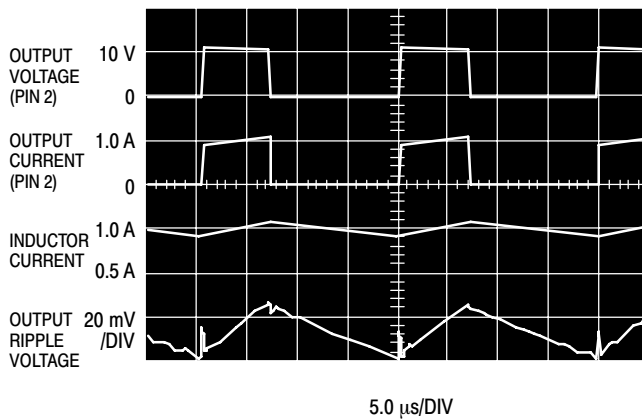


Figure 12. Switching Waveforms

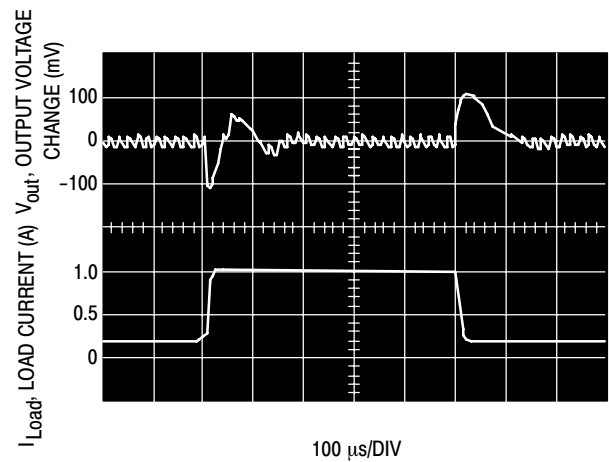
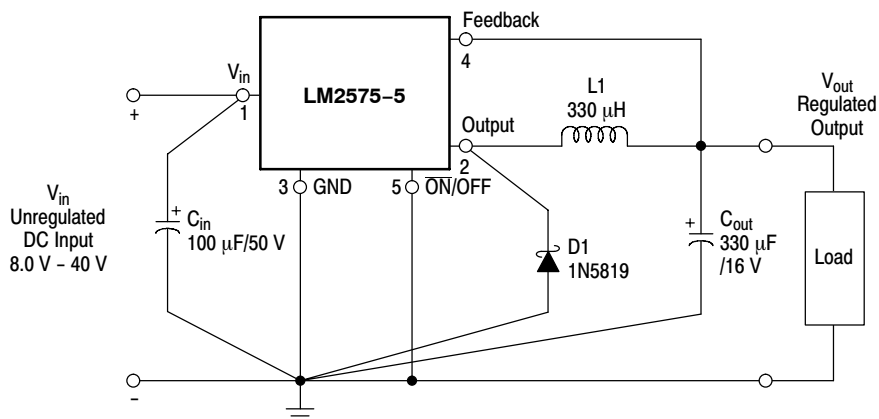


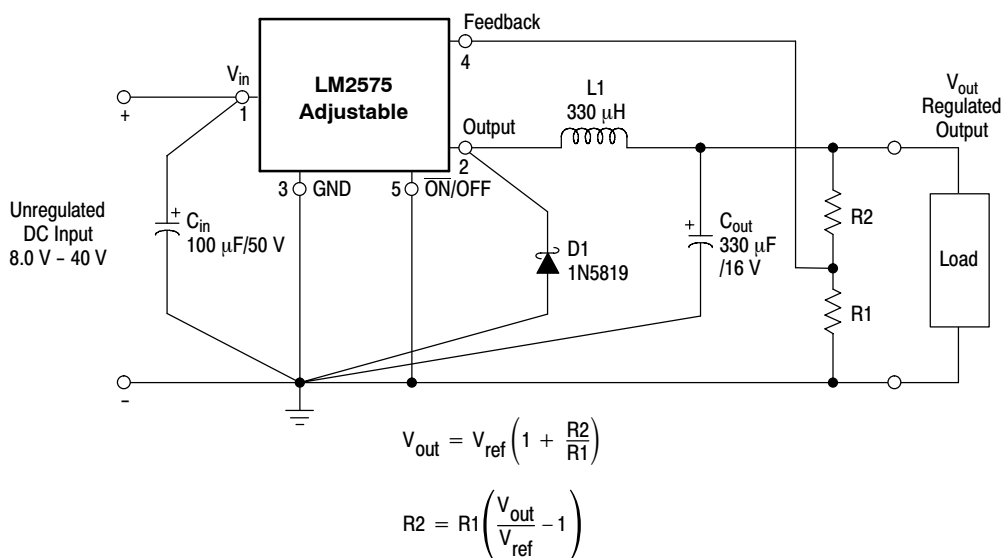
Figure 13. Load Transient Response

LM2575

5.0 Output Voltage Versions



Adjustable Output Voltage Versions



Where $V_{ref} = 1.23 \text{ V}$, R_1
between $1.0 \text{ k}\Omega$ and $5.0 \text{ k}\Omega$

Figure 14. Typical Test Circuit

PCB LAYOUT GUIDELINES

As in any switching regulator, the layout of the printed circuit board is very important. Rapidly switching currents associated with wiring inductance, stray capacitance and parasitic inductance of the printed circuit board traces can generate voltage transients which can generate electromagnetic interferences (EMI) and affect the desired operation. As indicated in the Figure 14, to minimize inductance and ground loops, the length of the leads indicated by heavy lines should be kept as short as possible. For best results, single-point grounding (as indicated) or ground plane construction should be used.

On the other hand, the PCB area connected to the Pin 2 (emitter of the internal switch) of the LM2575 should be kept to a minimum in order to minimize coupling to sensitive circuitry.

Another sensitive part of the circuit is the feedback. It is important to keep the sensitive feedback wiring short. To assure this, physically locate the programming resistors near to the regulator, when using the adjustable version of the LM2575 regulator.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description (Refer to Figure 1)
1	V_{in}	This pin is the positive input supply for the LM2575 step-down switching regulator. In order to minimize voltage transients and to supply the switching currents needed by the regulator, a suitable input bypass capacitor must be present (C_{in} in Figure 1).
2	Output	This is the emitter of the internal switch. The saturation voltage V_{sat} of this output switch is typically 1.0 V. It should be kept in mind that the PCB area connected to this pin should be kept to a minimum in order to minimize coupling to sensitive circuitry.
3	GND	Circuit ground pin. See the information about the printed circuit board layout.
4	Feedback	This pin senses regulated output voltage to complete the feedback loop. The signal is divided by the internal resistor divider network R2, R1 and applied to the non-inverting input of the internal error amplifier. In the Adjustable version of the LM2575 switching regulator this pin is the direct input of the error amplifier and the resistor network R2, R1 is connected externally to allow programming of the output voltage.
5	$\overline{ON}/OFF$	It allows the switching regulator circuit to be shut down using logic level signals, thus dropping the total input supply current to approximately 80 μA . The input threshold voltage is typically 1.4 V. Applying a voltage above this value (up to $+V_{in}$) shuts the regulator off. If the voltage applied to this pin is lower than 1.4 V or if this pin is connected to ground, the regulator will be in the "on" condition.

DESIGN PROCEDURE

Buck Converter Basics

The LM2575 is a "Buck" or Step-Down Converter which is the most elementary forward-mode converter. Its basic schematic can be seen in Figure 15.

The operation of this regulator topology has two distinct time periods. The first one occurs when the series switch is on, the input voltage is connected to the input of the inductor.

The output of the inductor is the output voltage, and the rectifier (or catch diode) is reverse biased. During this period, since there is a constant voltage source connected across the inductor, the inductor current begins to linearly ramp upwards, as described by the following equation:

$$I_{L(on)} = \frac{(V_{in} - V_{out}) t_{on}}{L}$$

During this "on" period, energy is stored within the core material in the form of magnetic flux. If the inductor is properly designed, there is sufficient energy stored to carry the requirements of the load during the "off" period.

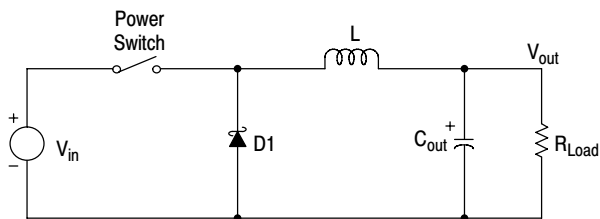


Figure 15. Basic Buck Converter

The next period is the "off" period of the power switch. When the power switch turns off, the voltage across the inductor reverses its polarity and is clamped at one diode voltage drop below ground by catch diode. Current now flows through the catch diode thus maintaining the load current loop. This removes the stored energy from the inductor.

The inductor current during this time is:

$$I_{L(off)} = \frac{(V_{out} - V_D) t_{off}}{L}$$

This period ends when the power switch is once again turned on. Regulation of the converter is accomplished by varying the duty cycle of the power switch. It is possible to describe the duty cycle as follows:

$$d = \frac{t_{on}}{T}, \text{ where } T \text{ is the period of switching.}$$

For the buck converter with ideal components, the duty cycle can also be described as:

$$d = \frac{V_{out}}{V_{in}}$$

Figure 16 shows the buck converter idealized waveforms of the catch diode voltage and the inductor current.

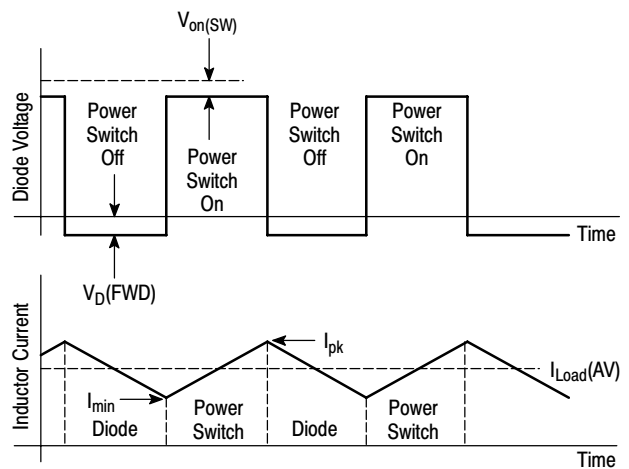


Figure 16. Buck Converter Idealized Waveforms

Procedure (Fixed Output Voltage Version) In order to simplify the switching regulator design, a step-by-step design procedure and example is provided.

Procedure	Example
Given Parameters: V_{out} = Regulated Output Voltage (3.3 V, 5.0 V, 12 V or 15 V) $V_{in(max)}$ = Maximum DC Input Voltage $I_{Load(max)}$ = Maximum Load Current	Given Parameters: V_{out} = 5.0 V $V_{in(max)}$ = 20 V $I_{Load(max)}$ = 0.8 A
1. Controller IC Selection According to the required input voltage, output voltage and current, select the appropriate type of the controller IC output voltage version.	1. Controller IC Selection According to the required input voltage, output voltage, current polarity and current value, use the LM2575-5 controller IC
2. Input Capacitor Selection (C_{in}) To prevent large voltage transients from appearing at the input and for stable operation of the converter, an aluminium or tantalum electrolytic bypass capacitor is needed between the input pin + V_{in} and ground pin GND. This capacitor should be located close to the IC using short leads. This capacitor should have a low ESR (Equivalent Series Resistance) value.	2. Input Capacitor Selection (C_{in}) A 47 μ F, 25 V aluminium electrolytic capacitor located near to the input and ground pins provides sufficient bypassing.
3. Catch Diode Selection ($D1$) A. Since the diode maximum peak current exceeds the regulator maximum load current the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design the diode should have a current rating equal to the maximum current limit of the LM2575 to be able to withstand a continuous output short B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.	3. Catch Diode Selection ($D1$) A. For this example the current rating of the diode is 1.0 A. B. Use a 30 V 1N5818 Schottky diode, or any of the suggested fast recovery diodes shown in the Table 4.
4. Inductor Selection ($L1$) A. According to the required working conditions, select the correct inductor value using the selection guide from Figures 17 to 21. B. From the appropriate inductor selection guide, identify the inductance region intersected by the Maximum Input Voltage line and the Maximum Load Current line. Each region is identified by an inductance value and an inductor code. C. Select an appropriate inductor from the several different manufacturers part numbers listed in Table 1 or Table 2. When using Table 2 for selecting the right inductor the designer must realize that the inductor current rating must be higher than the maximum peak current flowing through the inductor. This maximum peak current can be calculated as follows: $I_{p(max)} = I_{Load(max)} + \frac{(V_{in} - V_{out}) t_{on}}{2L}$ where t_{on} is the "on" time of the power switch and $t_{on} = \frac{V_{out}}{V_{in}} \times \frac{1}{f_{osc}}$ For additional information about the inductor, see the inductor section in the "External Components" section of this data sheet.	4. Inductor Selection ($L1$) A. Use the inductor selection guide shown in Figures 17 to 21. B. From the selection guide, the inductance area intersected by the 20 V line and 0.8 A line is L330. C. Inductor value required is 330 μ H. From the Table 1 or Table 2, choose an inductor from any of the listed manufacturers.

Procedure (Fixed Output Voltage Version) (continued) In order to simplify the switching regulator design, a step-by-step design procedure and example is provided.

Procedure	Example
5. Output Capacitor Selection (C_{out}) A. Since the LM2575 is a forward-mode switching regulator with voltage mode control, its open loop 2-pole-2-zero frequency characteristic has the dominant pole-pair determined by the output capacitor and inductor values. For stable operation and an acceptable ripple voltage, (approximately 1% of the output voltage) a value between 100 μ F and 470 μ F is recommended. B. Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating at least 8V is appropriate, and a 10 V or 16 V rating is recommended.	5. Output Capacitor Selection (C_{out}) A. $C_{out} = 100 \mu\text{F}$ to 470 μF standard aluminium electrolytic. B. Capacitor voltage rating = 16 V.

Procedure (Adjustable Output Version: LM2575-Adj)

Procedure	Example
Given Parameters: V_{out} = Regulated Output Voltage $V_{in(max)}$ = Maximum DC Input Voltage $I_{Load(max)}$ = Maximum Load Current	Given Parameters: $V_{out} = 8.0 \text{ V}$ $V_{in(max)} = 12 \text{ V}$ $I_{Load(max)} = 1.0 \text{ A}$
1. Programming Output Voltage To select the right programming resistor R1 and R2 value (see Figure 14) use the following formula: $V_{out} = V_{ref} \left(1 + \frac{R2}{R1} \right) \text{ where } V_{ref} = 1.23 \text{ V}$ Resistor R1 can be between 1.0 k and 5.0 k Ω . (For best temperature coefficient and stability with time, use 1% metal film resistors). $R2 = R1 \left(\frac{V_{out}}{V_{ref}} - 1 \right)$	1. Programming Output Voltage (selecting R1 and R2) Select R1 and R2: $V_{out} = 1.23 \left(1 + \frac{R2}{R1} \right) \text{ Select } R1 = 1.8 \text{ k}\Omega$ $R2 = R1 \left(\frac{V_{out}}{V_{ref}} - 1 \right) = 1.8 \text{ k} \left(\frac{8.0 \text{ V}}{1.23 \text{ V}} - 1 \right)$ $R2 = 9.91 \text{ k}\Omega, \text{ choose a } 9.88 \text{ k metal film resistor.}$
2. Input Capacitor Selection (C_{in}) To prevent large voltage transients from appearing at the input and for stable operation of the converter, an aluminium or tantalum electrolytic bypass capacitor is needed between the input pin + V_{in} and ground pin GND. This capacitor should be located close to the IC using short leads. This capacitor should have a low ESR (Equivalent Series Resistance) value. For additional information see input capacitor section in the "External Components" section of this data sheet.	2. Input Capacitor Selection (C_{in}) A 100 μ F aluminium electrolytic capacitor located near the input and ground pin provides sufficient bypassing.
3. Catch Diode Selection (D1) A. Since the diode maximum peak current exceeds the regulator maximum load current the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design, the diode should have a current rating equal to the maximum current limit of the LM2575 to be able to withstand a continuous output short. B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.	3. Catch Diode Selection (D1) A. For this example, a 3.0 A current rating is adequate. B. Use a 20 V 1N5820 or MBR320 Schottky diode or any suggested fast recovery diode in the Table 4.

Procedure (Adjustable Output Version: LM2575–Adj) (continued)

Procedure	Example
4. Inductor Selection (L1) A. Use the following formula to calculate the inductor Volt x microsecond [V x μs] constant: $E \times T = (V_{in} - V_{out}) \frac{V_{out}}{V_{on}} \times \frac{10^6}{F[\text{Hz}]} \text{ [V x } \mu\text{s]}$ B. Match the calculated E x T value with the corresponding number on the vertical axis of the Inductor Value Selection Guide shown in Figure 21. This E x T constant is a measure of the energy handling capability of an inductor and is dependent upon the type of core, the core area, the number of turns, and the duty cycle. C. Next step is to identify the inductance region intersected by the E x T value and the maximum load current value on the horizontal axis shown in Figure 21. D. From the inductor code, identify the inductor value. Then select an appropriate inductor from the Table 1 or Table 2. The inductor chosen must be rated for a switching frequency of 52 kHz and for a current rating of $1.15 \times I_{load}$. The inductor current rating can also be determined by calculating the inductor peak current: $I_{p(\text{max})} = I_{\text{Load}(\text{max})} + \frac{(V_{in} - V_{out}) t_{on}}{2L}$ where t_{on} is the “on” time of the power switch and $t_{on} = \frac{V_{out}}{V_{in}} \times \frac{1}{f_{osc}}$ For additional information about the inductor, see the inductor section in the “External Components” section of this data sheet.	4. Inductor Selection (L1) A. Calculate E x T [V x μs] constant: $E \times T = (12 - 8.0) \times \frac{8.0}{12} \times \frac{1000}{52} = 51 \text{ [V x } \mu\text{s]}$ B. E x T = 51 [V x μs] C. $I_{\text{Load}(\text{max})} = 1.0 \text{ A}$ Inductance Region = L220 D. Proper inductor value = 220 μH Choose the inductor from the Table 1 or Table 2.
5. Output Capacitor Selection (C_{out}) A. Since the LM2575 is a forward-mode switching regulator with voltage mode control, its open loop 2-pole-2-zero frequency characteristic has the dominant pole-pair determined by the output capacitor and inductor values. For stable operation, the capacitor must satisfy the following requirement: $C_{out} \geq 7.785 \frac{V_{in(\text{max})}}{V_{out} \times L [\mu\text{H}]} \text{ } [\mu\text{F}]$ B. Capacitor values between 10 μF and 2000 μF will satisfy the loop requirements for stable operation. To achieve an acceptable output ripple voltage and transient response, the output capacitor may need to be several times larger than the above formula yields. C. Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating of at least 8V is appropriate, and a 10 V or 16 V rating is recommended.	5. Output Capacitor Selection (C_{out}) A. $C_{out} \geq 7.785 \frac{12}{8.220} = 53 \mu\text{F}$ To achieve an acceptable ripple voltage, select $C_{out} = 100 \mu\text{F}$ electrolytic capacitor.

LM2575

INDUCTOR VALUE SELECTION GUIDE

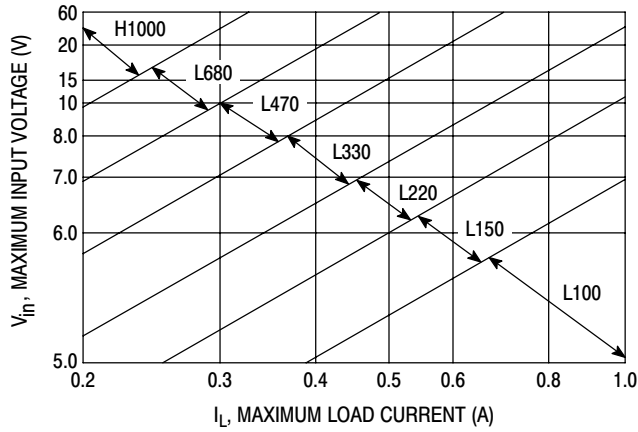


Figure 17. LM2575-3.3

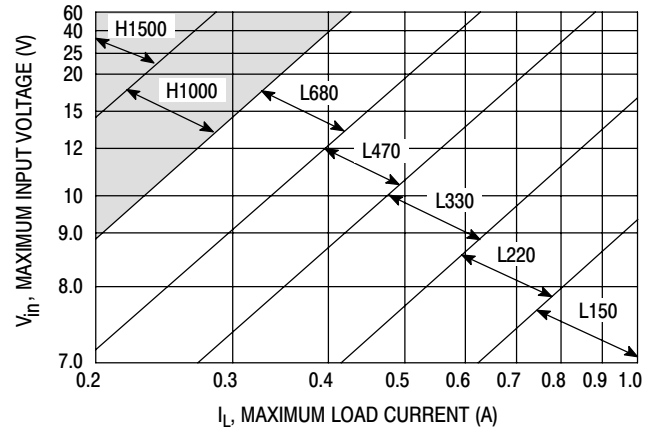


Figure 18. LM2575-5.0

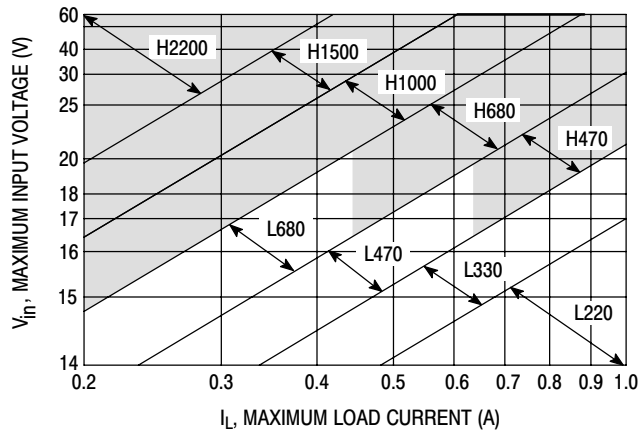


Figure 19. LM2575-12

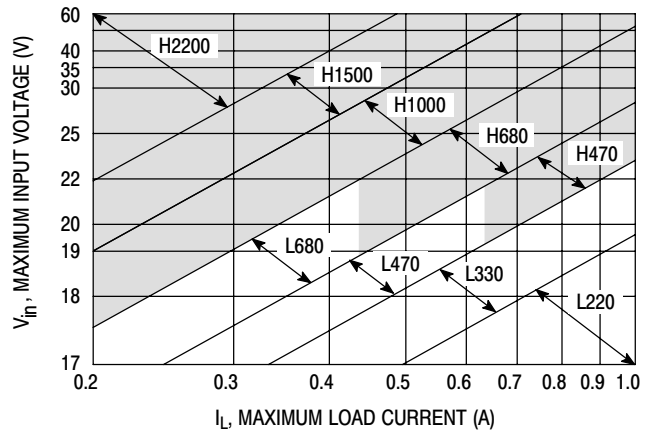


Figure 20. LM2575-15

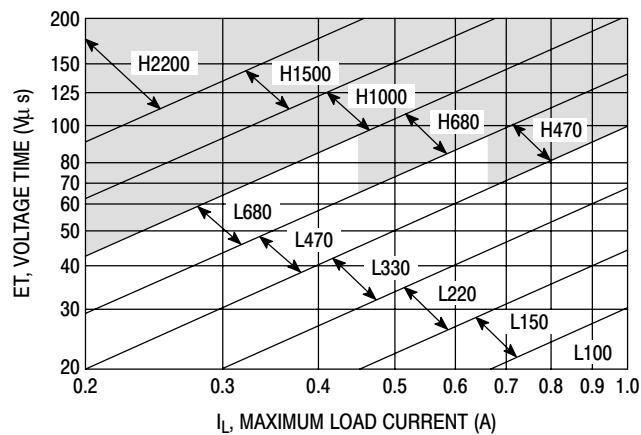


Figure 21. LM2575-Adj

NOTE: This Inductor Value Selection Guide is applicable for continuous mode only.

LM2575

Table 1. Inductor Selection Guide

Inductor Code	Inductor Value	Pulse Eng	Renco	AIE	Tech 39
L100	100 μ H	PE-92108	RL2444	415-0930	77 308 BV
L150	150 μ H	PE-53113	RL1954	415-0953	77 358 BV
L220	220 μ H	PE-52626	RL1953	415-0922	77 408 BV
L330	330 μ H	PE-52627	RL1952	415-0926	77 458 BV
L470	470 μ H	PE-53114	RL1951	415-0927	–
L680	680 μ H	PE-52629	RL1950	415-0928	77 508 BV
H150	150 μ H	PE-53115	RL2445	415-0936	77 368 BV
H220	220 μ H	PE-53116	RL2446	430-0636	77 410 BV
H330	330 μ H	PE-53117	RL2447	430-0635	77 460 BV
H470	470 μ H	PE-53118	RL1961	430-0634	–
H680	680 μ H	PE-53119	RL1960	415-0935	77 510 BV
H1000	1000 μ H	PE-53120	RL1959	415-0934	77 558 BV
H1500	1500 μ H	PE-53121	RL1958	415-0933	–
H2200	2200 μ H	PE-53122	RL2448	415-0945	77 610 BV

Table 2. Inductor Selection Guide

Inductance (μ H)	Current (A)	Schott		Renco		Pulse Engineering		Coilcraft
		THT	SMT	THT	SMT	THT	SMT	SMT
68	0.32	67143940	67144310	RL-1284-68-43	RL1500-68	PE-53804	PE-53804-S	DO1608-68
	0.58	67143990	67144360	RL-5470-6	RL1500-68	PE-53812	PE-53812-S	DO3308-683
	0.99	67144070	67144450	RL-5471-5	RL1500-68	PE-53821	PE-53821-S	DO3316-683
	1.78	67144140	67144520	RL-5471-5	–	PE-53830	PE-53830-S	DO5022P-683
100	0.48	67143980	67144350	RL-5470-5	RL1500-100	PE-53811	PE-53811-S	DO3308-104
	0.82	67144060	67144440	RL-5471-4	RL1500-100	PE-53820	PE-53820-S	DO3316-104
	1.47	67144130	67144510	RL-5471-4	–	PE-53829	PE-53829-S	DO5022P-104
150	0.39	–	67144340	RL-5470-4	RL1500-150	PE-53810	PE-53810-S	DO3308-154
	0.66	67144050	67144430	RL-5471-3	RL1500-150	PE-53819	PE-53819-S	DO3316-154
	1.20	67144120	67144500	RL-5471-3	–	PE-53828	PE-53828-S	DO5022P-154
220	0.32	67143960	67144330	RL-5470-3	RL1500-220	PE-53809	PE-53809-S	DO3308-224
	0.55	67144040	67144420	RL-5471-2	RL1500-220	PE-53818	PE-53818-S	DO3316-224
	1.00	67144110	67144490	RL-5471-2	–	PE-53827	PE-53827-S	DO5022P-224
330	0.42	67144030	67144410	RL-5471-1	RL1500-330	PE-53817	PE-53817-S	DO3316-334
	0.80	67144100	67144480	RL-5471-1	–	PE-53826	PE-53826-S	DO5022P-334

NOTE: Table 1 and Table 2 of this Indicator Selection Guide shows some examples of different manufacturer products suitable for design with the LM2575.

Table 3. Example of Several Inductor Manufacturers Phone/Fax Numbers

Pulse Engineering Inc.	Phone Fax	+ 1-619-674-8100 + 1-619-674-8262
Pulse Engineering Inc. Europe	Phone Fax	+ 353 93 24 107 + 353 93 24 459
Renco Electronics Inc.	Phone Fax	+ 1-516-645-5828 + 1-516-586-5562
AIE Magnetics	Phone Fax	+ 1-813-347-2181
Coilcraft Inc.	Phone Fax	+ 1-708-322-2645 + 1-708-639-1469
Coilcraft Inc., Europe	Phone Fax	+ 44 1236 730 595 + 44 1236 730 627
Tech 39	Phone Fax	+ 33 8425 2626 + 33 8425 2610
Schott Corp.	Phone Fax	+ 1-612-475-1173 + 1-612-475-1786

Table 4. Diode Selection Guide gives an overview about both surface-mount and through-hole diodes for an effective design. Device listed in bold are available from ON Semiconductor.

V _R	Schottky				Ultra-Fast Recovery			
	1.0 A		3.0 A		1.0 A		3.0 A	
	SMT	THT	SMT	THT	SMT	THT	SMT	THT
20 V	SK12	1N5817 SR102	SK32 MBRD320	1N5820 MBR320 SR302	MURS120T3 10BF10	MUR120 11DF1 HER102	MURS320T3 MURD320	MUR320 30WF10 MUR420
30 V	MBRS130LT3 SK13	1N5818 SR103 11DQ03	SK33 MBRD330	1N5821 MBR330 SR303 31DQ03				
40 V	MBRS140T3 SK14 10BQ040 10MQ040	1N5819 SR104 11DQ04	MBRS340T3 MBRD340 30WQ04 SK34	1N5822 MBR340 SR304 31DQ04				
50 V	MBRS150 10BQ050	MBR150 SR105 11DQ05	MBRD350 SK35 30WQ05	MBR350 SR305 11DQ05			31DF1 HER302	

EXTERNAL COMPONENTS

Input Capacitor (C_{in})***The Input Capacitor Should Have a Low ESR***

For stable operation of the switch mode converter a low ESR (Equivalent Series Resistance) aluminium or solid tantalum bypass capacitor is needed between the input pin and the ground pin to prevent large voltage transients from appearing at the input. It must be located near the regulator and use short leads. With most electrolytic capacitors, the capacitance value decreases and the ESR increases with lower temperatures. For reliable operation in temperatures below -25°C larger values of the input capacitor may be needed. Also paralleling a ceramic or solid tantalum capacitor will increase the regulator stability at cold temperatures.

RMS Current Rating of C_{in}

The important parameter of the input capacitor is the RMS current rating. Capacitors that are physically large and have large surface area will typically have higher RMS current ratings. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower voltage capacitor, and thus be able to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating. The consequence of operating an electrolytic capacitor above the RMS current rating is a shortened operating life. In order to assure maximum capacitor operating lifetime, the capacitor's RMS ripple current rating should be:

$$I_{rms} > 1.2 \times d \times I_{Load}$$

where d is the duty cycle, for a buck regulator

$$d = \frac{t_{on}}{T} = \frac{V_{out}}{V_{in}}$$

$$\text{and } d = \frac{t_{on}}{T} = \frac{|V_{out}|}{|V_{out}| + V_{in}} \text{ for a buck-boost regulator.}$$

Output Capacitor (C_{out})

For low output ripple voltage and good stability, low ESR output capacitors are recommended. An output capacitor has two main functions: it filters the output and provides regulator loop stability. The ESR of the output capacitor and the peak-to-peak value of the inductor ripple current are the main factors contributing to the output ripple voltage value. Standard aluminium electrolytics could be adequate for some applications but for quality design low ESR types are recommended.

An aluminium electrolytic capacitor's ESR value is related to many factors such as the capacitance value, the voltage rating, the physical size and the type of construction. In most cases, the higher voltage electrolytic capacitors have lower ESR value. Often capacitors with much higher voltage ratings may be needed to provide low ESR values that are required for low output ripple voltage.

The Output Capacitor Requires an ESR Value That Has an Upper and Lower Limit

As mentioned above, a low ESR value is needed for low output ripple voltage, typically 1% to 2% of the output voltage. But if the selected capacitor's ESR is extremely low

(below 0.05Ω), there is a possibility of an unstable feedback loop, resulting in oscillation at the output. This situation can occur when a tantalum capacitor, that can have a very low ESR, is used as the only output capacitor.

At Low Temperatures, Put in Parallel Aluminium Electrolytic Capacitors with Tantalum Capacitors

Electrolytic capacitors are not recommended for temperatures below -25°C . The ESR rises dramatically at cold temperatures and typically rises 3 times at -25°C and as much as 10 times at -40°C . Solid tantalum capacitors have much better ESR spec at cold temperatures and are recommended for temperatures below -25°C . They can be also used in parallel with aluminium electrolytics. The value of the tantalum capacitor should be about 10% or 20% of the total capacitance. The output capacitor should have at least 50% higher RMS ripple current rating at 52 kHz than the peak-to-peak inductor ripple current.

Catch Diode***Locate the Catch Diode Close to the LM2575***

The LM2575 is a step-down buck converter; it requires a fast diode to provide a return path for the inductor current when the switch turns off. This diode must be located close to the LM2575 using short leads and short printed circuit traces to avoid EMI problems.

Use a Schottky or a Soft Switching Ultra-Fast Recovery Diode

Since the rectifier diodes are very significant source of losses within switching power supplies, choosing the rectifier that best fits into the converter design is an important process. Schottky diodes provide the best performance because of their fast switching speed and low forward voltage drop.

They provide the best efficiency especially in low output voltage applications (5.0 V and lower). Another choice could be Fast-Recovery, or Ultra-Fast Recovery diodes. It has to be noted, that some types of these diodes with an abrupt turnoff characteristic may cause instability or EMI troubles.

A fast-recovery diode with soft recovery characteristics can better fulfill a quality, low noise design requirements. Table 4 provides a list of suitable diodes for the LM2575 regulator. Standard 50/60 Hz rectifier diodes such as the 1N4001 series or 1N5400 series are **NOT** suitable.

Inductor

The magnetic components are the cornerstone of all switching power supply designs. The style of the core and the winding technique used in the magnetic component's design has a great influence on the reliability of the overall power supply.

Using an improper or poorly designed inductor can cause high voltage spikes generated by the rate of transitions in current within the switching power supply, and the possibility of core saturation can arise during an abnormal operational mode. Voltage spikes can cause the semiconductors to enter avalanche breakdown and the part can instantly fail if enough energy is applied. It can also

cause significant RFI (Radio Frequency Interference) and EMI (Electro-Magnetic Interference) problems.

Continuous and Discontinuous Mode of Operation

The LM2575 step-down converter can operate in both the continuous and the discontinuous modes of operation. The regulator works in the continuous mode when loads are relatively heavy, the current flows through the inductor continuously and never falls to zero. Under light load conditions, the circuit will be forced to the discontinuous mode when inductor current falls to zero for certain period of time (see Figure 22 and Figure 23). Each mode has distinctively different operating characteristics, which can affect the regulator performance and requirements. In many cases the preferred mode of operation is the continuous mode. It offers greater output power, lower peak currents in the switch, inductor and diode, and can have a lower output ripple voltage. On the other hand it does require larger inductor values to keep the inductor current flowing continuously, especially at low output load currents and/or high input voltages.

To simplify the inductor selection process, an inductor selection guide for the LM2575 regulator was added to this data sheet (Figures 17 through 21). This guide assumes that the regulator is operating in the continuous mode, and selects an inductor that will allow a peak-to-peak inductor ripple current to be a certain percentage of the maximum design load current. This percentage is allowed to change as different design load currents are selected. For light loads (less than approximately 200 mA) it may be desirable to operate the regulator in the discontinuous mode, because the inductor value and size can be kept relatively low. Consequently, the percentage of inductor peak-to-peak current increases. This discontinuous mode of operation is perfectly acceptable for this type of switching converter. Any buck regulator will be forced to enter discontinuous mode if the load current is light enough.

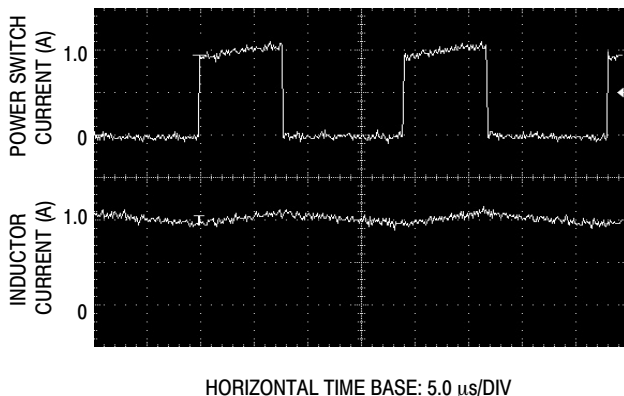


Figure 22. Continuous Mode Switching Current Waveforms

Selecting the Right Inductor Style

Some important considerations when selecting a core type are core material, cost, the output power of the power supply,

the physical volume the inductor must fit within, and the amount of EMI (Electro-Magnetic Interference) shielding that the core must provide. The inductor selection guide covers different styles of inductors, such as pot core, E-core, toroid and bobbin core, as well as different core materials such as ferrites and powdered iron from different manufacturers.

For high quality design regulators the toroid core seems to be the best choice. Since the magnetic flux is completely contained within the core, it generates less EMI, reducing noise problems in sensitive circuits. The least expensive is the bobbin core type, which consists of wire wound on a ferrite rod core. This type of inductor generates more EMI due to the fact that its core is open, and the magnetic flux is not completely contained within the core.

When multiple switching regulators are located on the same printed circuit board, open core magnetics can cause interference between two or more of the regulator circuits, especially at high currents due to mutual coupling. A toroid, pot core or E-core (closed magnetic structure) should be used in such applications.

Do Not Operate an Inductor Beyond its Maximum Rated Current

Exceeding an inductor's maximum current rating may cause the inductor to overheat because of the copper wire losses, or the core may saturate. Core saturation occurs when the flux density is too high and consequently the cross sectional area of the core can no longer support additional lines of magnetic flux.

This causes the permeability of the core to drop, the inductance value decreases rapidly and the inductor begins to look mainly resistive. It has only the dc resistance of the winding. This can cause the switch current to rise very rapidly and force the LM2575 internal switch into cycle-by-cycle current limit, thus reducing the dc output load current. This can also result in overheating of the inductor and/or the LM2575. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.

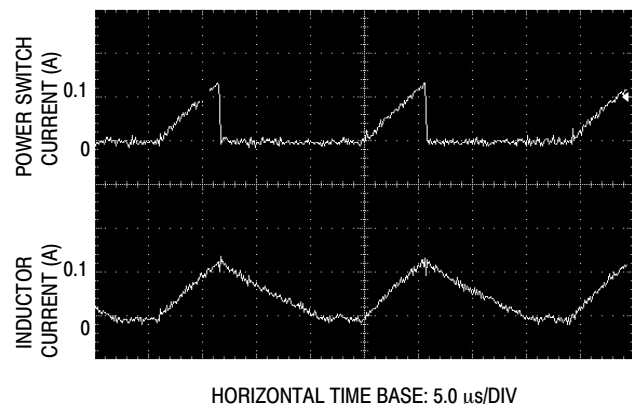


Figure 23. Discontinuous Mode Switching Current Waveforms

GENERAL RECOMMENDATIONS

Output Voltage Ripple and Transients**Source of the Output Ripple**

Since the LM2575 is a switch mode power supply regulator, its output voltage, if left unfiltered, will contain a sawtooth ripple voltage at the switching frequency. The output ripple voltage value ranges from 0.5% to 3% of the output voltage. It is caused mainly by the inductor sawtooth ripple current multiplied by the ESR of the output capacitor.

Short Voltage Spikes and How to Reduce Them

The regulator output voltage may also contain short voltage spikes at the peaks of the sawtooth waveform (see Figure 24). These voltage spikes are present because of the fast switching action of the output switch, and the parasitic inductance of the output filter capacitor. There are some other important factors such as wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all these contribute to the amplitude of these spikes. To minimize these voltage spikes, low inductance capacitors should be used, and their lead lengths must be kept short. The importance of quality printed circuit board layout design should also be highlighted.

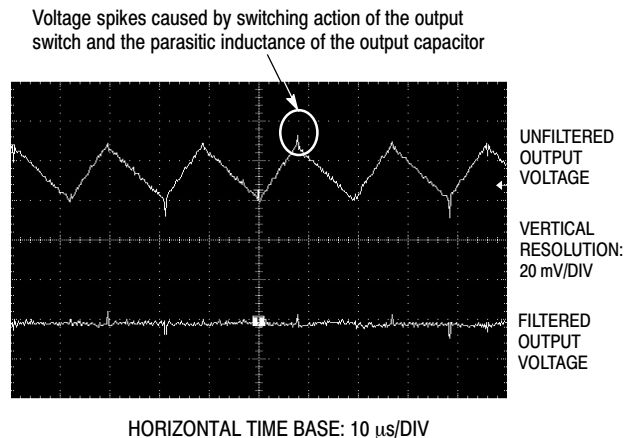


Figure 24. Output Ripple Voltage Waveforms

Minimizing the Output Ripple

In order to minimize the output ripple voltage it is possible to enlarge the inductance value of the inductor L1 and/or to use a larger value output capacitor. There is also another way to smooth the output by means of an additional LC filter (20 μ H, 100 μ F), that can be added to the output (see Figure 33) to further reduce the amount of output ripple and transients. With such a filter it is possible to reduce the output ripple voltage transients 10 times or more. Figure 24 shows the difference between filtered and unfiltered output waveforms of the regulator shown in Figure 33.

The upper waveform is from the normal unfiltered output of the converter, while the lower waveform shows the output ripple voltage filtered by an additional LC filter.

Heatsinking and Thermal Considerations**The Through-Hole Package TO-220**

The LM2575 is available in two packages, a 5-pin TO-220(T, TV) and a 5-pin surface mount D²PAK(D2T). There are many applications that require no heatsink to keep the LM2575 junction temperature within the allowed operating range. The TO-220 package can be used without a heatsink for ambient temperatures up to approximately 50°C (depending on the output voltage and load current). Higher ambient temperatures require some heatsinking, either to the printed circuit (PC) board or an external heatsink.

The Surface Mount Package D²PAK and its Heatsinking

The other type of package, the surface mount D²PAK, is designed to be soldered to the copper on the PC board. The copper and the board are the heatsink for this package and the other heat producing components, such as the catch diode and inductor. The PC board copper area that the package is soldered to should be at least 0.4 in² (or 100 mm²) and ideally should have 2 or more square inches (1300 mm²) of 0.0028 inch copper. Additional increasing of copper area beyond approximately 3.0 in² (2000 mm²) will not improve heat dissipation significantly. If further thermal improvements are needed, double sided or multilayer PC boards with large copper areas should be considered.

Thermal Analysis and Design

The following procedure must be performed to determine whether or not a heatsink will be required. First determine:

1. $P_{D(max)}$ maximum regulator power dissipation in the application.
2. $T_{A(max)}$ maximum ambient temperature in the application.
3. $T_{J(max)}$ maximum allowed junction temperature (125°C for the LM2575). For a conservative design, the maximum junction temperature should not exceed 110°C to assure safe operation. For every additional 10°C temperature rise that the junction must withstand, the estimated operating lifetime of the component is halved.
4. $R_{\theta JC}$ package thermal resistance junction–case.
5. $R_{\theta JA}$ package thermal resistance junction–ambient.

(Refer to Absolute Maximum Ratings in this data sheet or $R_{\theta JC}$ and $R_{\theta JA}$ values).

The following formula is to calculate the total power dissipated by the LM2575:

$$P_D = (V_{in} \times I_Q) + d \times I_{Load} \times V_{sat}$$

where d is the duty cycle and for buck converter

$$d = \frac{t_{on}}{T} = \frac{V_O}{V_{in}}$$

I_Q (quiescent current) and V_{sat} can be found in the LM2575 data sheet,

V_{in} is minimum input voltage applied,

V_O is the regulator output voltage,

I_{Load} is the load current.

The dynamic switching losses during turn-on and turn-off can be neglected if proper type catch diode is used.

Packages Not on a Heatsink (Free-Standing)

For a free-standing application when no heatsink is used, the junction temperature can be determined by the following expression:

$$T_J = (R_{\theta JA}) (P_D) + T_A$$

where $(R_{\theta JA})(P_D)$ represents the junction temperature rise caused by the dissipated power and T_A is the maximum ambient temperature.

Packages on a Heatsink

If the actual operating junction temperature is greater than the selected safe operating junction temperature determined in step 3, than a heatsink is required. The junction temperature will be calculated as follows:

$$T_J = P_D (R_{\theta JA} + R_{\theta CS} + R_{\theta SA}) + T_A$$

where $R_{\theta JC}$ is the thermal resistance junction-case,
 $R_{\theta CS}$ is the thermal resistance case-heatsink,
 $R_{\theta SA}$ is the thermal resistance heatsink-ambient.

If the actual operating temperature is greater than the selected safe operating junction temperature, then a larger heatsink is required.

Some Aspects That can Influence Thermal Design

It should be noted that the package thermal resistance and the junction temperature rise numbers are all approximate, and there are many factors that will affect these numbers, such as PC board size, shape, thickness, physical position, location, board temperature, as well as whether the surrounding air is moving or still.

Other factors are trace width, total printed circuit copper area, copper thickness, single- or double-sided, multilayer board, the amount of solder on the board or even color of the traces.

The size, quantity and spacing of other components on the board can also influence its effectiveness to dissipate the heat.

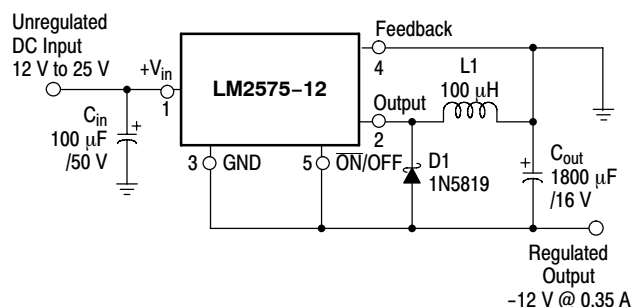


Figure 25. Inverting Buck-Boost Regulator Using the LM2575-12 Develops -12 V @ 0.35 A

ADDITIONAL APPLICATIONS

Inverting Regulator

An inverting buck-boost regulator using the LM2575-12 is shown in Figure 25. This circuit converts a positive input voltage to a negative output voltage with a common ground by bootstrapping the regulators ground to the negative output voltage. By grounding the feedback pin, the regulator senses the inverted output voltage and regulates it.

In this example the LM2575-12 is used to generate a -12 V output. The maximum input voltage in this case cannot exceed +28 V because the maximum voltage appearing across the regulator is the absolute sum of the input and output voltages and this must be limited to a maximum of 40 V.

This circuit configuration is able to deliver approximately 0.35 A to the output when the input voltage is 12 V or higher. At lighter loads the minimum input voltage required drops to approximately 4.7 V, because the buck-boost regulator topology can produce an output voltage that, in its absolute value, is either greater or less than the input voltage.

Since the switch currents in this buck-boost configuration are higher than in the standard buck converter topology, the available output current is lower.

This type of buck-boost inverting regulator can also require a larger amount of startup input current, even for light loads. This may overload an input power source with a current limit less than 1.5 A.

Such an amount of input startup current is needed for at least 2.0 ms or more. The actual time depends on the output voltage and size of the output capacitor.

Because of the relatively high startup currents required by this inverting regulator topology, the use of a delayed startup or an undervoltage lockout circuit is recommended.

Using a delayed startup arrangement, the input capacitor can charge up to a higher voltage before the switch-mode regulator begins to operate.

The high input current needed for startup is now partially supplied by the input capacitor C_{in} .

Design Recommendations:

The inverting regulator operates in a different manner than the buck converter and so a different design procedure has to be used to select the inductor L_1 or the output capacitor C_{out} .

The output capacitor values must be larger than is normally required for buck converter designs. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of μF).

The recommended range of inductor values for the inverting converter design is between $68\ \mu\text{H}$ and $220\ \mu\text{H}$. To select an inductor with an appropriate current rating, the inductor peak current has to be calculated.

The following formula is used to obtain the peak inductor current:

$$I_{\text{peak}} \approx \frac{I_{\text{Load}} (V_{\text{in}} + |V_{\text{O}}|)}{V_{\text{in}}} + \frac{V_{\text{in}} \times t_{\text{on}}}{2L_1}$$

where $t_{\text{on}} = \frac{|V_{\text{O}}|}{V_{\text{in}} + |V_{\text{O}}|} \times \frac{1}{f_{\text{osc}}}$, and $f_{\text{osc}} = 52\ \text{kHz}$.

Under normal continuous inductor current operating conditions, the worst case occurs when V_{in} is minimal.

Note that the voltage appearing across the regulator is the absolute sum of the input and output voltage, and must not exceed $40\ \text{V}$.

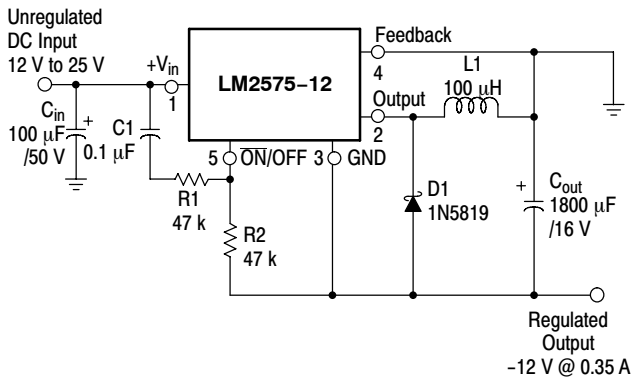
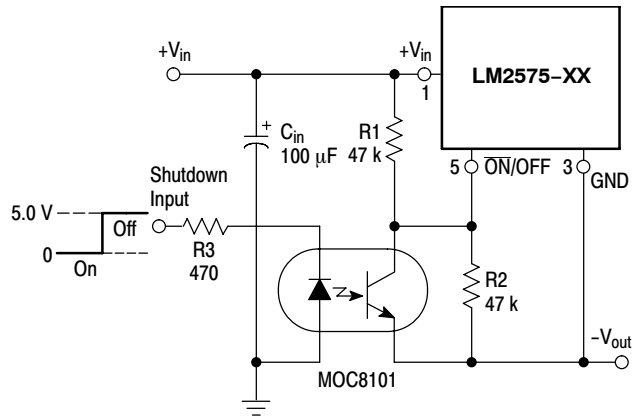


Figure 26. Inverting Buck-Boost Regulator with Delayed Startup

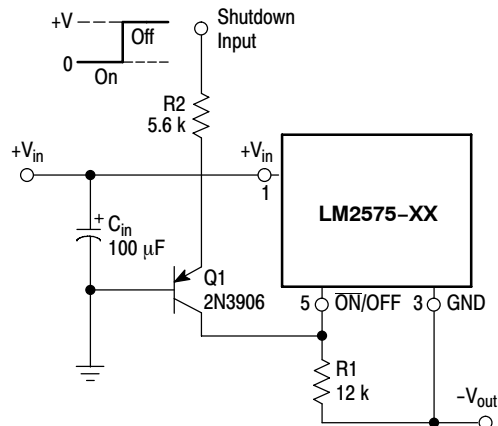
It has been already mentioned above, that in some situations, the delayed startup or the undervoltage lockout features could be very useful. A delayed startup circuit applied to a buck-boost converter is shown in Figure 26. Figure 32 in the “Undervoltage Lockout” section describes an undervoltage lockout feature for the same converter topology.



NOTE: This picture does not show the complete circuit.

Figure 27. Inverting Buck-Boost Regulator Shut Down Circuit Using an Optocoupler

With the inverting configuration, the use of the $\overline{\text{ON/OFF}}$ pin requires some level shifting techniques. This is caused by the fact, that the ground pin of the converter IC is no longer at ground. Now, the $\overline{\text{ON/OFF}}$ pin threshold voltage ($1.4\ \text{V}$ approximately) has to be related to the negative output voltage level. There are many different possible shut down methods, two of them are shown in Figures 27 and 28.



NOTE: This picture does not show the complete circuit.

Figure 28. Inverting Buck-Boost Regulator Shut Down Circuit Using a PNP Transistor

Negative Boost Regulator

This example is a variation of the buck-boost topology and is called a negative boost regulator. This regulator experiences relatively high switch current, especially at low input voltages. The internal switch current limiting results in lower output load current capability.

The circuit in Figure 29 shows the negative boost configuration. The input voltage in this application ranges from $-5.0\ \text{V}$ to $-12\ \text{V}$ and provides a regulated $-12\ \text{V}$ output.

If the input voltage is greater than -12 V, the output will rise above -12 V accordingly, but will not damage the regulator.

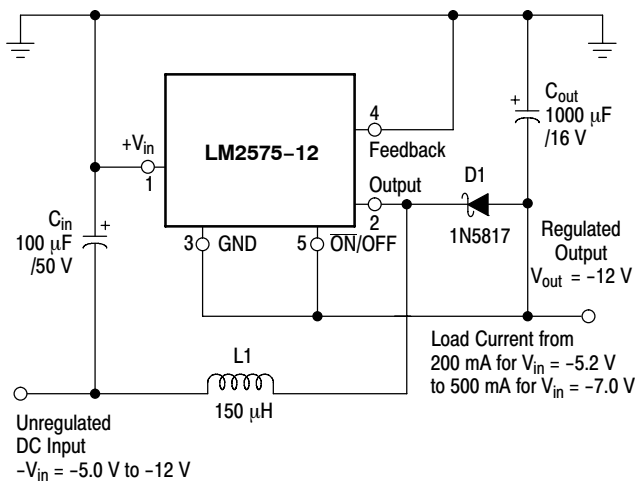


Figure 29. Negative Boost Regulator

Design Recommendations:

The same design rules as for the previous inverting buck-boost converter can be applied. The output capacitor C_{out} must be chosen larger than would be required for a standard buck converter. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of μF). The recommended range of inductor values for the negative boost regulator is the same as for inverting converter design.

Another important point is that these negative boost converters cannot provide current limiting load protection in the event of a short in the output so some other means, such as a fuse, may be necessary to provide the load protection.

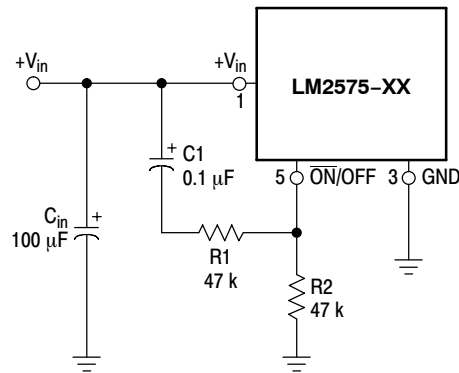
Delayed Startup

There are some applications, like the inverting regulator already mentioned above, which require a higher amount of startup current. In such cases, if the input power source is limited, this delayed startup feature becomes very useful.

To provide a time delay between the time the input voltage is applied and the time when the output voltage comes up, the circuit in Figure 30 can be used. As the input voltage is applied, the capacitor C_1 charges up, and the voltage across the resistor R_2 falls down. When the voltage on the $\overline{ON}/OFF$ pin falls below the threshold value 1.4 V, the regulator starts up. Resistor R_1 is included to limit the maximum voltage applied to the $\overline{ON}/OFF$ pin, reduces the power supply noise sensitivity, and also limits the capacitor C_1 discharge current, but its use is not mandatory.

When a high 50 Hz or 60 Hz (100 Hz or 120 Hz respectively) ripple voltage exists, a long delay time can

cause some problems by coupling the ripple into the $\overline{ON}/OFF$ pin, the regulator could be switched periodically on and off with the line (or double) frequency.



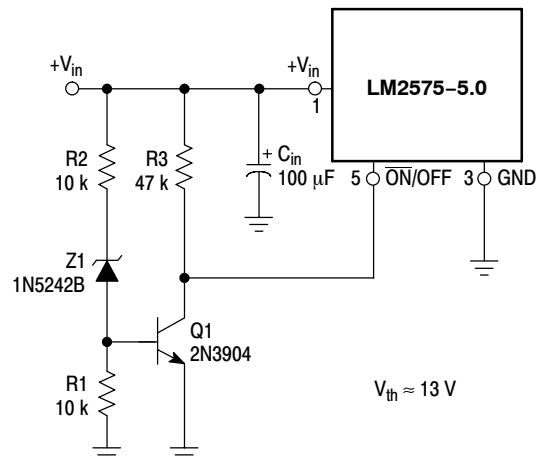
NOTE: This picture does not show the complete circuit.

Figure 30. Delayed Startup Circuitry

Undervoltage Lockout

Some applications require the regulator to remain off until the input voltage reaches a certain threshold level. Figure 31 shows an undervoltage lockout circuit applied to a buck regulator. A version of this circuit for buck-boost converter is shown in Figure 32. Resistor R_3 pulls the $\overline{ON}/OFF$ pin high and keeps the regulator off until the input voltage reaches a predetermined threshold level, which is determined by the following expression:

$$V_{th} \approx V_{Z1} + \left(1 + \frac{R_2}{R_1}\right) V_{BE}(Q1)$$



NOTE: This picture does not show the complete circuit.

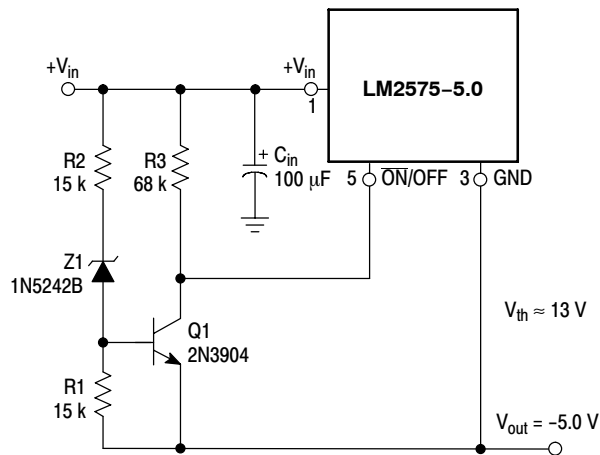
Figure 31. Undervoltage Lockout Circuit for Buck Converter

LM2575

Adjustable Output, Low-Ripple Power Supply

A 1.0 A output current capability power supply that features an adjustable output voltage is shown in Figure 33.

This regulator delivers 1.0 A into 1.2 V to 35 V output. The input voltage ranges from roughly 8.0 V to 40 V. In order to achieve a 10 or more times reduction of output ripple, an additional L–C filter is included in this circuit.



NOTE: This picture does not show the complete circuit.

Figure 32. Undervoltage Lockout Circuit for Buck-Boost Converter

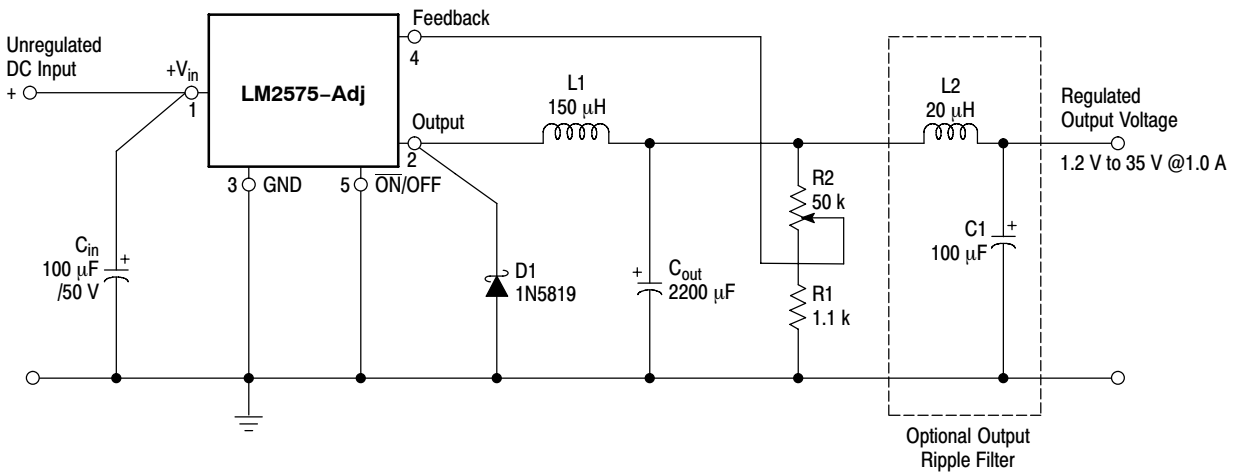


Figure 33. Adjustable Power Supply with Low Ripple Voltage

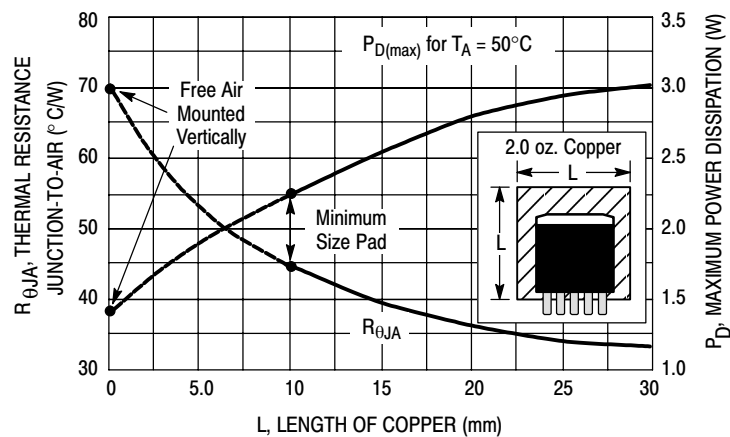


Figure 34. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

LM2575

THE LM2575-5.0 STEP-DOWN VOLTAGE REGULATOR WITH 5.0 V @ 1.0 A OUTPUT POWER CAPABILITY. TYPICAL APPLICATION WITH THROUGH-HOLE PC BOARD LAYOUT

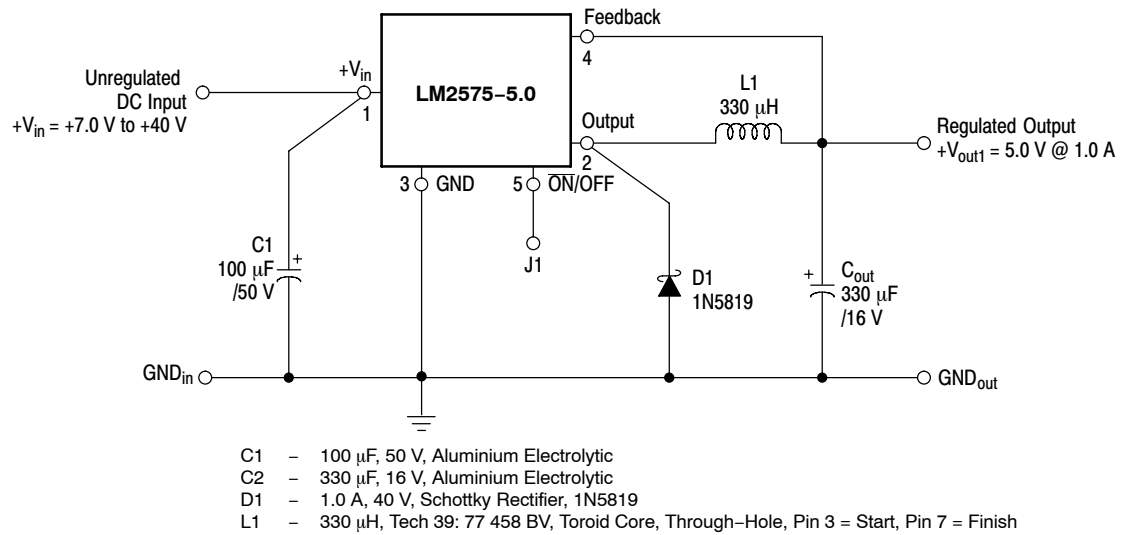
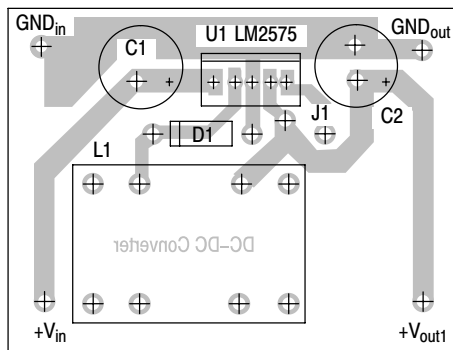
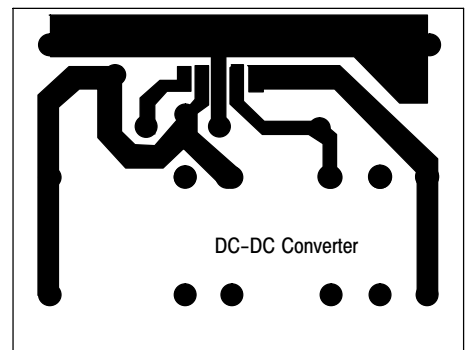


Figure 35. Schematic Diagram of the LM2575-5.0 Step-Down Converter



NOTE: Not to scale.

Figure 36. Printed Circuit Board Component Side



NOTE: Not to scale.

Figure 37. Printed Circuit Board Copper Side

LM2575

THE LM2575-ADJ STEP-DOWN VOLTAGE REGULATOR WITH 8.0 V @ 1.0 A OUTPUT POWER CAPABILITY. TYPICAL APPLICATION WITH THROUGH-HOLE PC BOARD LAYOUT

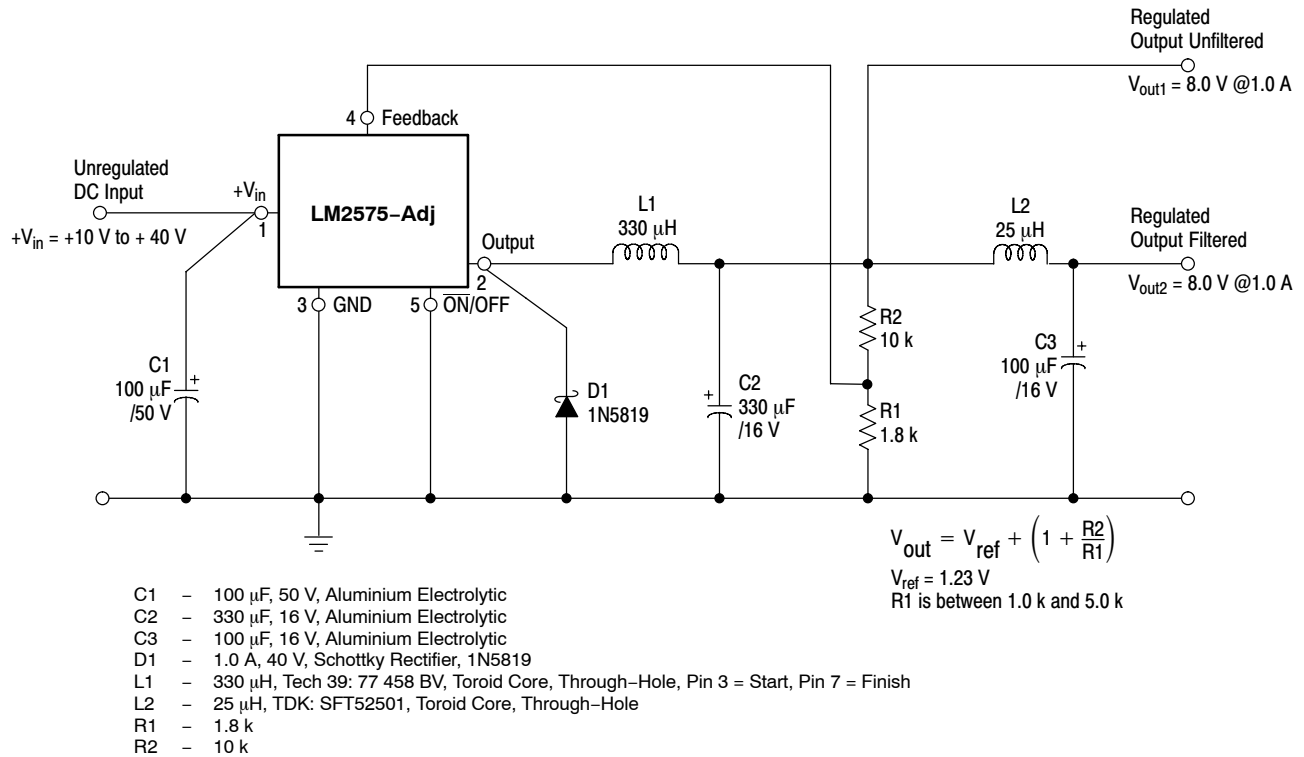
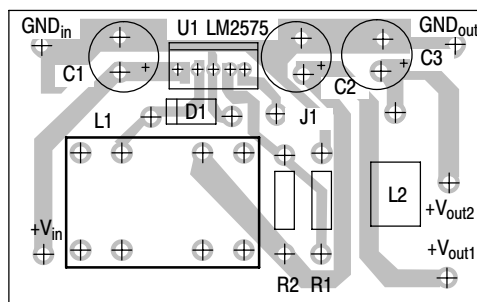
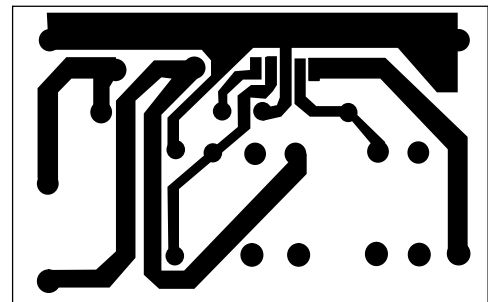


Figure 38. Schematic Diagram of the 8.0 V @ 1.0 V Step-Down Converter Using the LM2575-Adj
 (An additional LC filter is included to achieve low output ripple voltage)



NOTE: Not to scale.

Figure 39. PC Board Component Side



NOTE: Not to scale.

Figure 40. PC Board Copper Side

References

- National Semiconductor LM2575 Data Sheet and Application Note
- National Semiconductor LM2595 Data Sheet and Application Note
- Marty Brown "Practical Switching Power Supply Design", Academic Press, Inc., San Diego 1990
- Ray Ridley "High Frequency Magnetics Design", Ridley Engineering, Inc. 1995

LM2575

ORDERING INFORMATION

Device	Nominal Output Voltage	Operating Temperature Range	Package	Shipping [†]
LM2575TV-ADJ	1.23 V to 37 V	$T_J = -40^\circ \text{ to } +125^\circ \text{C}$	TO-220 (Vertical Mount)	50 Units/Rail
LM2575TV-ADJG			TO-220 (Vertical Mount) (Pb-Free)	50 Units/Rail
LM2575T-ADJ			TO-220 (Straight Lead)	50 Units/Rail
LM2575D2T-ADJ			D ² PAK (Surface Mount)	
LM2575D2T-ADJR4			D ² PAK (Surface Mount)	800 Tape & Reel
LM2575TV-3.3	3.3 V	$T_J = -40^\circ \text{ to } +125^\circ \text{C}$	TO-220 (Vertical Mount)	50 Units/Rail
LM2575T-3.3			TO-220 (Straight Lead)	
LM2575D2T-3.3			D ² PAK (Surface Mount)	
LM2575D2T-3.3R4			D ² PAK (Surface Mount)	800 Tape & Reel
LM2575TV-5	5.0 V	$T_J = -40^\circ \text{ to } +125^\circ \text{C}$	TO-220 (Vertical Mount)	50 Units/Rail
LM2575TV-5G			TO-220 (Vertical Mount) (Pb-Free)	50 Units/Rail
LM2575T-5			TO-220 (Straight Lead)	50 Units/Rail
LM2575D2T-5			D ² PAK (Surface Mount)	
LM2575D2T-5R4			D ² PAK (Surface Mount)	800 Tape & Reel
LM2575TV-12	12 V	$T_J = -40^\circ \text{ to } +125^\circ \text{C}$	TO-220 (Vertical Mount)	50 Units/Rail
LM2575T-12			TO-220 (Straight Lead)	
LM2575D2T-12			D ² PAK (Surface Mount)	
LM2575D2T-12R4			D ² PAK (Surface Mount)	800 Tape & Reel
LM2575TV-15	15 V	$T_J = -40^\circ \text{ to } +125^\circ \text{C}$	TO-220 (Vertical Mount)	50 Units/Rail
LM2575T-15			TO-220 (Straight Lead)	
LM2575D2T-15			D ² PAK (Surface Mount)	
LM2575D2T-15R4			D ² PAK (Surface Mount)	800 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

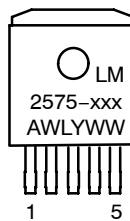
**TO-220
TV SUFFIX
CASE 314B**



**TO-220
T SUFFIX
CASE 314D**



**D²PAK
D2T SUFFIX
CASE 936A**



xxx = 3.3, 5.0, 12, 15, or ADJ
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

LM2576

3.0 A, 15 V, Step-Down Switching Regulator

The LM2576 series of regulators are monolithic integrated circuits ideally suited for easy and convenient design of a step-down switching regulator (buck converter). All circuits of this series are capable of driving a 3.0 A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3 V, 5.0 V, 12 V, 15 V, and an adjustable output version.

These regulators were designed to minimize the number of external components to simplify the power supply design. Standard series of inductors optimized for use with the LM2576 are offered by several different inductor manufacturers.

Since the LM2576 converter is a switch-mode power supply, its efficiency is significantly higher in comparison with popular three-terminal linear regulators, especially with higher input voltages. In many cases, the power dissipated is so low that no heatsink is required or its size could be reduced dramatically.

A standard series of inductors optimized for use with the LM2576 are available from several different manufacturers. This feature greatly simplifies the design of switch-mode power supplies.

The LM2576 features include a guaranteed $\pm 4\%$ tolerance on output voltage within specified input voltages and output load conditions, and $\pm 10\%$ on the oscillator frequency ($\pm 2\%$ over 0°C to 125°C). External shutdown is included, featuring $80\ \mu\text{A}$ (typical) standby current. The output switch includes cycle-by-cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

Features

- 3.3 V, 5.0 V, 12 V, 15 V, and Adjustable Output Versions
- Adjustable Version Output Voltage Range, 1.23 to 37 V $\pm 4\%$ Maximum Over Line and Load Conditions
- Guaranteed 3.0 A Output Current
- Wide Input Voltage Range
- Requires Only 4 External Components
- 52 kHz Fixed Frequency Internal Oscillator
- TTL Shutdown Capability, Low Power Standby Mode
- High Efficiency
- Uses Readily Available Standard Inductors
- Thermal Shutdown and Current Limit Protection
- Moisture Sensitivity Level (MSL) Equals 1
- Pb-Free Packages are Available*

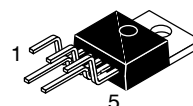
Applications

- Simple High-Efficiency Step-Down (Buck) Regulator
- Efficient Pre-Regulator for Linear Regulators
- On-Card Switching Regulators
- Positive to Negative Converter (Buck-Boost)
- Negative Step-Up Converters
- Power Supply for Battery Chargers



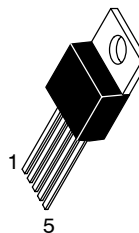
ON Semiconductor®

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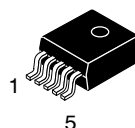
**TO-220
TV SUFFIX
CASE 314B**

Heatsink surface connected to Pin 3



**TO-220
T SUFFIX
CASE 314D**

- Pin
1. V_{in}
 2. Output
 3. Ground
 4. Feedback
 5. ON/OFF



**D2PAK
D2T SUFFIX
CASE 936A**

Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 181 of this data sheet.

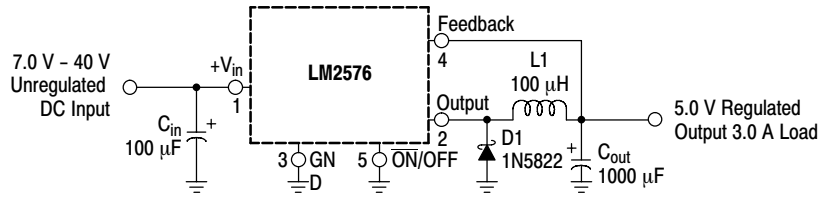
DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 181 of this data sheet.

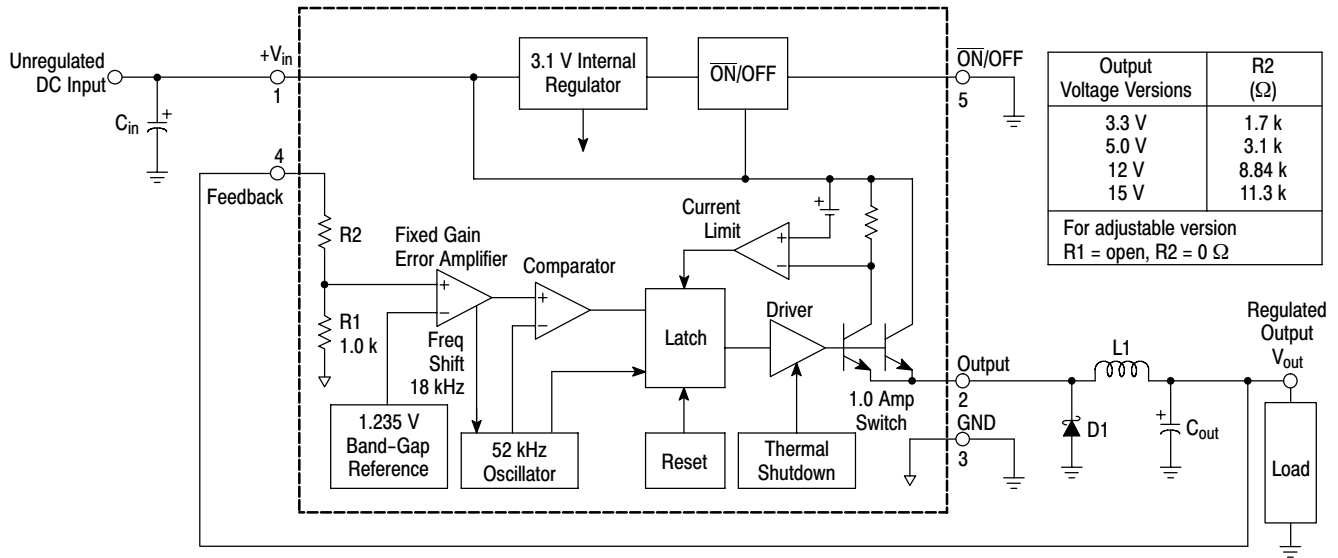
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

LM2576

Typical Application (Fixed Output Voltage Versions)



Representative Block Diagram and Typical Application



This device contains 162 active transistors.

Figure 1. Block Diagram and Typical Application

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Maximum Supply Voltage	V_{in}	45	V
ON/OFF Pin Input Voltage	–	$-0.3 \text{ V} \leq V \leq +V_{in}$	V
Output Voltage to Ground (Steady-State)	–	-1.0	V
Power Dissipation			
Case 314B and 314D (TO-220, 5-Lead)	P_D	Internally Limited	W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	65	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	5.0	°C/W
Case 936A (D ² PAK)	P_D	Internally Limited	W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	70	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	5.0	°C/W
Storage Temperature Range	T_{stg}	-65 to +150	°C
Minimum ESD Rating (Human Body Model: C = 100 pF, R = 1.5 kΩ)	–	2.0	kV
Lead Temperature (Soldering, 10 seconds)	–	260	°C
Maximum Junction Temperature	T_J	150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

LM2576

OPERATING RATINGS (Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	-40 to +125	°C
Supply Voltage	V_{in}	40	V

SYSTEM PARAMETERS (Note 1 Test Circuit Figure 15)

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $V_{in} = 12$ V for the 3.3 V, 5.0 V, and Adjustable version, $V_{in} = 25$ V for the 12 V version, and $V_{in} = 30$ V for the 15 V version. $I_{Load} = 500$ mA. For typical values $T_J = 25^\circ\text{C}$, for min/max values T_J is the operating junction temperature range that applies Note 2, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit

LM2576-3.3 (Note 1 Test Circuit Figure 15)

Output Voltage ($V_{in} = 12$ V, $I_{Load} = 0.5$ A, $T_J = 25^\circ\text{C}$)	V_{out}	3.234	3.3	3.366	V
Output Voltage (6.0 V $\leq V_{in} \leq 40$ V, 0.5 A $\leq I_{Load} \leq 3.0$ A) $T_J = 25^\circ\text{C}$ $T_J = -40$ to $+125^\circ\text{C}$	V_{out}	3.168 3.135	3.3 –	3.432 3.465	V
Efficiency ($V_{in} = 12$ V, $I_{Load} = 3.0$ A)	η	–	75	–	%

LM2576-5 (Note 1 Test Circuit Figure 15)

Output Voltage ($V_{in} = 12$ V, $I_{Load} = 0.5$ A, $T_J = 25^\circ\text{C}$)	V_{out}	4.9	5.0	5.1	V
Output Voltage (8.0 V $\leq V_{in} \leq 40$ V, 0.5 A $\leq I_{Load} \leq 3.0$ A) $T_J = 25^\circ\text{C}$ $T_J = -40$ to $+125^\circ\text{C}$	V_{out}	4.8 4.75	5.0 –	5.2 5.25	V
Efficiency ($V_{in} = 12$ V, $I_{Load} = 3.0$ A)	η	–	77	–	%

LM2576-12 (Note 1 Test Circuit Figure 15)

Output Voltage ($V_{in} = 25$ V, $I_{Load} = 0.5$ A, $T_J = 25^\circ\text{C}$)	V_{out}	11.76	12	12.24	V
Output Voltage (15 V $\leq V_{in} \leq 40$ V, 0.5 A $\leq I_{Load} \leq 3.0$ A) $T_J = 25^\circ\text{C}$ $T_J = -40$ to $+125^\circ\text{C}$	V_{out}	11.52 11.4	12 –	12.48 12.6	V
Efficiency ($V_{in} = 15$ V, $I_{Load} = 3.0$ A)	η	–	88	–	%

LM2576-15 (Note 1 Test Circuit Figure 15)

Output Voltage ($V_{in} = 30$ V, $I_{Load} = 0.5$ A, $T_J = 25^\circ\text{C}$)	V_{out}	14.7	15	15.3	V
Output Voltage (18 V $\leq V_{in} \leq 40$ V, 0.5 A $\leq I_{Load} \leq 3.0$ A) $T_J = 25^\circ\text{C}$ $T_J = -40$ to $+125^\circ\text{C}$	V_{out}	14.4 14.25	15 –	15.6 15.75	V
Efficiency ($V_{in} = 18$ V, $I_{Load} = 3.0$ A)	η	–	88	–	%

LM2576 ADJUSTABLE VERSION (Note 1 Test Circuit Figure 15)

Feedback Voltage ($V_{in} = 12$ V, $I_{Load} = 0.5$ A, $V_{out} = 5.0$ V, $T_J = 25^\circ\text{C}$)	V_{out}	1.217	1.23	1.243	V
Feedback Voltage (8.0 V $\leq V_{in} \leq 40$ V, 0.5 A $\leq I_{Load} \leq 3.0$ A, $V_{out} = 5.0$ V) $T_J = 25^\circ\text{C}$ $T_J = -40$ to $+125^\circ\text{C}$	V_{out}	1.193 1.18	1.23 –	1.267 1.28	V
Efficiency ($V_{in} = 12$ V, $I_{Load} = 3.0$ A, $V_{out} = 5.0$ V)	η	–	77	–	%

- External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2576 is used as shown in the Figure 15 test circuit, system performance will be as shown in system parameters section.
- Tested junction temperature range for the LM2576: $T_{low} = -40^\circ\text{C}$ $T_{high} = +125^\circ\text{C}$

DEVICE PARAMETERS

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $V_{in} = 12\text{ V}$ for the 3.3 V, 5.0 V, and Adjustable version, $V_{in} = 25\text{ V}$ for the 12 V version, and $V_{in} = 30\text{ V}$ for the 15 V version. $I_{Load} = 500\text{ mA}$. For typical values $T_J = 25^\circ\text{C}$, for min/max values T_J is the operating junction temperature range that applies [Note 2], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
ALL OUTPUT VOLTAGE VERSIONS					
Feedback Bias Current ($V_{out} = 5.0\text{ V}$ Adjustable Version Only) $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	I_b	– –	25 –	100 200	nA
Oscillator Frequency Note 3 $T_J = 25^\circ\text{C}$ $T_J = 0\text{ to }+125^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	f_{osc}	– 47 42	52 – –	– 58 63	kHz
Saturation Voltage ($I_{out} = 3.0\text{ A}$ Note 4) $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	V_{sat}	– –	1.5 –	1.8 2.0	V
Max Duty Cycle ("on") Note 5	DC	94	98	–	%
Current Limit (Peak Current Notes 3 and 4) $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	I_{CL}	4.2 3.5	5.8 –	6.9 7.5	A
Output Leakage Current Notes 6 and 7, $T_J = 25^\circ\text{C}$ Output = 0 V Output = –1.0 V	I_L	– –	0.8 6.0	2.0 20	mA
Quiescent Current Note 6 $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	I_Q	– –	5.0 –	9.0 11	mA
Standby Quiescent Current ($\overline{\text{ON}}/\text{OFF}$ Pin = 5.0 V ("off")) $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	I_{stby}	– –	80 –	200 400	μA
$\overline{\text{ON}}/\text{OFF}$ Pin Logic Input Level (Test Circuit Figure 15) $V_{out} = 0\text{ V}$ $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$ $V_{out} = \text{Nominal Output Voltage}$ $T_J = 25^\circ\text{C}$ $T_J = -40\text{ to }+125^\circ\text{C}$	V_{IH} V_{IL}	2.2 2.4 – –	1.4 – 1.2 –	– – 1.0 0.8	V
$\overline{\text{ON}}/\text{OFF}$ Pin Input Current (Test Circuit Figure 15) $\overline{\text{ON}}/\text{OFF}$ Pin = 5.0 V ("off"), $T_J = 25^\circ\text{C}$ $\overline{\text{ON}}/\text{OFF}$ Pin = 0 V ("on"), $T_J = 25^\circ\text{C}$	I_{IH} I_{IL}	– –	15 0	30 5.0	μA

- The oscillator frequency reduces to approximately 18 kHz in the event of an output short or an overload which causes the regulated output voltage to drop approximately 40% from the nominal output voltage. This self protection feature lowers the average dissipation of the IC by lowering the minimum duty cycle from 5% down to approximately 2%.
- Output (Pin 2) sourcing current. No diode, inductor or capacitor connected to output pin.
- Feedback (Pin 4) removed from output and connected to 0 V.
- Feedback (Pin 4) removed from output and connected to +12 V for the Adjustable, 3.3 V, and 5.0 V versions, and +25 V for the 12 V and 15 V versions, to force the output transistor "off".
- $V_{in} = 40\text{ V}$.

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 15)

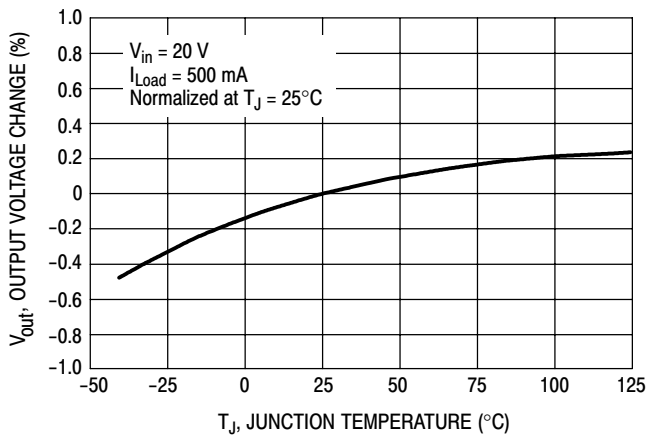


Figure 2. Normalized Output Voltage

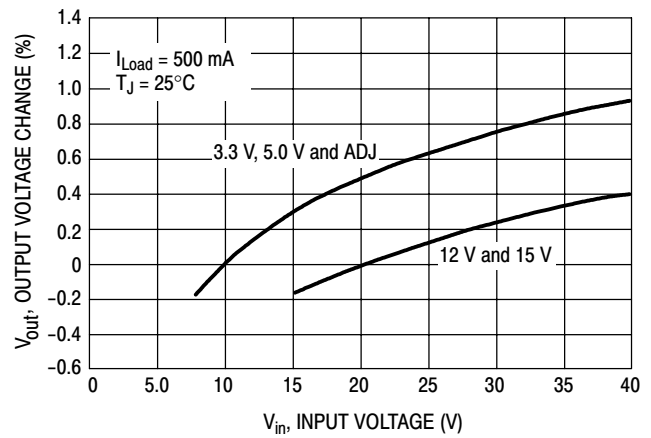


Figure 3. Line Regulation

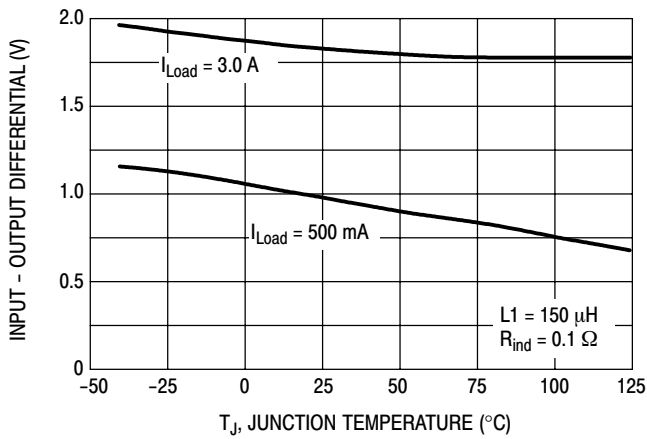


Figure 4. Dropout Voltage

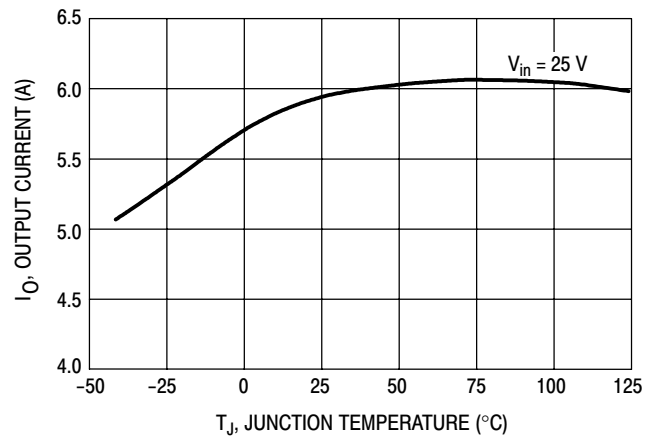


Figure 5. Current Limit

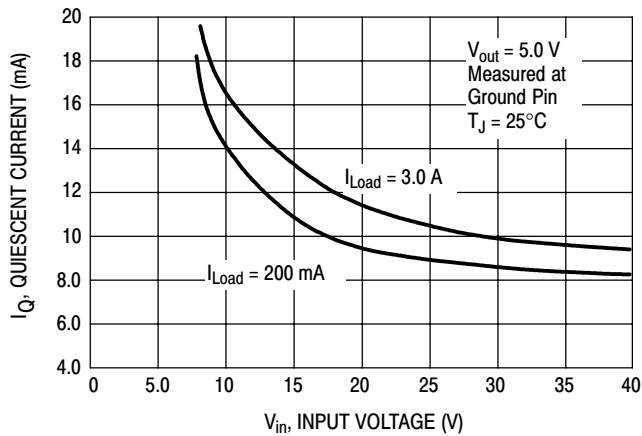


Figure 6. Quiescent Current

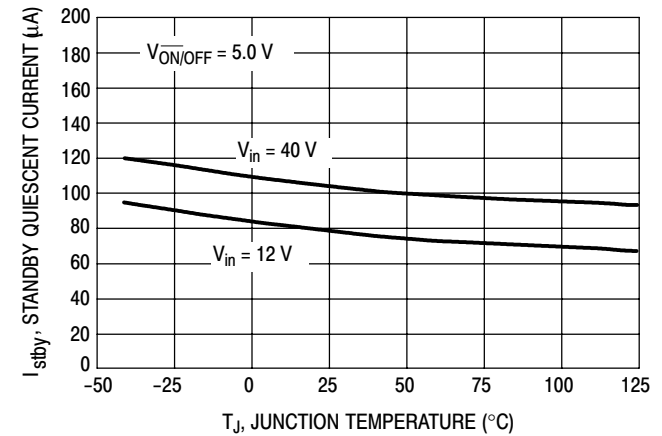


Figure 7. Standby Quiescent Current

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 15)

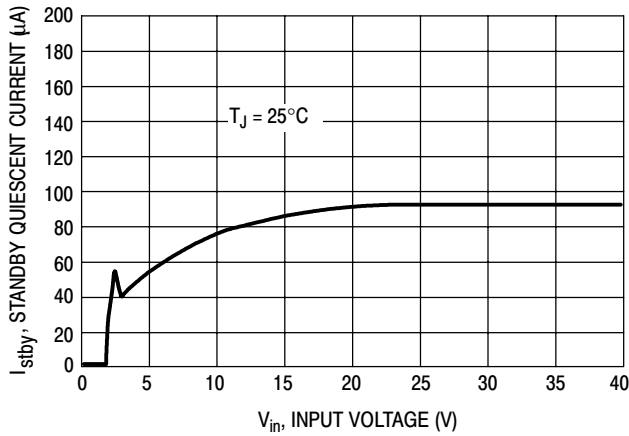


Figure 8. Standby Quiescent Current

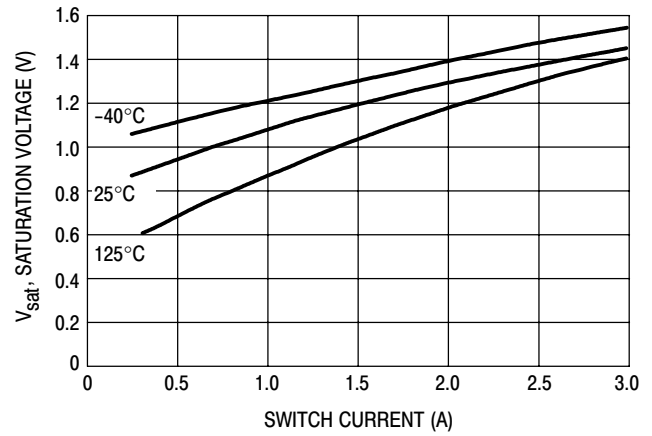


Figure 9. Switch Saturation Voltage

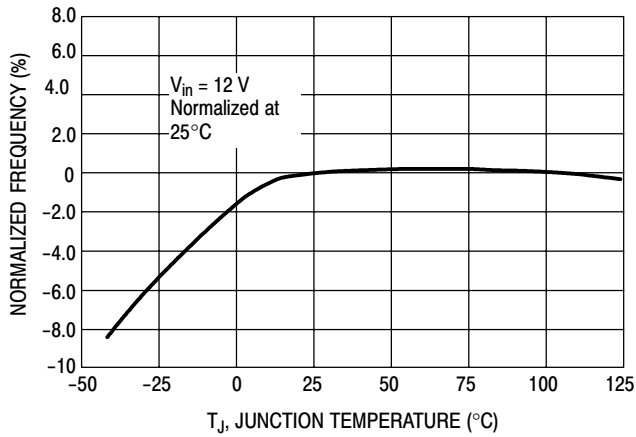


Figure 10. Oscillator Frequency

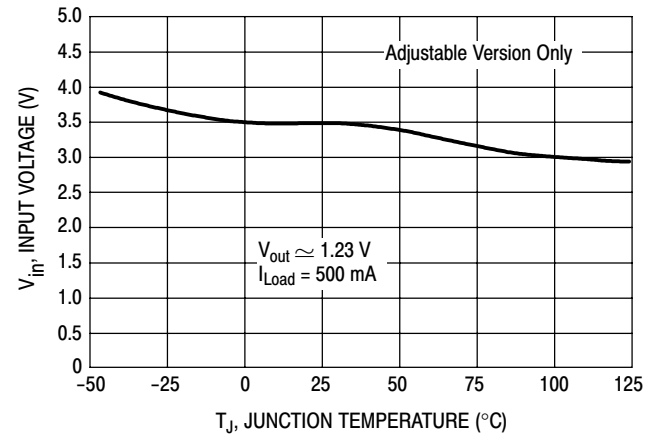


Figure 11. Minimum Operating Voltage

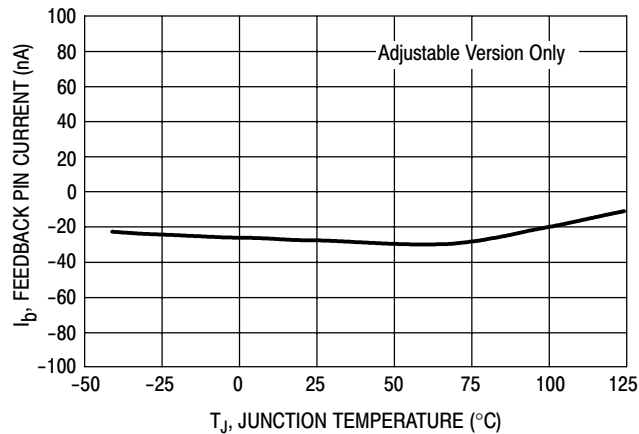


Figure 12. Feedback Pin Current

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 15)

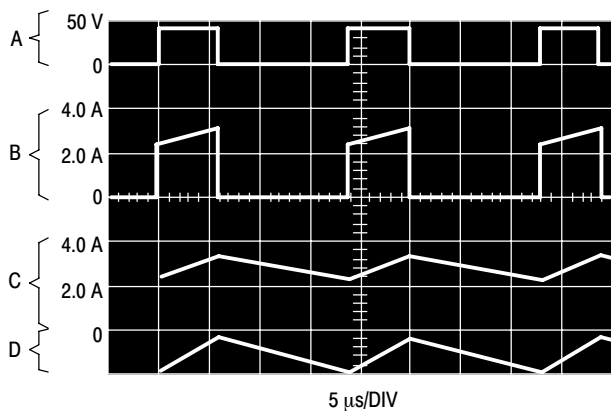


Figure 13. Switching Waveforms

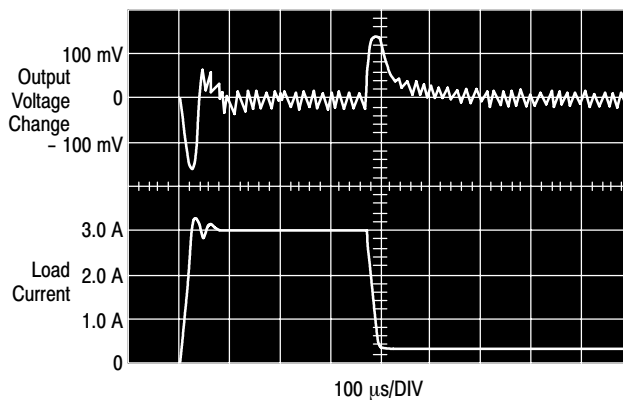


Figure 14. Load Transient Response

Vout = 15 V

A: Output Pin Voltage, 10 V/DIV

B: Inductor Current, 2.0 A/DIV

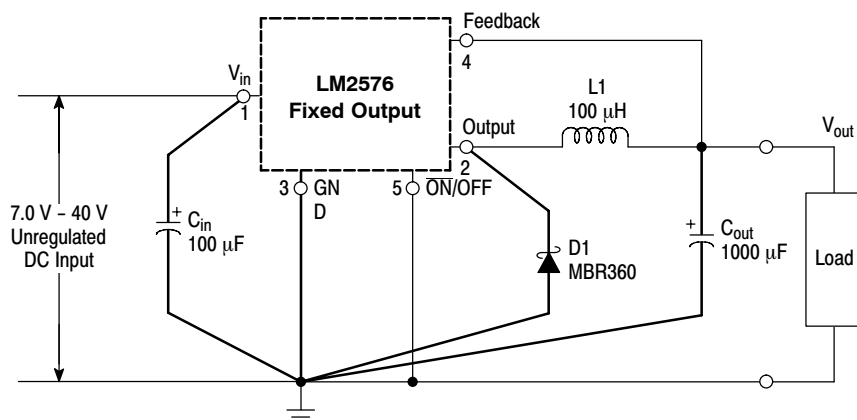
C: Inductor Current, 2.0 A/DIV, AC-Coupled

D: Output Ripple Voltage, 50 mV/dDIV, AC-Coupled

Horizontal Time Base: 5.0 μ s/DIV

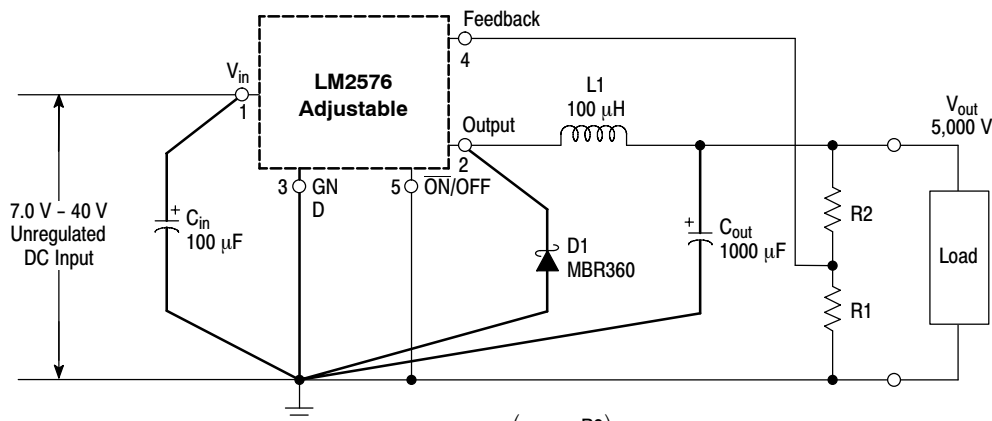
LM2576

Fixed Output Voltage Versions



- C_{in} - 100 μ F, 75 V, Aluminium Electrolytic
- C_{out} - 1000 μ F, 25 V, Aluminium Electrolytic
- D1 - Schottky, MBR360
- L1 - 100 μ H, Pulse Eng. PE-92108
- R1 - 2.0 k, 0.1%
- R2 - 6.12 k, 0.1%

Adjustable Output Voltage Versions



$$V_{out} = V_{ref} \left(1.0 + \frac{R2}{R1} \right)$$

$$R2 = R1 \left(\frac{V_{out}}{V_{ref}} - 1.0 \right)$$

Where $V_{ref} = 1.23$ V, $R1$
between 1.0 k and 5.0 k

Figure 15. Typical Test Circuit

PCB LAYOUT GUIDELINES

As in any switching regulator, the layout of the printed circuit board is very important. Rapidly switching currents associated with wiring inductance, stray capacitance and parasitic inductance of the printed circuit board traces can generate voltage transients which can generate electromagnetic interferences (EMI) and affect the desired operation. As indicated in the Figure 15, to minimize inductance and ground loops, the length of the leads indicated by heavy lines should be kept as short as possible.

For best results, single-point grounding (as indicated) or ground plane construction should be used.

On the other hand, the PCB area connected to the Pin 2 (emitter of the internal switch) of the LM2576 should be kept to a minimum in order to minimize coupling to sensitive circuitry.

Another sensitive part of the circuit is the feedback. It is important to keep the sensitive feedback wiring short. To assure this, physically locate the programming resistors near to the regulator, when using the adjustable version of the LM2576 regulator.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description (Refer to Figure 1)
1	V_{in}	This pin is the positive input supply for the LM2576 step-down switching regulator. In order to minimize voltage transients and to supply the switching currents needed by the regulator, a suitable input bypass capacitor must be present (C_{in} in Figure 1).
2	Output	This is the emitter of the internal switch. The saturation voltage V_{sat} of this output switch is typically 1.5 V. It should be kept in mind that the PCB area connected to this pin should be kept to a minimum in order to minimize coupling to sensitive circuitry.
3	GND	Circuit ground pin. See the information about the printed circuit board layout.
4	Feedback	This pin senses regulated output voltage to complete the feedback loop. The signal is divided by the internal resistor divider network R2, R1 and applied to the non-inverting input of the internal error amplifier. In the Adjustable version of the LM2576 switching regulator this pin is the direct input of the error amplifier and the resistor network R2, R1 is connected externally to allow programming of the output voltage.
5	$\overline{ON/OFF}$	It allows the switching regulator circuit to be shut down using logic level signals, thus dropping the total input supply current to approximately 80 μA . The threshold voltage is typically 1.4 V. Applying a voltage above this value (up to $+V_{in}$) shuts the regulator off. If the voltage applied to this pin is lower than 1.4 V or if this pin is left open, the regulator will be in the "on" condition.

DESIGN PROCEDURE

Buck Converter Basics

The LM2576 is a "Buck" or Step-Down Converter which is the most elementary forward-mode converter. Its basic schematic can be seen in Figure 16.

The operation of this regulator topology has two distinct time periods. The first one occurs when the series switch is on, the input voltage is connected to the input of the inductor.

The output of the inductor is the output voltage, and the rectifier (or catch diode) is reverse biased. During this period, since there is a constant voltage source connected across the inductor, the inductor current begins to linearly ramp upwards, as described by the following equation:

$$I_{L(on)} = \frac{(V_{in} - V_{out}) t_{on}}{L}$$

During this "on" period, energy is stored within the core material in the form of magnetic flux. If the inductor is properly designed, there is sufficient energy stored to carry the requirements of the load during the "off" period.

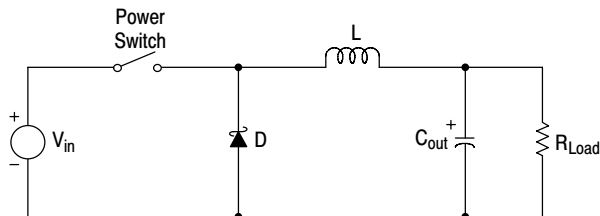


Figure 16. Basic Buck Converter

The next period is the "off" period of the power switch. When the power switch turns off, the voltage across the inductor reverses its polarity and is clamped at one diode voltage drop below ground by the catch diode. The current now flows through the catch diode thus maintaining the load current loop. This removes the stored energy from the inductor. The inductor current during this time is:

$$I_{L(off)} = \frac{(V_{out} - V_D) t_{off}}{L}$$

This period ends when the power switch is once again turned on. Regulation of the converter is accomplished by varying the duty cycle of the power switch. It is possible to describe the duty cycle as follows:

$$d = \frac{t_{on}}{T}, \text{ where } T \text{ is the period of switching.}$$

For the buck converter with ideal components, the duty cycle can also be described as:

$$d = \frac{V_{out}}{V_{in}}$$

Figure 17 shows the buck converter, idealized waveforms of the catch diode voltage and the inductor current.

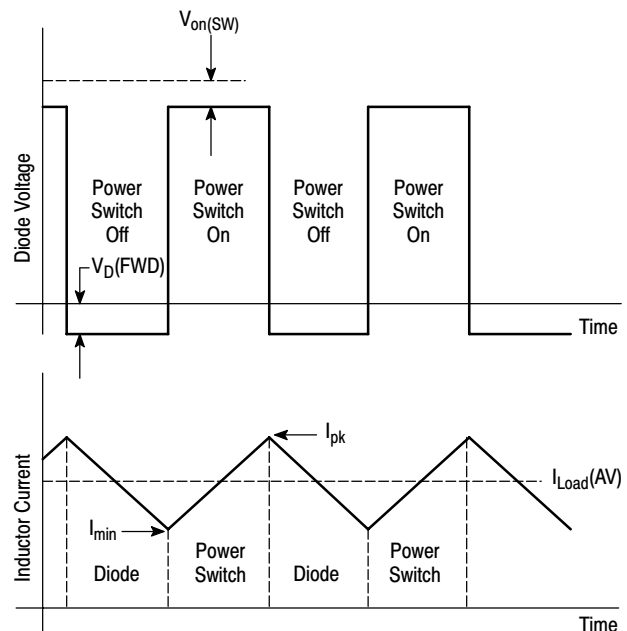


Figure 17. Buck Converter Idealized Waveforms

Procedure (Fixed Output Voltage Version) In order to simplify the switching regulator design, a step-by-step design procedure and some examples are provided.

Procedure	Example
Given Parameters: V_{out} = Regulated Output Voltage (3.3 V, 5.0 V, 12 V or 15 V) $V_{in(max)}$ = Maximum Input Voltage $I_{Load(max)}$ = Maximum Load Current	Given Parameters: V_{out} = 5.0 V $V_{in(max)}$ = 15 V $I_{Load(max)}$ = 3.0 A
1. Controller IC Selection According to the required input voltage, output voltage and current, select the appropriate type of the controller IC output voltage version.	1. Controller IC Selection According to the required input voltage, output voltage, current polarity and current value, use the LM2576-5 controller IC
2. Input Capacitor Selection (C_{in}) To prevent large voltage transients from appearing at the input and for stable operation of the converter, an aluminium or tantalum electrolytic bypass capacitor is needed between the input pin + V_{in} and ground pin GND. This capacitor should be located close to the IC using short leads. This capacitor should have a low ESR (Equivalent Series Resistance) value.	2. Input Capacitor Selection (C_{in}) A 100 μ F, 25 V aluminium electrolytic capacitor located near to the input and ground pins provides sufficient bypassing.
3. Catch Diode Selection (D1) A. Since the diode maximum peak current exceeds the regulator maximum load current the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design the diode should have a current rating equal to the maximum current limit of the LM2576 to be able to withstand a continuous output short B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.	3. Catch Diode Selection (D1) A. For this example the current rating of the diode is 3.0 A. B. Use a 20 V 1N5820 Schottky diode, or any of the suggested fast recovery diodes shown in Table 1.
4. Inductor Selection (L1) A. According to the required working conditions, select the correct inductor value using the selection guide from Figures 18 to 22. B. From the appropriate inductor selection guide, identify the inductance region intersected by the Maximum Input Voltage line and the Maximum Load Current line. Each region is identified by an inductance value and an inductor code. C. Select an appropriate inductor from the several different manufacturers part numbers listed in Table 2. The designer must realize that the inductor current rating must be higher than the maximum peak current flowing through the inductor. This maximum peak current can be calculated as follows: $I_{p(max)} = I_{Load(max)} + \frac{(V_{in} - V_{out}) t_{on}}{2L}$ where t_{on} is the "on" time of the power switch and $t_{on} = \frac{V_{out}}{V_{in}} \times \frac{1.0}{f_{osc}}$ For additional information about the inductor, see the inductor section in the "Application Hints" section of this data sheet.	4. Inductor Selection (L1) A. Use the inductor selection guide shown in Figures 19. B. From the selection guide, the inductance area intersected by the 15 V line and 3.0 A line is L100. C. Inductor value required is 100 μ H. From Table 2, choose an inductor from any of the listed manufacturers.

Procedure (Fixed Output Voltage Version) (continued) In order to simplify the switching regulator design, a step-by-step design procedure and some examples are provided.

Procedure	Example
5. Output Capacitor Selection (C_{out}) A. Since the LM2576 is a forward-mode switching regulator with voltage mode control, its open loop 2-pole-1-zero frequency characteristic has the dominant pole-pair determined by the output capacitor and inductor values. For stable operation and an acceptable ripple voltage, (approximately 1% of the output voltage) a value between 680 μ F and 2000 μ F is recommended. B. Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating at least 8.0 V is appropriate, and a 10 V or 16 V rating is recommended.	5. Output Capacitor Selection (C_{out}) A. $C_{out} = 680 \mu\text{F}$ to 2000 μF standard aluminium electrolytic. B. Capacitor voltage rating = 20 V.

Procedure (Adjustable Output Version: LM2576-ADJ)

Procedure	Example
Given Parameters: V_{out} = Regulated Output Voltage $V_{in(max)}$ = Maximum DC Input Voltage $I_{Load(max)}$ = Maximum Load Current	Given Parameters: $V_{out} = 8.0 \text{ V}$ $V_{in(max)} = 25 \text{ V}$ $I_{Load(max)} = 2.5 \text{ A}$
1. Programming Output Voltage To select the right programming resistor R1 and R2 value (see Figure 2) use the following formula: $V_{out} = V_{ref} \left(1.0 + \frac{R2}{R1} \right) \quad \text{where } V_{ref} = 1.23 \text{ V}$ Resistor R1 can be between 1.0 k and 5.0 k Ω . (For best temperature coefficient and stability with time, use 1% metal film resistors). $R2 = R1 \left(\frac{V_{out}}{V_{ref}} - 1.0 \right)$	1. Programming Output Voltage (selecting R1 and R2) Select R1 and R2: $V_{out} = 1.23 \left(1.0 + \frac{R2}{R1} \right) \quad \text{Select } R1 = 1.8 \text{ k}\Omega$ $R2 = R1 \left(\frac{V_{out}}{V_{ref}} - 1.0 \right) = 1.8 \text{ k} \left(\frac{8.0 \text{ V}}{1.23 \text{ V}} - 1.0 \right)$ $R2 = 9.91 \text{ k}\Omega, \text{ choose a } 9.88 \text{ k metal film resistor.}$
2. Input Capacitor Selection (C_{in}) To prevent large voltage transients from appearing at the input and for stable operation of the converter, an aluminium or tantalum electrolytic bypass capacitor is needed between the input pin + V_{in} and ground pin GND. This capacitor should be located close to the IC using short leads. This capacitor should have a low ESR (Equivalent Series Resistance) value. For additional information see input capacitor section in the "Application Hints" section of this data sheet.	2. Input Capacitor Selection (C_{in}) A 100 μ F, 150 V aluminium electrolytic capacitor located near the input and ground pin provides sufficient bypassing.
3. Catch Diode Selection (D1) A. Since the diode maximum peak current exceeds the regulator maximum load current the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design, the diode should have a current rating equal to the maximum current limit of the LM2576 to be able to withstand a continuous output short. B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.	3. Catch Diode Selection (D1) A. For this example, a 3.0 A current rating is adequate. B. Use a 30 V 1N5821 Schottky diode or any suggested fast recovery diode in the Table 1.

Procedure (Adjustable Output Version: LM2576–ADJ) (continued)

Procedure	Example
4. Inductor Selection (L1) A. Use the following formula to calculate the inductor Volt x microsecond [V x μs] constant: $E \times T = (V_{in} - V_{out}) \frac{V_{out}}{V_{in}} \times \frac{10^6}{F[\text{Hz}]} \text{ [V x } \mu\text{s]}$ B. Match the calculated E x T value with the corresponding number on the vertical axis of the Inductor Value Selection Guide shown in Figure 22. This E x T constant is a measure of the energy handling capability of an inductor and is dependent upon the type of core, the core area, the number of turns, and the duty cycle. C. Next step is to identify the inductance region intersected by the E x T value and the maximum load current value on the horizontal axis shown in Figure 25. D. From the inductor code, identify the inductor value. Then select an appropriate inductor from Table 2. The inductor chosen must be rated for a switching frequency of 52 kHz and for a current rating of $1.15 \times I_{Load}$. The inductor current rating can also be determined by calculating the inductor peak current: $I_{p(max)} = I_{Load(max)} + \frac{(V_{in} - V_{out}) t_{on}}{2L}$ where t_{on} is the “on” time of the power switch and $t_{on} = \frac{V_{out}}{V_{in}} \times \frac{1.0}{f_{osc}}$ For additional information about the inductor, see the inductor section in the “External Components” section of this data sheet.	4. Inductor Selection (L1) A. Calculate E x T [V x μs] constant: $E \times T = (25 - 8.0) \times \frac{8.0}{25} \times \frac{1000}{52} = 80 \text{ [V x } \mu\text{s]}$ B. E x T = 80 [V x μs] C. $I_{Load(max)} = 2.5 \text{ A}$ Inductance Region = H150 D. Proper inductor value = 150 μH Choose the inductor from Table 2.
5. Output Capacitor Selection (C_{out}) A. Since the LM2576 is a forward-mode switching regulator with voltage mode control, its open loop 2-pole-1-zero frequency characteristic has the dominant pole-pair determined by the output capacitor and inductor values. For stable operation, the capacitor must satisfy the following requirement: $C_{out} \geq 13,300 \frac{V_{in(max)}}{V_{out} \times L [\mu\text{H}]} \text{ } [\mu\text{F}]$ B. Capacitor values between 10 μF and 2000 μF will satisfy the loop requirements for stable operation. To achieve an acceptable output ripple voltage and transient response, the output capacitor may need to be several times larger than the above formula yields. C. Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating of at least 8.0 V is appropriate, and a 10 V or 16 V rating is recommended.	5. Output Capacitor Selection (C_{out}) A. $C_{out} \geq 13,300 \times \frac{25}{8 \times 150} = 332.5 \mu\text{F}$ To achieve an acceptable ripple voltage, select $C_{out} = 680 \mu\text{F}$ electrolytic capacitor.

LM2576

LM2576 Series Buck Regulator Design Procedures (continued)

Indicator Value Selection Guide (For Continuous Mode Operation)

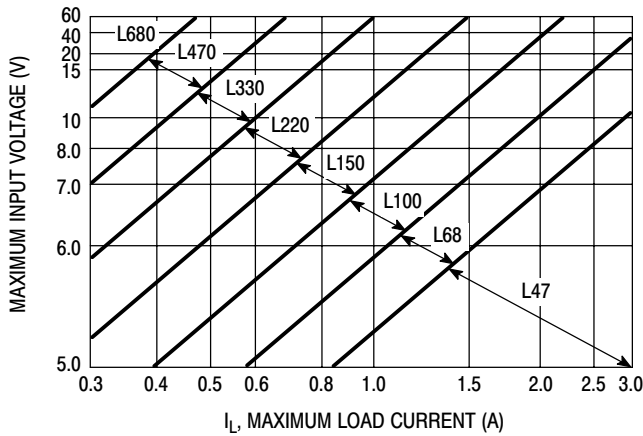


Figure 18. LM2576-3.3

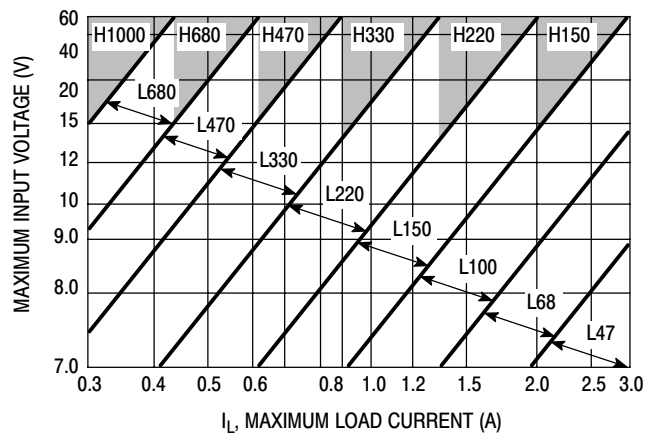


Figure 19. LM2576-5

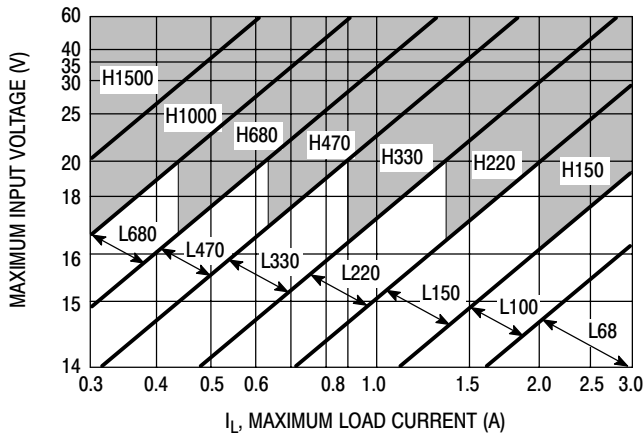


Figure 20. LM2576-12

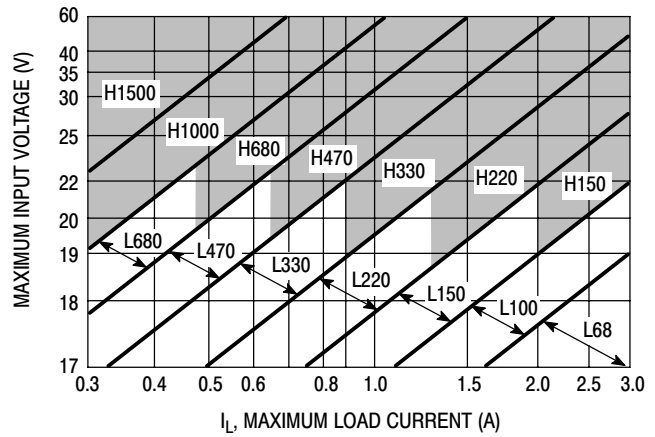


Figure 21. LM2576-15

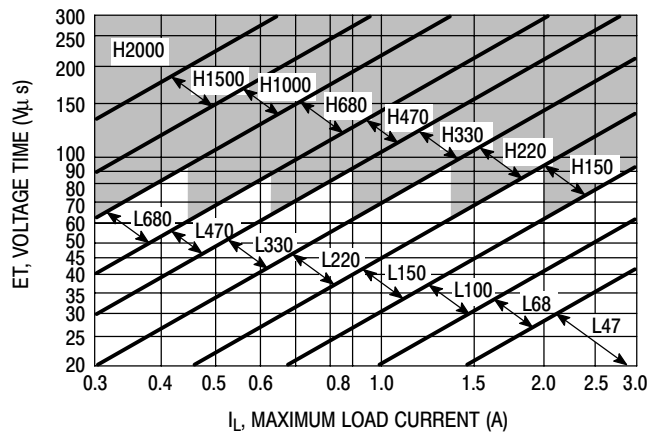


Figure 22. LM2576-ADJ

Table 1. Diode Selection Guide

V _R	Schottky				Fast Recovery			
	3.0 A		4.0 – 6.0 A		3.0 A		4.0 – 6.0 A	
	Through Hole	Surface Mount	Through Hole	Surface Mount	Through Hole	Surface Mount	Through Hole	Surface Mount
20 V	1N5820 MBR320P SR302	SK32	1N5823 SR502 SB520		MUR320 31DF1 HER302 (all diodes rated to at least 100 V)	MURS320T3 MURD320 30WF10 (all diodes rated to at least 100 V)	MUR420 HER602 (all diodes rated to at least 100 V)	MURD620CT 50WF10 (all diodes rated to at least 100 V)
30 V	1N5821 MBR330 SR303 31DQ03	SK33 30WQ03	1N5824 SR503 SB530	50WQ03				
40 V	1N5822 MBR340 SR304 31DQ04	SK34 30WQ04 MBRS340T3 MBRD340	1N5825 SR504 SB540	MBRD640CT 50WQ04				
50 V	MBR350 31DQ05 SR305	SK35 30WQ05	SB550	50WQ05				
60 V	MBR360 DQ06 SR306	MBRS360T3 MBRD360	50SQ080	MBRD660CT				

NOTE: Diodes listed in bold are available from ON Semiconductor.

Table 2. Inductor Selection by Manufacturer's Part Number

Inductor Code	Inductor Value	Tech 39	Schott Corp.	Pulse Eng.	Renco
L47	47 μ H	77 212	671 26980	PE-53112	RL2442
L68	68 μ H	77 262	671 26990	PE-92114	RL2443
L100	100 μ H	77 312	671 27000	PE-92108	RL2444
L150	150 μ H	77 360	671 27010	PE-53113	RL1954
L220	220 μ H	77 408	671 27020	PE-52626	RL1953
L330	330 μ H	77 456	671 27030	PE-52627	RL1952
L470	470 μ H	*	671 27040	PE-53114	RL1951
L680	680 μ H	77 506	671 27050	PE-52629	RL1950
H150	150 μ H	77 362	671 27060	PE-53115	RL2445
H220	220 μ H	77 412	671 27070	PE-53116	RL2446
H330	330 μ H	77 462	671 27080	PE-53117	RL2447
H470	470 μ H	*	671 27090	PE-53118	RL1961
H680	680 μ H	77 508	671 27100	PE-53119	RL1960
H1000	1000 μ H	77 556	671 27110	PE-53120	RL1959
H1500	1500 μ H	*	671 27120	PE-53121	RL1958
H2200	2200 μ H	*	671 27130	PE-53122	RL2448

NOTE: *Contact Manufacturer

Table 3. Example of Several Inductor Manufacturers Phone/Fax Numbers

Pulse Engineering, Inc.	Phone Fax	+ 1-619-674-8100 + 1-619-674-8262
Pulse Engineering, Inc. Europe	Phone Fax	+ 353-9324-107 + 353-9324-459
Renco Electronics, Inc.	Phone Fax	+ 1-516-645-5828 + 1-516-586-5562
Tech 39	Phone Fax	+ 33-1-4115-1681 + 33-1-4709-5051
Schott Corporation	Phone Fax	+ 1-612-475-1173 + 1-612-475-1786

EXTERNAL COMPONENTS

Input Capacitor (C_{in})

The Input Capacitor Should Have a Low ESR

For stable operation of the switch mode converter a low ESR (Equivalent Series Resistance) aluminium or solid tantalum bypass capacitor is needed between the input pin and the ground pin, to prevent large voltage transients from appearing at the input. It must be located near the regulator and use short leads. With most electrolytic capacitors, the capacitance value decreases and the ESR increases with lower temperatures. For reliable operation in temperatures below -25°C larger values of the input capacitor may be needed. Also paralleling a ceramic or solid tantalum capacitor will increase the regulator stability at cold temperatures.

RMS Current Rating of C_{in}

The important parameter of the input capacitor is the RMS current rating. Capacitors that are physically large and have large surface area will typically have higher RMS current ratings. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower voltage capacitor, and thus be able to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating. The consequence of operating an electrolytic capacitor beyond the RMS current rating is a shortened operating life. In order to assure maximum capacitor operating lifetime, the capacitor's RMS ripple current rating should be:

$$I_{rms} > 1.2 \times d \times I_{Load}$$

where d is the duty cycle, for a buck regulator

$$d = \frac{t_{on}}{T} = \frac{V_{out}}{V_{in}}$$

and $d = \frac{t_{on}}{T} = \frac{|V_{out}|}{|V_{out}| + V_{in}}$ for a buck-boost regulator.

Output Capacitor (C_{out})

For low output ripple voltage and good stability, low ESR output capacitors are recommended. An output capacitor has two main functions: it filters the output and provides regulator loop stability. The ESR of the output capacitor and the peak-to-peak value of the inductor ripple current are the main factors contributing to the output ripple voltage value. Standard aluminium electrolytics could be adequate for some applications but for quality design, low ESR types are recommended.

An aluminium electrolytic capacitor's ESR value is related to many factors such as the capacitance value, the voltage rating, the physical size and the type of construction. In most cases, the higher voltage electrolytic capacitors have lower ESR value. Often capacitors with much higher voltage ratings may be needed to provide low ESR values that, are required for low output ripple voltage.

The Output Capacitor Requires an ESR Value That Has an Upper and Lower Limit

As mentioned above, a low ESR value is needed for low output ripple voltage, typically 1% to 2% of the output voltage. But if the selected capacitor's ESR is extremely low (below 0.05Ω), there is a possibility of an unstable feedback loop, resulting in oscillation at the output. This situation can occur when a tantalum capacitor, that can have a very low ESR, is used as the only output capacitor.

At Low Temperatures, Put in Parallel Aluminium Electrolytic Capacitors with Tantalum Capacitors

Electrolytic capacitors are not recommended for temperatures below -25°C . The ESR rises dramatically at cold temperatures and typically rises 3 times at -25°C and as much as 10 times at -40°C . Solid tantalum capacitors have much better ESR spec at cold temperatures and are recommended for temperatures below -25°C . They can be also used in parallel with aluminium electrolytics. The value of the tantalum capacitor should be about 10% or 20% of the total capacitance. The output capacitor should have at least 50% higher RMS ripple current rating at 52 kHz than the peak-to-peak inductor ripple current.

Catch Diode

Locate the Catch Diode Close to the LM2576

The LM2576 is a step-down buck converter; it requires a fast diode to provide a return path for the inductor current when the switch turns off. This diode must be located close to the LM2576 using short leads and short printed circuit traces to avoid EMI problems.

Use a Schottky or a Soft Switching

Ultra-Fast Recovery Diode

Since the rectifier diodes are very significant sources of losses within switching power supplies, choosing the rectifier that best fits into the converter design is an important process. Schottky diodes provide the best performance because of their fast switching speed and low forward voltage drop.

They provide the best efficiency especially in low output voltage applications (5.0 V and lower). Another choice could be Fast-Recovery, or Ultra-Fast Recovery diodes. It has to be noted, that some types of these diodes with an abrupt turnoff characteristic may cause instability or EMI troubles.

A fast-recovery diode with soft recovery characteristics can better fulfill some quality, low noise design requirements. Table 1 provides a list of suitable diodes for the LM2576 regulator. Standard 50/60 Hz rectifier diodes, such as the 1N4001 series or 1N5400 series are **NOT** suitable.

Inductor

The magnetic components are the cornerstone of all switching power supply designs. The style of the core and the winding technique used in the magnetic component's design has a great influence on the reliability of the overall power supply.

Using an improper or poorly designed inductor can cause high voltage spikes generated by the rate of transitions in current within the switching power supply, and the possibility of core saturation can arise during an abnormal operational mode. Voltage spikes can cause the semiconductors to enter avalanche breakdown and the part can instantly fail if enough energy is applied. It can also cause significant RFI (Radio Frequency Interference) and EMI (Electro-Magnetic Interference) problems.

Continuous and Discontinuous Mode of Operation

The LM2576 step-down converter can operate in both the continuous and the discontinuous modes of operation. The regulator works in the continuous mode when loads are relatively heavy, the current flows through the inductor continuously and never falls to zero. Under light load conditions, the circuit will be forced to the discontinuous mode when inductor current falls to zero for certain period of time (see Figure 23 and Figure 24). Each mode has distinctively different operating characteristics, which can affect the regulator performance and requirements. In many cases the preferred mode of operation is the continuous mode. It offers greater output power, lower peak currents in the switch, inductor and diode, and can have a lower output

ripple voltage. On the other hand it does require larger inductor values to keep the inductor current flowing continuously, especially at low output load currents and/or high input voltages.

To simplify the inductor selection process, an inductor selection guide for the LM2576 regulator was added to this data sheet (Figures 18 through 22). This guide assumes that the regulator is operating in the continuous mode, and selects an inductor that will allow a peak-to-peak inductor ripple current to be a certain percentage of the maximum design load current. This percentage is allowed to change as different design load currents are selected. For light loads (less than approximately 300 mA) it may be desirable to operate the regulator in the discontinuous mode, because the inductor value and size can be kept relatively low. Consequently, the percentage of inductor peak-to-peak current increases. This discontinuous mode of operation is perfectly acceptable for this type of switching converter. Any buck regulator will be forced to enter discontinuous mode if the load current is light enough.

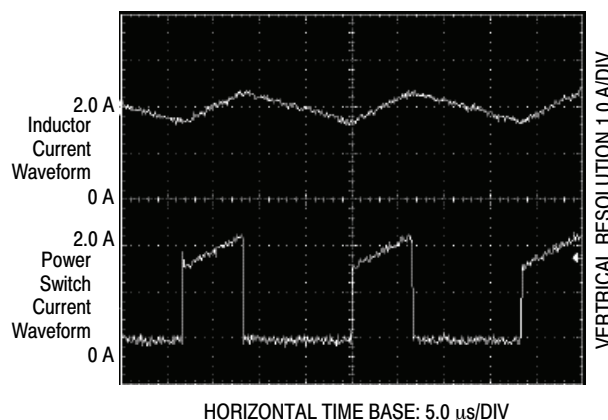


Figure 23. Continuous Mode Switching Current Waveforms

Selecting the Right Inductor Style

Some important considerations when selecting a core type are core material, cost, the output power of the power supply, the physical volume the inductor must fit within, and the amount of EMI (Electro-Magnetic Interference) shielding that the core must provide. The inductor selection guide covers different styles of inductors, such as pot core, E-core, toroid and bobbin core, as well as different core materials such as ferrites and powdered iron from different manufacturers.

For high quality design regulators the toroid core seems to be the best choice. Since the magnetic flux is contained within the core, it generates less EMI, reducing noise problems in sensitive circuits. The least expensive is the bobbin core type, which consists of wire wound on a ferrite rod core. This type of inductor generates more EMI due to the fact that its core is open, and the magnetic flux is not contained within the core.

When multiple switching regulators are located on the same printed circuit board, open core magnetics can cause interference between two or more of the regulator circuits, especially at high currents due to mutual coupling. A toroid, pot core or E-core (closed magnetic structure) should be used in such applications.

Do Not Operate an Inductor Beyond its Maximum Rated Current

Exceeding an inductor's maximum current rating may cause the inductor to overheat because of the copper wire losses, or the core may saturate. Core saturation occurs when the flux density is too high and consequently the cross sectional area of the core can no longer support additional lines of magnetic flux.

This causes the permeability of the core to drop, the inductance value decreases rapidly and the inductor begins to look mainly resistive. It has only the DC resistance of the winding. This can cause the switch current to rise very rapidly and force the LM2576 internal switch into cycle-by-cycle current limit, thus reducing the DC output load current. This can also result in overheating of the

inductor and/or the LM2576. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.

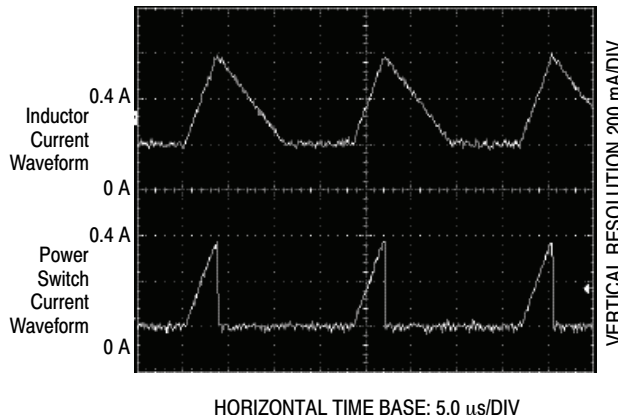


Figure 24. Discontinuous Mode Switching Current Waveforms

GENERAL RECOMMENDATIONS

Output Voltage Ripple and Transients **Source of the Output Ripple**

Since the LM2576 is a switch mode power supply regulator, its output voltage, if left unfiltered, will contain a sawtooth ripple voltage at the switching frequency. The output ripple voltage value ranges from 0.5% to 3% of the output voltage. It is caused mainly by the inductor sawtooth ripple current multiplied by the ESR of the output capacitor.

Short Voltage Spikes and How to Reduce Them

The regulator output voltage may also contain short voltage spikes at the peaks of the sawtooth waveform (see Figure 25). These voltage spikes are present because of the fast switching action of the output switch, and the parasitic inductance of the output filter capacitor. There are some other important factors such as wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all these contribute to the amplitude of these spikes. To minimize these voltage spikes, low inductance capacitors should be used, and their lead lengths must be kept short. The importance of quality printed circuit board layout design should also be highlighted.

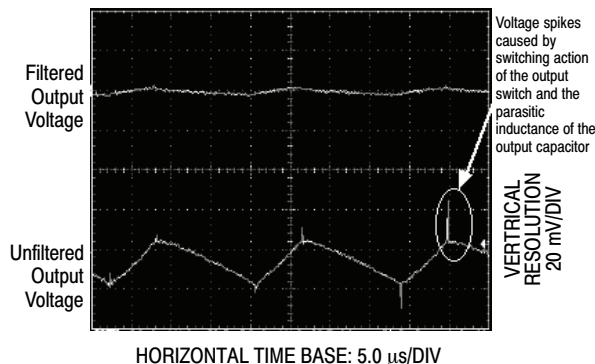


Figure 25. Output Ripple Voltage Waveforms

Minimizing the Output Ripple

In order to minimize the output ripple voltage it is possible to enlarge the inductance value of the inductor L1 and/or to use a larger value output capacitor. There is also another way to smooth the output by means of an additional LC filter (20 μ H, 100 μ F), that can be added to the output (see Figure 34) to further reduce the amount of output ripple and transients. With such a filter it is possible to reduce the output ripple voltage transients 10 times or more. Figure 25 shows the difference between filtered and unfiltered output waveforms of the regulator shown in Figure 34.

The lower waveform is from the normal unfiltered output of the converter, while the upper waveform shows the output ripple voltage filtered by an additional LC filter.

Heatsinking and Thermal Considerations **The Through-Hole Package TO-220**

The LM2576 is available in two packages, a 5-pin TO-220(T, TV) and a 5-pin surface mount D²PAK(D2T). Although the TO-220(T) package needs a heatsink under most conditions, there are some applications that require no heatsink to keep the LM2576 junction temperature within the allowed operating range. Higher ambient temperatures require some heat sinking, either to the printed circuit (PC) board or an external heatsink.

The Surface Mount Package D²PAK and its Heatsinking

The other type of package, the surface mount D²PAK, is designed to be soldered to the copper on the PC board. The copper and the board are the heatsink for this package and the other heat producing components, such as the catch diode and inductor. The PC board copper area that the package is soldered to should be at least 0.4 in² (or 260 mm²) and ideally should have 2 or more square inches (1300 mm²) of 0.0028 inch copper. Additional increases of copper area

beyond approximately 6.0 in² (4000 mm²) will not improve heat dissipation significantly. If further thermal improvements are needed, double sided or multilayer PC boards with large copper areas should be considered. In order to achieve the best thermal performance, it is highly recommended to use wide copper traces as well as large areas of copper in the printed circuit board layout. The only exception to this is the OUTPUT (switch) pin, which should not have large areas of copper (see page 165 'PCB Layout Guideline').

Thermal Analysis and Design

The following procedure must be performed to determine whether or not a heatsink will be required. First determine:

1. $P_{D(max)}$ maximum regulator power dissipation in the application.
2. $T_{A(max)}$ maximum ambient temperature in the application.
3. $T_{J(max)}$ maximum allowed junction temperature (125°C for the LM2576). For a conservative design, the maximum junction temperature should not exceed 110°C to assure safe operation. For every additional +10°C temperature rise that the junction must withstand, the estimated operating lifetime of the component is halved.
4. $R_{\theta JC}$ package thermal resistance junction–case.
5. $R_{\theta JA}$ package thermal resistance junction–ambient.

(Refer to Maximum Ratings on page 159 of this data sheet or $R_{\theta JC}$ and $R_{\theta JA}$ values).

The following formula is to calculate the approximate total power dissipated by the LM2576:

$$P_D = (V_{in} \times I_Q) + d \times I_{Load} \times V_{sat}$$

where d is the duty cycle and for buck converter

$$d = \frac{t_{on}}{T} = \frac{V_O}{V_{in}}$$

I_Q (quiescent current) and V_{sat} can be found in the LM2576 data sheet,

V_{in} is minimum input voltage applied,

V_O is the regulator output voltage,

I_{Load} is the load current.

The dynamic switching losses during turn-on and turn-off can be neglected if proper type catch diode is used.

Packages Not on a Heatsink (Free-Standing)

For a free-standing application when no heatsink is used, the junction temperature can be determined by the following expression:

$$T_J = (R_{\theta JA}) (P_D) + T_A$$

where $(R_{\theta JA})(P_D)$ represents the junction temperature rise caused by the dissipated power and T_A is the maximum ambient temperature.

Packages on a Heatsink

If the actual operating junction temperature is greater than the selected safe operating junction temperature determined in step 3, then a heatsink is required. The junction temperature will be calculated as follows:

$$T_J = P_D (R_{\theta JA} + R_{\theta CS} + R_{\theta SA}) + T_A$$

where $R_{\theta JC}$ is the thermal resistance junction–case,

$R_{\theta CS}$ is the thermal resistance case–heatsink,

$R_{\theta SA}$ is the thermal resistance heatsink–ambient.

If the actual operating temperature is greater than the selected safe operating junction temperature, then a larger heatsink is required.

Some Aspects That can Influence Thermal Design

It should be noted that the package thermal resistance and the junction temperature rise numbers are all approximate, and there are many factors that will affect these numbers, such as PC board size, shape, thickness, physical position, location, board temperature, as well as whether the surrounding air is moving or still.

Other factors are trace width, total printed circuit copper area, copper thickness, single- or double-sided, multilayer board, the amount of solder on the board or even color of the traces.

The size, quantity and spacing of other components on the board can also influence its effectiveness to dissipate the heat.

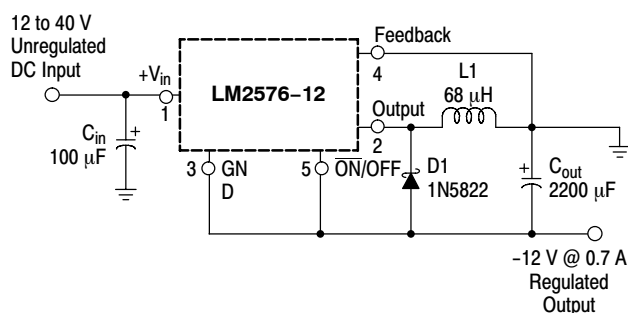


Figure 26. Inverting Buck-Boost Develops -12 V

ADDITIONAL APPLICATIONS

Inverting Regulator

An inverting buck-boost regulator using the LM2576-12 is shown in Figure 26. This circuit converts a positive input voltage to a negative output voltage with a common ground by bootstrapping the regulators ground to the negative output voltage. By grounding the feedback pin, the regulator senses the inverted output voltage and regulates it.

In this example the LM2576-12 is used to generate a -12 V output. The maximum input voltage in this case cannot exceed +28 V because the maximum voltage appearing across the regulator is the absolute sum of the input and output voltages and this must be limited to a maximum of 40 V.

This circuit configuration is able to deliver approximately 0.7 A to the output when the input voltage is 12 V or higher. At lighter loads the minimum input voltage required drops to approximately 4.7 V, because the buck-boost regulator topology can produce an output voltage that, in its absolute value, is either greater or less than the input voltage.

Since the switch currents in this buck-boost configuration are higher than in the standard buck converter topology, the available output current is lower.

This type of buck-boost inverting regulator can also require a larger amount of start-up input current, even for light loads. This may overload an input power source with a current limit less than 5.0 A.

Such an amount of input start-up current is needed for at least 2.0 ms or more. The actual time depends on the output voltage and size of the output capacitor.

Because of the relatively high start-up currents required by this inverting regulator topology, the use of a delayed start-up or an undervoltage lockout circuit is recommended.

Using a delayed start-up arrangement, the input capacitor can charge up to a higher voltage before the switch-mode regulator begins to operate.

The high input current needed for start-up is now partially supplied by the input capacitor C_{in} .

It has been already mentioned above, that in some situations, the delayed start-up or the undervoltage lockout features could be very useful. A delayed start-up circuit applied to a buck-boost converter is shown in Figure 27, Figure 33 in the “Undervoltage Lockout” section describes an undervoltage lockout feature for the same converter topology.

Design Recommendations:

The inverting regulator operates in a different manner than the buck converter and so a different design procedure has to be used to select the inductor L1 or the output capacitor C_{out} .

The output capacitor values must be larger than what is normally required for buck converter designs. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of μF).

The recommended range of inductor values for the inverting converter design is between 68 μH and 220 μH . To select an inductor with an appropriate current rating, the inductor peak current has to be calculated.

The following formula is used to obtain the peak inductor current:

$$I_{\text{peak}} \approx \frac{I_{\text{Load}} (V_{\text{in}} + |V_{\text{O}}|)}{V_{\text{in}}} + \frac{V_{\text{in}} \times t_{\text{on}}}{2L_1}$$

$$\text{where } t_{\text{on}} = \frac{|V_{\text{O}}|}{V_{\text{in}} + |V_{\text{O}}|} \times \frac{1.0}{f_{\text{osc}}}, \text{ and } f_{\text{osc}} = 52 \text{ kHz.}$$

Under normal continuous inductor current operating conditions, the worst case occurs when V_{in} is minimal.

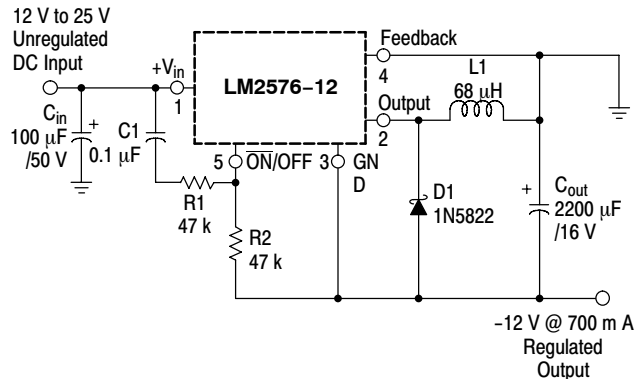
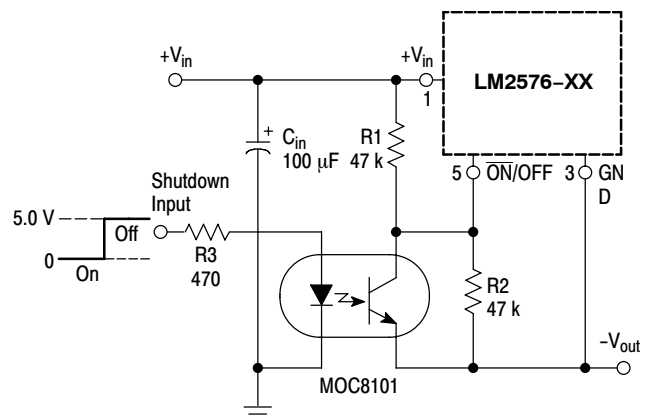


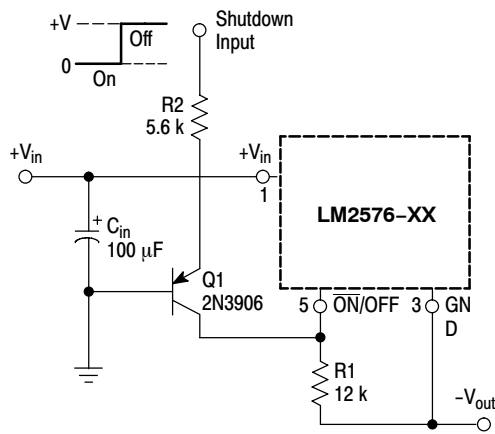
Figure 27. Inverting Buck-Boost Regulator with Delayed start-up



NOTE: This picture does not show the complete circuit.

Figure 28. Inverting Buck-Boost Regulator Shutdown Circuit Using an Optocoupler

With the inverting configuration, the use of the $\overline{\text{ON/OFF}}$ pin requires some level shifting techniques. This is caused by the fact, that the ground pin of the converter IC is no longer at ground. Now, the $\overline{\text{ON/OFF}}$ pin threshold voltage (1.3 V approximately) has to be related to the negative output voltage level. There are many different possible shut down methods, two of them are shown in Figures 28 and 29.



NOTE: This picture does not show the complete circuit.

Figure 29. Inverting Buck-Boost Regulator Shutdown Circuit Using a PNP Transistor

Negative Boost Regulator

This example is a variation of the buck-boost topology and it is called negative boost regulator. This regulator experiences relatively high switch current, especially at low input voltages. The internal switch current limiting results in lower output load current capability.

The circuit in Figure 30 shows the negative boost configuration. The input voltage in this application ranges from -5.0 V to -12 V and provides a regulated -12 V output. If the input voltage is greater than -12 V, the output will rise above -12 V accordingly, but will not damage the regulator.

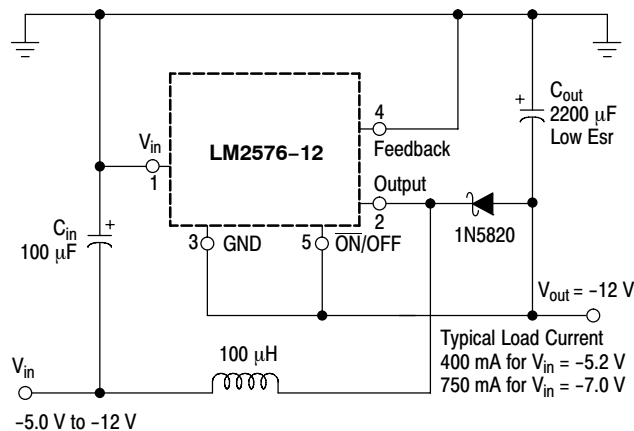


Figure 30. Negative Boost Regulator

Design Recommendations:

The same design rules as for the previous inverting buck-boost converter can be applied. The output capacitor C_{out} must be chosen larger than would be required for a what standard buck converter. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of μF). The recommended range of inductor values for the negative boost regulator is the same as for inverting converter design.

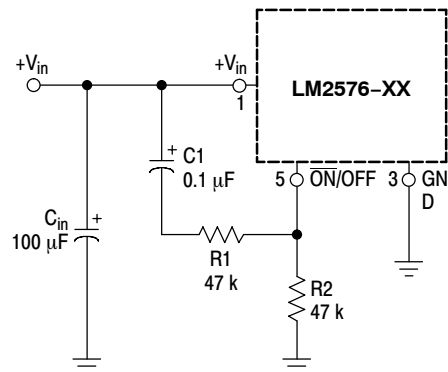
Another important point is that these negative boost converters cannot provide current limiting load protection in the event of a short in the output so some other means, such as a fuse, may be necessary to provide the load protection.

Delayed Start-up

There are some applications, like the inverting regulator already mentioned above, which require a higher amount of start-up current. In such cases, if the input power source is limited, this delayed start-up feature becomes very useful.

To provide a time delay between the time when the input voltage is applied and the time when the output voltage comes up, the circuit in Figure 31 can be used. As the input voltage is applied, the capacitor C_1 charges up, and the voltage across the resistor R_2 falls down. When the voltage on the ON/OFF pin falls below the threshold value 1.3 V, the regulator starts up. Resistor R_1 is included to limit the maximum voltage applied to the ON/OFF pin. It reduces the power supply noise sensitivity, and also limits the capacitor C_1 discharge current, but its use is not mandatory.

When a high 50 Hz or 60 Hz (100 Hz or 120 Hz respectively) ripple voltage exists, a long delay time can cause some problems by coupling the ripple into the ON/OFF pin, the regulator could be switched periodically on and off with the line (or double) frequency.



NOTE: This picture does not show the complete circuit.

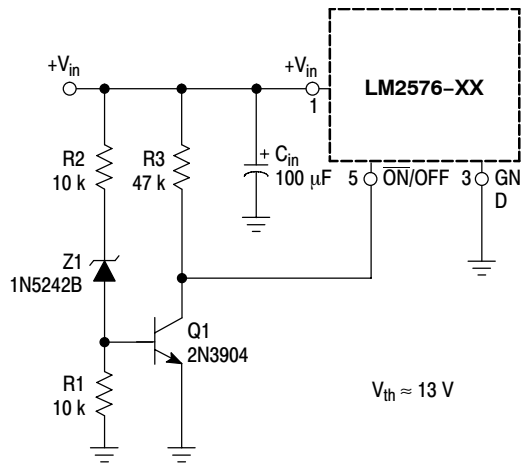
Figure 31. Delayed Start-up Circuitry

Undervoltage Lockout

Some applications require the regulator to remain off until the input voltage reaches a certain threshold level. Figure 32 shows an undervoltage lockout circuit applied to a buck regulator. A version of this circuit for buck-boost converter is shown in Figure 33. Resistor R_3 pulls the ON/OFF pin high and keeps the regulator off until the input voltage reaches a predetermined threshold level with respect to the ground Pin 3, which is determined by the following expression:

$$V_{th} \approx V_{Z1} + \left(1.0 + \frac{R_2}{R_1}\right) V_{BE}(Q1)$$

LM2576



NOTE: This picture does not show the complete circuit.

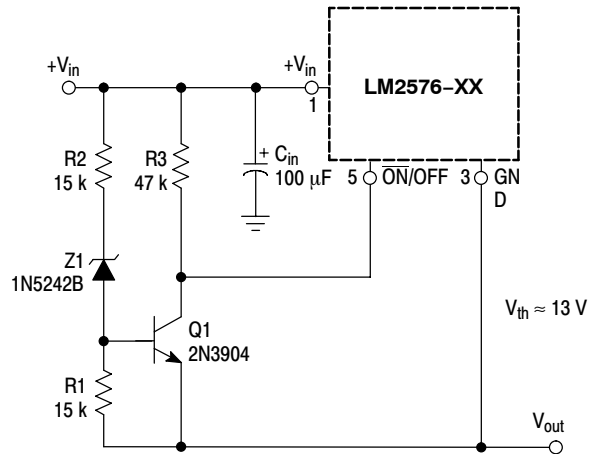
Figure 32. Undervoltage Lockout Circuit for Buck Converter

The following formula is used to obtain the peak inductor current:

$$I_{\text{peak}} \approx \frac{I_{\text{Load}} (V_{\text{in}} + |V_{\text{O}}|)}{V_{\text{in}}} + \frac{V_{\text{in}} \times t_{\text{on}}}{2L_1}$$

$$\text{where } t_{\text{on}} = \frac{|V_{\text{O}}|}{V_{\text{in}} + |V_{\text{O}}|} \times \frac{1.0}{f_{\text{osc}}}, \text{ and } f_{\text{osc}} = 52 \text{ kHz.}$$

Under normal continuous inductor current operating conditions, the worst case occurs when V_{in} is minimal.



NOTE: This picture does not show the complete circuit.

Figure 33. Undervoltage Lockout Circuit for Buck-Boost Converter

Adjustable Output, Low-Ripple Power Supply

A 3.0 A output current capability power supply that features an adjustable output voltage is shown in Figure 34.

This regulator delivers 3.0 A into 1.2 V to 35 V output. The input voltage ranges from roughly 3.0 V to 40 V. In order to achieve a 10 or more times reduction of output ripple, an additional L-C filter is included in this circuit.

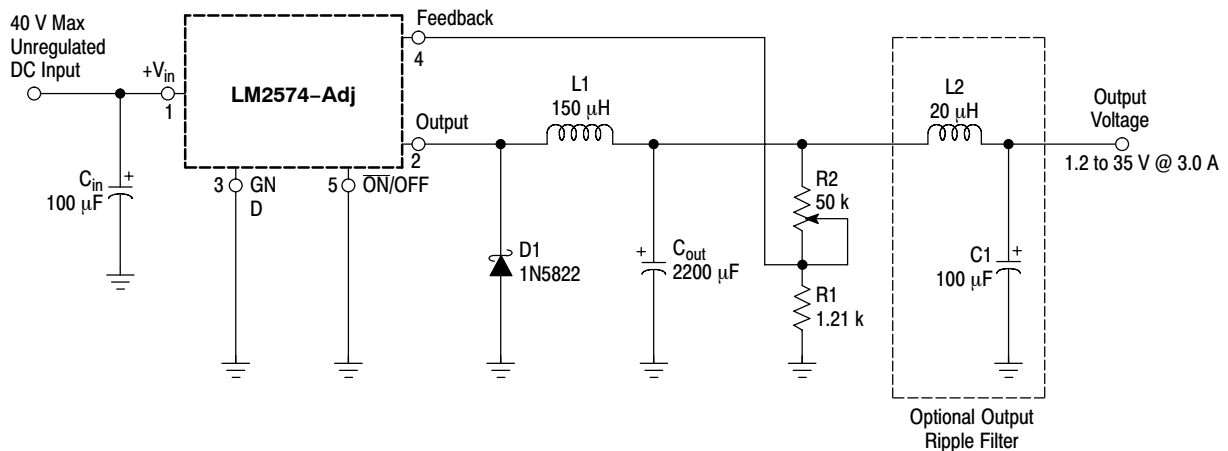


Figure 34. 1.2 to 35 V Adjustable 3.0 A Power Supply with Low Output Ripple

LM2576

THE LM2576-5 STEP-DOWN VOLTAGE REGULATOR WITH 5.0 V @ 3.0 A OUTPUT POWER CAPABILITY. TYPICAL APPLICATION WITH THROUGH-HOLE PC BOARD LAYOUT

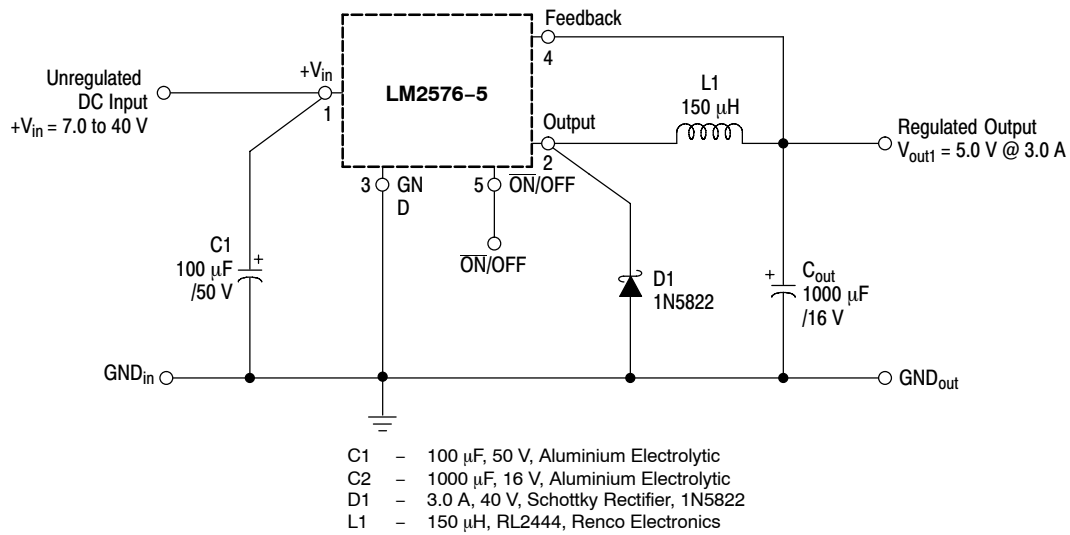


Figure 35. Schematic Diagram of the LM2576-5 Step-Down Converter

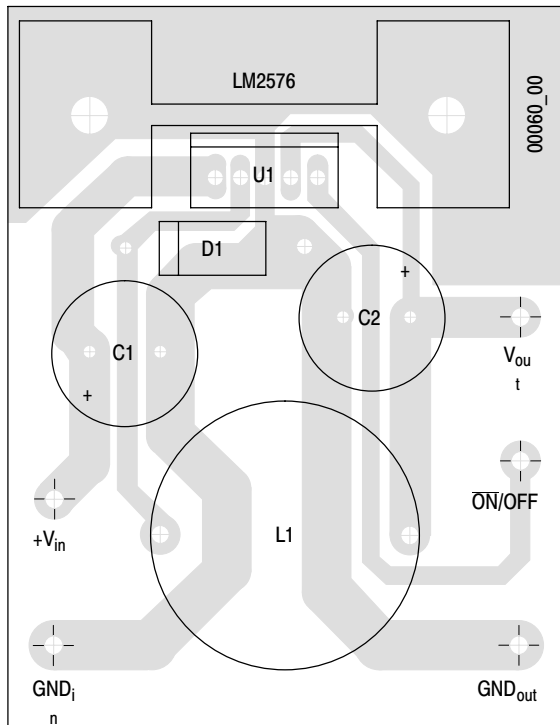


Figure 36. Printed Circuit Board Layout
Component Side

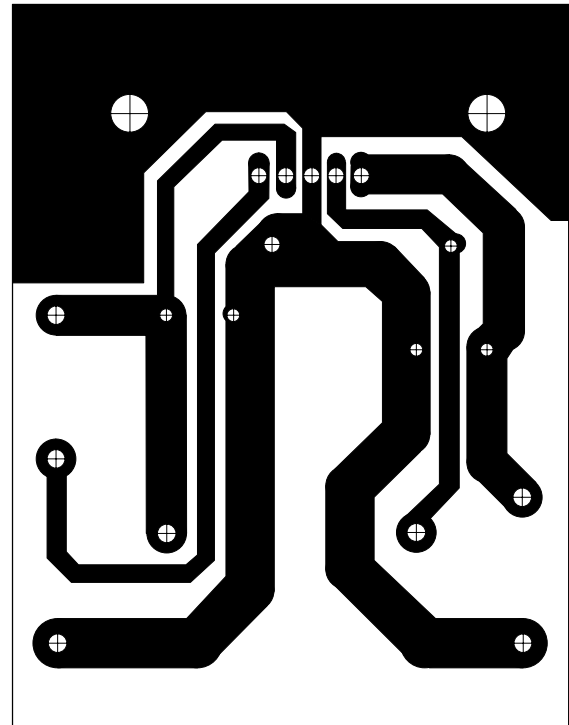


Figure 37. Printed Circuit Board Layout
Copper Side

LM2576

THE LM2576-ADJ STEP-DOWN VOLTAGE REGULATOR WITH 8.0 V @ 1.0 A OUTPUT POWER CAPABILITY. TYPICAL APPLICATION WITH THROUGH-HOLE PC BOARD LAYOUT

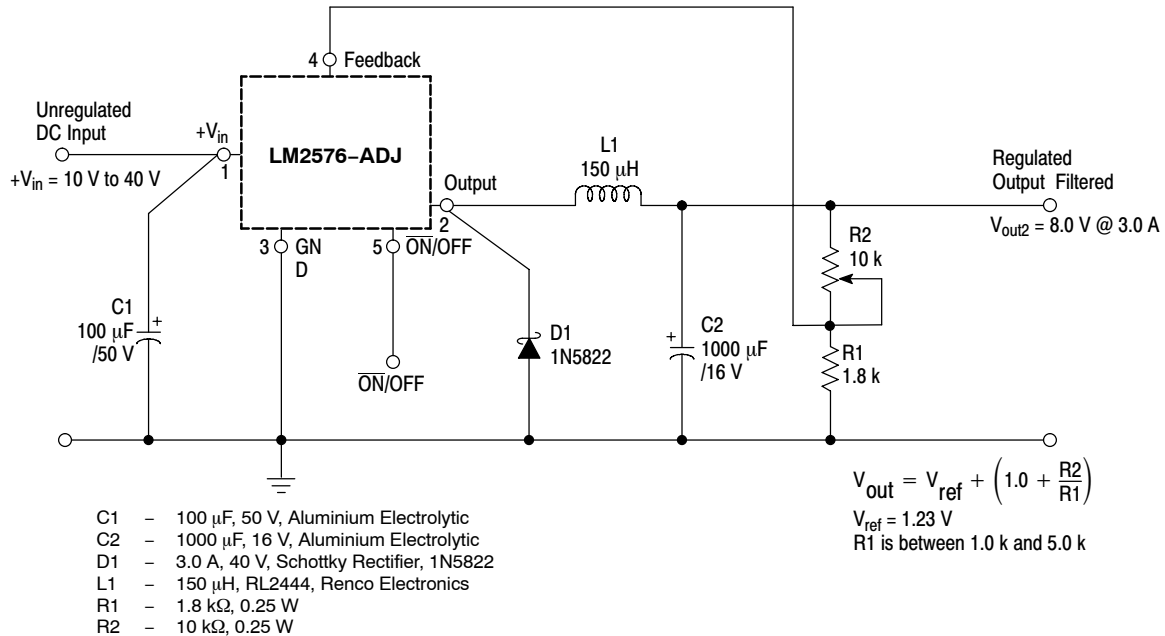


Figure 38. Schematic Diagram of the 8.0 V @ 3.0 A Step-Down Converter Using the LM2576-ADJ

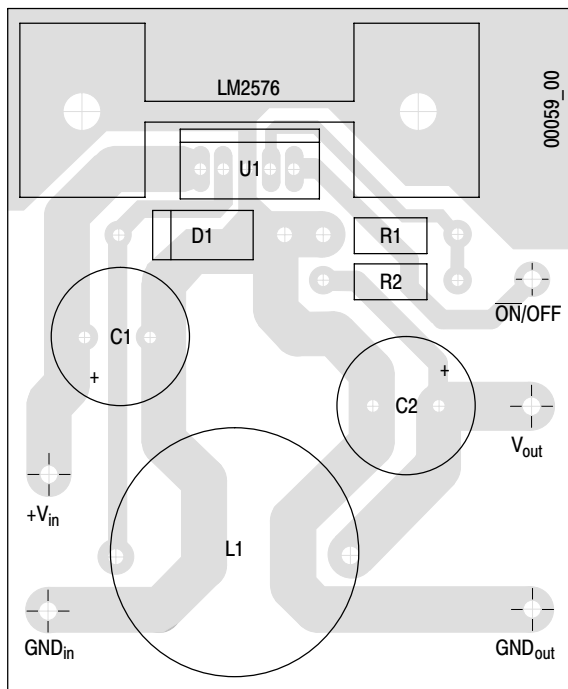


Figure 39. Printed Circuit Board Layout
Component Side

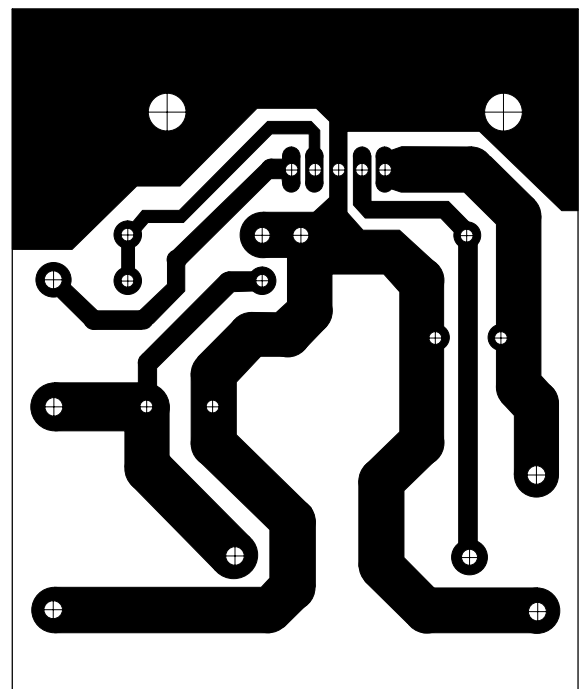


Figure 40. Printed Circuit Board Layout
Copper Side

References

- National Semiconductor LM2576 Data Sheet and Application Note
- National Semiconductor LM2595 Data Sheet and Application Note
- Marty Brown "Practical Switching Power Supply Design", Academic Press, Inc., San Diego 1990
- Ray Ridley "High Frequency Magnetics Design", Ridley Engineering, Inc. 1995

LM2576

ORDERING INFORMATION

Device	Nominal Output Voltage	Operating Temperature Range	Package	Shipping [†]
LM2576TV-ADJ	1.23 V to 37 V	$T_J = -40^\circ \text{ to } +125^\circ \text{C}$	TO-220 (Vertical Mount)	50 Units/Rail
LM2576TV-ADJG			TO-220 (Vertical Mount) (Pb-Free)	50 Units/Rail
LM2576T-ADJ			TO-220 (Straight Lead)	50 Units/Rail
LM2576D2T-ADJ			D ² PAK (Surface Mount)	
LM2576D2T-ADJR4			D ² PAK (Surface Mount)	2500 Tape & Reel
LM2576TV-3.3	3.3 V	$T_J = -40^\circ \text{ to } +125^\circ \text{C}$	TO-220 (Vertical Mount)	50 Units/Rail
LM2576T-3.3			TO-220 (Straight Lead)	
LM2576D2T-3.3			D ² PAK (Surface Mount)	
LM2576D2TR4-3.3			D ² PAK (Surface Mount)	2500 Tape & Reel
LM2576D2TR4-3.3G			D ² PAK (Surface Mount) (Pb-Free)	2500 Tape & Reel
LM2576TV-5	5.0 V	$T_J = -40^\circ \text{ to } +125^\circ \text{C}$	TO-220 (Vertical Mount)	50 Units/Rail
LM2576T-5			TO-220 (Straight Lead)	
LM2576D2T-5			D ² PAK (Surface Mount)	
LM2576D2T-5G			D ² PAK (Surface Mount) (Pb-Free)	50 Units/Rail
LM2576D2TR4-5			D ² PAK (Surface Mount)	2500 Tape & Reel
LM2576TV-12	12 V	$T_J = -40^\circ \text{ to } +125^\circ \text{C}$	TO-220 (Vertical Mount)	50 Units/Rail
LM2576TV-12G			TO-220 (Vertical Mount) (Pb-Free)	50 Units/Rail
LM2576T-12			TO-220 (Straight Lead)	50 Units/Rail
LM2576D2T-12			D ² PAK (Surface Mount)	
LM2576D2TR4-12			D ² PAK (Surface Mount)	2500 Tape & Reel
LM2576TV-15	15 V	$T_J = -40^\circ \text{ to } +125^\circ \text{C}$	TO-220 (Vertical Mount)	50 Units/Rail
LM2576T-15			TO-220 (Straight Lead)	
LM2576D2T-15			D ² PAK (Surface Mount)	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

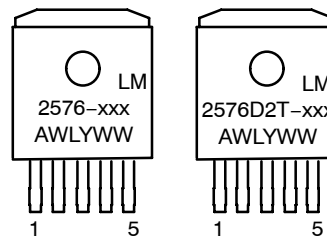
**TO-220
TV SUFFIX
CASE 314B**



**TO-220
T SUFFIX
CASE 314D**



**D²PAK
D2T SUFFIX
CASE 936A**



xxx = 3.3, 5.0, 12, 15, or ADJ
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

MC34060A, MC33060A

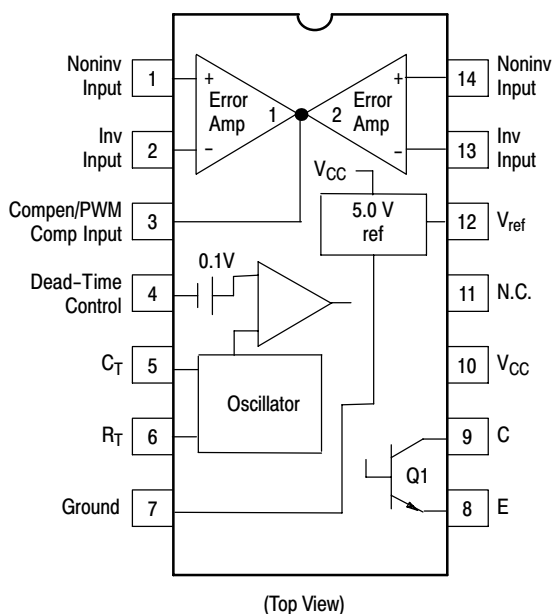
Fixed Frequency, PWM, Voltage Mode Single Ended Controllers

The MC34060A is a low cost fixed frequency, pulse width modulation control circuit designed primarily for single-ended SWITCHMODE™ power supply control.

The MC34060A is specified over the commercial operating temperature range of 0° to +70°C, and the MC33060A is specified over an automotive temperature range of -40° to +85°C.

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator with Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 V Reference, 1.5% Accuracy
- Adjustable Dead-Time Control
- Uncommitted Output Transistor Rated to 200 mA Source or Sink
- Undervoltage Lockout

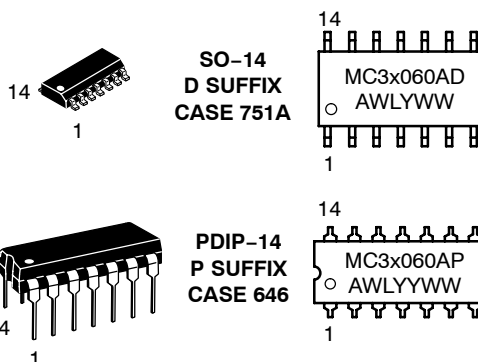
PIN CONNECTIONS



ON Semiconductor™

<http://onsemi.com>

MARKING DIAGRAMS



x = 3 or 4
 A = Assembly Location
 WL = Wafer Lot
 YY, Y = Year
 WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 195 of this data sheet.

MC34060A, MC33060A

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	42	V
Collector Output Voltage	V_C	42	V
Collector Output Current (Note 1)	I_C	500	mA
Amplifier Input Voltage Range	V_{in}	-0.3 to +42	V
Power Dissipation @ $T_A \leq 45^\circ\text{C}$	P_D	1000	mW
Operating Junction Temperature	T_J	125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +125	$^\circ\text{C}$
Operating Ambient Temperature Range For MC34060A For MC33060A	T_A	0 to +70 -40 to +85	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	P Suffix Package	D Suffix Package	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	80	120	$^\circ\text{C}/\text{W}$
Derating Ambient Temperature	T_A	45	45	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_C	-	30	40	V
Collector Output Current	I_C	-	-	200	mA
Amplifier Input Voltage	V_{in}	-0.3	-	$V_{CC} - 2$	V
Current Into Feedback Terminal	I_{fb}	-	-	0.3	mA
Reference Output Current	I_{ref}	-	-	10	mA
Timing Resistor	R_T	1.8	47	500	$k\Omega$
Timing Capacitor	C_T	0.00047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	25	200	kHz
PWM Input Voltage (Pins 3 and 4)	-	-0.3	-	5.3	V

1. Maximum thermal limits must be observed.

MC34060A, MC33060A

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$, unless otherwise noted. For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit

REFERENCE SECTION

Reference Voltage ($I_O = 1.0\text{ mA}$, $T_A = 25^\circ\text{C}$) $T_A = T_{\text{low}}$ to T_{high} – MC34060A – MC33060A	V_{ref}	4.925 4.9 4.85	5.0 – –	5.075 5.1 5.1	V
Line Regulation ($V_{CC} = 7.0\text{ V}$ to 40 V , $I_O = 10\text{ mA}$)	Reg_{line}	–	2.0	25	mV
Load Regulation ($I_O = 1.0\text{ mA}$ to 10 mA)	Reg_{load}	–	2.0	15	mV
Short Circuit Output Current ($V_{\text{ref}} = 0\text{ V}$)	I_{SC}	15	35	75	mA

OUTPUT SECTION

Collector Off-State Current ($V_{CC} = 40\text{ V}$, $V_{CE} = 40\text{ V}$)	$I_{C(\text{off})}$	–	2.0	100	μA
Emitter Off-State Current ($V_{CC} = 40\text{ V}$, $V_{CE} = 40\text{ V}$, $V_E = 0\text{ V}$)	$I_{E(\text{off})}$	–	–	–100	μA
Collector-Emitter Saturation Voltage (Note 2) Common-Emitter ($V_E = 0\text{ V}$, $I_C = 200\text{ mA}$) Emitter-Follower ($V_C = 15\text{ V}$, $I_E = -200\text{ mA}$)	$V_{\text{sat}(C)}$ $V_{\text{sat}(E)}$	– –	1.1 1.5	1.5 2.5	V
Output Voltage Rise Time ($T_A = 25^\circ\text{C}$) Common-Emitter (See Figure 12) Emitter-Follower (See Figure 13)	t_r	– –	100 100	200 200	ns
Output Voltage Fall Time ($T_A = 25^\circ\text{C}$) Common-Emitter (See Figure 12) Emitter-Follower (See Figure 13)	t_f	– –	40 40	100 100	ns

ERROR AMPLIFIER SECTION

Input Offset Voltage ($V_{O[\text{Pin } 3]} = 2.5\text{ V}$)	V_{IO}	–	2.0	10	mV
Input Offset Current ($V_{C[\text{Pin } 3]} = 2.5\text{ V}$)	I_{IO}	–	5.0	250	nA
Input Bias Current ($V_{O[\text{Pin } 3]} = 2.5\text{ V}$)	I_{IB}	–	–0.1	–2.0	μA
Input Common Mode Voltage Range ($V_{CC} = 40\text{ V}$)	V_{ICR}	0 to $V_{CC} - 2.0$	–	–	V
Inverting Input Voltage Range	$V_{IR(\text{INV})}$	–0.3 to $V_{CC} - 2.0$	–	–	V
Open-Loop Voltage Gain ($\Delta V_O = 3.0\text{ V}$, $V_O = 0.5\text{ V}$ to 3.5 V , $R_L = 2.0\text{ k}\Omega$)	A_{VOL}	70	95	–	dB
Unity-Gain Crossover Frequency ($V_O = 0.5\text{ V}$ to 3.5 V , $R_L = 2.0\text{ k}\Omega$)	f_c	–	600	–	kHz
Phase Margin at Unity-Gain ($V_O = 0.5\text{ V}$ to 3.5 V , $R_L = 2.0\text{ k}\Omega$)	ϕ_m	–	65	–	deg.
Common Mode Rejection Ratio ($V_{CC} = 40\text{ V}$, $V_{in} = 0\text{ V}$ to 38 V)	CMRR	65	90	–	dB
Power Supply Rejection Ratio ($\Delta V_{CC} = 33\text{ V}$, $V_O = 2.5\text{ V}$, $R_L = 2.0\text{ k}\Omega$)	PSRR	–	100	–	dB
Output Sink Current ($V_{O[\text{Pin } 3]} = 0.7\text{ V}$)	I_{O-}	0.3	0.7	–	mA
Output Source Current ($V_{O[\text{Pin } 3]} = 3.5\text{ V}$)	I_{O+}	–2.0	–4.0	–	mA

2. Low duty cycle techniques are used during test to maintain junction temperature as close to ambient temperatures as possible.

$T_{\text{low}} = -40^\circ\text{C}$ for MC33060A
= 0°C for MC34060A

$T_{\text{high}} = +85^\circ\text{C}$ for MC33060A
= $+70^\circ\text{C}$ for MC34060A

MC34060A, MC33060A

ELECTRICAL CHARACTERISTICS (continued) ($V_{CC} = 15\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$, unless otherwise noted.)

For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit

PWM COMPARATOR SECTION (Test circuit Figure 11)

Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	–	3.5	4.5	V
Input Sink Current ($V_{Pin\ 3} = 0.7\text{ V}$)	I_I	0.3	0.7	–	mA

DEAD-TIME CONTROL SECTION (Test circuit Figure 11)

Input Bias Current (Pin 4) ($V_{in} = 0\text{ V}$ to 5.25 V)	$I_{IB(DT)}$	–	–1.0	–10	μA
Maximum Output Duty Cycle ($V_{in} = 0\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$) ($V_{in} = 0\text{ V}$, $C_T = 0.001\text{ }\mu\text{F}$, $R_T = 47\text{ k}\Omega$)	DC_{max}	90 –	96 92	100 –	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	– 0	2.8 –	3.3 –	V

OSCILLATOR SECTION

Frequency ($C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$, $T_A = 25^\circ\text{C}$) $T_A = T_{low}$ to T_{high} – MC34060A – MC33060A ($C_T = 0.001\text{ }\mu\text{F}$, $R_T = 47\text{ k}\Omega$)	f_{osc}	9.7 9.5 9.0 –	10.5 – – 25	11.3 11.5 11.5 –	kHz
Standard Deviation of Frequency* ($C_T = 0.001\text{ }\mu\text{F}$, $R_T = 47\text{ k}\Omega$)	σf_{osc}	–	1.5	–	%
Frequency Change with Voltage ($V_{CC} = 7.0\text{ V}$ to 40 V)	$\Delta f_{osc}(\Delta V)$	–	0.5	2.0	%
Frequency Change with Temperature ($\Delta T_A = T_{low}$ to T_{high}) ($C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$)	$\Delta f_{osc}(\Delta T)$	– –	4.0 –	– –	%

UNDERVOLTAGE LOCKOUT SECTION

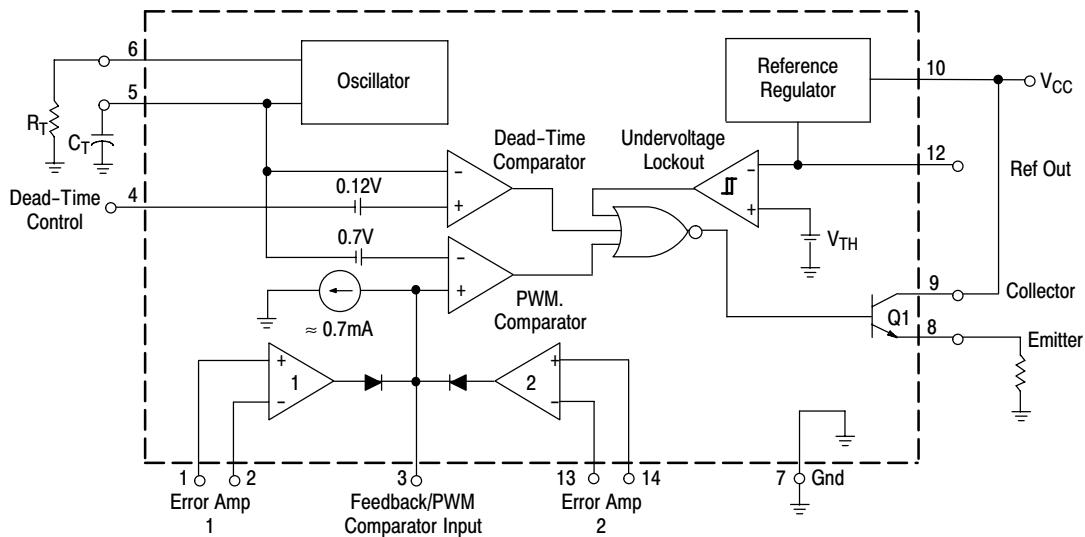
Turn-On Threshold (V_{CC} increasing, $I_{ref} = 1.0\text{ mA}$)	V_{th}	4.0	4.7	5.5	V
Hysteresis	V_H	50	150	300	mV

TOTAL DEVICE

Standby Supply Current (Pin 6 at V_{ref} , all other inputs and outputs open) ($V_{CC} = 15\text{ V}$) ($V_{CC} = 40\text{ V}$)	I_{CC}	– –	5.5 7.0	10 15	mA
Average Supply Current ($V_{Pin\ 4} = 2.0\text{ V}$, $C_T = 0.001\text{ }\mu\text{F}$, $R_T = 47\text{ k}\Omega$). See Figure 11.	I_S	–	7.0	–	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula; $\sigma = \sqrt{\frac{\sum_{n=1}^N (x_n - \bar{x})^2}{N-1}}$

MC34060A, MC33060A



This device contains 46 active transistors.

Figure 1. Block Diagram

Description

The MC34060A is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply (see Figure 1). An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T . The approximate oscillator frequency is determined by:

$$f_{osc} \cong \frac{1.2}{R_T \cdot C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The output is enabled only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

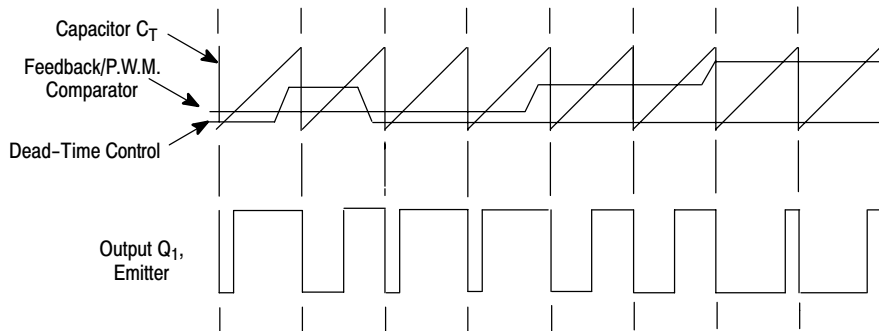


Figure 2. Timing Diagram

APPLICATIONS INFORMATION

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feed-back input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle of 96%. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 V to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback

pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common mode input range from -0.3 V to $(V_{CC} - 2.0\text{ V})$, and may be used to sense power supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the noninverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

The MC34060A has an internal 5.0 V reference capable of sourcing up to 10 mA of load currents for external bias circuits. The reference has an internal accuracy of $\pm 5\%$ with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to $+70^\circ\text{C}$.

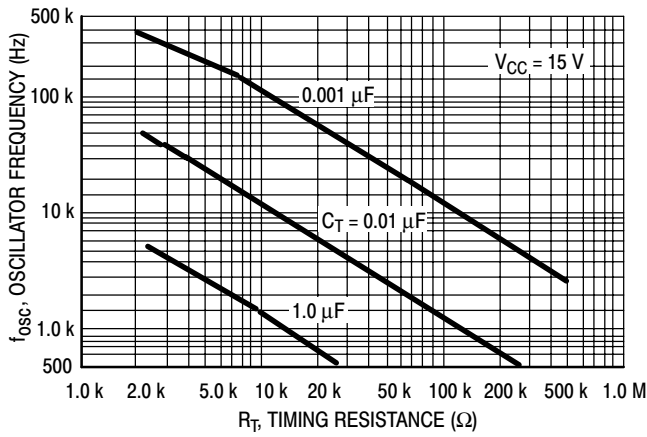


Figure 3. Oscillator Frequency versus Timing Resistance

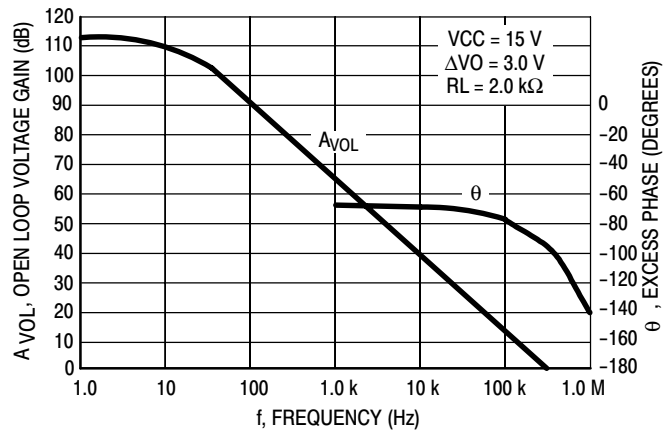


Figure 4. Open Loop Voltage Gain and Phase versus Frequency

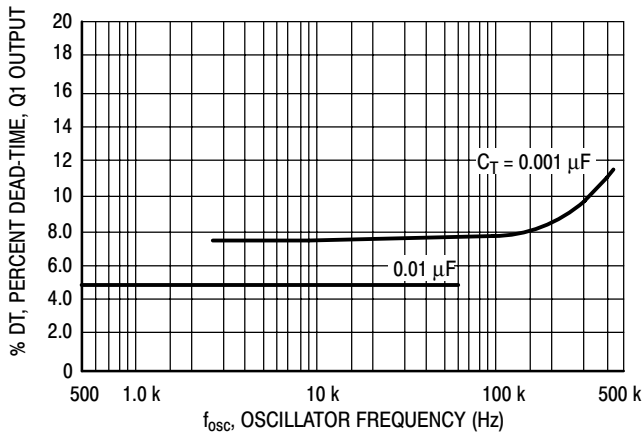


Figure 5. Percent Deadtime versus Oscillator Frequency

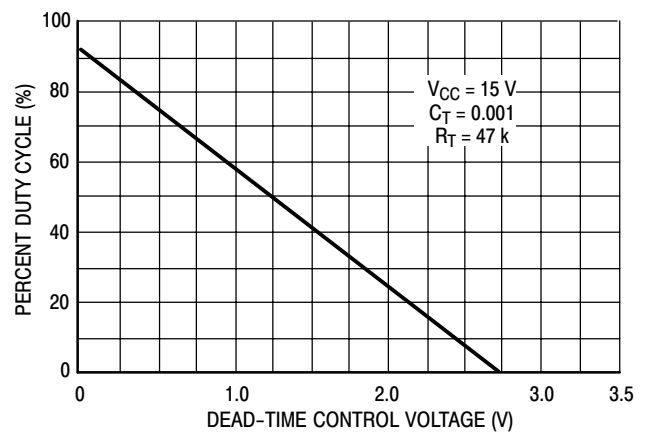


Figure 6. Percent Duty Cycle versus Dead-Time Control Voltage

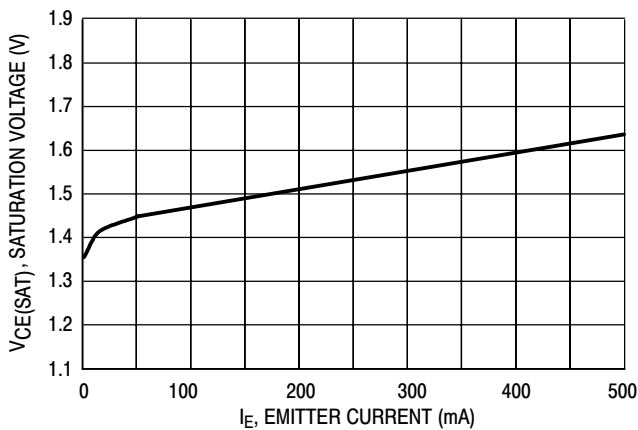


Figure 7. Emitter-Follower Configuration Output Saturation Voltage versus Emitter Current

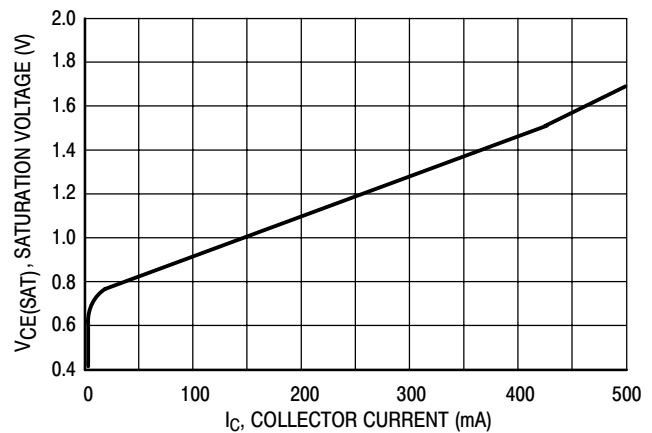


Figure 8. Common-Emitter Configuration Output Saturation Voltage versus Collector Current

MC34060A, MC33060A

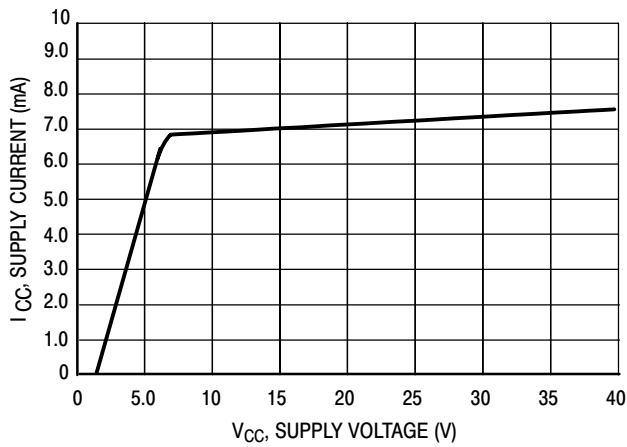


Figure 9. Standby Supply Current versus Supply Voltage

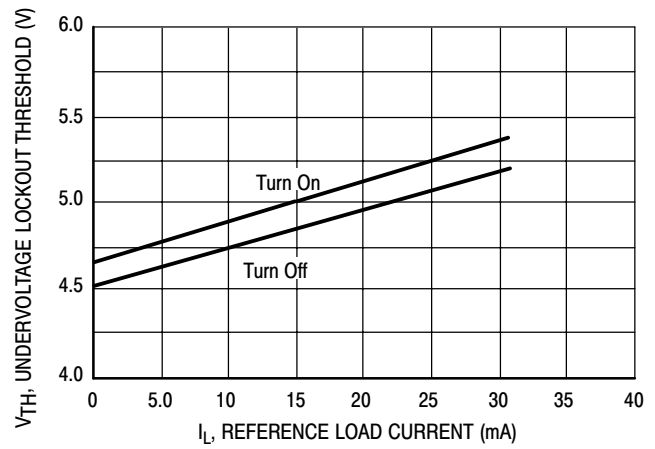


Figure 10. Undervoltage Lockout Thresholds versus Reference Load Current

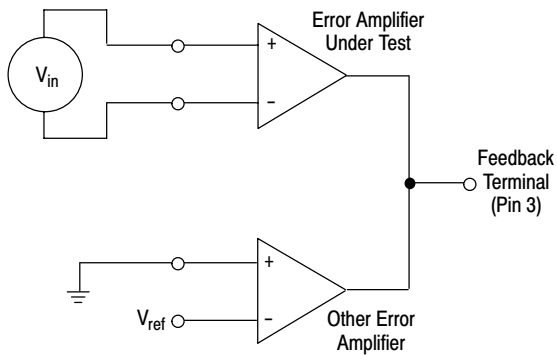


Figure 11. Error Amplifier Characteristics

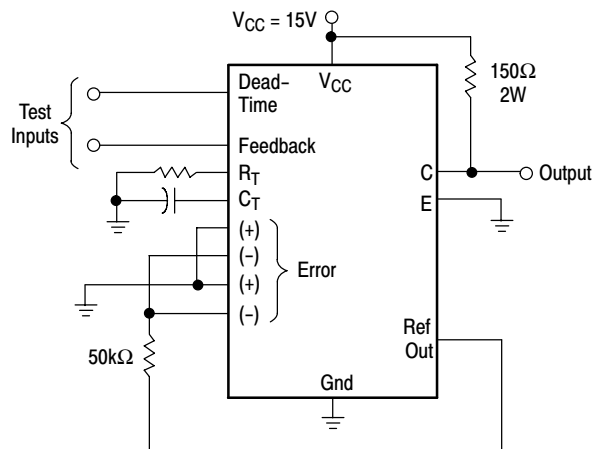


Figure 12. Deadtime and Feedback Control

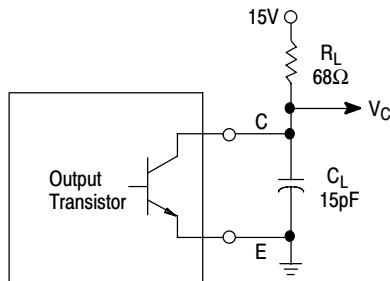


Figure 13. Common-Emitter Configuration and Waveform

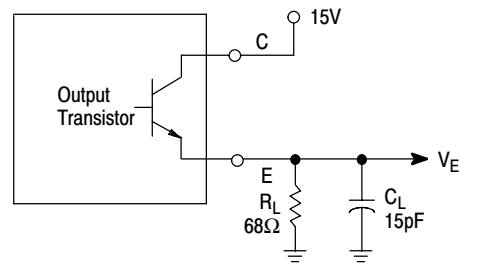


Figure 14. Emitter-Follower Configuration and Waveform

MC34060A, MC33060A

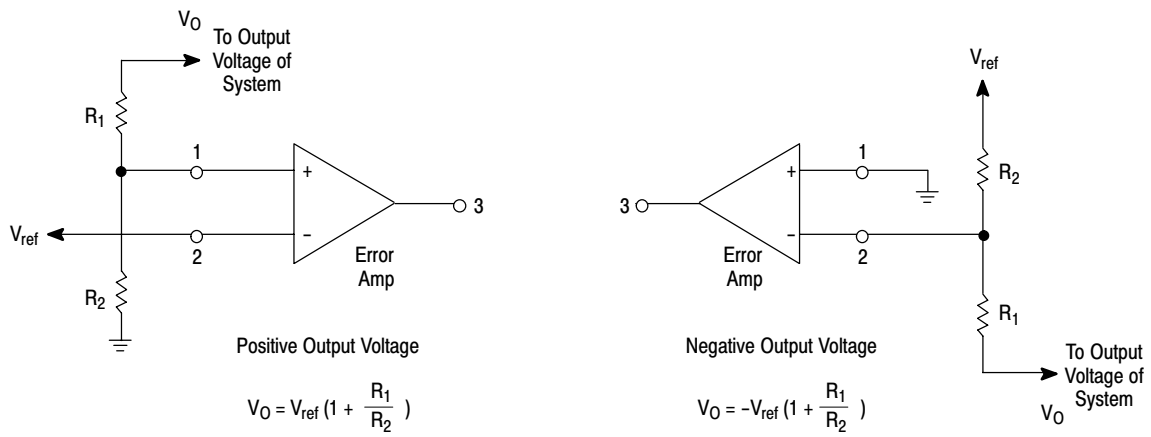


Figure 15. Error Amplifier Sensing Techniques

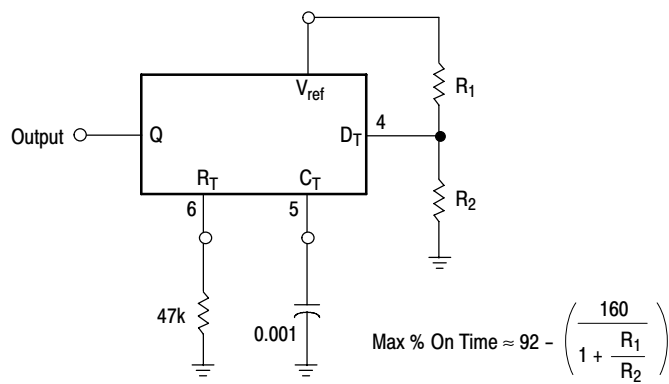


Figure 16. Deadtime Control Circuit

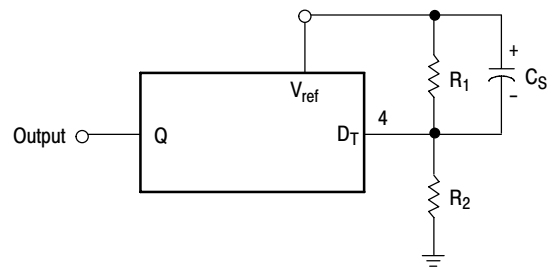


Figure 17. Soft-Start Circuit

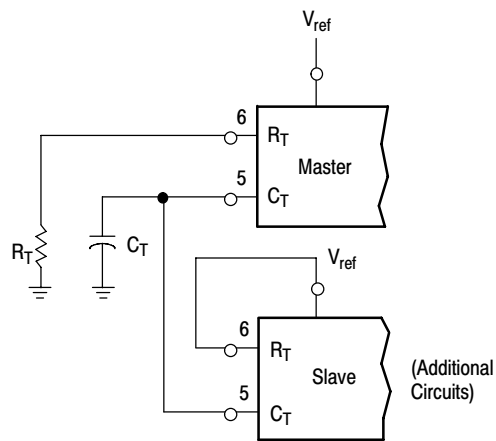
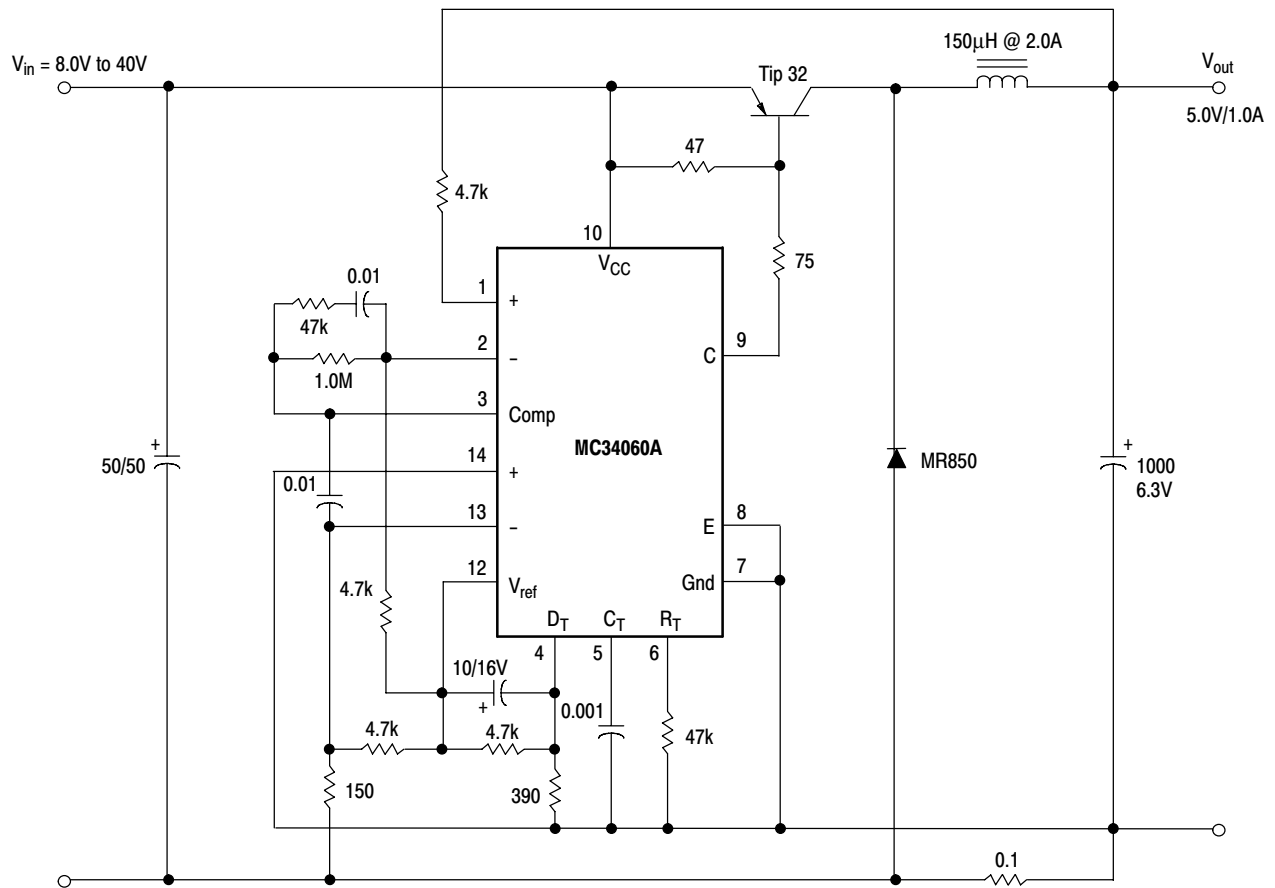


Figure 18. Slaving Two or More Control Circuits

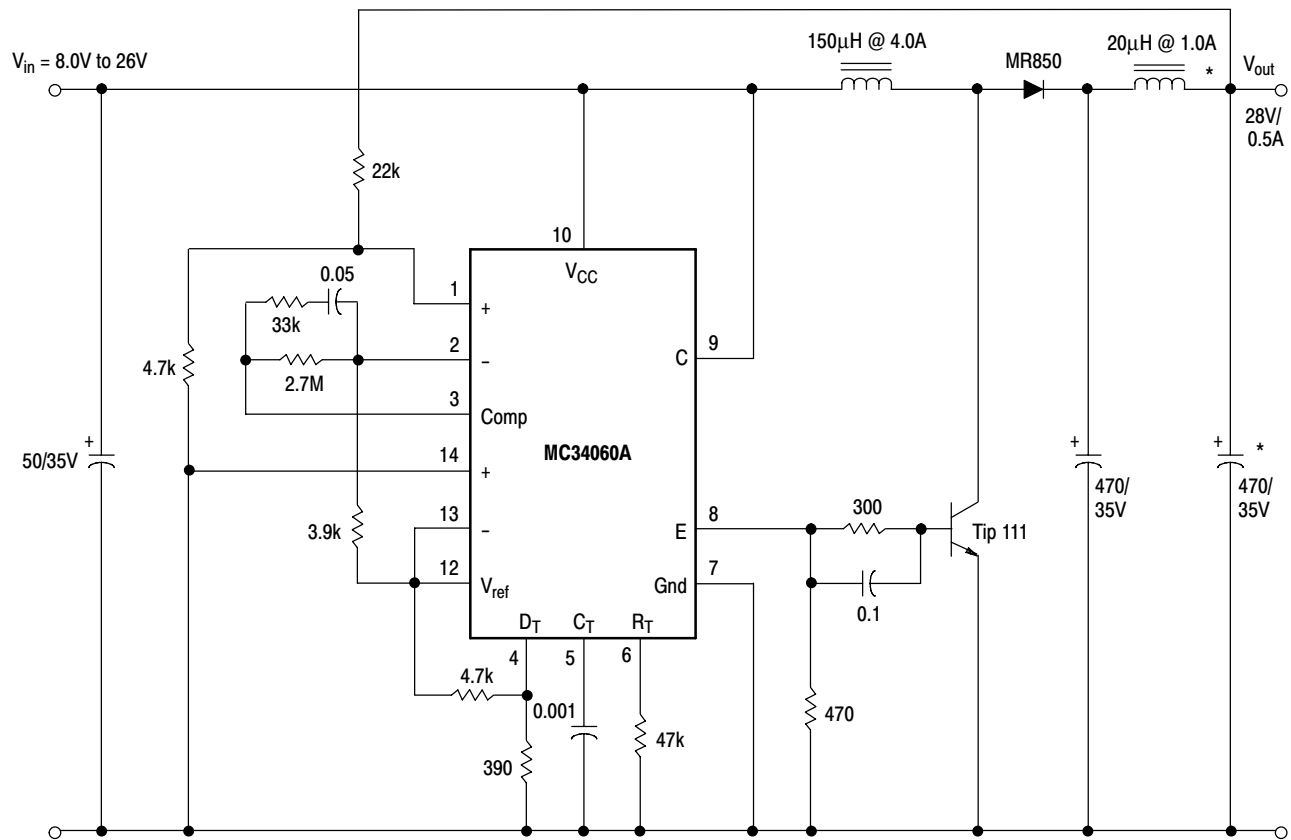
MC34060A, MC33060A



Test	Conditions	Results
Line Regulation	$V_{in} = 8.0 \text{ V to } 40 \text{ V}$, $I_O = 1.0 \text{ A}$	25 mV 0.5%
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ mA to } 1.0 \text{ A}$	3.0 mV 0.06%
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ A}$	75 mV p-p P.A.R.D.
Short Circuit Current	$V_{in} = 12 \text{ V}$, $R_L = 0.1 \Omega$	1.6 A
Efficiency	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ A}$	73%

Figure 19. Step-Down Converter with Soft-Start and Output Current Limiting

MC34060A, MC33060A



Test	Conditions	Results
Line Regulation	$V_{in} = 8.0 \text{ V to } 26 \text{ V}, I_O = 0.5 \text{ A}$	40 mV 0.14%
Load Regulation	$V_{in} = 12 \text{ V}, I_O = 1.0 \text{ mA to } 0.5 \text{ A}$	5.0 mV 0.18%
Output Ripple	$V_{in} = 12 \text{ V}, I_O = 0.5 \text{ A}$	24 mV p-p P.A.R.D.
Efficiency	$V_{in} = 12 \text{ V}, I_O = 0.5 \text{ A}$	75%

*Optional circuit to minimize output ripple

Figure 20. Step-Up Converter

The circuit diagram shows an MC34060A regulator configured as a negative voltage regulator. The input voltage V_{in} is 8.0V to 40V. The output voltage V_{out} is -15V at 0.25A. The circuit includes a 30k resistor connected to V_{in} and a 7.5k resistor connected to the non-inverting input (pin 1). The inverting input (pin 2) is connected to a 47k resistor and a 1.0M resistor. The output (pin 9) is connected to a 75 resistor and a 47 resistor. The regulator is powered by a 50/50V transformer. The output is filtered by a 20μH inductor and a 330/16V capacitor. The circuit also includes a 150μH inductor and a 330/16V capacitor for the input filter. The output is connected to a 1.0 resistor.

*Optional circuit to minimize output ripple

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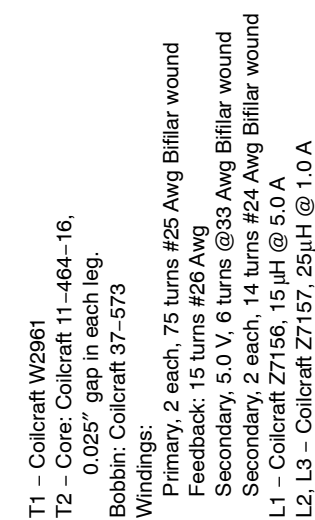


Figure 22. 33 W Off-Line Flyback Converter with Soft-Start and Primary Power Limiting

Test	Conditions	Results
Line Regulation 5.0 V	$V_{in} = 95 \text{ Vac to } 135 \text{ Vac}, I_O = 3.0 \text{ A}$	20 mV 0.40%
Line Regulation $\pm 12 \text{ V}$	$V_{in} = 95 \text{ Vac to } 135 \text{ Vac}, I_O = \pm 0.75 \text{ A}$	52 mV 0.26%
Load Regulation 5.0 V	$V_{in} = 115 \text{ Vac}, I_O = 1.0 \text{ A to } 4.0 \text{ A}$	476 mV 9.5%
Load Regulation $\pm 12 \text{ V}$	$V_{in} = 115 \text{ Vac}, I_O = \pm 0.4 \text{ A to } \pm 0.9 \text{ A}$	300 mV 2.5%
Output Ripple 5.0 V	$V_{in} = 115 \text{ Vac}, I_O = 3.0 \text{ A}$	45 mV p-p P.A.R.D.
Output Ripple $\pm 12 \text{ V}$	$V_{in} = 115 \text{ Vac}, I_O = \pm 0.75 \text{ A}$	75 mV p-p P.A.R.D.
Efficiency	$V_{in} = 115 \text{ Vac}, I_O 5.0 \text{ V} = 3.0 \text{ A}$ $I_O \pm 12 \text{ V} = \pm 0.75 \text{ A}$	74%

MC34060A, MC33060A

ORDERING INFORMATION

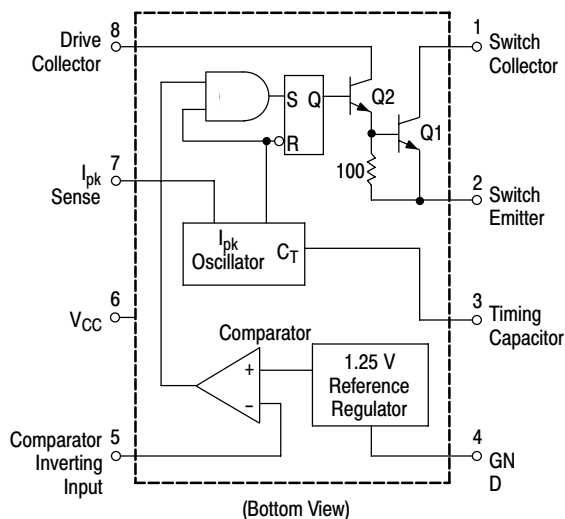
Device	Operating Temperature Range	Package	Shipping
MC34060AD	$T_A = 0^\circ \text{ to } +70^\circ\text{C}$	SO-14	55 Units/Rail
MC34060ADR2		SO-14	2500 Tape & Reel
MC34060AP		PDIP-14	25 Units/Rail
MC33060AD	$T_A = -40^\circ \text{ to } +85^\circ\text{C}$	SO-14	55 Units/Rail
MC33060ADR2		SO-14	2500 Tape & Reel
MC33060AP		PDIP-14	25 Units/Rail

MC34063A, MC33063A, NCV33063A

1.5 A, Step-Up/Down/ Inverting Switching Regulators

The MC34063A Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components. Refer to Application Notes AN920A/D and AN954/D for additional design information.

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference
- Pb-Free Packages are Available



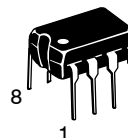
This device contains 51 active transistors.

Figure 1. Representative Schematic Diagram



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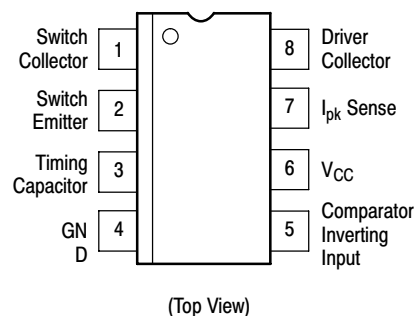


PDIP-8
P, P1 SUFFIX
CASE 626



SOIC-8
D SUFFIX
CASE 751

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 206 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 206 of this data sheet.

MC34063A, MC33063A, NCV33063A

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	-0.3 to +40	Vdc
Switch Collector Voltage	$V_{C(switch)}$	40	Vdc
Switch Emitter Voltage ($V_{Pin\ 1} = 40\text{ V}$)	$V_{E(switch)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	Vdc
Driver Collector Voltage	$V_{C(driver)}$	40	Vdc
Driver Collector Current (Note 1)	$I_{C(driver)}$	100	mA
Switch Current	I_{SW}	1.5	A
Power Dissipation and Thermal Characteristics			
Plastic Package, P, P1 Suffix			
$T_A = 25^\circ\text{C}$	P_D	1.25	W
Thermal Resistance	$R_{\theta JA}$	100	$^\circ\text{C/W}$
SOIC Package, D Suffix			
$T_A = 25^\circ\text{C}$	P_D	625	mW
Thermal Resistance	$R_{\theta JA}$	160	$^\circ\text{C/W}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A		$^\circ\text{C}$
MC34063A		0 to +70	
MC33063AV, NCV33063A		-40 to +125	
MC33063A		-40 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Maximum package power dissipation limits must be observed.
2. ESD data available upon request.
3. NCV prefix is for automotive and other applications requiring site and change control.

MC34063A, MC33063A, NCV33063A

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = T_{low}$ to T_{high} [Note 4], unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit

OSCILLATOR

Frequency ($V_{Pin\ 5} = 0\text{ V}$, $C_T = 1.0\text{ nF}$, $T_A = 25^\circ\text{C}$)	f_{osc}	24	33	42	kHz
Charge Current ($V_{CC} = 5.0\text{ V}$ to 40 V , $T_A = 25^\circ\text{C}$)	I_{chg}	24	35	42	μA
Discharge Current ($V_{CC} = 5.0\text{ V}$ to 40 V , $T_A = 25^\circ\text{C}$)	I_{dischg}	140	220	260	μA
Discharge to Charge Current Ratio (Pin 7 to V_{CC} , $T_A = 25^\circ\text{C}$)	I_{dischg}/I_{chg}	5.2	6.5	7.5	–
Current Limit Sense Voltage ($I_{chg} = I_{dischg}$, $T_A = 25^\circ\text{C}$)	$V_{ipk(sense)}$	250	300	350	mV

OUTPUT SWITCH (Note 5)

Saturation Voltage, Darlington Connection ($I_{SW} = 1.0\text{ A}$, Pins 1, 8 connected)	$V_{CE(sat)}$	–	1.0	1.3	V
Saturation Voltage (Note 6) ($I_{SW} = 1.0\text{ A}$, $R_{Pin\ 8} = 82\ \Omega$ to V_{CC} , Forced $\beta \approx 20$)	$V_{CE(sat)}$	–	0.45	0.7	V
DC Current Gain ($I_{SW} = 1.0\text{ A}$, $V_{CE} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)	h_{FE}	50	75	–	–
Collector Off-State Current ($V_{CE} = 40\text{ V}$)	$I_{C(off)}$	–	0.01	100	μA

COMPARATOR

Threshold Voltage $T_A = 25^\circ\text{C}$ $T_A = T_{low}$ to T_{high}	V_{th}	1.225 1.21	1.25 –	1.275 1.29	V
Threshold Voltage Line Regulation ($V_{CC} = 5.0\text{ V}$ to 40 V) MC33063A, MC34063A MC33063AV, NCV33063A	Reg_{line}	– –	1.4 1.4	5.0 6.0	mV
Input Bias Current ($V_{in} = 0\text{ V}$)	I_{IB}	–	–20	–400	nA

TOTAL DEVICE

Supply Current ($V_{CC} = 5.0\text{ V}$ to 40 V , $C_T = 1.0\text{ nF}$, Pin 7 = V_{CC} , $V_{Pin\ 5} > V_{th}$, Pin 2 = GND, remaining pins open)	I_{CC}	–	–	4.0	mA

4. $T_{low} = 0^\circ\text{C}$ for MC34063A, -40°C for MC33063A, AV, NCV33063A
 $T_{high} = +70^\circ\text{C}$ for MC34063A, $+85^\circ\text{C}$ for MC33063A, $+125^\circ\text{C}$ for MC33063AV, NCV33063A
5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
6. If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents ($\leq 300\text{ mA}$) and high driver currents ($\geq 30\text{ mA}$), it may take up to $2.0\ \mu\text{s}$ for it to come out of saturation. This condition will shorten the off time at frequencies $\geq 30\text{ kHz}$, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended:

$$\text{Forced } \beta \text{ of output switch : } \frac{I_{C \text{ output}}}{I_{C \text{ driver}} - 7.0\text{ mA}} \geq 10$$

* The $100\ \Omega$ resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.

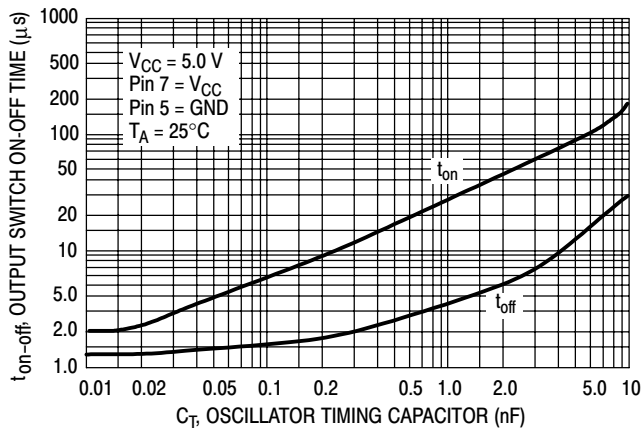


Figure 2. Output Switch On-Off Time versus Oscillator Timing Capacitor

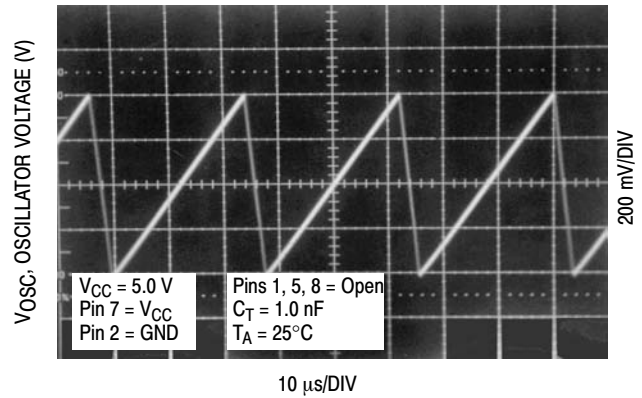


Figure 3. Timing Capacitor Waveform

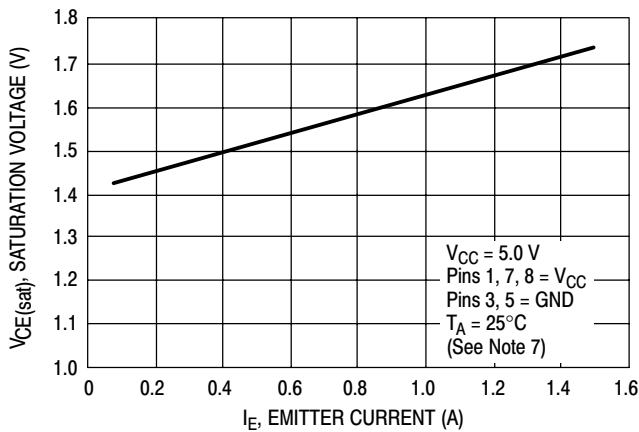


Figure 4. Emitter Follower Configuration Output Saturation Voltage versus Emitter Current

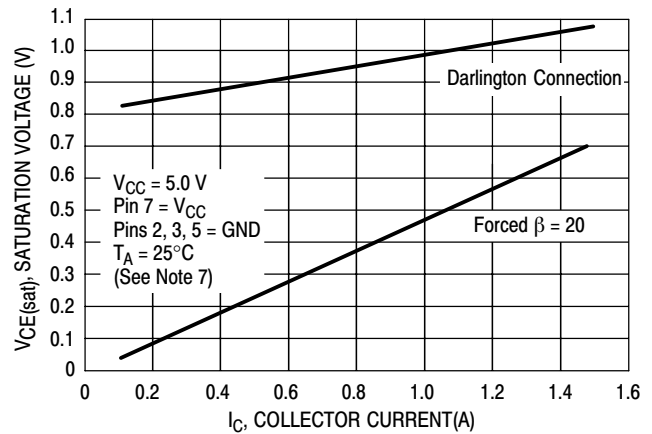


Figure 5. Common Emitter Configuration Output Switch Saturation Voltage versus Collector Current

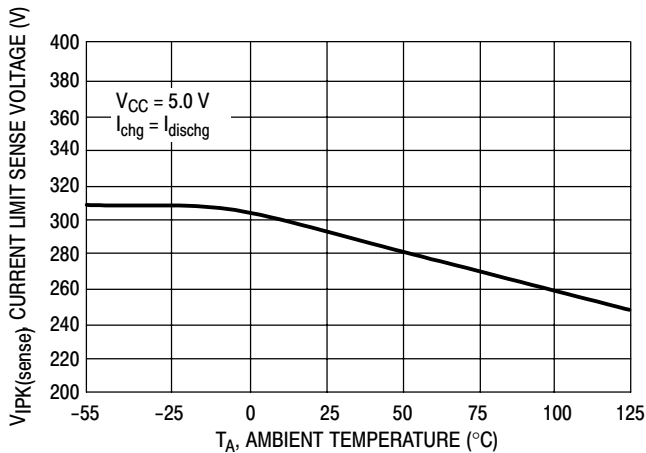


Figure 6. Current Limit Sense Voltage versus Temperature

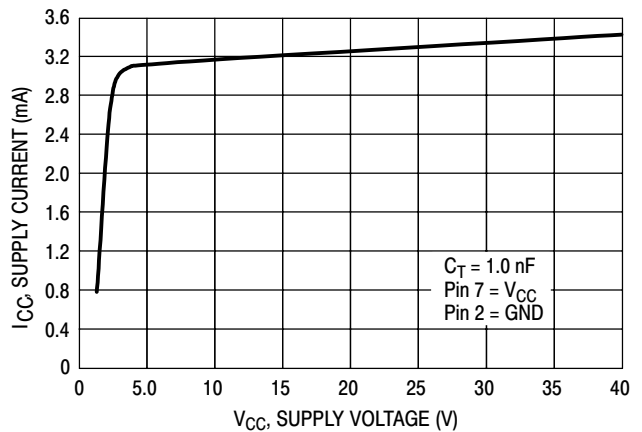
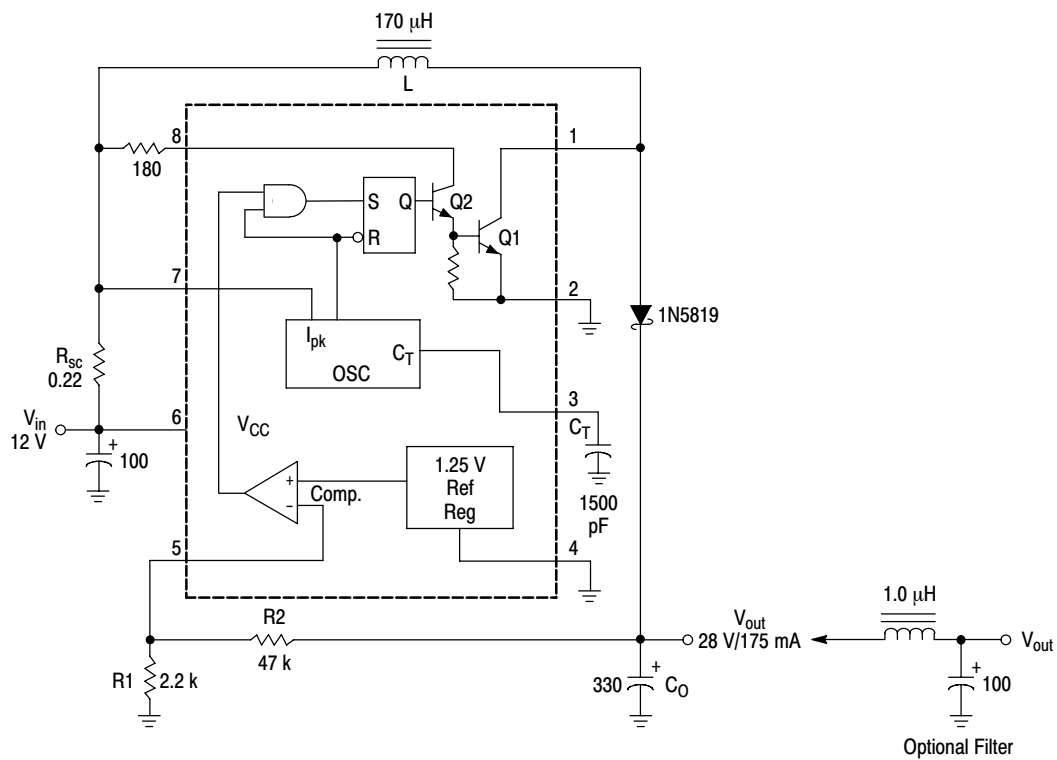


Figure 7. Standby Supply Current versus Supply Voltage

- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

MC34063A, MC33063A, NCV33063A



Test	Conditions	Results
Line Regulation	$V_{in} = 8.0\text{ V to }16\text{ V}$, $I_O = 175\text{ mA}$	$30\text{ mV} = \pm 0.05\%$
Load Regulation	$V_{in} = 12\text{ V}$, $I_O = 75\text{ mA to }175\text{ mA}$	$10\text{ mV} = \pm 0.017\%$
Output Ripple	$V_{in} = 12\text{ V}$, $I_O = 175\text{ mA}$	400 mVpp
Efficiency	$V_{in} = 12\text{ V}$, $I_O = 175\text{ mA}$	87.7%
Output Ripple With Optional Filter	$V_{in} = 12\text{ V}$, $I_O = 175\text{ mA}$	40 mVpp

Figure 8. Step-Up Converter

MC34063A, MC33063A, NCV33063A

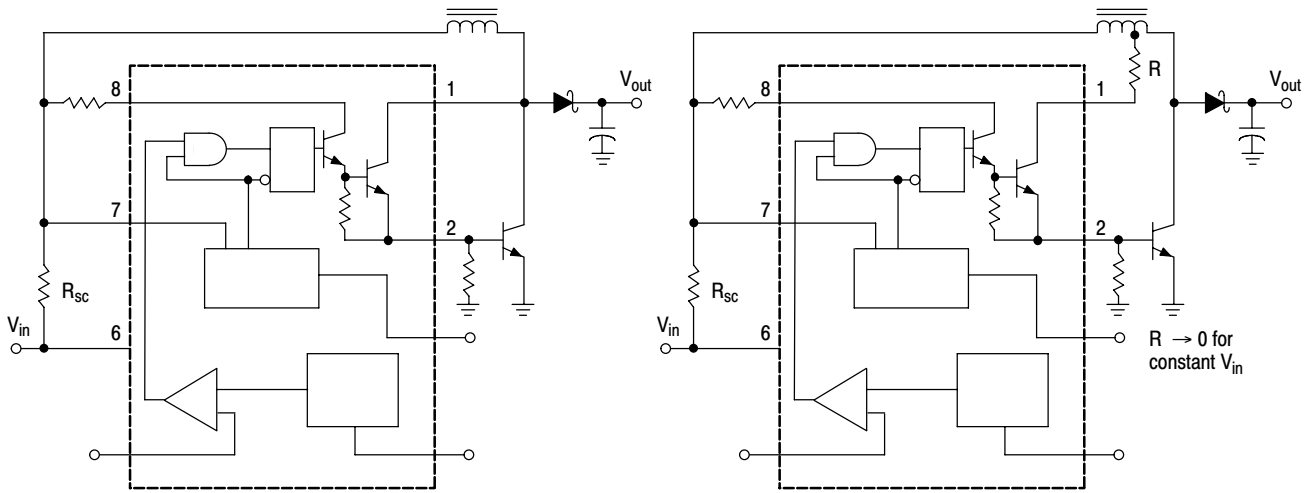


Figure 9. External Current Boost Connections for I_C Peak Greater than 1.5 A

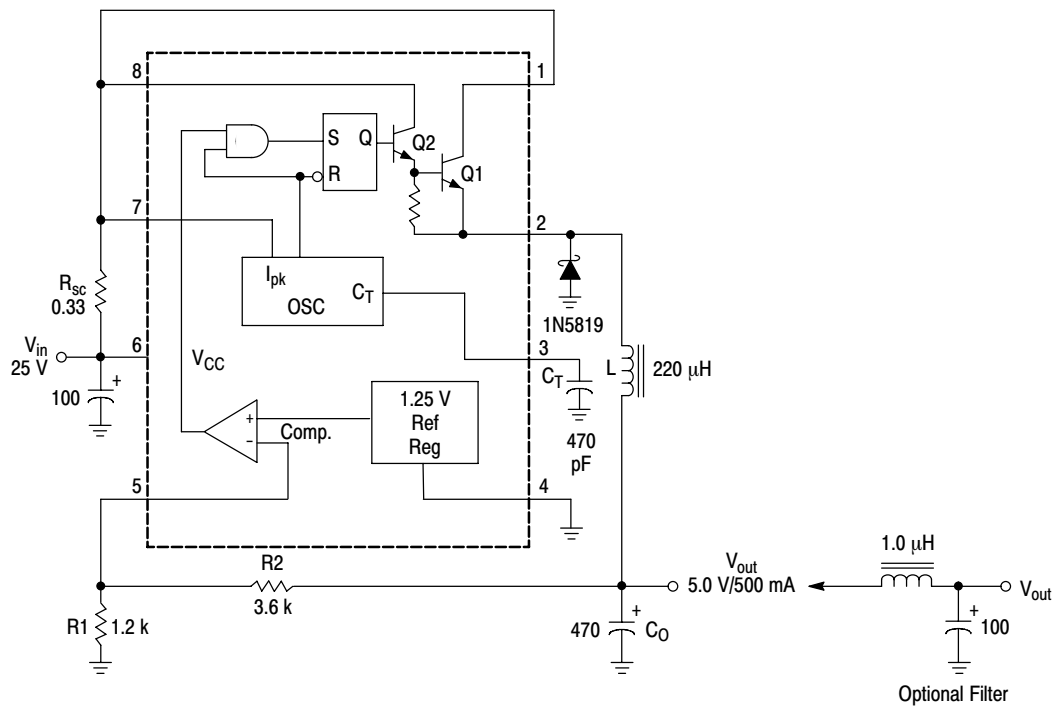
9a. External NPN Switch

9b. External NPN Saturated Switch

(See Note 8)

8. If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥ 30 mA), it may take up to $2.0 \mu\text{s}$ to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended.

MC34063A, MC33063A, NCV33063A



Test	Conditions	Results
Line Regulation	$V_{in} = 15\text{ V to }25\text{ V}, I_O = 500\text{ mA}$	$12\text{ mV} = \pm 0.12\%$
Load Regulation	$V_{in} = 25\text{ V}, I_O = 50\text{ mA to }500\text{ mA}$	$3.0\text{ mV} = \pm 0.03\%$
Output Ripple	$V_{in} = 25\text{ V}, I_O = 500\text{ mA}$	120 mVpp
Short Circuit Current	$V_{in} = 25\text{ V}, R_L = 0.1\ \Omega$	1.1 A
Efficiency	$V_{in} = 25\text{ V}, I_O = 500\text{ mA}$	83.7%
Output Ripple With Optional Filter	$V_{in} = 25\text{ V}, I_O = 500\text{ mA}$	40 mVpp

Figure 10. Step-Down Converter

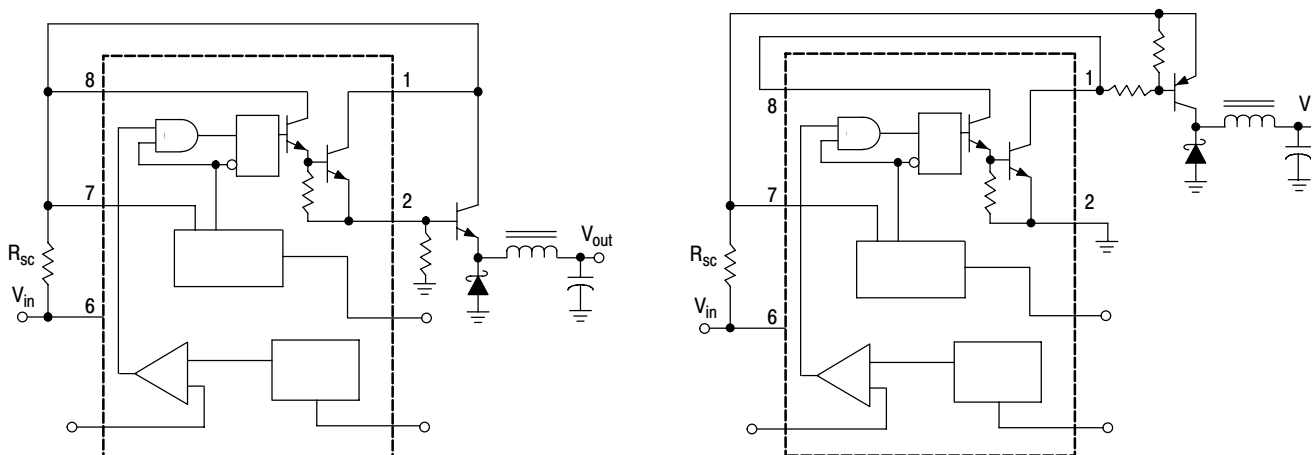
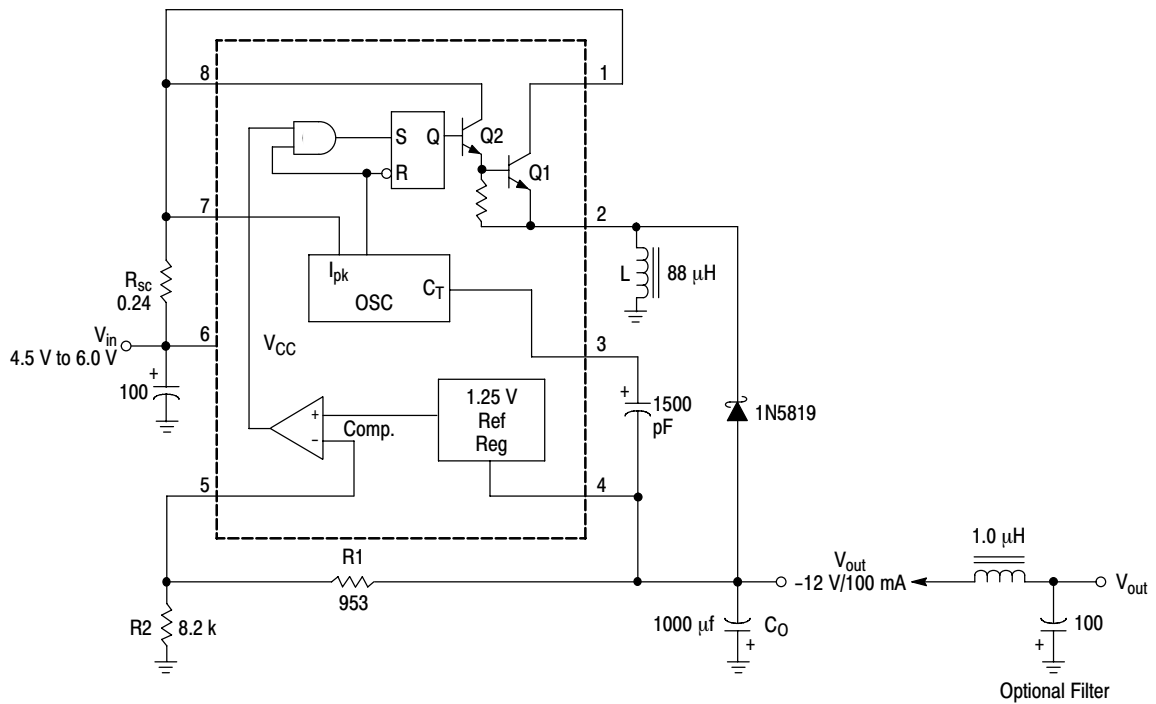


Figure 11. External Current Boost Connections for I_C Peak Greater than 1.5 A

11a. External NPN Switch

11b. External PNP Saturated Switch

MC34063A, MC33063A, NCV33063A



Test	Conditions	Results
Line Regulation	$V_{in} = 4.5 \text{ V to } 6.0 \text{ V}$, $I_O = 100 \text{ mA}$	$3.0 \text{ mV} = \pm 0.012\%$
Load Regulation	$V_{in} = 5.0 \text{ V}$, $I_O = 10 \text{ mA to } 100 \text{ mA}$	$0.022 \text{ V} = \pm 0.09\%$
Output Ripple	$V_{in} = 5.0 \text{ V}$, $I_O = 100 \text{ mA}$	500 mVpp
Short Circuit Current	$V_{in} = 5.0 \text{ V}$, $R_L = 0.1 \Omega$	910 mA
Efficiency	$V_{in} = 5.0 \text{ V}$, $I_O = 100 \text{ mA}$	62.2%
Output Ripple With Optional Filter	$V_{in} = 5.0 \text{ V}$, $I_O = 100 \text{ mA}$	70 mVpp

Figure 12. Voltage Inverting Converter

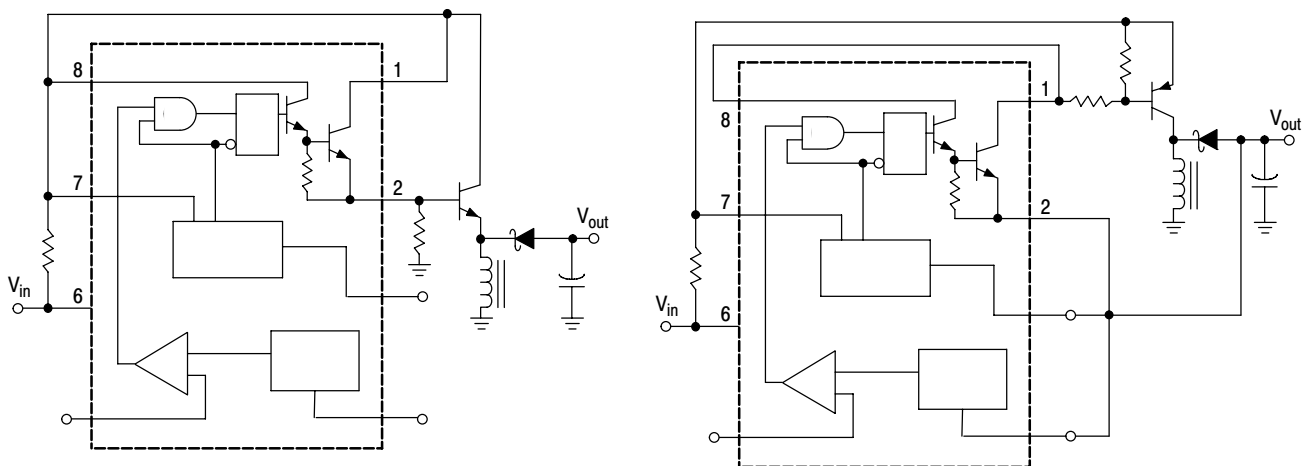
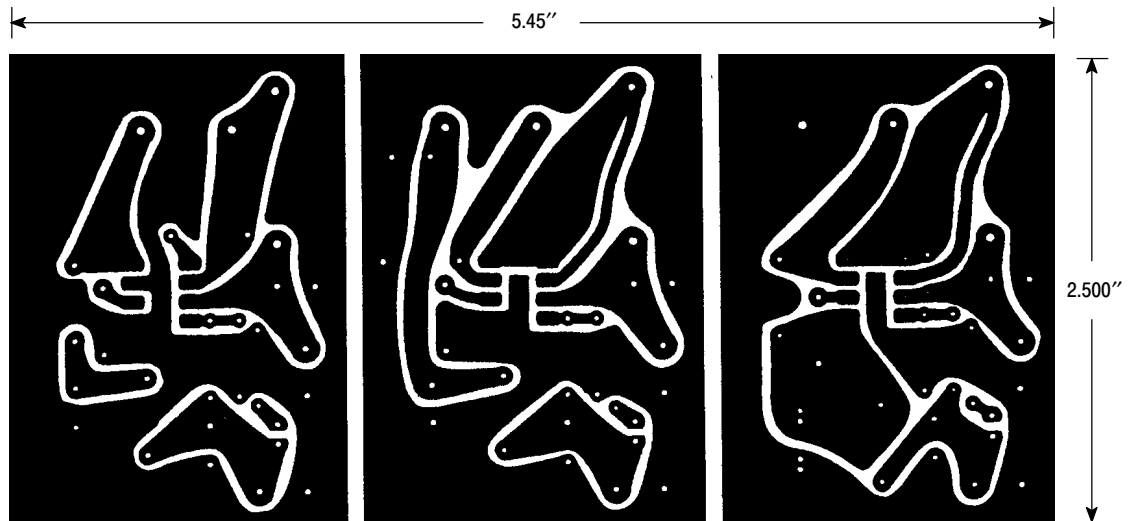


Figure 13. External Current Boost Connections for I_C Peak Greater than 1.5 A

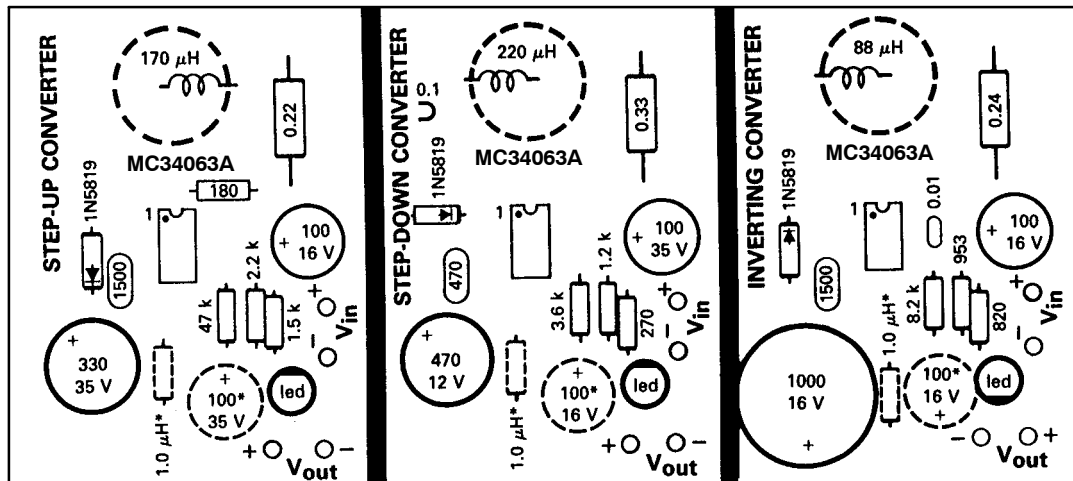
13a. External NPN Switch

13b. External PNP Saturated Switch

MC34063A, MC33063A, NCV33063A



(Top view, copper foil as seen through the board from the component side)



(Top View, Component Side)

*Optional Filter.

Figure 14. Printed Circuit Board and Component Layout

(Circuits of Figures 8, 10, 12)

INDUCTOR DATA

Converter	Inductance (μH)	Turns/Wire
Step-Up	170	38 Turns of #22 AWG
Step-Down	220	48 Turns of #22 AWG
Voltage-Inverting	88	28 Turns of #22 AWG

All inductors are wound on Magnetics Inc. 55117 toroidal core.

MC34063A, MC33063A, NCV33063A

Calculation	Step-Up	Step-Down	Voltage-Inverting
t_{on}/t_{off}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{ V_{out} + V_F}{V_{in} - V_{sat}}$
$(t_{on} + t_{off})$	$\frac{1}{f}$	$\frac{1}{f}$	$\frac{1}{f}$
t_{off}	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$
t_{on}	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$
C_T	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$
$I_{pk(switch)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$	$2I_{out(max)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$
R_{sc}	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}} \right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat} - V_{out})}{I_{pk(switch)}} \right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}} \right) t_{on(max)}$
C_O	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$

V_{sat} = Saturation voltage of the output switch.

V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{in} – Nominal input voltage.

V_{out} – Desired output voltage, $|V_{out}| = 1.25 \left(1 + \frac{R2}{R1} \right)$

I_{out} – Desired output current.

f_{min} – Minimum desired output switching frequency at the selected values of V_{in} and I_O .

$V_{ripple(pp)}$ – Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

NOTE: For further information refer to Application Note AN920A/D and AN954/D.

Figure 15. Design Formula Table

MC34063A, MC33063A, NCV33063A

ORDERING INFORMATION

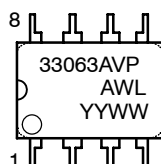
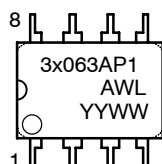
Device	Package	Shipping [†]
MC33063AD	SOIC-8	98 Units / Rail
MC33063ADG	SOIC-8 (Pb-Free)	98 Units / Rail
MC33063ADR2	SOIC-8	2500 Units / Tape & Reel
MC33063ADR2G	SOIC-8 (Pb-Free)	2500 Units / Tape & Reel
MC33063AP1	DIP-8	50 Units / Rail
MC33063AP1G	DIP-8 (Pb-Free)	50 Units / Rail
MC33063AVD	SOIC-8	98 Units / Rail
MC33063AVDG	SOIC-8 (Pb-Free)	98 Units / Rail
MC33063AVDR2	SOIC-8	2500 Units / Tape & Reel
NCV33063AVDR2*	SOIC-8	2500 Units / Tape & Reel
NCV33063AVDR2G	SOIC-8 (Pb-Free)	2500 Units / Tape & Reel
MC33063AVP	DIP-8	50 Units / Rail
MC34063AD	SOIC-8	98 Units / Rail
MC34063ADG	SOIC-8 (Pb-Free)	98 Units / Rail
MC34063ADR2	SOIC-8	2500 Units / Tape & Reel
MC34063ADR2G	SOIC-8 (Pb-Free)	2500 Units / Tape & Reel
MC34063AP1	DIP-8	50 Units / Rail
MC34063AP1G	DIP-8 (Pb-Free)	50 Units / Rail

*NCV33063A: $T_{low} = -40^{\circ}\text{C}$, $T_{high} = +125^{\circ}\text{C}$. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.

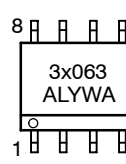
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MARKING DIAGRAMS

PDIP-8
P, P1 SUFFIX
CASE 626



SOIC-8
D SUFFIX
CASE 751



x = 3 or 4
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

MC34163, MC33163

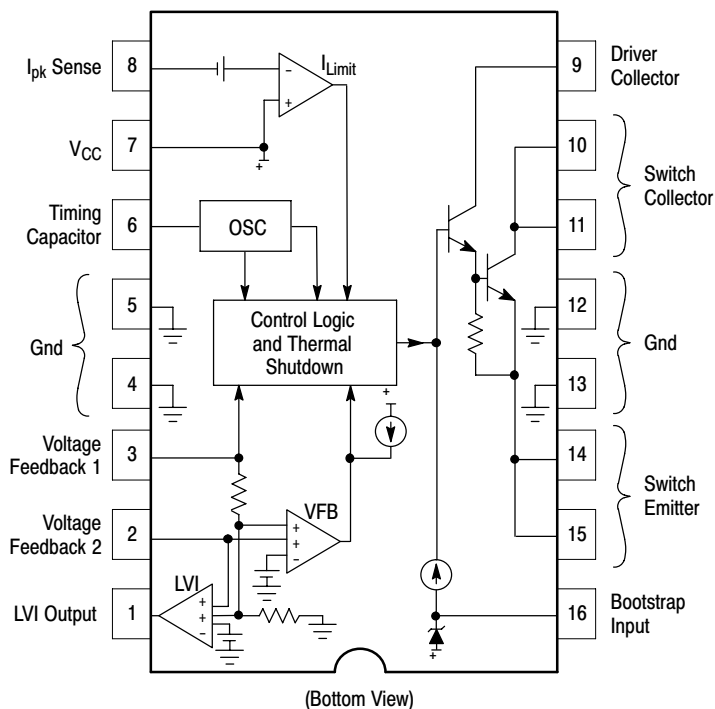
3.4 A, Step-Up/Down/Inverting Switching Regulators

The MC34163 series are monolithic power switching regulators that contain the primary functions required for dc-to-dc converters. This series is specifically designed to be incorporated in step-up, step-down, and voltage-inverting applications with a minimum number of external components.

These devices consist of two high gain voltage feedback comparators, temperature compensated reference, controlled duty cycle oscillator, driver with bootstrap capability for increased efficiency, and a high current output switch. Protective features consist of cycle-by-cycle current limiting, and internal thermal shutdown. Also included is a low voltage indicator output designed to interface with microprocessor based systems.

These devices are contained in a 16 pin dual-in-line heat tab plastic package for improved thermal conduction.

- Output Switch Current in Excess of 3.0 A
- Operation from 2.5 V to 40 V Input
- Low Standby Current
- Precision 2% Reference
- Controlled Duty Cycle Oscillator
- Driver with Bootstrap Capability for Increased Efficiency
- Cycle-by-Cycle Current Limiting
- Internal Thermal Shutdown Protection
- Low Voltage Indicator Output for Direct Microprocessor Interface
- Heat Tab Power Package
- Moisture Sensitivity Level (MSL) Equals 1



This device contains 114 active transistors.

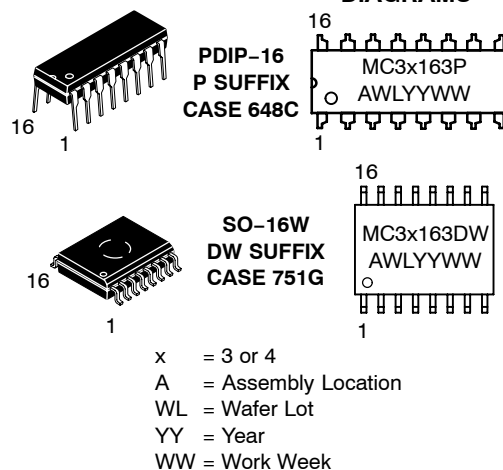
Figure 1. Representative Block Diagram



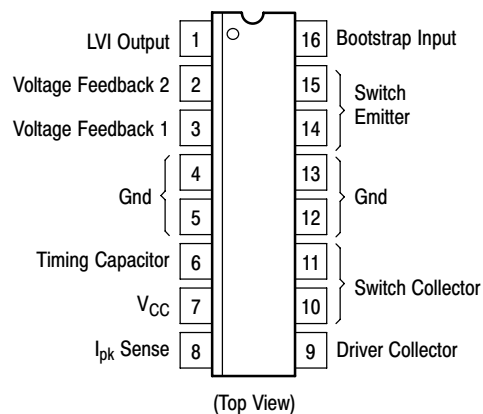
ON Semiconductor™

<http://onsemi.com>

MARKING DIAGRAMS



PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping
MC33163DW	SO-16W	47 Units/Rail
MC33163DWR2	SO-16W	1000 Tape & Reel
MC33163P	PDIP-16	25 Units/Rail
MC34163DW	SO-16W	47 Units/Rail
MC34163DWR2	SO-16W	1000 Tape & Reel
MC34163P	PDIP-16	25 Units/Rail

MC34163, MC33163

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Switch Collector Voltage Range	$V_{C(switch)}$	-1.0 to +40	V
Switch Emitter Voltage Range	$V_{E(switch)}$	-2.0 to $V_{C(switch)}$	V
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	V
Switch Current (Note 2)	I_{SW}	3.4	A
Driver Collector Voltage	$V_{C(driver)}$	-1.0 to +40	V
Driver Collector Current	$I_{C(driver)}$	150	mA
Bootstrap Input Current Range (Note 2)	I_{BS}	-100 to +100	mA
Current Sense Input Voltage Range	$V_{lpk (Sense)}$	$(V_{CC}-7.0)$ to $(V_{CC}+1.0)$	V
Feedback and Timing Capacitor Input Voltage Range	V_{in}	-1.0 to +7.0	V
Low Voltage Indicator Output Voltage Range	$V_{C(LVI)}$	-1.0 to +40	V
Low Voltage Indicator Output Sink Current	$I_{C(LVI)}$	10	mA
Thermal Characteristics			°C/W
P Suffix, Dual-In-Line Case 648C			
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	80	
Thermal Resistance, Junction-to-Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	15	
DW Suffix, Surface Mount Case 751G			
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	94	
Thermal Resistance, Junction-to-Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	18	
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 4)	T_A		°C
MC34163		0 to +70	
MC33163		-40 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15$ V, Pin 16 = V_{CC} , $C_T = 620$ pF, for typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies (Note 4), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit

OSCILLATOR

Frequency $T_A = 25^\circ\text{C}$ Total Variation over $V_{CC} = 2.5$ V to 40 V, and Temperature	f_{OSC}	46 45	50 -	54 55	kHz
Charge Current	I_{chg}	-	225	-	μA
Discharge Current	I_{dischg}	-	25	-	μA
Charge to Discharge Current Ratio	I_{chg}/I_{dischg}	8.0	9.0	10	-
Sawtooth Peak Voltage	$V_{OSC(P)}$	-	1.25	-	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	-	0.55	-	V

FEEDBACK COMPARATOR 1

Threshold Voltage $T_A = 25^\circ\text{C}$ Line Regulation ($V_{CC} = 2.5$ V to 40 V, $T_A = 25^\circ\text{C}$) Total Variation over Line, and Temperature	$V_{th(FB1)}$	4.9 - 4.85	5.05 0.008 -	5.2 0.03 5.25	V %/V V
Input Bias Current ($V_{FB1} = 5.05$ V)	$I_{IB(FB1)}$	-	100	200	μA

- This device series contains ESD protection and exceeds the following tests:
Human Body Model 1500 V per MIL-STD-883, Method 3015.
Machine Model Method 150 V.
- Maximum package power dissipation limits must be observed.
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
- $T_{low} = 0^\circ\text{C}$ for MC34163
 $T_{high} = +70^\circ\text{C}$ for MC34163
 $T_{low} = -40^\circ\text{C}$ for MC33163
 $T_{high} = +85^\circ\text{C}$ for MC33163

MC34163, MC33163

ELECTRICAL CHARACTERISTICS (continued) ($V_{CC} = 15\text{ V}$, Pin 16 = V_{CC} , $C_T = 620\text{ pF}$, for typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies (Note 6), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit

FEEDBACK COMPARATOR 2

Threshold Voltage $T_A = 25^\circ\text{C}$ Line Regulation ($V_{CC} = 2.5\text{ V to } 40\text{ V}$, $T_A = 25^\circ\text{C}$) Total Variation over Line, and Temperature	$V_{th}(FB2)$	1.225 – 1.213	1.25 0.008 –	1.275 0.03 1.287	V %/V V
Input Bias Current ($V_{FB2} = 1.25\text{ V}$)	$I_{IB}(FB2)$	– 0.4	0	0.4	μA

CURRENT LIMIT COMPARATOR

Threshold Voltage $T_A = 25^\circ\text{C}$ Total Variation over $V_{CC} = 2.5\text{ V to } 40\text{ V}$, and Temperature	$V_{th}(I_{pk}\text{ Sense})$	– 230	250 –	– 270	mV
Input Bias Current ($V_{I_{pk}}(\text{Sense}) = 15\text{ V}$)	$I_{IB}(\text{sense})$	–	1.0	20	μA

DRIVER AND OUTPUT SWITCH (Note 5)

Sink Saturation Voltage ($I_{SW} = 2.5\text{ A}$, Pins 14, 15 grounded) Non-Darlington Connection ($R_{Pin\ 9} = 110\ \Omega$ to V_{CC} , $I_{SW}/I_{DRV} \approx 20$) Darlington Connection (Pins 9, 10, 11 connected)	$V_{CE(sat)}$	– –	0.6 1.0	1.0 1.4	V
Collector Off-State Leakage Current ($V_{CE} = 40\text{ V}$)	$I_{C(off)}$	–	0.02	100	μA
Bootstrap Input Current Source ($V_{BS} = V_{CC} + 5.0\text{ V}$)	$I_{source}(DRV)$	0.5	2.0	4.0	mA
Bootstrap Input Zener Clamp Voltage ($I_Z = 25\text{ mA}$)	V_Z	$V_{CC} + 6.0$	$V_{CC} + 7.0$	$V_{CC} + 9.0$	V

LOW VOLTAGE INDICATOR

Input Threshold (V_{FB2} Increasing)	V_{th}	1.07	1.125	1.18	V
Input Hysteresis (V_{FB2} Decreasing)	V_H	–	15	–	mV
Output Sink Saturation Voltage ($I_{sink} = 2.0\text{ mA}$)	$V_{OL}(LVI)$	–	0.15	0.4	V
Output Off-State Leakage Current ($V_{OH} = 15\text{ V}$)	I_{OH}	–	0.01	5.0	μA

TOTAL DEVICE

Standby Supply Current ($V_{CC} = 2.5\text{ V to } 40\text{ V}$, Pin 8 = V_{CC} , Pins 6, 14, 15 = Gnd, remaining pins open)	I_{CC}	–	6.0	10	mA

5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

6. $T_{low} = 0^\circ\text{C}$ for MC34163 $T_{high} = +70^\circ\text{C}$ for MC34163
 $= -40^\circ\text{C}$ for MC33163 $= +85^\circ\text{C}$ for MC33163

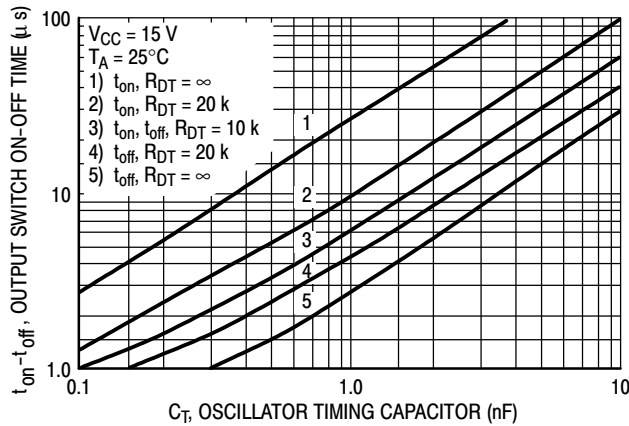


Figure 2. Output Switch On-Off Time versus Oscillator Timing Capacitor

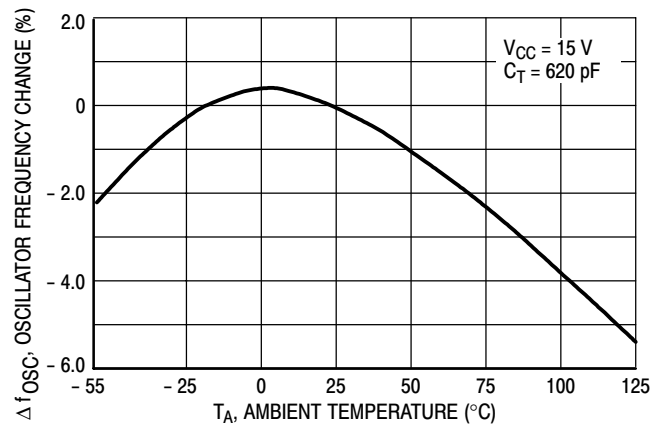


Figure 3. Oscillator Frequency Change versus Temperature

MC34163, MC33163

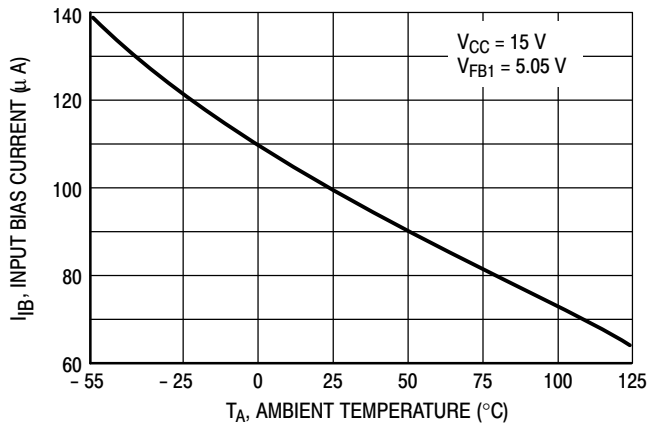


Figure 4. Feedback Comparator 1 Input Bias Current versus Temperature

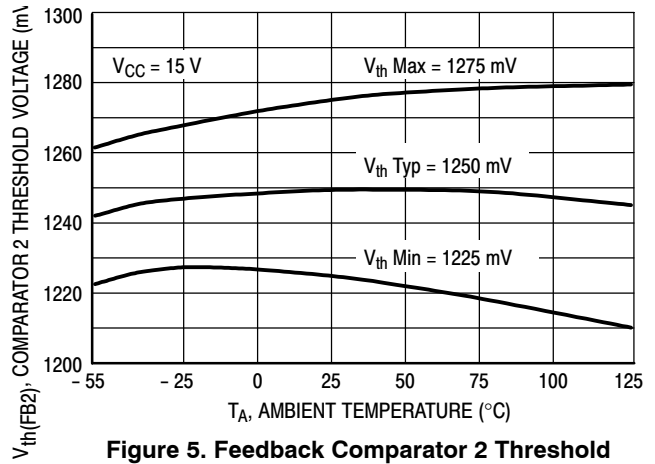


Figure 5. Feedback Comparator 2 Threshold Voltage versus Temperature

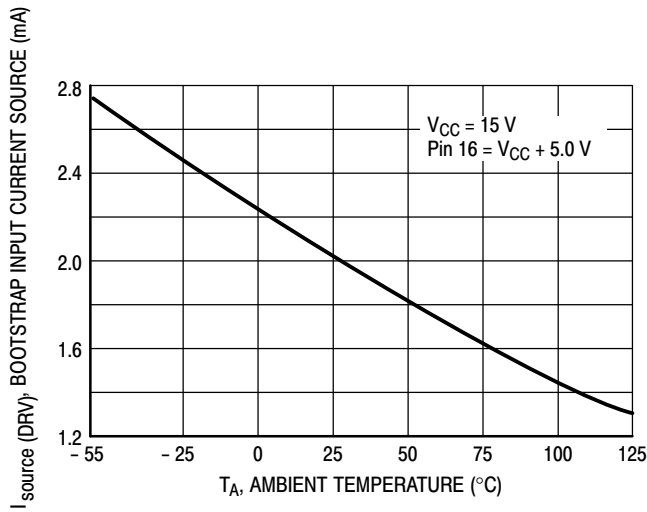


Figure 6. Bootstrap Input Current Source versus Temperature

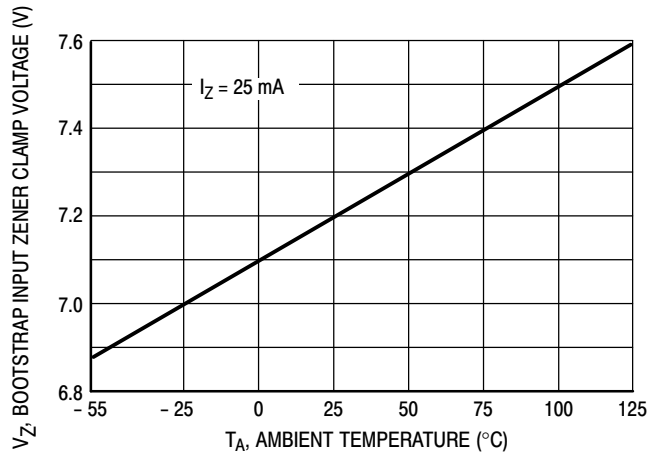


Figure 7. Bootstrap Input Zener Clamp Voltage versus Temperature

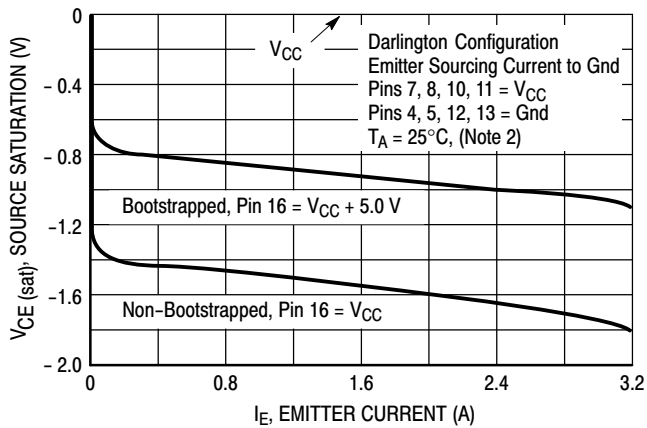


Figure 8. Output Switch Source Saturation versus Emitter Current

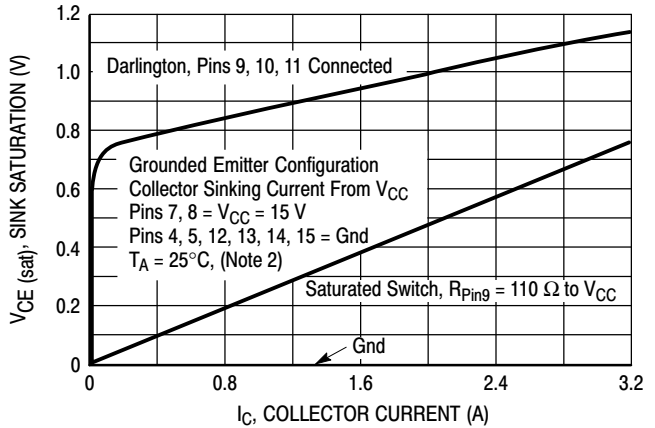


Figure 9. Output Switch Sink Saturation versus Collector Current

MC34163, MC33163

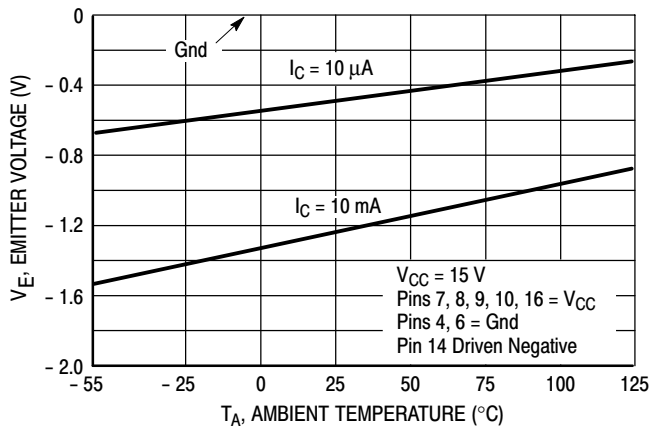


Figure 10. Output Switch Negative Emitter Voltage versus Temperature

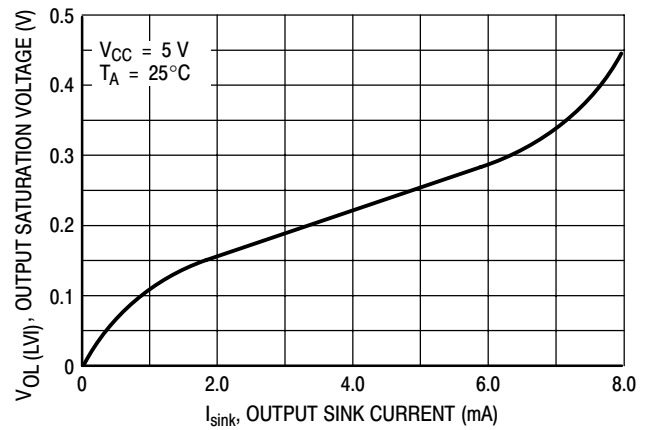


Figure 11. Low Voltage Indicator Output Sink Saturation Voltage versus Sink Current

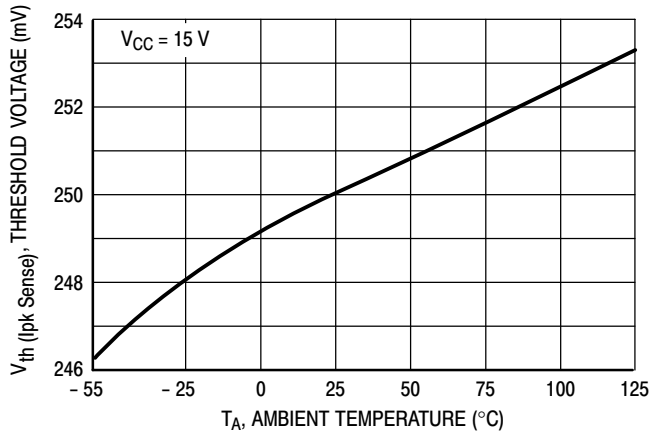


Figure 12. Current Limit Comparator Threshold Voltage versus Temperature

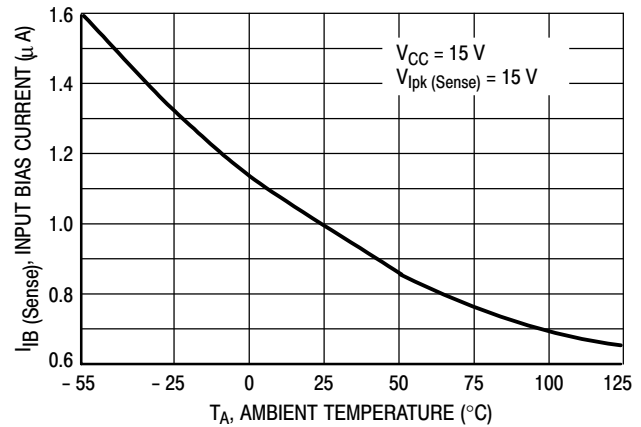


Figure 13. Current Limit Comparator Input Bias Current versus Temperature

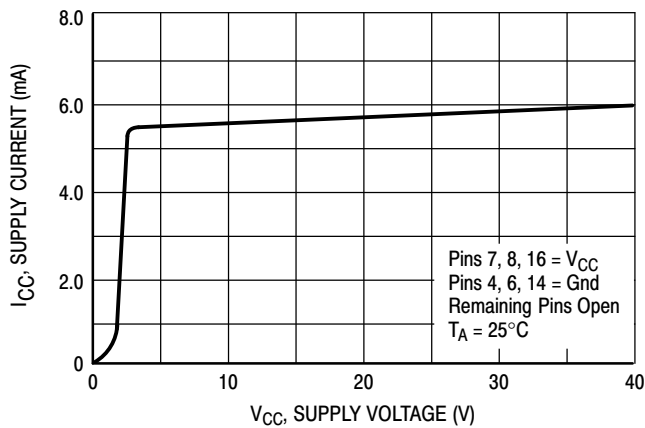


Figure 14. Standby Supply Current versus Supply Voltage

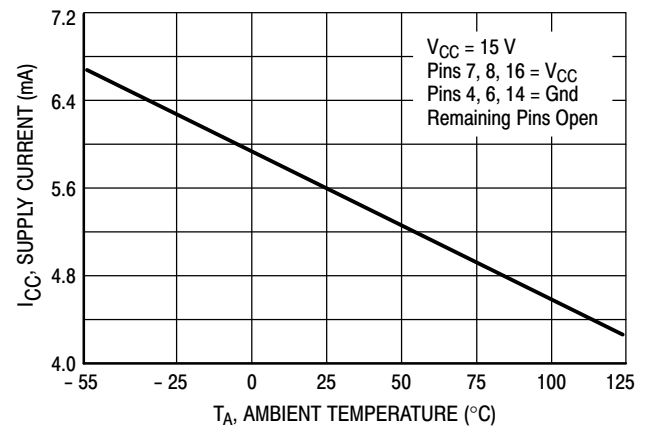


Figure 15. Standby Supply Current versus Temperature

MC34163, MC33163

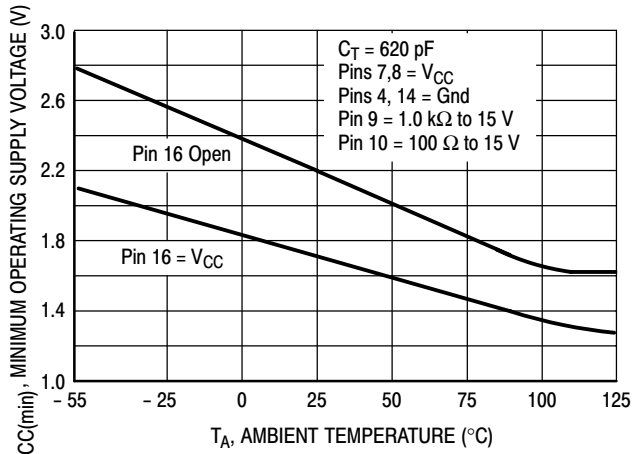


Figure 16. Minimum Operating Supply Voltage versus Temperature

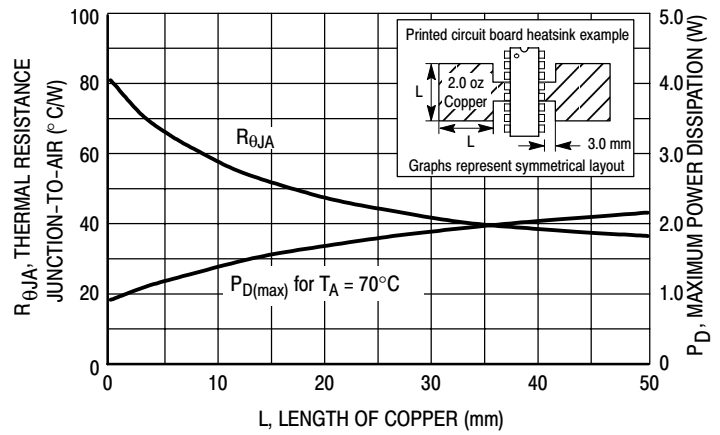


Figure 17. P Suffix (DIP-16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

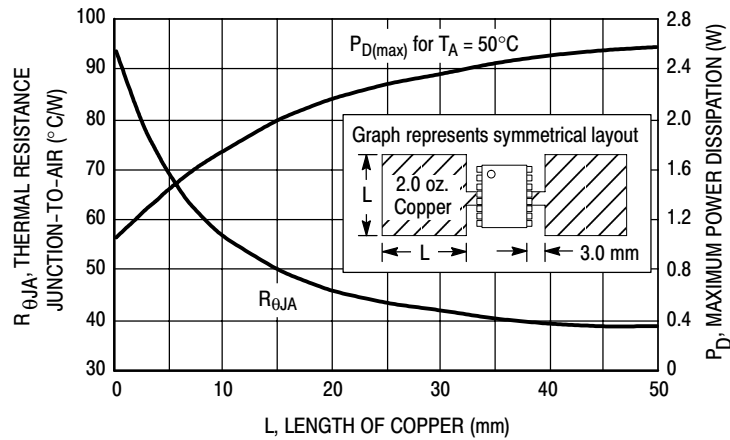


Figure 18. DW Suffix (SOP-16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

MC34163, MC33163

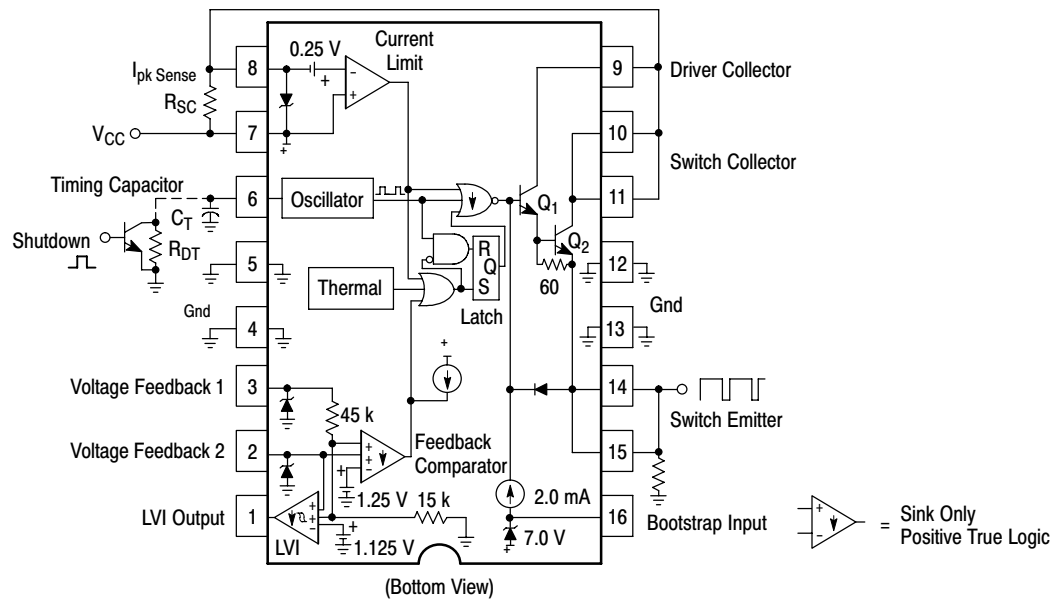


Figure 19. Representative Block Diagram

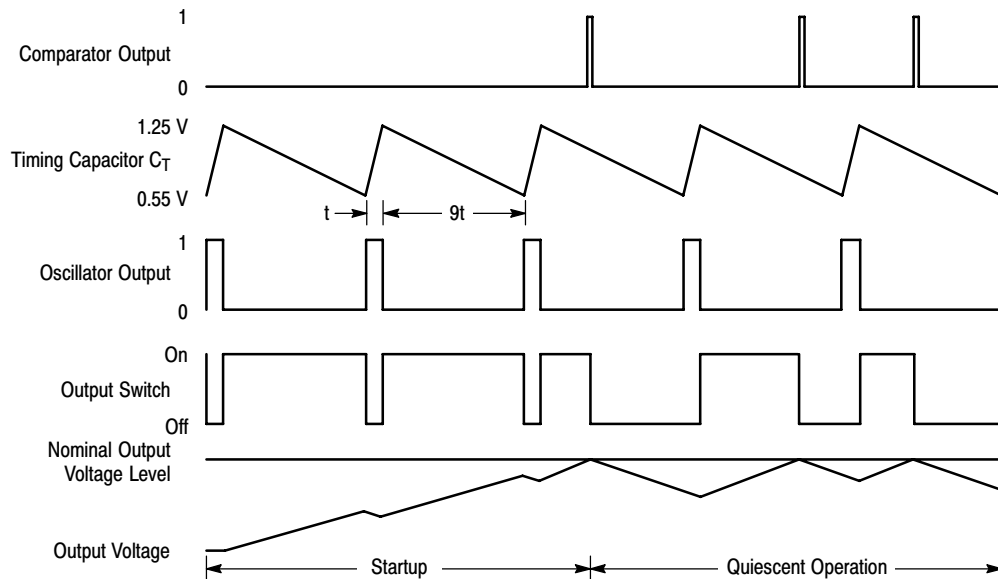


Figure 20. Typical Operating Waveforms

INTRODUCTION

The MC34163 series are monolithic power switching regulators optimized for dc-to-dc converter applications. The combination of features in this series enables the system designer to directly implement step-up, step-down, and voltage-inverting converters with a minimum number of external components. Potential applications include cost sensitive consumer products as well as equipment for the automotive, computer, and industrial markets. A Representative Block Diagram is shown in Figure 19.

OPERATING DESCRIPTION

The MC34163 operates as a fixed on-time, variable off-time voltage mode ripple regulator. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The Typical Operating Waveforms are shown in Figure 20. The output voltage waveform shown is for a step-down converter with the ripple and phasing exaggerated for clarity. During initial converter startup, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal, the feedback comparator sets the latch, immediately terminating switch conduction. The feedback comparator will inhibit the switch until the load current causes the output voltage to fall below nominal. Under these conditions, output switch conduction can be inhibited for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles.

Oscillator

The oscillator frequency and on-time of the output switch are programmed by the value selected for timing capacitor C_T . Capacitor C_T is charged and discharged by a 9 to 1 ratio internal current source and sink, generating a negative going sawtooth waveform at Pin 6. As C_T charges, an internal pulse is generated at the oscillator output. This pulse is connected to the NOR gate center input, preventing output switch conduction, and to the AND gate upper input, allowing the latch to be reset if the comparator output is low. Thus, the output switch is always disabled during ramp-up and can be enabled by the comparator output only at the start of ramp-down. The oscillator peak and valley thresholds are 1.25 V and 0.55 V, respectively, with a charge current of 225 μ A and a discharge current of 25 μ A, yielding a maximum on-time duty cycle of 90%. A reduction of the maximum duty cycle may be required for specific converter configurations. This can be accomplished with the addition of an external deadtime resistor (R_{DT}) placed across C_T . The

resistor increases the discharge current which reduces the on-time of the output switch. A graph of the Output Switch On-Off Time versus Oscillator Timing Capacitance for various values of R_{DT} is shown in Figure 2. Note that the maximum output duty cycle, $t_{on}/t_{on} + t_{off}$, remains constant for values of C_T greater than 0.2 nF. The converter output can be inhibited by clamping C_T to ground with an external NPN small-signal transistor.

Feedback and Low Voltage Indicator Comparators

Output voltage control is established by the Feedback comparator. The inverting input is internally biased at 1.25 V and is not pinned out. The converter output voltage is typically divided down with two external resistors and monitored by the high impedance noninverting input at Pin 2. The maximum input bias current is $\pm 0.4 \mu$ A, which can cause an output voltage error that is equal to the product of the input bias current and the upper divider resistance value. For applications that require 5.0 V, the converter output can be directly connected to the noninverting input at Pin 3. The high impedance input, Pin 2, must be grounded to prevent noise pickup. The internal resistor divider is set for a nominal voltage of 5.05 V. The additional 50 mV compensates for a 1.0% voltage drop in the cable and connector from the converter output to the load. The Feedback comparator's output state is controlled by the highest voltage applied to either of the two noninverting inputs.

The Low Voltage Indicator (LVI) comparator is designed for use as a reset controller in microprocessor-based systems. The inverting input is internally biased at 1.125 V, which sets the noninverting input thresholds to 90% of nominal. The LVI comparator has 15 mV of hysteresis to prevent erratic reset operation. The Open Collector output is capable of sinking in excess of 6.0 mA (see Figure 11). An external resistor (R_{LVI}) and capacitor (C_{DLY}) can be used to program a reset delay time (t_{DLY}) by the formula shown below, where $V_{th(MPU)}$ is the microprocessor reset input threshold. Refer to Figure 21.

$$t_{DLY} = R_{LVI} C_{DLY} \ln \left(\frac{1}{1 - \frac{V_{th(MPU)}}{V_{out}}} \right)$$

Current Limit Comparator, Latch and Thermal Shutdown

With a voltage mode ripple converter operating under normal conditions, output switch conduction is initiated by the oscillator and terminated by the Voltage Feedback comparator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the Current Limit comparator will protect the Output Switch.

The switch current is converted to a voltage by inserting a fractional ohm resistor, R_{SC} , in series with V_{CC} and output switch transistor Q_2 . The voltage drop across R_{SC} is monitored by the Current Sense comparator. If the voltage drop exceeds 250 mV with respect to V_{CC} , the comparator will set the latch and terminate output switch conduction on a cycle-by-cycle basis. This Comparator/Latch configuration ensures that the Output Switch has only a single on-time during a given oscillator cycle. The calculation for a value of R_{SC} is:

$$R_{SC} = \frac{0.25 \text{ V}}{I_{pk} (\text{Switch})}$$

Figures 12 and 13 show that the Current Sense comparator threshold is tightly controlled over temperature and has a typical input bias current of 1.0 μA . The propagation delay from the comparator input to the Output Switch is typically 200 ns. The parasitic inductance associated with R_{SC} and the circuit layout should be minimized. This will prevent unwanted voltage spikes that may falsely trip the Current Limit comparator.

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the Latch is forced into the “Set” state, disabling the Output Switch. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.

Driver and Output Switch

To aid in system design flexibility and conversion efficiency, the driver current source and collector, and output switch collector and emitter are pinned out separately. This allows the designer the option of driving the output switch into saturation with a selected force gain or driving it near saturation when connected as a Darlington. The output switch has a typical current gain of 70 at 2.5 A and is designed to switch a maximum of 40 V collector to emitter, with up to 3.4 A peak collector current. The minimum value for R_{SC} is:

$$R_{SC}(\text{min}) = \frac{0.25 \text{ V}}{3.4 \text{ A}} = 0.0735 \Omega$$

When configured for step-down or voltage-inverting applications, as in Figures 21 and 25, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn-on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing

additional device heating and reduced conversion efficiency.

Figure 10 shows that by clamping the emitter to 0.5 V, the collector current will be in the range 10 μA over temperature. A 1N5822 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

A bootstrap input is provided to reduce the output switch saturation voltage in step-down and voltage-inverting converter applications. This input is connected through a series resistor and capacitor to the switch emitter and is used to raise the internal 2.0 mA bias current source above V_{CC} . An internal zener limits the bootstrap input voltage to $V_{CC} + 7.0 \text{ V}$. The capacitor's equivalent series resistance must limit the zener current to less than 100 mA. An additional series resistor may be required when using tantalum or other low ESR capacitors. The equation below is used to calculate a minimum value bootstrap capacitor based on a minimum zener voltage and an upper limit current source.

$$C_B(\text{min}) = I \frac{\Delta t}{\Delta V} = 4.0 \text{ mA} \frac{t_{on}}{4.0 \text{ V}} = 0.001 t_{on}$$

Parametric operation of the MC34163 is guaranteed over a supply voltage range of 2.5 V to 40 V. When operating below 3.0 V, the Bootstrap Input should be connected to V_{CC} . Figure 16 shows that functional operation down to 1.7 V at room temperature is possible.

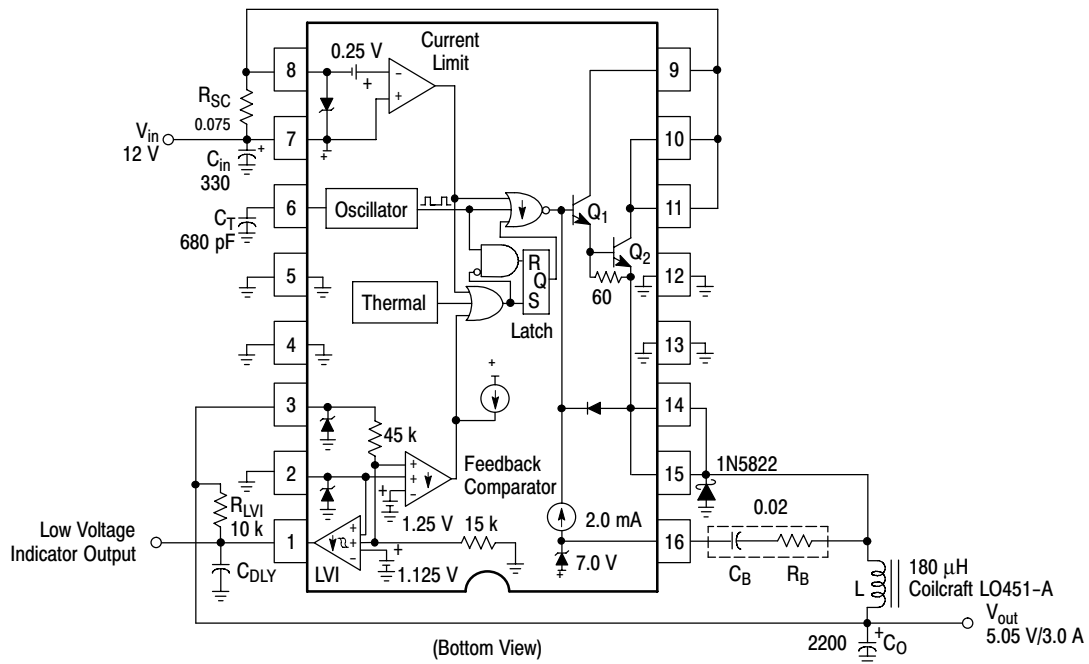
Package

The MC34163 is contained in a heatsinkable 16-lead plastic dual-in-line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 17 and 18 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction-to-air thermal resistance. These examples are for a symmetrical layout on a single-sided board with two ounce per square foot of copper.

APPLICATIONS

The following converter applications show the simplicity and flexibility of this circuit architecture. Three main converter topologies are demonstrated with actual test data shown below each of the circuit diagrams.

MC34163, MC33163



Test	Condition	Results
Line Regulation	$V_{in} = 8.0 \text{ V to } 24 \text{ V}$, $I_O = 3.0 \text{ A}$	$6.0 \text{ mV} = \pm 0.06\%$
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 0.6 \text{ A to } 3.0 \text{ A}$	$2.0 \text{ mV} = \pm 0.02\%$
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 3.0 \text{ A}$	36 mVpp
Short Circuit Current	$V_{in} = 12 \text{ V}$, $R_L = 0.1 \Omega$	3.3 A
Efficiency, Without Bootstrap	$V_{in} = 12 \text{ V}$, $I_O = 3.0 \text{ A}$	76.7%
Efficiency, With Bootstrap	$V_{in} = 12 \text{ V}$, $I_O = 3.0 \text{ A}$	81.2%

Figure 21. Step-Down Converter

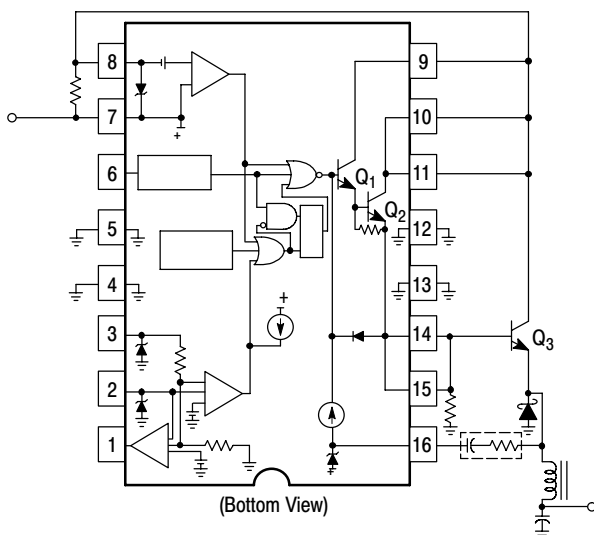


Figure 22A. External NPN Switch

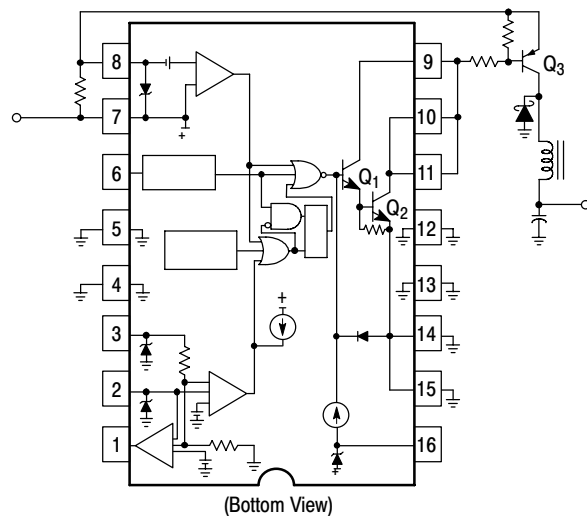
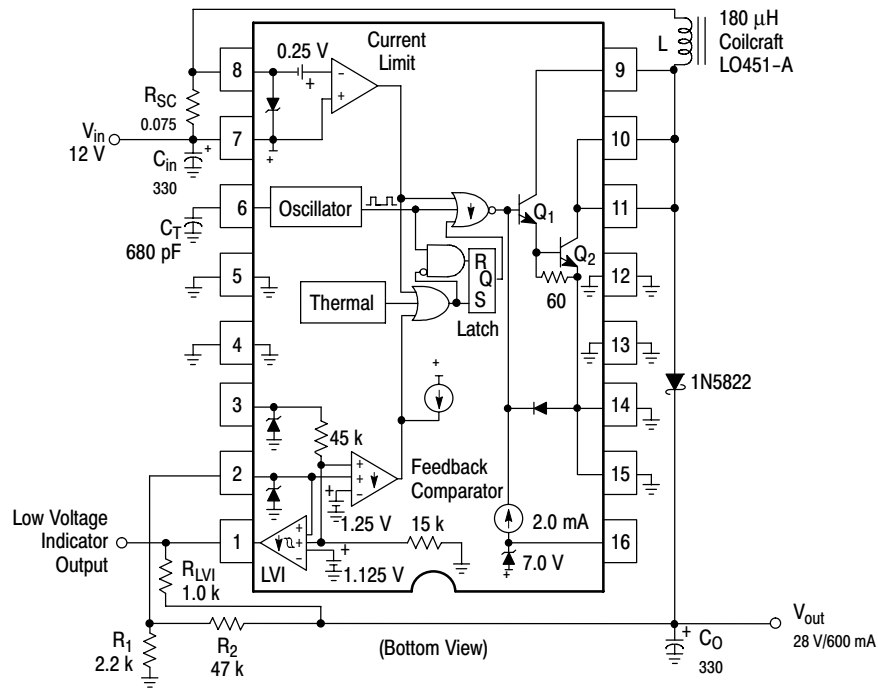


Figure 22B. External PNP Saturated Switch

Figure 22. External Current Boost Connections for $I_{pk} \text{ (Switch) Greater Than } 3.4 \text{ A}$

MC34163, MC33163



Test	Condition	Results
Line Regulation	$V_{in} = 9.0 \text{ V to } 16 \text{ V}$, $I_O = 0.6 \text{ A}$	$30 \text{ mV} = \pm 0.05\%$
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 0.1 \text{ A to } 0.6 \text{ A}$	$50 \text{ mV} = \pm 0.09\%$
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 0.6 \text{ A}$	140 mVpp
Efficiency	$V_{in} = 12 \text{ V}$, $I_O = 0.6 \text{ A}$	88.1%

Figure 23. Step-Up Converter

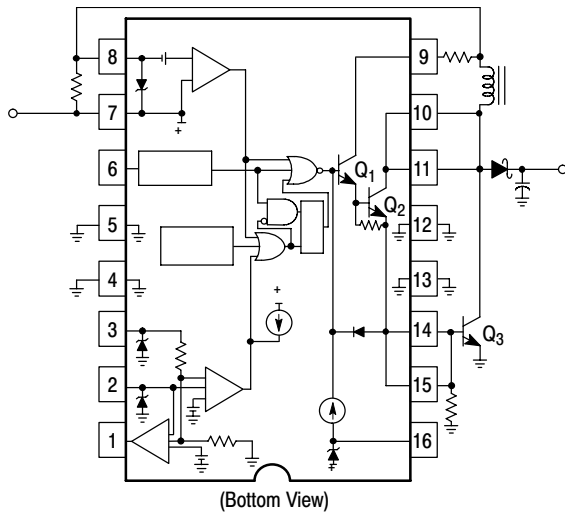


Figure 24A. External NPN Switch

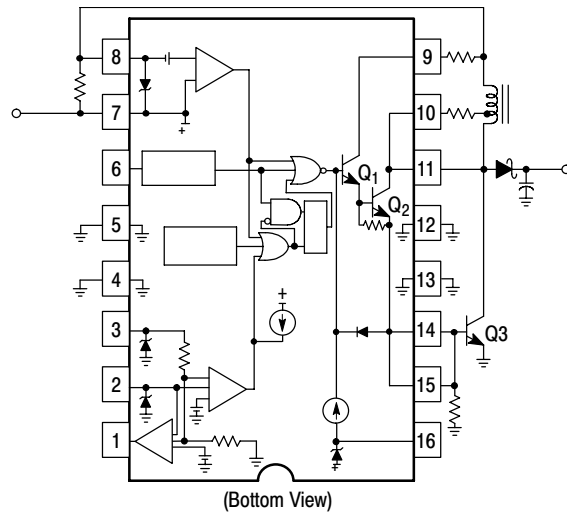
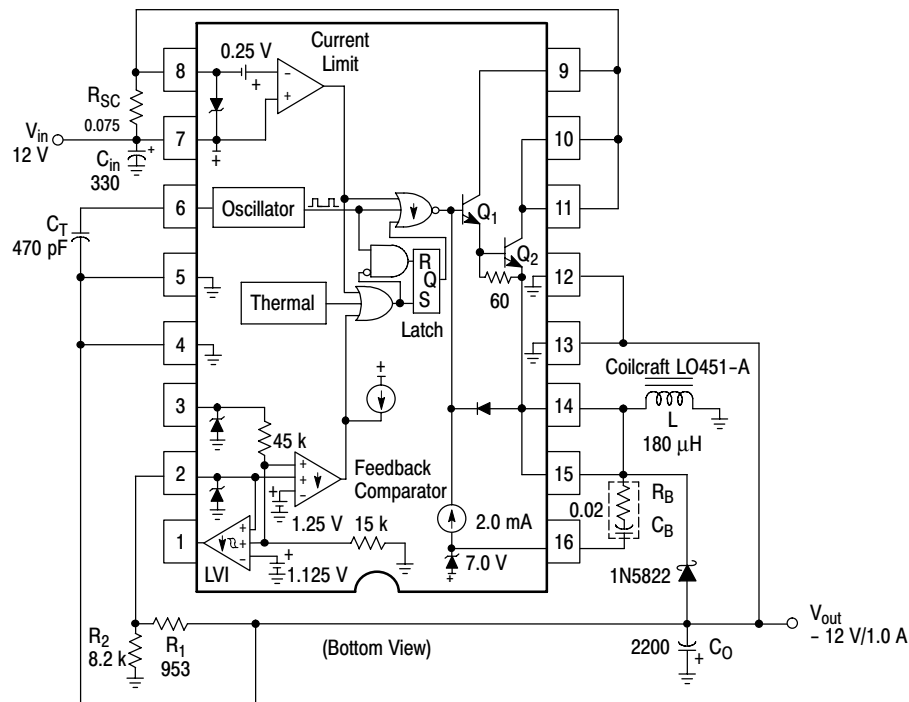


Figure 24B. External PNP Saturated Switch

Figure 24. External Current Boost Connections for $I_{pk} \text{ (Switch) Greater Than } 3.4 \text{ A}$

MC34163, MC33163



Test	Condition	Results
Line Regulation	$V_{in} = 9.0 \text{ V to } 16 \text{ V}$, $I_O = 1.0 \text{ A}$	$5.0 \text{ mV} = \pm 0.02\%$
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 0.6 \text{ A to } 1.0 \text{ A}$	$2.0 \text{ mV} = \pm 0.01\%$
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ A}$	130 mVpp
Short Circuit Current	$V_{in} = 12 \text{ V}$, $R_L = 0.1 \Omega$	3.2 A
Efficiency, Without Bootstrap	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ A}$	73.1%
Efficiency, With Bootstrap	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ A}$	77.5%

Figure 25. Voltage-Inverting Converter

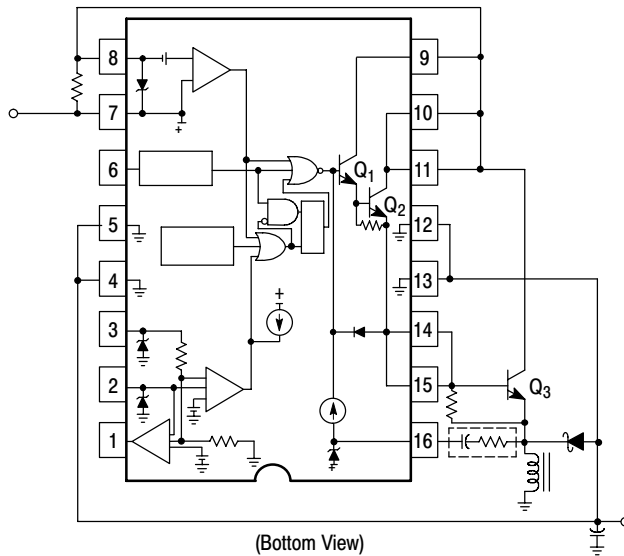


Figure 26A. External NPN Switch

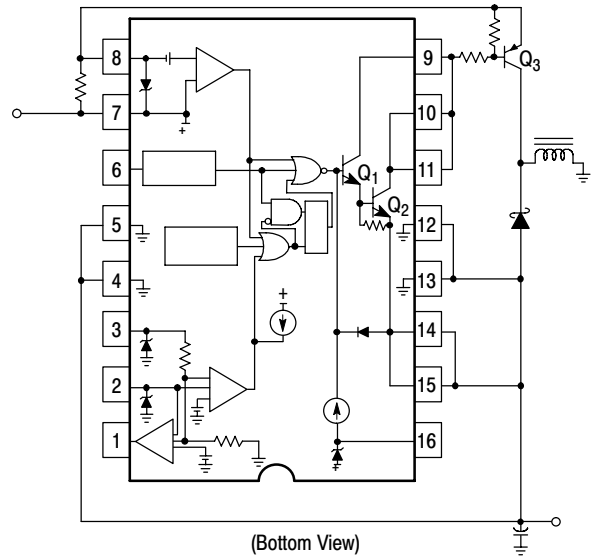
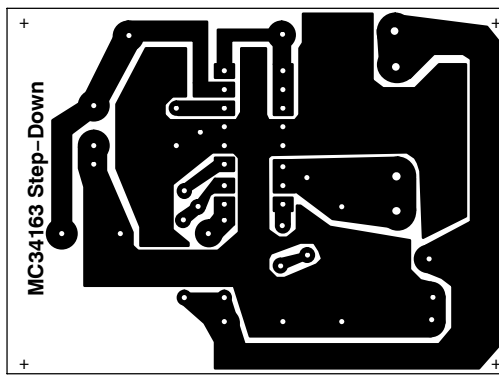


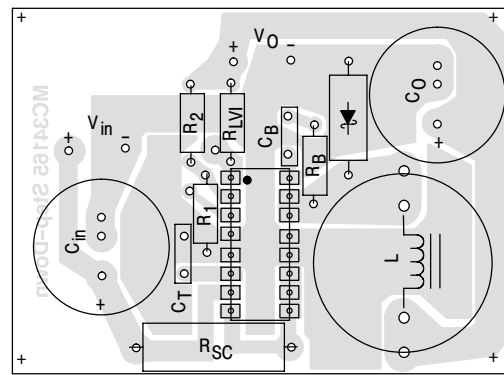
Figure 26B. External PNP Saturated Switch

Figure 26. External Current Boost Connections for $I_{pk} \text{ (Switch)}$ Greater Than 3.4 A

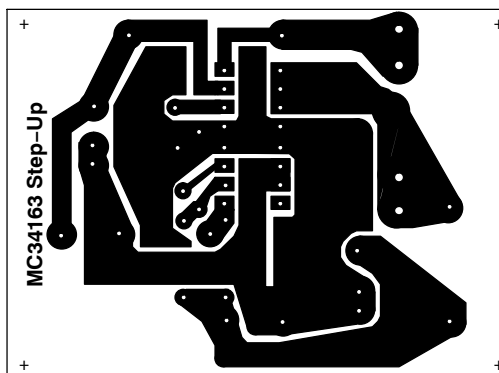
MC34163, MC33163



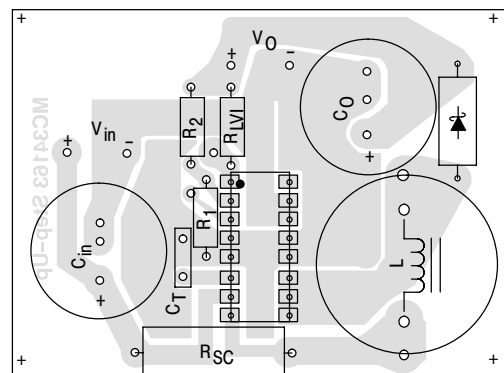
Bottom View



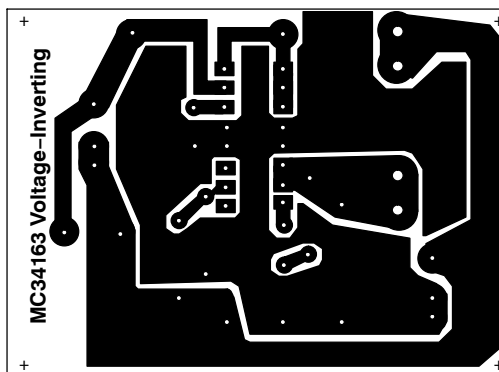
Top View



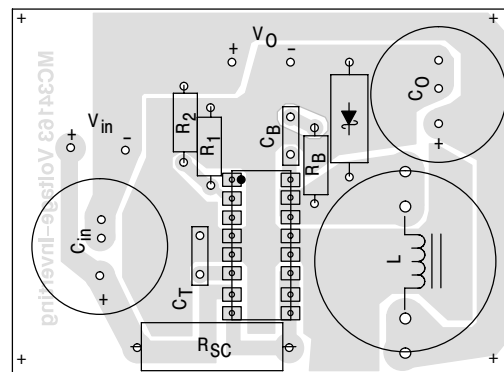
Bottom View



Top View



Bottom View



Top View

All printed circuit boards are 2.58" in width by 1.9" in height.

Figure 27. Printed Circuit Board and Component Layout
(Circuits of Figures 21, 23, 25)

MC34163, MC33163

Calculation	Step-Down	Step-Up	Voltage-Inverting
$\frac{t_{on}}{t_{off}}$ (Notes 1, 2, 3)	$\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in}}{V_{in} - V_{sat}}$	$\frac{ V_{out} + V_F}{V_{in} - V_{sat}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f \left(\frac{t_{on}}{t_{off}} + 1 \right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f \left(\frac{t_{on}}{t_{off}} + 1 \right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f \left(\frac{t_{on}}{t_{off}} + 1 \right)}$
C_T	$\frac{32.143 \cdot 10^{-6}}{f}$	$\frac{32.143 \cdot 10^{-6}}{f}$	$\frac{32.143 \cdot 10^{-6}}{f}$
$I_{L(avg)}$	I_{out}	$I_{out} \left(\frac{t_{on}}{t_{off}} + 1 \right)$	$I_{out} \left(\frac{t_{on}}{t_{off}} + 1 \right)$
$I_{pk} \text{ (Switch)}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$
R_{SC}	$\frac{0.25}{I_{pk} \text{ (Switch)}}$	$\frac{0.25}{I_{pk} \text{ (Switch)}}$	$\frac{0.25}{I_{pk} \text{ (Switch)}}$
L	$\left(\frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L} \right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L} \right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L} \right) t_{on}$
$V_{ripple(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8 \cdot C_O} \right)^2 + (ESR)^2}$	$\approx \frac{t_{on} I_{out}}{C_O}$	$\approx \frac{t_{on} I_{out}}{C_O}$
V_{out}	$V_{ref} \left(\frac{R_2}{R_1} + 1 \right)$	$V_{ref} \left(\frac{R_2}{R_1} + 1 \right)$	$V_{ref} \left(\frac{R_2}{R_1} + 1 \right)$

The following Converter Characteristics must be chosen:

- V_{in} – Nominal operating input voltage.
- V_{out} – Desired output voltage.
- I_{out} – Desired output current.
- ΔI_L – Desired peak-to-peak inductor ripple current. For maximum output current it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L(avg)}$. This will help prevent $I_{pk} \text{ (Switch)}$ from reaching the current limit threshold set by R_{SC} . If the design goal is to use a minimum inductance value, let $\Delta I_L = 2(I_{L(avg)})$. This will proportionally reduce converter output current capability.
- f – Maximum output switch frequency.
- $V_{ripple(pp)}$ – Desired peak-to-peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

- NOTES:**
- V_{sat} – Saturation voltage of the output switch, refer to Figures 8 and 9.
 - V_F – Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.5 V.
 - The calculated t_{on}/t_{off} must not exceed the minimum guaranteed oscillator charge to discharge ratio of 8, at the minimum operating input voltage.

Figure 28. Design Equations

MC34166, MC33166

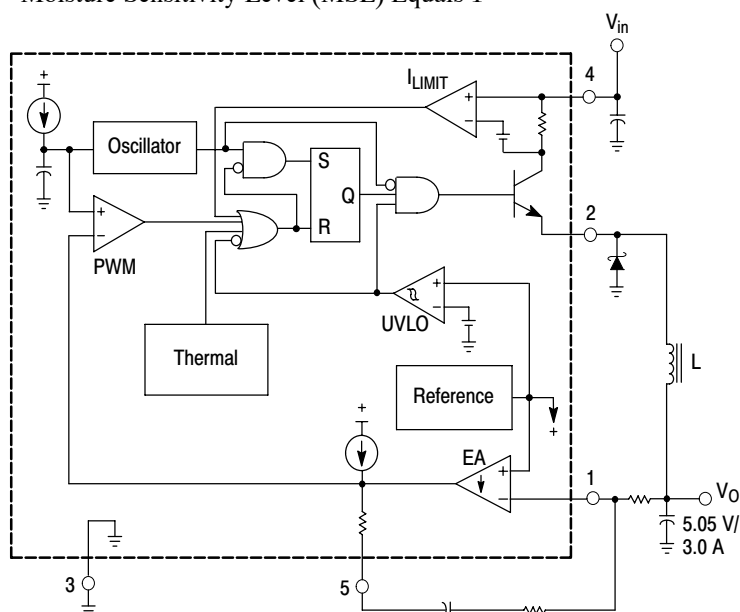
3.0 A, Step-Up/Down/Inverting Switching Regulators

The MC34166, MC33166 series are high performance fixed frequency power switching regulators that contain the primary functions required for dc-to-dc converters. This series was specifically designed to be incorporated in step-down and voltage-inverting configurations with a minimum number of external components and can also be used cost effectively in step-up applications.

These devices consist of an internal temperature compensated reference, fixed frequency oscillator with on-chip timing components, latching pulse width modulator for single pulse metering, high gain error amplifier, and a high current output switch.

Protective features consist of cycle-by-cycle current limiting, undervoltage lockout, and thermal shutdown. Also included is a low power standby mode that reduces power supply current to 36 μ A.

- Output Switch Current in Excess of 3.0 A
- Fixed Frequency Oscillator (72 kHz) with On-Chip Timing
- Provides 5.05 V Output without External Resistor Divider
- Precision 2% Reference
- 0% to 95% Output Duty Cycle
- Cycle-by-Cycle Current Limiting
- Undervoltage Lockout with Hysteresis
- Internal Thermal Shutdown
- Operation from 7.5 V to 40 V
- Standby Mode Reduces Power Supply Current to 36 μ A
- Economical 5-Lead TO-220 Package with Two Optional Leadforms
- Also Available in Surface Mount D²PAK Package
- Moisture Sensitivity Level (MSL) Equals 1



This device contains 143 active transistors.

Figure 1. Simplified Block Diagram
(Step Down Application)

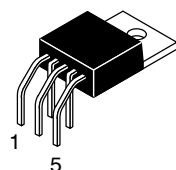


ON Semiconductor™

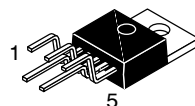
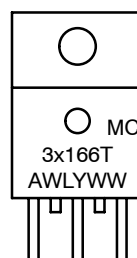
<http://onsemi.com>

x = 3 or 4
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

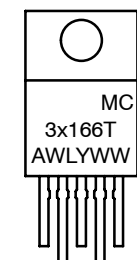
MARKING DIAGRAMS



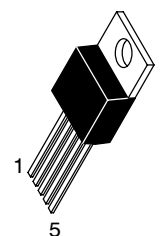
**TO-220
TH SUFFIX
CASE 314A**



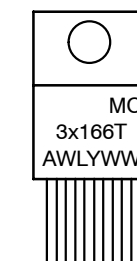
**TO-220
TV SUFFIX
CASE 314B**



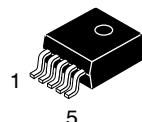
Heatsink surface connected to Pin 3



**TO-220
T SUFFIX
CASE 314D**



- Pin
1. Voltage Feedback Input
 2. Switch Output
 3. Ground
 4. Input Voltage/V_{CC}
 5. Compensation/Standby



**D²PAK
D2T SUFFIX
CASE 936A**



Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 237 of this data sheet.

MC34166, MC33166

MAXIMUM RATINGS (Note 2)

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	40	V
Switch Output Voltage Range	$V_{O(switch)}$	-1.5 to + V_{in}	V
Voltage Feedback and Compensation Input Voltage Range	V_{FB}, V_{Comp}	-1.0 to + 7.0	V
Power Dissipation			
Case 314A, 314B and 314D ($T_A = +25^{\circ}\text{C}$)	P_D	Internally Limited	W
Thermal Resistance, Junction-to-Ambient	θ_{JA}	65	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Case	θ_{JC}	5.0	$^{\circ}\text{C/W}$
Case 936A (D ² PAK) ($T_A = +25^{\circ}\text{C}$)	P_D	Internally Limited	W
Thermal Resistance, Junction-to-Ambient	θ_{JA}	70	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Case	θ_{JC}	5.0	$^{\circ}\text{C/W}$
Operating Junction Temperature	T_J	+150	$^{\circ}\text{C}$
Operating Ambient Temperature (Note 3)	T_A		$^{\circ}\text{C}$
MC34166		0 to + 70	
MC33166		- 40 to + 85	
Storage Temperature Range	T_{stg}	- 65 to +150	$^{\circ}\text{C}$

- Maximum package power dissipation limits must be observed to prevent thermal shutdown activation.
- This device series contains ESD protection and exceeds the following tests:
Human Body Model 2000 V per MIL-STD-883, Method 3015.
Machine Model Method 200 V.
- $T_{low} = 0^{\circ}\text{C}$ for MC34166
 $T_{low} = - 40^{\circ}\text{C}$ for MC33166
 $T_{high} = + 70^{\circ}\text{C}$ for MC34166
 $T_{high} = + 85^{\circ}\text{C}$ for MC33166

MC34166, MC33166

ELECTRICAL CHARACTERISTICS ($V_{CC} = 12\text{ V}$, for typical values $T_A = +25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies [Notes 4, 5], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit

OSCILLATOR

Frequency ($V_{CC} = 7.5\text{ V to } 40\text{ V}$)	$T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}} \text{ to } T_{\text{high}}$	f_{OSC}	65 62	72 –	79 81	kHz

ERROR AMPLIFIER

Voltage Feedback Input Threshold	$T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}} \text{ to } T_{\text{high}}$	$V_{\text{FB(th)}}$	4.95 4.85	5.05 –	5.15 5.2	V
Line Regulation ($V_{CC} = 7.5\text{ V to } 40\text{ V}$, $T_A = +25^\circ\text{C}$)		Reg_{line}	–	0.03	0.078	%/V
Input Bias Current ($V_{\text{FB}} = V_{\text{FB(th)}} + 0.15\text{ V}$)		I_{IB}	–	0.15	1.0	μA
Power Supply Rejection Ratio ($V_{CC} = 10\text{ V to } 20\text{ V}$, $f = 120\text{ Hz}$)		PSRR	60	80	–	dB
Output Voltage Swing						V
High State ($I_{\text{Source}} = 75\text{ }\mu\text{A}$, $V_{\text{FB}} = 4.5\text{ V}$)		V_{OH}	4.2	4.9	–	
Low State ($I_{\text{Sink}} = 0.4\text{ mA}$, $V_{\text{FB}} = 5.5\text{ V}$)		V_{OL}	–	1.6	1.9	

PWM COMPARATOR

Duty Cycle						%
Maximum ($V_{\text{FB}} = 0\text{ V}$)	$\text{DC}_{(\text{max})}$	92	95	100		
Minimum ($V_{\text{Comp}} = 1.9\text{ V}$)	$\text{DC}_{(\text{min})}$	0	0	0		

SWITCH OUTPUT

Output Voltage Source Saturation ($V_{CC} = 7.5\text{ V}$, $I_{\text{Source}} = 3.0\text{ A}$)	V_{sat}	–	($V_{CC} - 1.5$)	($V_{CC} - 1.8$)	V
Off-State Leakage ($V_{CC} = 40\text{ V}$, Pin 2 = Gnd)	$I_{\text{sw(off)}}$	–	0	100	μA
Current Limit Threshold	$I_{\text{pk(switch)}}$	3.3	4.3	6.0	A
Switching Times ($V_{CC} = 40\text{ V}$, $I_{\text{pk}} = 3.0\text{ A}$, $L = 375\text{ }\mu\text{H}$, $T_A = +25^\circ\text{C}$)					ns
Output Voltage Rise Time	t_r	–	100	200	
Output Voltage Fall Time	t_f	–	50	100	

UNDERVOLTAGE LOCKOUT

Startup Threshold (V_{CC} Increasing, $T_A = +25^\circ\text{C}$)	$V_{\text{th(UVLO)}}$	5.5	5.9	6.3	V
Hysteresis (V_{CC} Decreasing, $T_A = +25^\circ\text{C}$)	$V_{\text{H(UVLO)}}$	0.6	0.9	1.2	V

TOTAL DEVICE

Power Supply Current ($T_A = +25^\circ\text{C}$)	I_{CC}				
Standby ($V_{CC} = 12\text{ V}$, $V_{\text{Comp}} < 0.15\text{ V}$)		–	36	100	μA
Operating ($V_{CC} = 40\text{ V}$, Pin 1 = Gnd for maximum duty cycle)		–	31	55	mA

4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
 5. $T_{\text{low}} = 0^\circ\text{C}$ for MC34166 $T_{\text{high}} = +70^\circ\text{C}$ for MC34166
 = -40°C for MC33166 = $+85^\circ\text{C}$ for MC33166

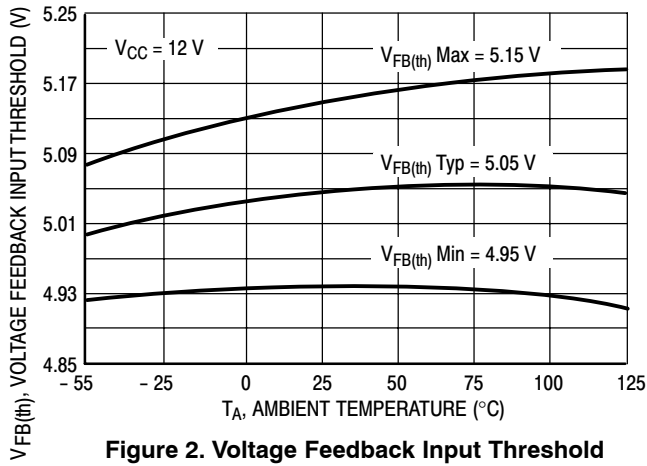


Figure 2. Voltage Feedback Input Threshold versus Temperature

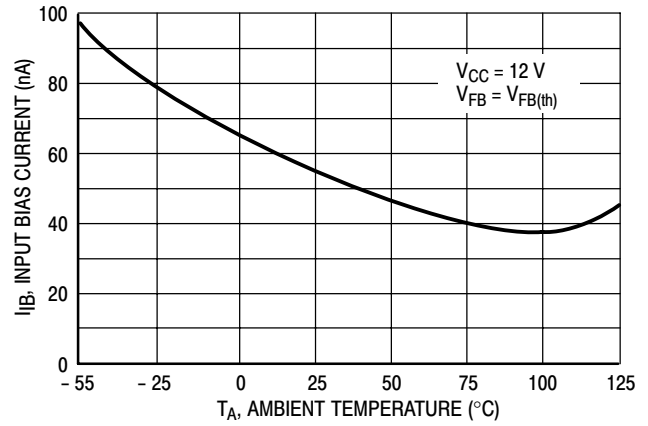


Figure 3. Voltage Feedback Input Bias Current versus Temperature

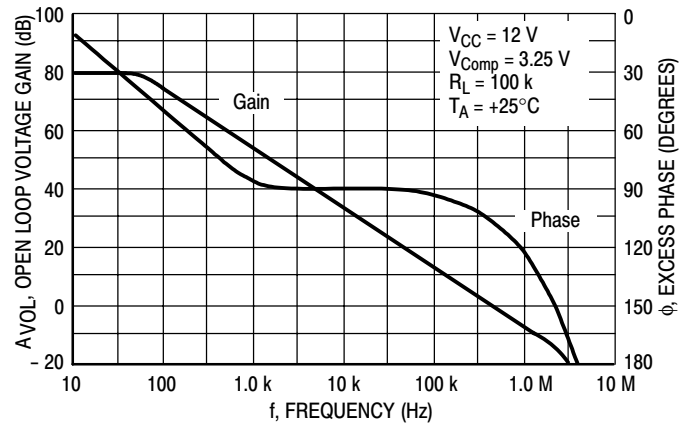


Figure 4. Error Amp Open Loop Gain and Phase versus Frequency

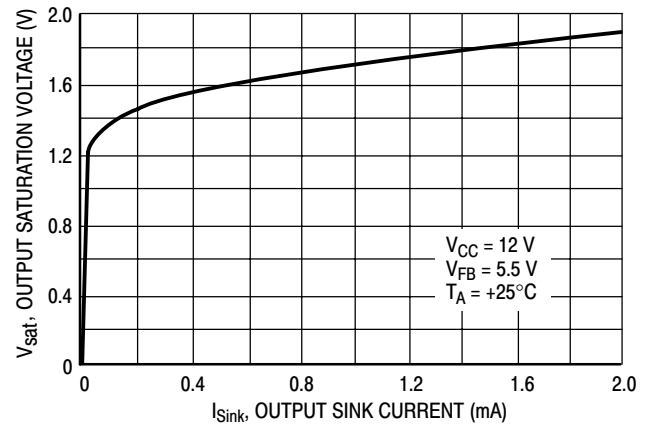


Figure 5. Error Amp Output Saturation versus Sink Current

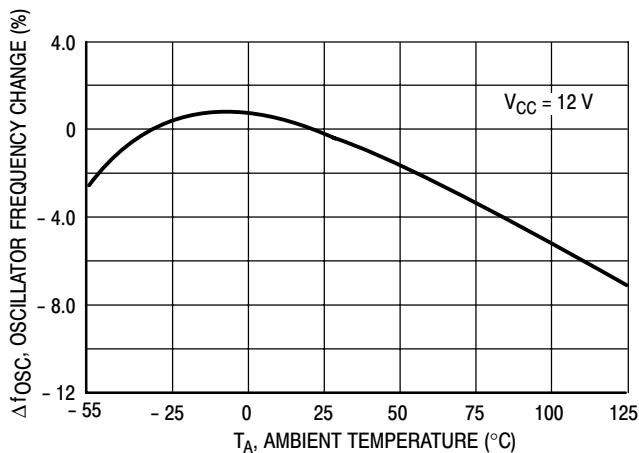


Figure 6. Oscillator Frequency Change versus Temperature

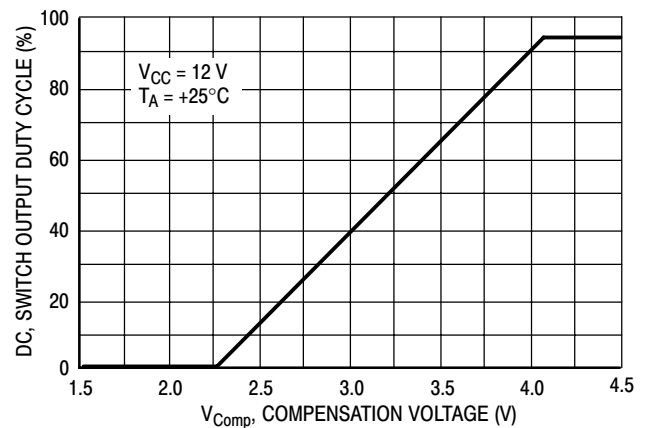


Figure 7. Switch Output Duty Cycle versus Compensation Voltage

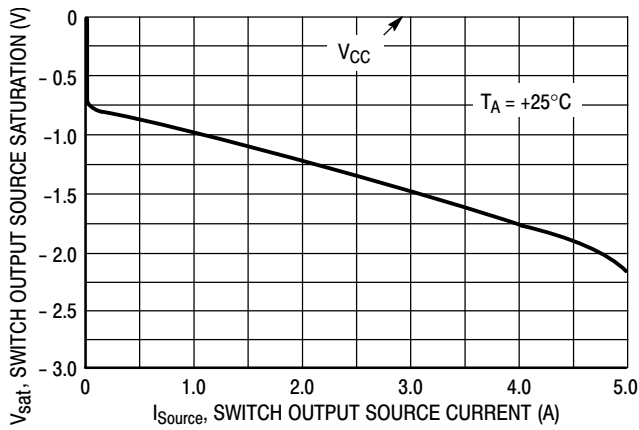


Figure 8. Switch Output Source Saturation versus Source Current

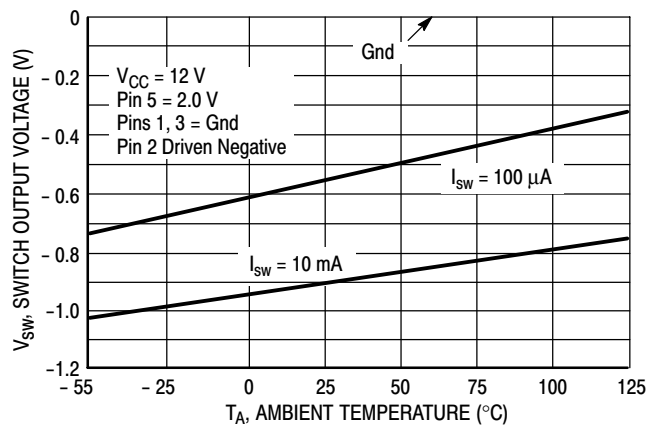


Figure 9. Negative Switch Output Voltage versus Temperature

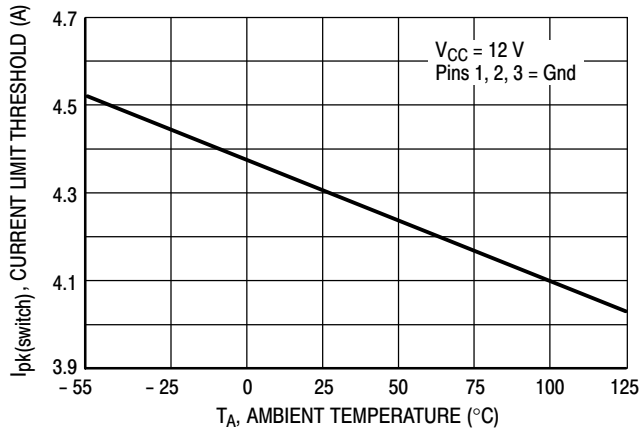


Figure 10. Switch Output Current Limit Threshold versus Temperature

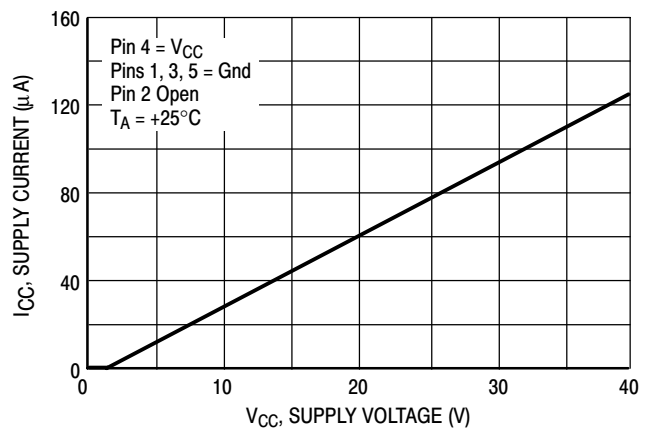


Figure 11. Standby Supply Current versus Supply Voltage

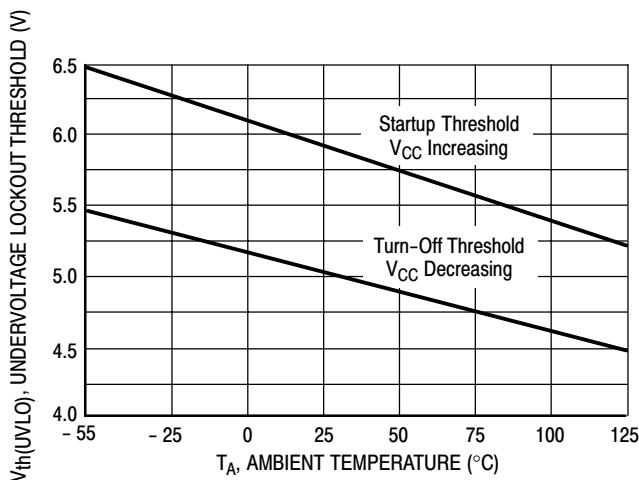


Figure 12. Undervoltage Lockout Threshold versus Temperature

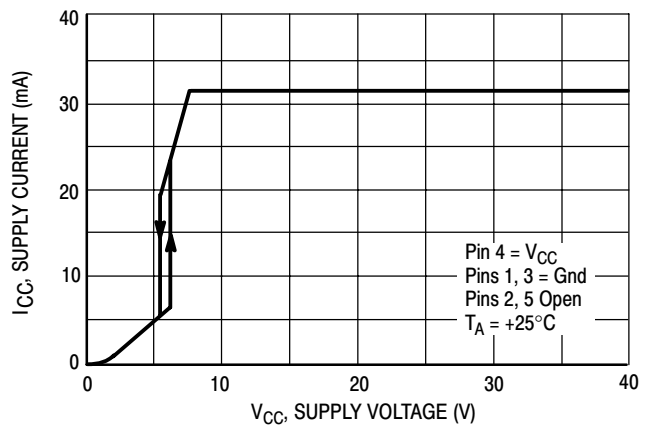


Figure 13. Operating Supply Current versus Supply Voltage

MC34166, MC33166

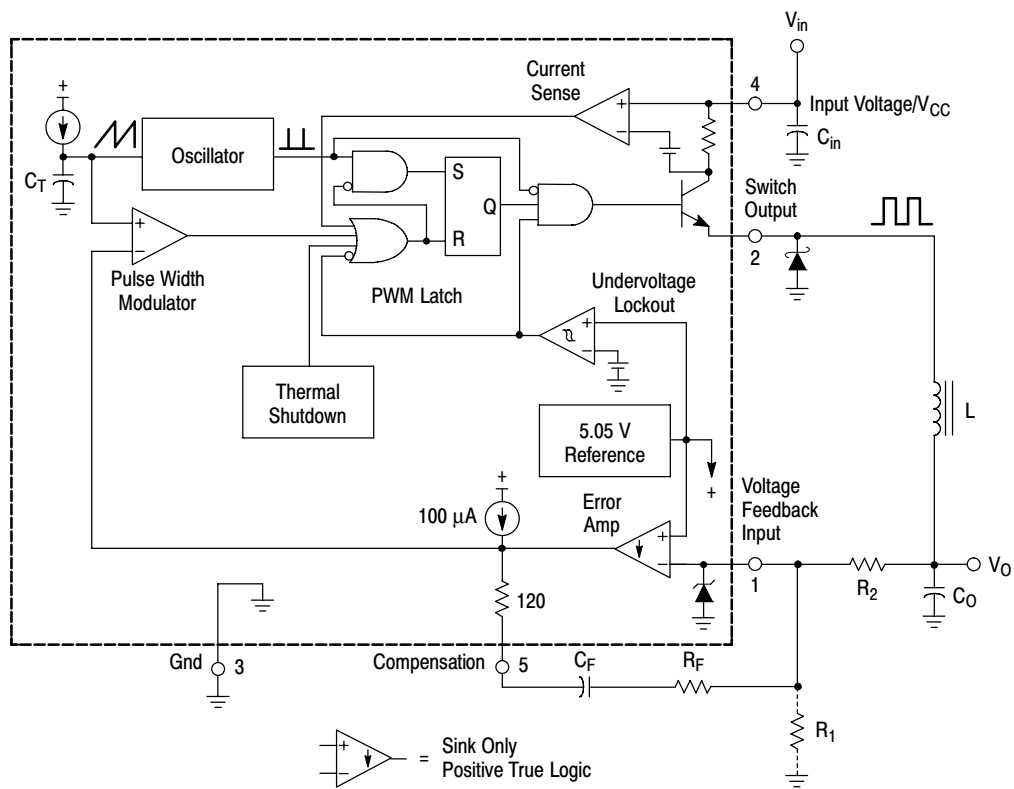


Figure 14. MC34166 Representative Block Diagram

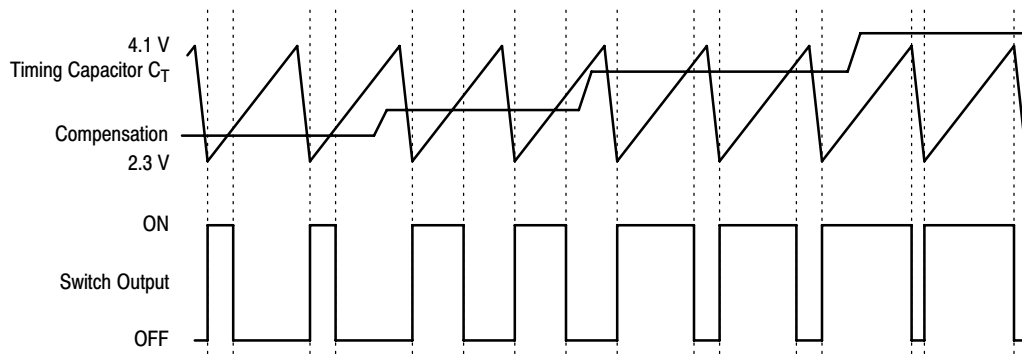


Figure 15. Timing Diagram

INTRODUCTION

The MC34166, MC33166 series are monolithic power switching regulators that are optimized for dc-to-dc converter applications. These devices operate as fixed frequency, voltage mode regulators containing all the active functions required to directly implement step-down and voltage-inverting converters with a minimum number of external components. They can also be used cost effectively in step-up converter applications. Potential markets include automotive, computer, industrial, and cost sensitive consumer products. A description of each section of the device is given below with the representative block diagram shown in Figure 14.

Oscillator

The oscillator frequency is internally programmed to 72 kHz by capacitor C_T and a trimmed current source. The charge to discharge ratio is controlled to yield a 95% maximum duty cycle at the Switch Output. During the discharge of C_T , the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate high, disabling the output switch transistor. The nominal oscillator peak and valley thresholds are 4.1 V and 2.3 V respectively.

Pulse Width Modulator

The Pulse Width Modulator consists of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied into the inverting input. Output switch conduction is initiated when C_T is discharged to the oscillator valley voltage. As C_T charges to a voltage that exceeds the error amplifier output, the latch resets, terminating output transistor conduction for the duration of the oscillator ramp-up period. This PWM/Latch combination prevents multiple output pulses during a given oscillator clock cycle. Figures 7 and 15 illustrate the switch output duty cycle versus the compensation voltage.

Current Sense

The MC34166 series utilizes cycle-by-cycle current limiting as a means of protecting the output switch transistor from overstress. Each on-cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch transistor current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp-up period.

The collector current is converted to a voltage by an internal trimmed resistor and compared against a reference by the Current Sense comparator. When the current limit threshold is reached, the comparator resets the PWM latch. The current limit threshold is typically set

at 4.3 A. Figure 10 illustrates switch output current limit threshold versus temperature.

Error Amplifier and Reference

A high gain Error Amplifier is provided with access to the inverting input and output. This amplifier features a typical dc voltage gain of 80 dB, and a unity gain bandwidth of 600 kHz with 70 degrees of phase margin (Figure 4). The noninverting input is biased to the internal 5.05 V reference and is not pinned out. The reference has an accuracy of $\pm 2.0\%$ at room temperature. To provide 5.0 V at the load, the reference is programmed 50 mV above 5.0 V to compensate for a 1.0% voltage drop in the cable and connector from the converter output. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input as shown in Figures 14 and 19. The equation for determining the output voltage with the divider network is:

$$V_{out} = 5.05 \left(\frac{R_2}{R_1} + 1 \right)$$

External loop compensation is required for converter stability. A simple low-pass filter is formed by connecting a resistor (R_2) from the regulated output to the inverting input, and a series resistor-capacitor (R_F , C_F) between Pins 1 and 5. The compensation network component values shown in each of the applications circuits were selected to provide stability over the tested operating conditions. The step-down converter (Figure 19) is the easiest to compensate for stability. The step-up (Figure 21) and voltage-inverting (Figure 23) configurations operate as continuous conduction flyback converters, and are more difficult to compensate. The simplest way to optimize the compensation network is to observe the response of the output voltage to a step load change, while adjusting R_F and C_F for critical damping. The final circuit should be verified for stability under four boundary conditions. These conditions are minimum and maximum input voltages, with minimum and maximum loads.

By clamping the voltage on the error amplifier output (Pin 5) to less than 150 mV, the internal circuitry will be placed into a low power standby mode, reducing the power supply current to 36 μ A with a 12 V supply voltage. Figure 11 illustrates the standby supply current versus supply voltage.

The Error Amplifier output has a 100 μ A current source pull-up that can be used to implement soft-start. Figure 18 shows the current source charging capacitor C_{SS} through a series diode. The diode disconnects C_{SS} from the feedback loop when the 1.0 M resistor charges it above the operating range of Pin 5.

Switch Output

The output transistor is designed to switch a maximum of 40 V, with a minimum peak collector current of 3.3 A. When configured for step-down or voltage-inverting applications, as in Figures 19 and 23, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn-on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency. Figure 9 shows that by clamping the emitter to 0.5 V, the collector current will be in the range of 100 μ A over temperature. A 1N5822 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit is fully

functional before the output stage is enabled. The internal 5.05 V reference is monitored by the comparator which enables the output stage when V_{CC} exceeds 5.9 V. To prevent erratic output switching as the threshold is crossed, 0.9 V of hysteresis is provided.

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the latch is forced into a 'reset' state, disabling the output switch. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended to be used as a substitute for proper heatsinking.** The MC34166 is contained in a 5-lead TO-220 type package. The tab of the package is common with the center pin (Pin 3) and is normally connected to ground.

DESIGN CONSIDERATIONS

Do not attempt to construct a converter on wire-wrap or plug-in prototype boards. Special care should be taken to separate ground paths from signal currents and ground paths from load currents. All high current loops should be kept as short as possible using heavy copper runs to minimize ringing and radiated EMI. For best operation, a

tight component layout is recommended. Capacitors C_{IN} , C_O , and all feedback components should be placed as close to the IC as physically possible. It is also imperative that the Schottky diode connected to the Switch Output be located as close to the IC as possible.

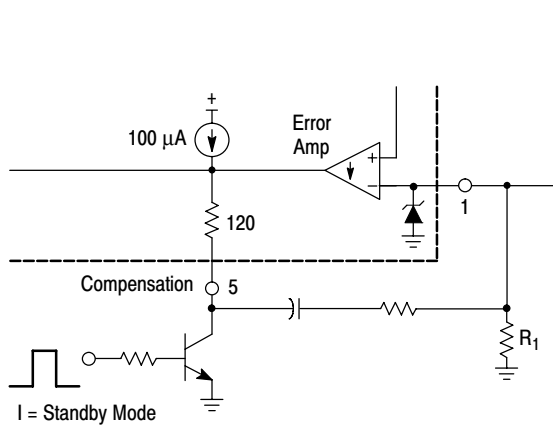


Figure 16. Low Power Standby Circuit

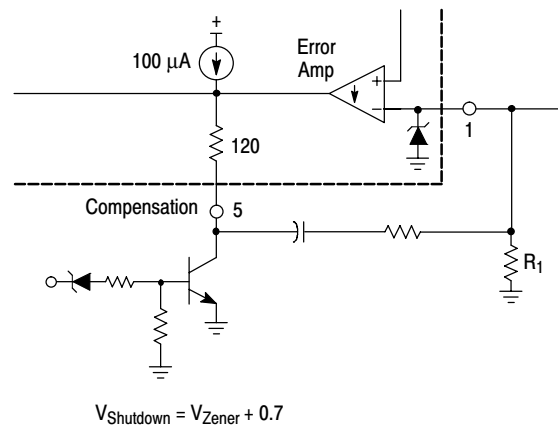


Figure 17. Over Voltage Shutdown Circuit

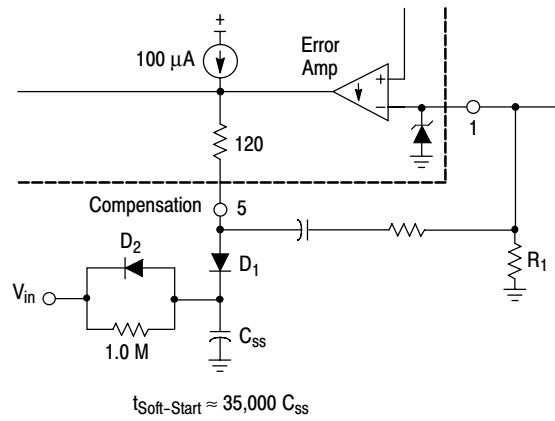
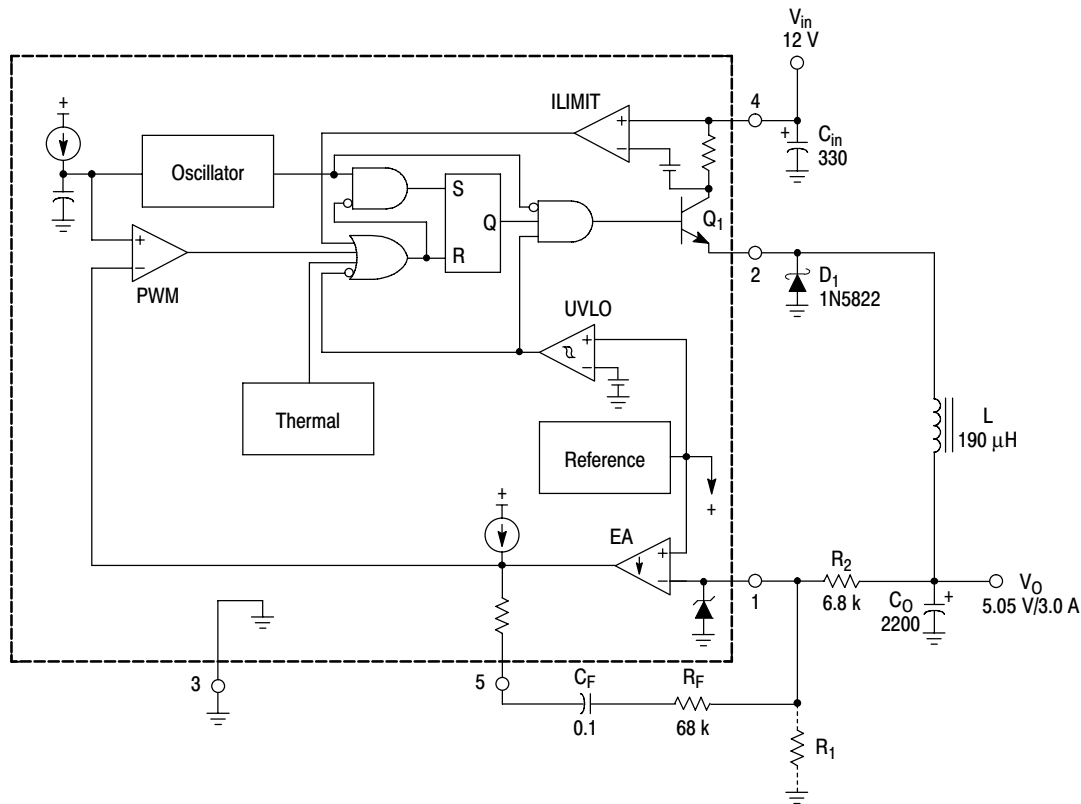


Figure 18. Soft-Start Circuit

MC34166, MC33166



Test	Conditions	Results
Line Regulation	$V_{in} = 8.0 \text{ V to } 36 \text{ V}$, $I_O = 3.0 \text{ A}$	$5.0 \text{ mV} = \pm 0.05\%$
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 0.25 \text{ A to } 3.0 \text{ A}$	$2.0 \text{ mV} = \pm 0.02\%$
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 3.0 \text{ A}$	10 mV_{pp}
Short Circuit Current	$V_{in} = 12 \text{ V}$, $R_L = 0.1 \Omega$	4.3 A
Efficiency	$V_{in} = 12 \text{ V}$, $I_O = 3.0 \text{ A}$	82.8%

L = Coilcraft M1496-A or General Magnetics Technology GMT-0223, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core. Heatsink = Aavid Engineering Inc. 5903B, or 5930B.

The Step-Down Converter application is shown in Figure 19. The output switch transistor Q_1 interrupts the input voltage, generating a squarewave at the LC_O filter input. The filter averages the squarewaves, producing a dc output voltage that can be set to any level between V_{in} and V_{ref} by controlling the percent conduction time of Q_1 to that of the total oscillator cycle time. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input.

Figure 19. Step-Down Converter

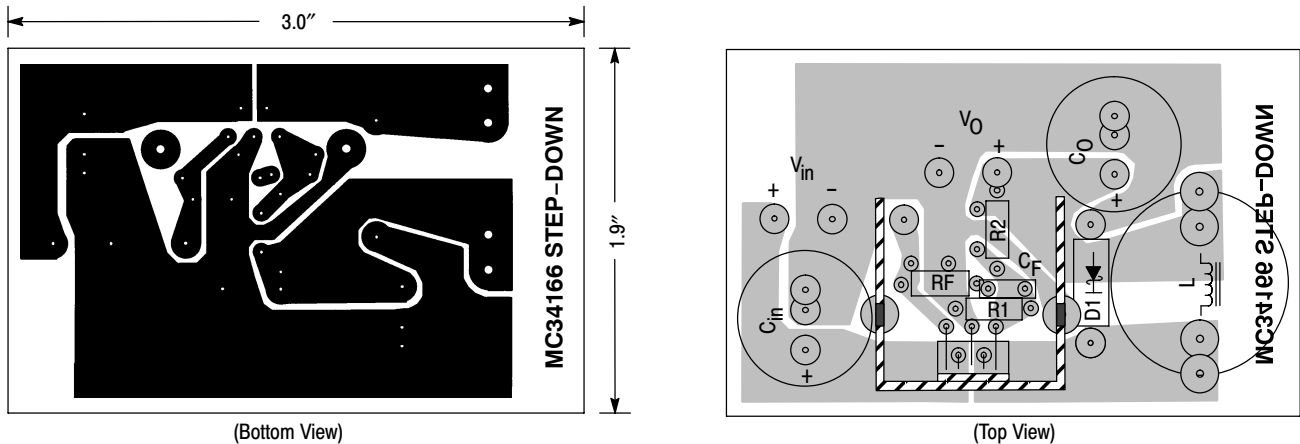
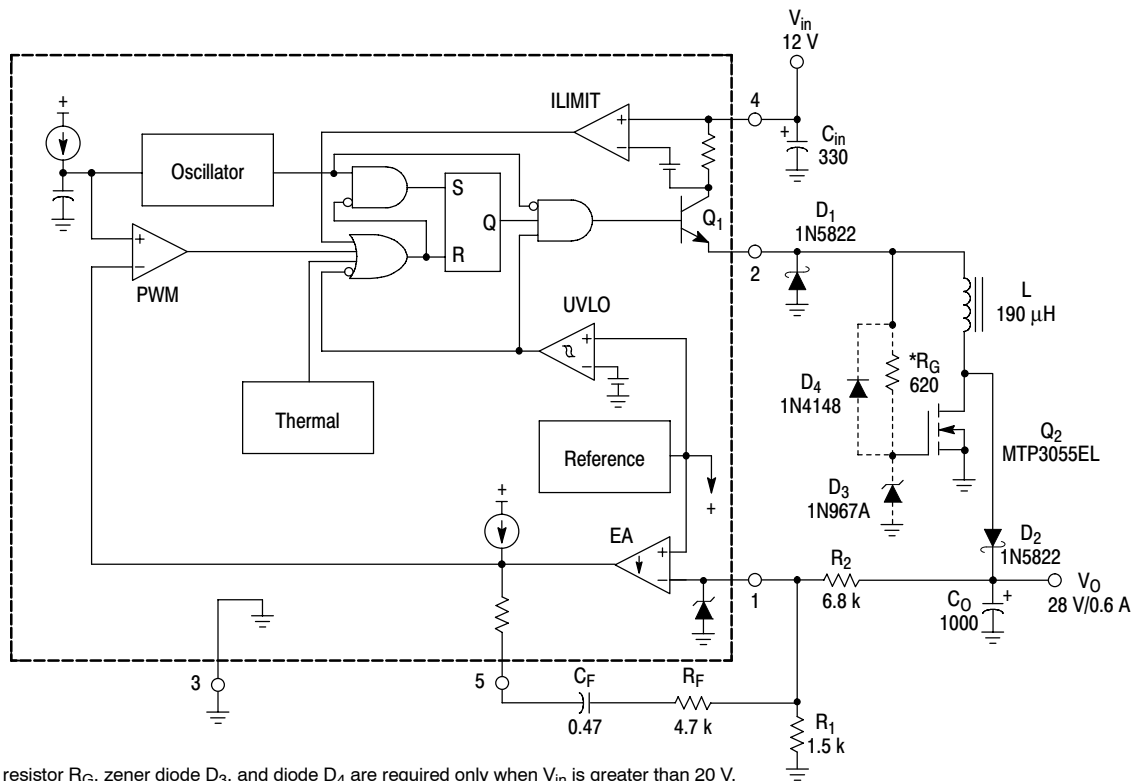


Figure 20. Step-Down Converter Printed Circuit Board and Component Layout

MC34166, MC33166



*Gate resistor R_G , zener diode D_3 , and diode D_4 are required only when V_{in} is greater than 20 V.

Test	Conditions	Results
Line Regulation	$V_{in} = 8.0 \text{ V to } 24 \text{ V}$, $I_O = 0.6 \text{ A}$	$23 \text{ mV} = \pm 0.41\%$
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 0.1 \text{ A to } 0.6 \text{ A}$	$3.0 \text{ mV} = \pm 0.005\%$
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 0.6 \text{ A}$	100 mV_{pp}
Short Circuit Current	$V_{in} = 12 \text{ V}$, $R_L = 0.1 \Omega$	4.0 A
Efficiency	$V_{in} = 12 \text{ V}$, $I_O = 0.6 \text{ A}$	82.8%

L = Coilcraft M1496-A or General Magnetics Technology GMT-0223, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.

Heatsink = AAVID Engineering Inc. MC34166: 5903B, or 5930B MTP3055EL: 5925B

Figure 21 shows that the MC34166 can be configured as a step-up/down converter with the addition of an external power MOSFET. Energy is stored in the inductor during the on-time of transistors Q_1 and Q_2 . During the off-time, the energy is transferred, with respect to ground, to the output filter capacitor and load. This circuit configuration has two significant advantages over the basic step-up converter circuit. The first advantage is that output short-circuit protection is provided by the MC34166, since Q_1 is directly in series with V_{in} and the load. Second, the output voltage can be programmed to be less than V_{in} . Notice that during the off-time, the inductor forward biases diodes D_1 and D_2 , transferring its energy with respect to ground rather than with respect to V_{in} . When operating with V_{in} greater than 20 V, a gate protection network is required for the MOSFET. The network consists of components R_G , D_3 , and D_4 .

Figure 21. Step-Up/Down Converter

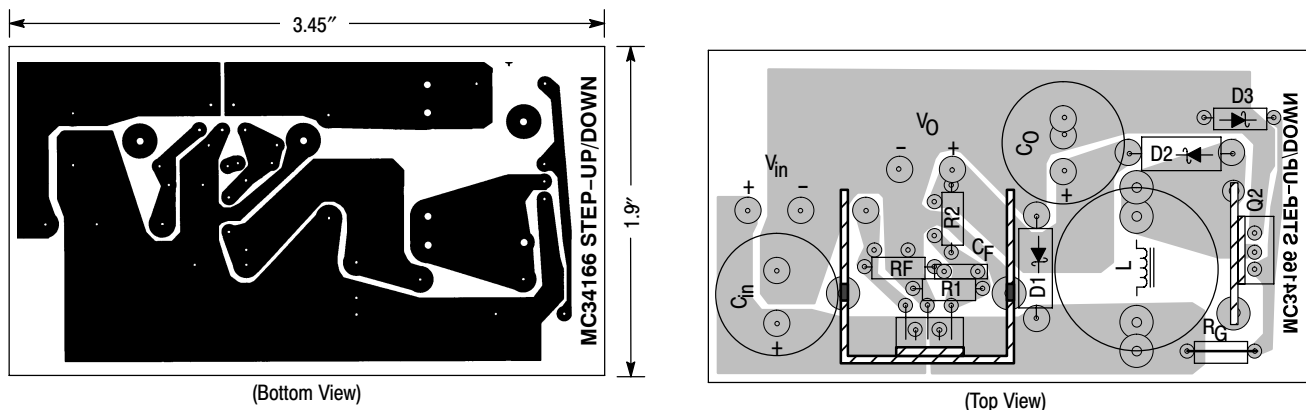
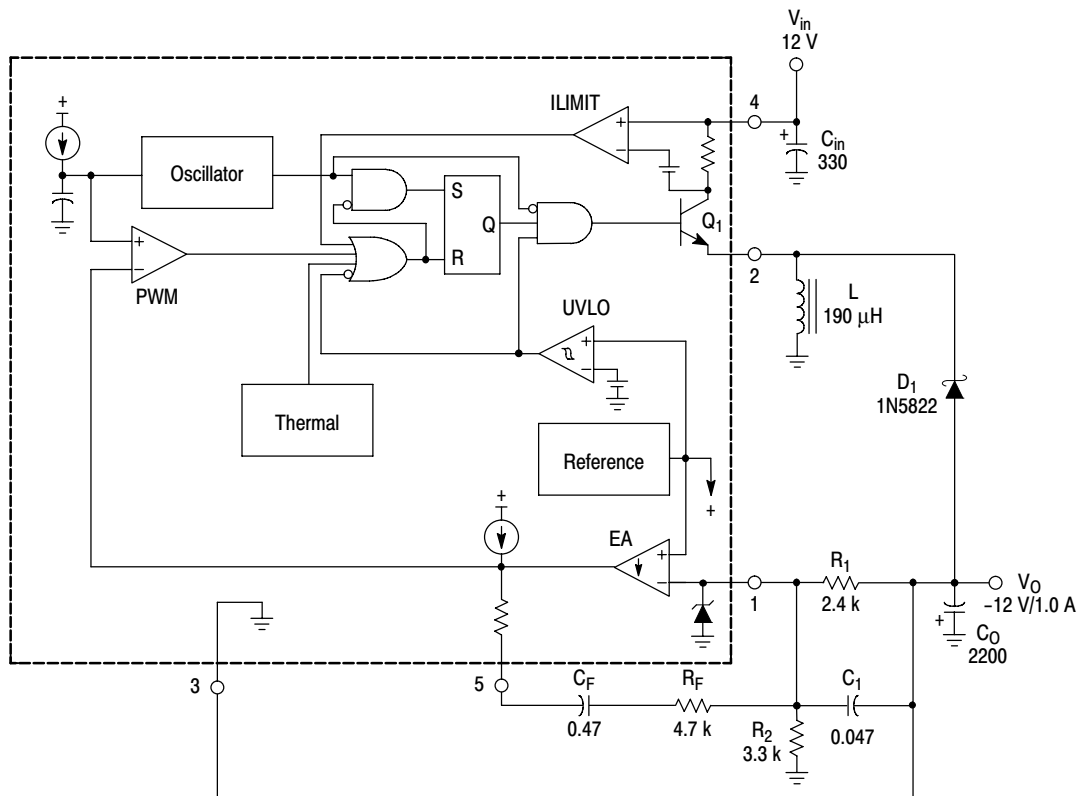


Figure 22. Step-Up/Down Converter Printed Circuit Board and Component Layout

MC34166, MC33166



Test	Conditions	Results
Line Regulation	$V_{in} = 8.0 \text{ V to } 24 \text{ V}$, $I_O = 1.0 \text{ A}$	$3.0 \text{ mV} \pm 0.01\%$
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 0.1 \text{ A to } 1.0 \text{ A}$	$4.0 \text{ mV} \pm 0.017\%$
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ A}$	80 mV_{pp}
Short Circuit Current	$V_{in} = 12 \text{ V}$, $R_L = 0.1 \Omega$	3.74 A
Efficiency	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ A}$	81.2%

L = Coilcraft M1496-A or General Magnetics Technology GMT-0223, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core. Heatsink = Aavid Engineering Inc. 5903B, or 5930B.

Two potential problems arise when designing the standard voltage-inverting converter with the MC34166. First, the Switch Output emitter is limited to -1.5 V with respect to the ground pin and second, the Error Amplifier's noninverting input is internally committed to the reference and is not pinned out. Both of these problems are resolved by connecting the IC ground pin to the converter's negative output as shown in Figure 23. This keeps the emitter of Q_1 positive with respect to the ground pin and has the effect of reversing the Error Amplifier inputs. Note that the voltage drop across R_1 is equal to 5.05 V when the output is in regulation.

Figure 23. Voltage-Inverting Converter

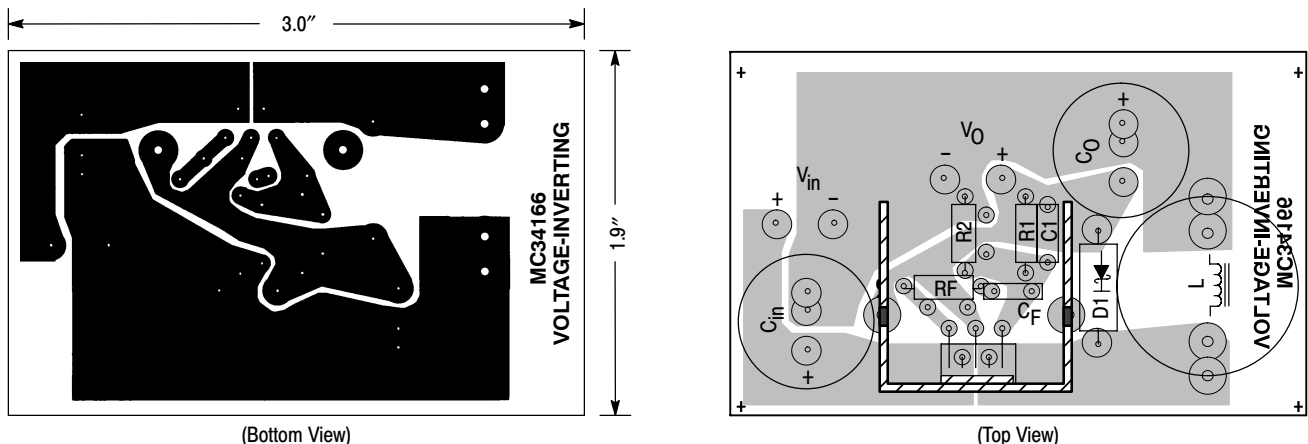
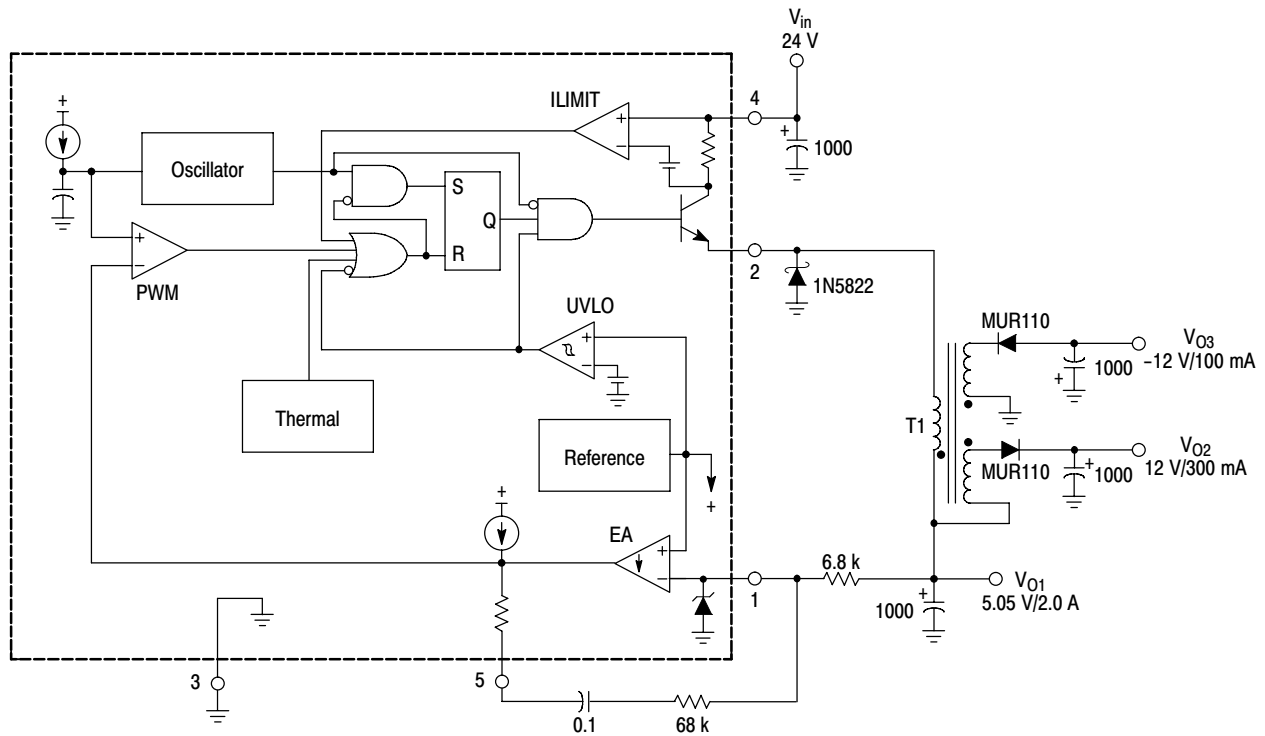


Figure 24. Voltage-Inverting Converter Printed Circuit Board and Component Layout

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Tests		Conditions	Results
Line Regulation	5.0 V	$V_{in} = 15 \text{ V to } 30 \text{ V}$, $I_{O1} = 2.0 \text{ A}$, $I_{O2} = 300 \text{ mA}$, $I_{O3} = 100 \text{ mA}$	4.0 mV = $\pm 0.04\%$
	12 V		450 mV = $\pm 1.9\%$
	-12 V		350 mV = $\pm 1.5\%$
Load Regulation	5.0 V	$V_{in} = 24 \text{ V}$, $I_{O1} = 500 \text{ mA to } 2.0 \text{ A}$, $I_{O2} = 300 \text{ mA}$, $I_{O3} = 100 \text{ mA}$	2.0 mV = $\pm 0.02\%$
	12 V	$V_{in} = 24 \text{ V}$, $I_{O1} = 2.0 \text{ A}$, $I_{O2} = 100 \text{ mA to } 300 \text{ mA}$, $I_{O3} = 100 \text{ mA}$	420 mV = $\pm 1.7\%$
	-12 V	$V_{in} = 24 \text{ V}$, $I_{O1} = 2.0 \text{ A}$, $I_{O2} = 300 \text{ mA}$, $I_{O3} = 30 \text{ mA to } 100 \text{ mA}$	310 mV = $\pm 1.3\%$
Output Ripple	5.0 V 12 V -12 V	$V_{in} = 24 \text{ V}$, $I_{O1} = 2.0 \text{ A}$, $I_{O2} = 300 \text{ mA}$, $I_{O3} = 100 \text{ mA}$	50 mV _{pp} 25 mV _{pp} 10 mV _{pp}
Short Circuit Current	5.0 V 12 V -12 V	$V_{in} = 24 \text{ V}$, $R_L = 0.1 \Omega$	4.3 A 1.83 A 1.47 A
Efficiency	TOTAL	$V_{in} = 24 \text{ V}$, $I_{O1} = 2.0 \text{ A}$, $I_{O2} = 300 \text{ mA}$, $I_{O3} = 100 \text{ mA}$	83.3%

T1 = Primary: Coilcraft M1496-A or General Magnetics Technology GMT-0223, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.

Secondary: V_{O2} – 65 turns of #26 AWG

V_{O3} – 96 turns of #28 AWG

Heatsink = Aavid Engineering Inc. 5903B, or 5930B.

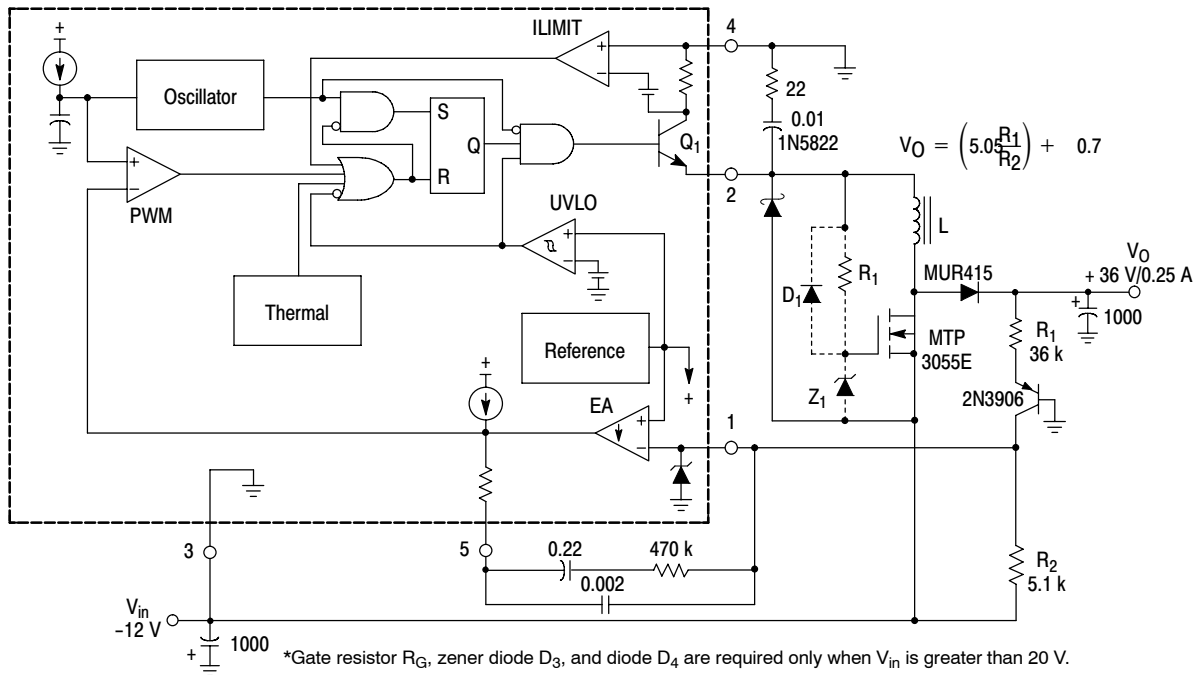
Multiple auxiliary outputs can easily be derived by winding secondaries on the main output inductor to form a transformer. The secondaries must be connected so that the energy is delivered to the auxiliary outputs when the Switch Output turns off. During the OFF time, the voltage across the primary winding is regulated by the feedback loop, yielding a constant Volts/Turn ratio. The number of turns for any given secondary voltage can be calculated by the following equation:

$$\# \text{ TURNS(SEC)} = \frac{V_O(\text{SEC}) + V_F(\text{SEC})}{\left(\frac{V_O(\text{PRI}) + V_F(\text{PRI})}{\# \text{ TURNS(PRI)}} \right)}$$

Note that the 12 V winding is stacked on top of the 5.0 V output. This reduces the number of secondary turns and improves load regulation. For best auxiliary regulation, the auxiliary outputs should be less than 33% of the total output power.

Figure 25. Triple Output Converter

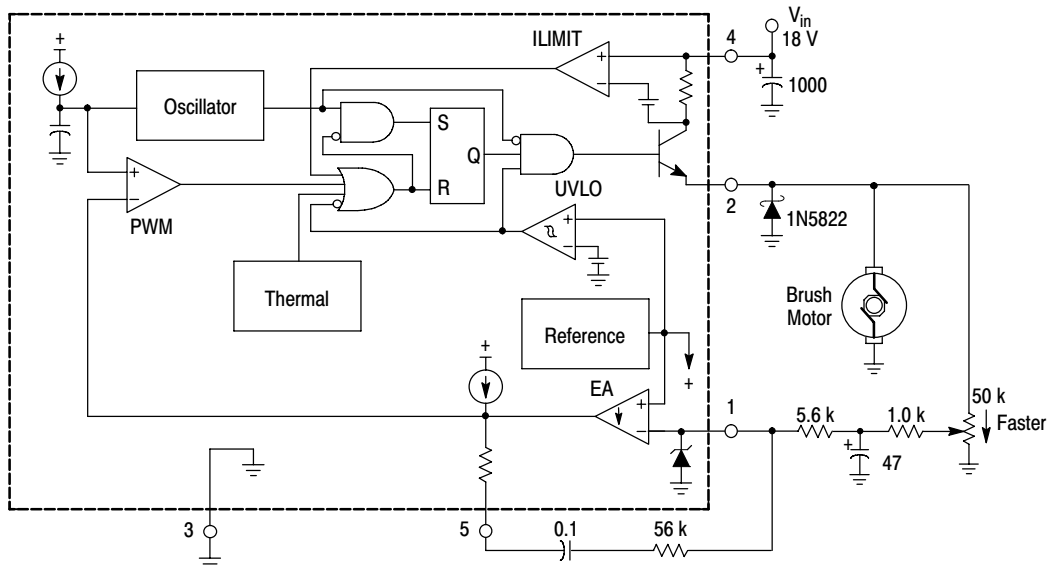
MC34166, MC33166



Test	Conditions	Results
Line Regulation	$V_{in} = -10 \text{ V to } -20 \text{ V}, I_O = 0.25 \text{ A}$	250 mV = $\pm 0.35\%$
Load Regulation	$V_{in} = -12 \text{ V}, I_O = 0.025 \text{ A to } 0.25 \text{ A}$	790 mV = $\pm 1.19\%$
Output Ripple	$V_{in} = -12 \text{ V}, I_O = 0.25 \text{ A}$	80 mV _{pp}
Efficiency	$V_{in} = -12 \text{ V}, I_O = 0.25 \text{ A}$	79.2%

L = Coilcraft M1496-A or ELMACO CHK1050, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.
 Heatsink = Aavid Engineering Inc. 5903B or 5930B

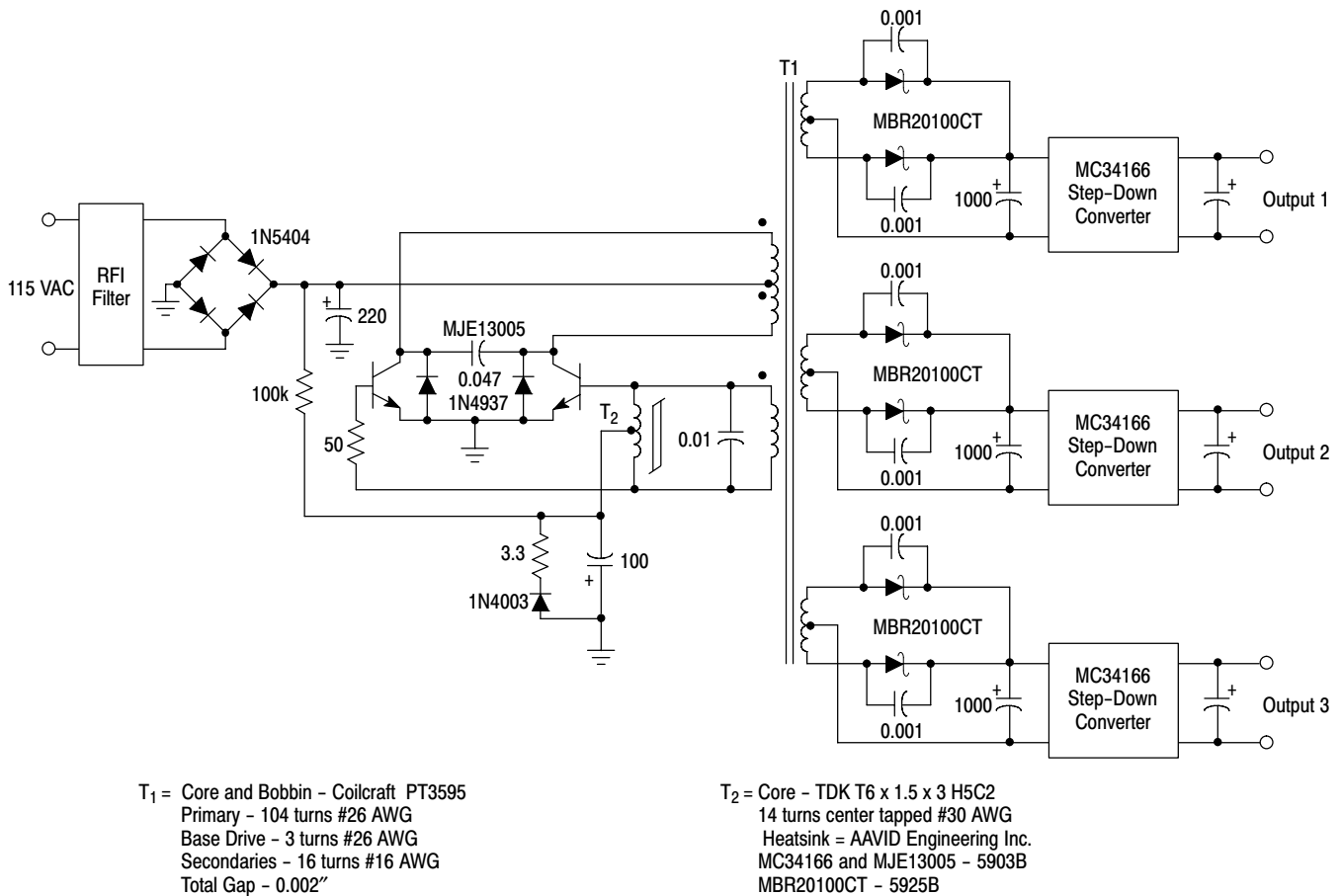
Figure 26. Negative Input/Positive Output Regulator



Test	Conditions	Results
Low Speed Line Regulation	$V_{in} = 12 \text{ V to } 24 \text{ V}$	1760 RPM $\pm 1\%$
High Speed Line Regulation	$V_{in} = 12 \text{ V to } 24 \text{ V}$	3260 RPM $\pm 6\%$

Figure 27. Variable Motor Speed Control with EMF Feedback Sensing

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The MC34166 can be used cost effectively in off-line applications even though it is limited to a maximum input voltage of 40 V. Figure 28 shows a simple and efficient method for converting the AC line voltage down to 24 V. This preconverter has a total power rating of 125 W with a conversion efficiency of 90%. Transformer T_1 provides output isolation from the AC line and isolation between each of the secondaries. The circuit self-oscillates at 50 kHz and is controlled by the saturation characteristics of T_2 . Multiple MC34166 post regulators can be used to provide accurate independently regulated outputs for a distributed power system.

Figure 28. Off-Line Preconverter

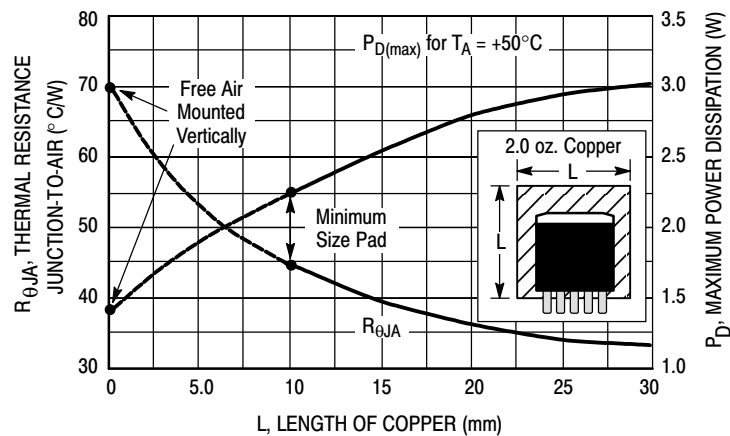


Figure 29. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

Table 1. Design Equations

Calculation	Step-Down	Step-Up/Down	Voltage-Inverting
$\frac{t_{on}}{t_{off}}$ (Notes 1, 2)	$\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_{F1} + V_{F2}}{V_{in} - V_{satQ1} - V_{satQ2}}$	$\frac{ V_{out} + V_F}{V_{in} - V_{sat}}$
t_{on}	$\frac{t_{on}}{t_{off}} \cdot \frac{1}{f_{osc} \left(\frac{t_{on}}{t_{off}} + 1 \right)}$	$\frac{t_{on}}{t_{off}} \cdot \frac{1}{f_{osc} \left(\frac{t_{on}}{t_{off}} + 1 \right)}$	$\frac{t_{on}}{t_{off}} \cdot \frac{1}{f_{osc} \left(\frac{t_{on}}{t_{off}} + 1 \right)}$
Duty Cycle (Note 3)	$t_{on} f_{osc}$	$t_{on} f_{osc}$	$t_{on} f_{osc}$
$I_{L\ avg}$	I_{out}	$I_{out} \left(\frac{t_{on}}{t_{off}} + 1 \right)$	$I_{out} \left(\frac{t_{on}}{t_{off}} + 1 \right)$
$I_{pk(switch)}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$
L	$\left(\frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L} \right) t_{on}$	$\left(\frac{V_{in} - V_{satQ1} - V_{satQ2}}{\Delta I_L} \right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L} \right) t_{on}$
$V_{ripple(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8f_{osc}C_O} \right)^2 + (ESR)^2}$	$\left(\frac{t_{on}}{t_{off}} + 1 \right) \sqrt{\left(\frac{1}{f_{osc}C_O} \right)^2 + (ESR)^2}$	$\left(\frac{t_{on}}{t_{off}} + 1 \right) \sqrt{\left(\frac{1}{f_{osc}C_O} \right)^2 + (ESR)^2}$
V_{out}	$V_{ref} \left(\frac{R_2}{R_1} + 1 \right)$	$V_{ref} \left(\frac{R_2}{R_1} + 1 \right)$	$V_{ref} \left(\frac{R_2}{R_1} + 1 \right)$

1. V_{sat} – Switch Output source saturation voltage, refer to Figure 8.

2. V_F – Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.5 V.

3. Duty cycle is calculated at the minimum operating input voltage and must not exceed the guaranteed minimum $DC_{(max)}$ specification of 0.92.

The following converter characteristics must be chosen:

V_{out} – Desired output voltage.

I_{out} – Desired output current.

ΔI_L – Desired peak-to-peak inductor ripple current. For maximum output current especially when the duty cycle is greater than 0.5, it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L\ avg}$. This will help prevent $I_{pk(switch)}$ from reaching the guaranteed minimum current limit threshold of 3.3 A. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2 (I_{L\ avg})$. This will proportionally reduce the converter's output current capability.

$V_{ripple(pp)}$ – Desired peak-to-peak output ripple voltage. For best performance, the ripple voltage should be kept to less than 2% of V_{out} . Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

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ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping
MC33166D2T	$T_A = -40^\circ$ to $+85^\circ\text{C}$	D ² PAK (Surface Mount)	50 Units/Rail
MC33166D2TR4		D ² PAK (Surface Mount)	
MC33166T		TO-220 (Straight Lead)	
MC33166TH		TO-220 (Horizontal Mount)	
MC33166TV		TO-220 (Vertical Mount)	
MC34166D2T	$T_A = 0^\circ$ to $+70^\circ\text{C}$	D ² PAK (Surface Mount)	
MC34166D2TR4		D ² PAK (Surface Mount)	
MC34166T		TO-220 (Straight Lead)	
MC34166TH		TO-220 (Horizontal Mount)	
MC34166TV		TO-220 (Vertical Mount)	

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5.0 A, Step-Up/Down/ Inverting Switching Regulators

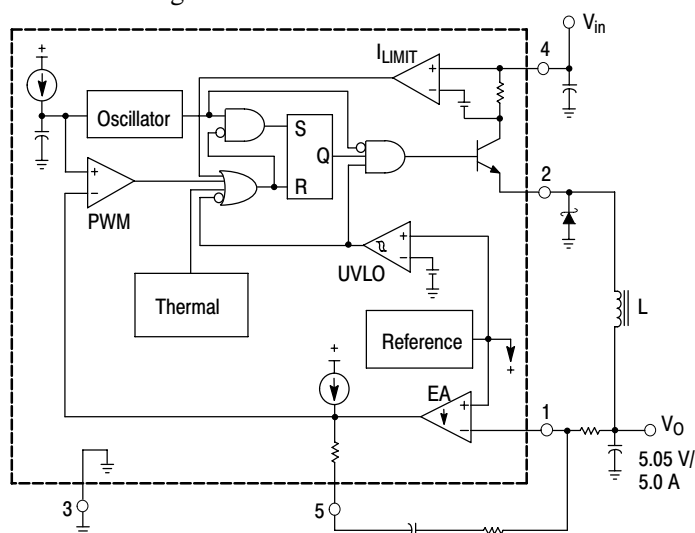
The MC34167, MC33167 series are high performance fixed frequency power switching regulators that contain the primary functions required for dc-to-dc converters. This series was specifically designed to be incorporated in step-down and voltage-inverting configurations with a minimum number of external components and can also be used cost effectively in step-up applications.

These devices consist of an internal temperature compensated reference, fixed frequency oscillator with on-chip timing components, latching pulse width modulator for single pulse metering, high gain error amplifier, and a high current output switch.

Protective features consist of cycle-by-cycle current limiting, undervoltage lockout, and thermal shutdown. Also included is a low power standby mode that reduces power supply current to 36 μ A.

Features

- Output Switch Current in Excess of 5.0 A
- Fixed Frequency Oscillator (72 kHz) with On-Chip Timing
- Provides 5.05 V Output without External Resistor Divider
- Precision 2% Reference
- 0% to 95% Output Duty Cycle
- Cycle-by-Cycle Current Limiting
- Undervoltage Lockout with Hysteresis
- Internal Thermal Shutdown
- Operation from 7.5 V to 40 V
- Standby Mode Reduces Power Supply Current to 36 μ A
- Economical 5-Lead TO-220 Package with Two Optional Leadforms
- Also Available in Surface Mount D²PAK Package
- Moisture Sensitivity Level (MSL) Equals 1
- Pb-Free Packages are Available



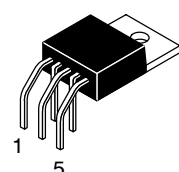
This device contains 143 active transistors.
Figure 1. Simplified Block Diagram
(Step Down Application)



ON Semiconductor®

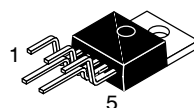
<http://onsemi.com>

MARKING DIAGRAMS

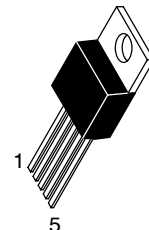


**TO-220
TH SUFFIX
CASE 314A**

Heatsink surface connected to Pin 3

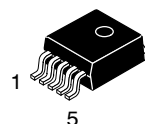


**TO-220
TV SUFFIX
CASE 314B**



**TO-220
T SUFFIX
CASE 314D**

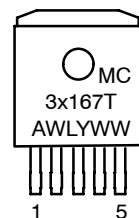
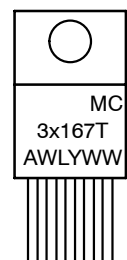
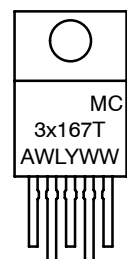
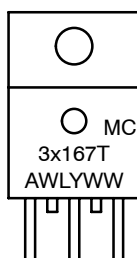
- Pin
1. Voltage Feedback Input
 2. Switch Output
 3. Ground
 4. Input Voltage/ V_{CC}
 5. Compensation/Standby



**D²PAK
D2T SUFFIX
CASE 936A**

Heatsink surface (shown as
terminal 6 in case outline
drawing) is connected to Pin 3

- x = 3 or 4
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 254 of this data sheet.

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MAXIMUM RATINGS (Note 2)

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	40	V
Switch Output Voltage Range	$V_{O(switch)}$	−2.0 to + V_{in}	V
Voltage Feedback and Compensation Input Voltage Range	V_{FB}, V_{Comp}	−1.0 to + 7.0	V
Power Dissipation			
Case 314A, 314B and 314D ($T_A = +25^{\circ}C$)	P_D	Internally Limited	W
Thermal Resistance, Junction-to-Ambient	θ_{JA}	65	$^{\circ}C/W$
Thermal Resistance, Junction-to-Case	θ_{JC}	5.0	$^{\circ}C/W$
Case 936A (D ² PAK) ($T_A = +25^{\circ}C$)	P_D	Internally Limited	W
Thermal Resistance, Junction-to-Ambient	θ_{JA}	70	$^{\circ}C/W$
Thermal Resistance, Junction-to-Case	θ_{JC}	5.0	$^{\circ}C/W$
Operating Junction Temperature	T_J	+150	$^{\circ}C$
Operating Ambient Temperature (Note 3)	T_A		$^{\circ}C$
MC34167		0 to + 70	
MC33167		− 40 to + 85	
Storage Temperature Range	T_{stg}	− 65 to +150	$^{\circ}C$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- Maximum package power dissipation limits must be observed to prevent thermal shutdown activation.
- This device series contains ESD protection and exceeds the following tests:
Human Body Model 2000 V per MIL-STD-883, Method 3015.
Machine Model Method 200 V.
- | | |
|---|--|
| $T_{low} = 0^{\circ}\text{C}$ for MC34167 | $T_{high} = +70^{\circ}\text{C}$ for MC34167 |
| $= -40^{\circ}\text{C}$ for MC33167 | $= +85^{\circ}\text{C}$ for MC33167 |

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ELECTRICAL CHARACTERISTICS ($V_{CC} = 12\text{ V}$, for typical values $T_A = +25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies (Notes 4, 5), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit

OSCILLATOR

Frequency ($V_{CC} = 7.5\text{ V to }40\text{ V}$)	$T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}} \text{ to } T_{\text{high}}$	f_{OSC}	65 62	72 –	79 81	kHz

ERROR AMPLIFIER

Voltage Feedback Input Threshold	$T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}} \text{ to } T_{\text{high}}$	$V_{\text{FB(th)}}$	4.95 4.85	5.05 –	5.15 5.20	V
Line Regulation ($V_{CC} = 7.5\text{ V to }40\text{ V}$, $T_A = +25^\circ\text{C}$)		Reg_{line}	–	0.03	0.078	%/V
Input Bias Current ($V_{\text{FB}} = V_{\text{FB(th)}} + 0.15\text{ V}$)		I_{IB}	–	0.15	1.0	μA
Power Supply Rejection Ratio ($V_{CC} = 10\text{ V to }20\text{ V}$, $f = 120\text{ Hz}$)		PSRR	60	80	–	dB
Output Voltage Swing	High State ($I_{\text{Source}} = 75\text{ }\mu\text{A}$, $V_{\text{FB}} = 4.5\text{ V}$) Low State ($I_{\text{Sink}} = 0.4\text{ mA}$, $V_{\text{FB}} = 5.5\text{ V}$)	V_{OH} V_{OL}	4.2 –	4.9 1.6	– 1.9	V

PWM COMPARATOR

Duty Cycle ($V_{CC} = 20\text{ V}$)	Maximum ($V_{\text{FB}} = 0\text{ V}$) Minimum ($V_{\text{Comp}} = 1.9\text{ V}$)	$\text{DC}_{(\text{max})}$ $\text{DC}_{(\text{min})}$	92 0	95 0	100 0	%

SWITCH OUTPUT

Output Voltage Source Saturation ($V_{CC} = 7.5\text{ V}$, $I_{\text{Source}} = 5.0\text{ A}$)	V_{sat}	–	($V_{CC} - 1.5$)	($V_{CC} - 1.8$)	V
Off-State Leakage ($V_{CC} = 40\text{ V}$, Pin 2 = GND)	$I_{\text{sw(off)}}$	–	0	100	μA
Current Limit Threshold ($V_{CC} = 7.5\text{ V}$)	$I_{\text{pk(switch)}}$	5.5	6.5	8.0	A
Switching Times ($V_{CC} = 40\text{ V}$, $I_{\text{pk}} = 5.0\text{ A}$, $L = 225\text{ }\mu\text{H}$, $T_A = +25^\circ\text{C}$)	t_r t_f	– –	100 50	200 100	ns

UNDERVOLTAGE LOCKOUT

Startup Threshold (V_{CC} Increasing, $T_A = +25^\circ\text{C}$)	$V_{\text{th(UVLO)}}$	5.5	5.9	6.3	V
Hysteresis (V_{CC} Decreasing, $T_A = +25^\circ\text{C}$)	$V_{\text{H(UVLO)}}$	0.6	0.9	1.2	V

TOTAL DEVICE

Power Supply Current ($T_A = +25^\circ\text{C}$)	I_{CC}	–	36	100	μA
Standby ($V_{CC} = 12\text{ V}$, $V_{\text{Comp}} < 0.15\text{ V}$)		–	40	60	mA
Operating ($V_{CC} = 40\text{ V}$, Pin 1 = GND for maximum duty cycle)		–			

4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
5. $T_{\text{low}} = 0^\circ\text{C}$ for MC34167 $T_{\text{high}} = +70^\circ\text{C}$ for MC34167
 $= -40^\circ\text{C}$ for MC33167 $= +85^\circ\text{C}$ for MC33167

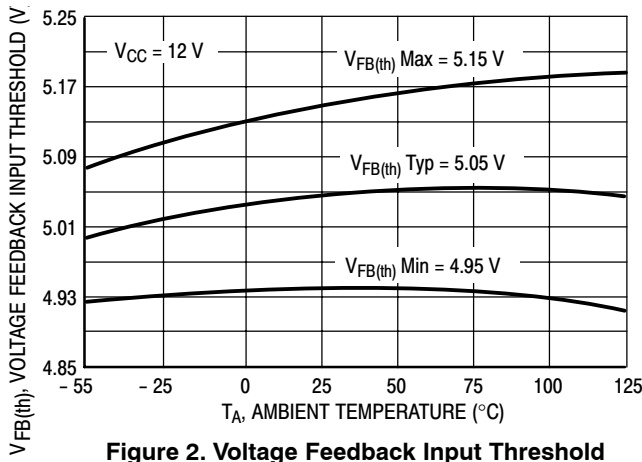


Figure 2. Voltage Feedback Input Threshold versus Temperature

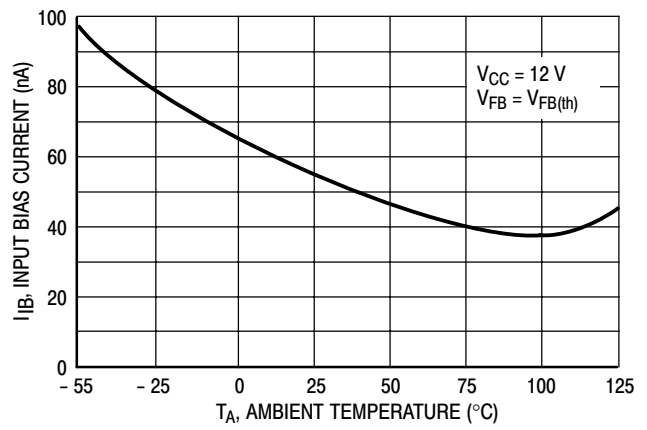


Figure 3. Voltage Feedback Input Bias Current versus Temperature

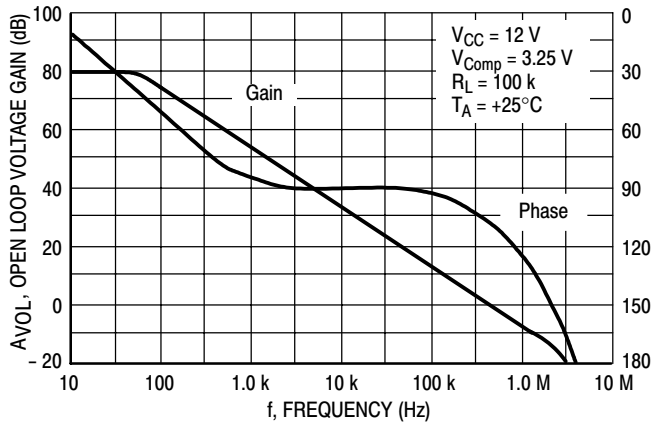


Figure 4. Error Amp Open Loop Gain and Phase versus Frequency

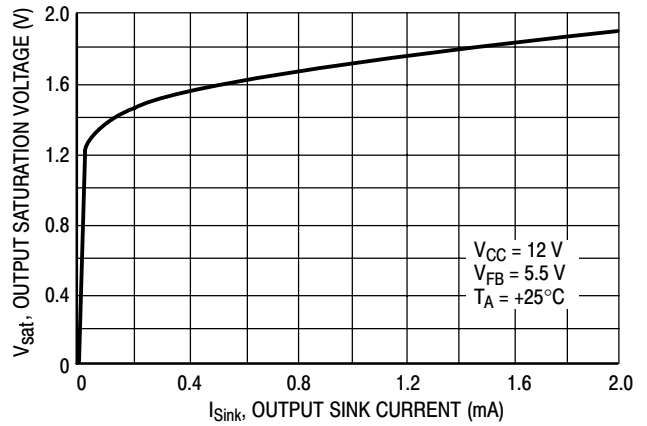


Figure 5. Error Amp Output Saturation versus Sink Current

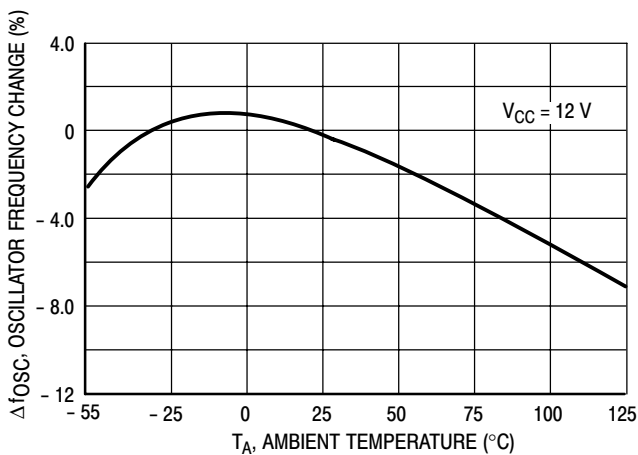


Figure 6. Oscillator Frequency Change versus Temperature

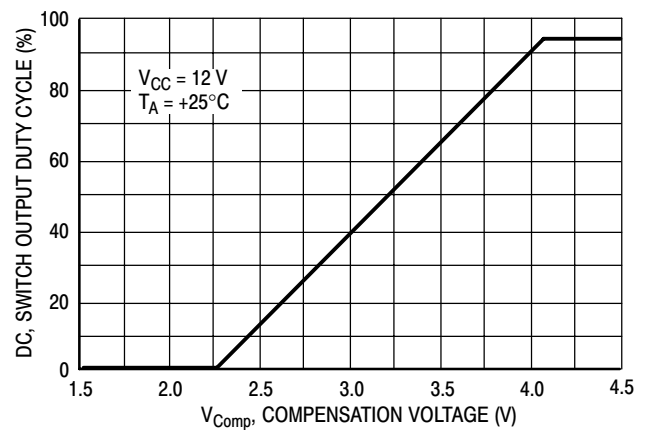


Figure 7. Switch Output Duty Cycle versus Compensation Voltage

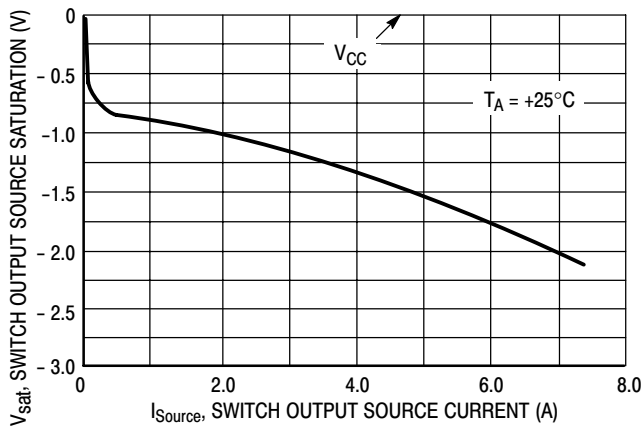


Figure 8. Switch Output Source Saturation versus Source Current

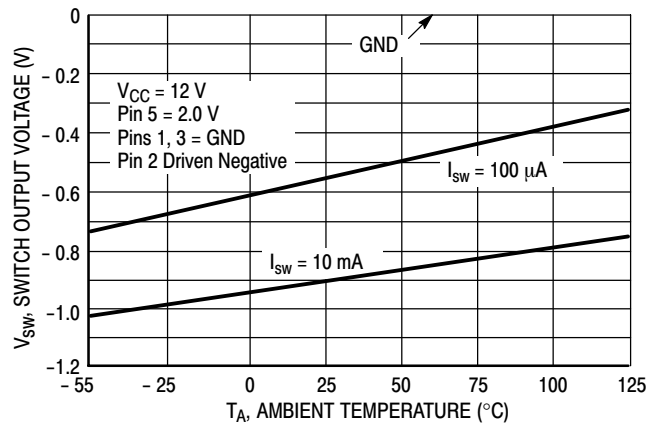


Figure 9. Negative Switch Output Voltage versus Temperature

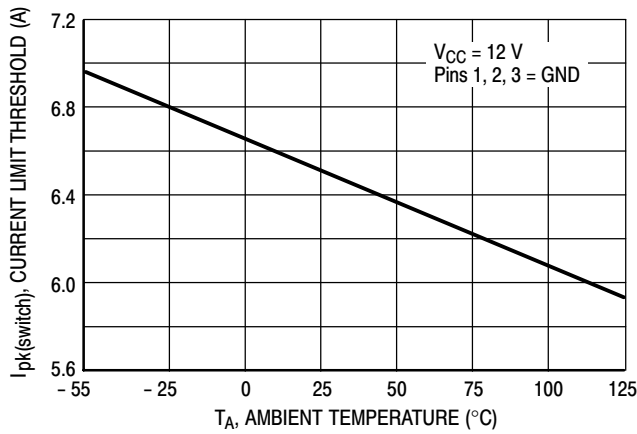


Figure 10. Switch Output Current Limit Threshold versus Temperature

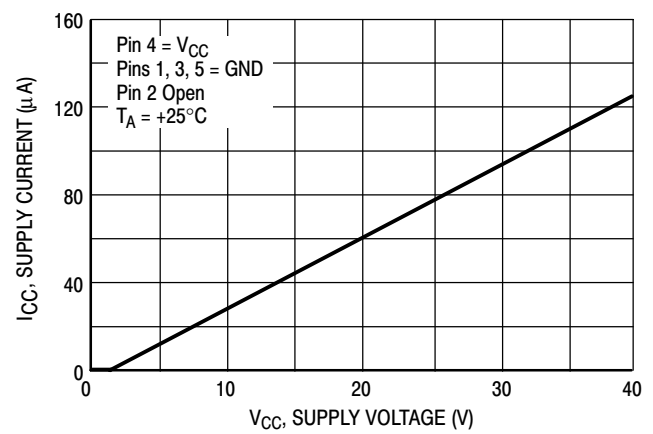


Figure 11. Standby Supply Current versus Supply Voltage

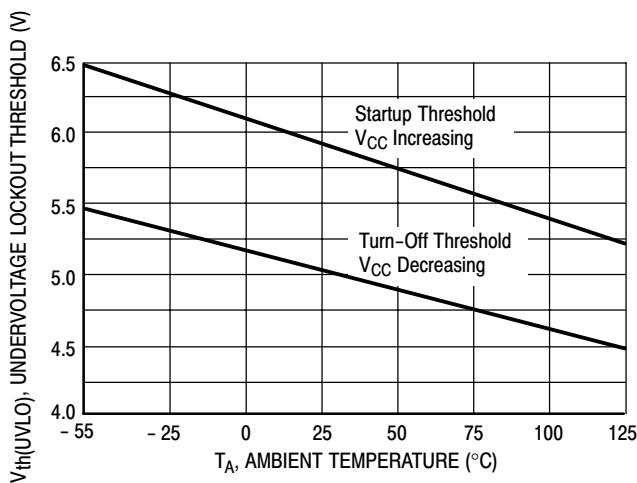


Figure 12. Undervoltage Lockout Thresholds versus Temperature

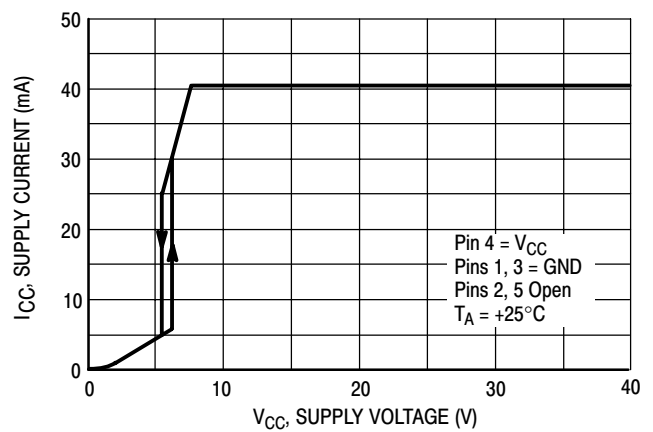


Figure 13. Operating Supply Current versus Supply Voltage

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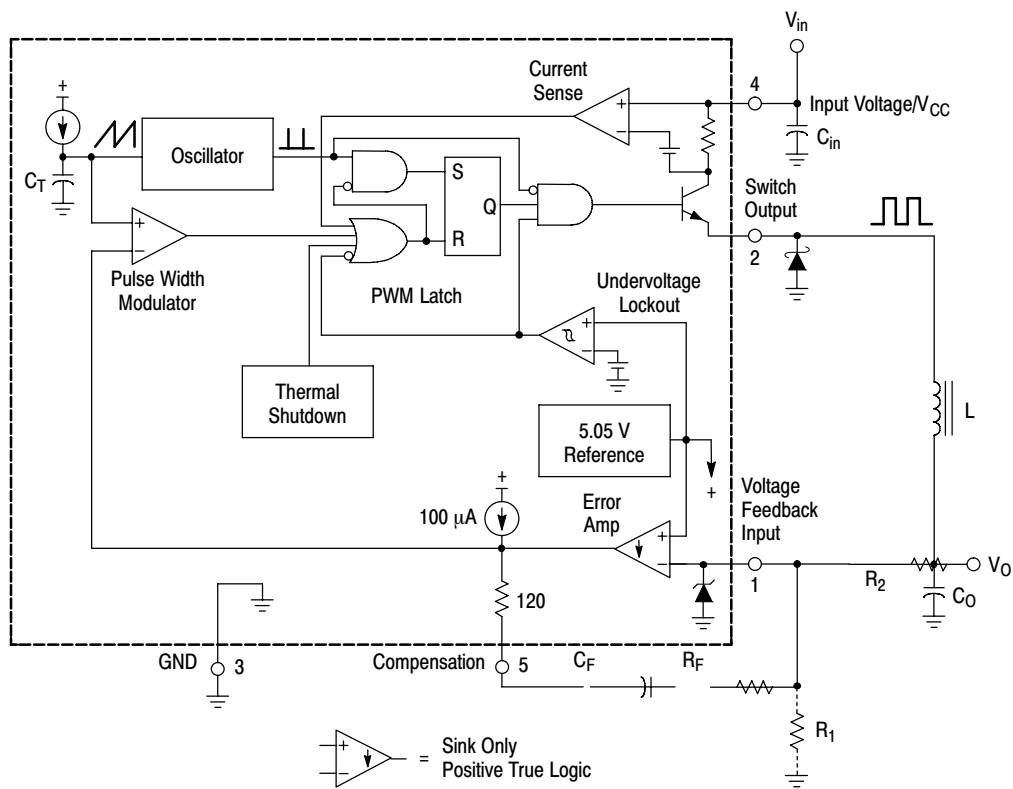


Figure 14. MC34167 Representative Block Diagram

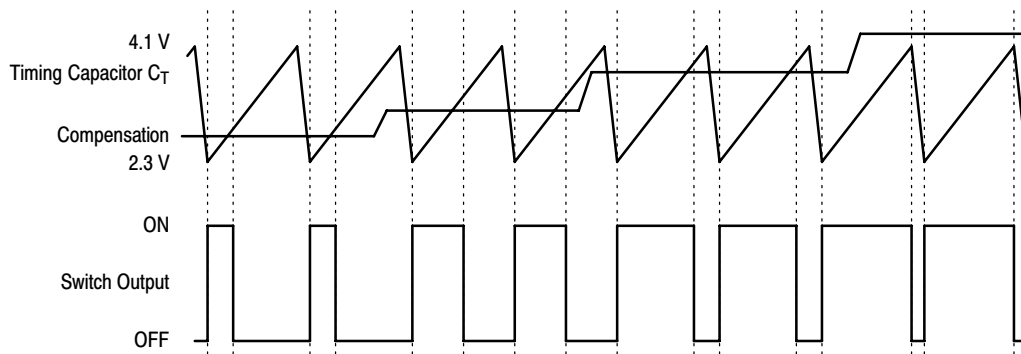


Figure 15. Timing Diagram

INTRODUCTION

The MC34167, MC33167 series are monolithic power switching regulators that are optimized for dc-to-dc converter applications. These devices operate as fixed frequency, voltage mode regulators containing all the active functions required to directly implement step-down and voltage-inverting converters with a minimum number of external components. They can also be used cost effectively in step-up converter applications. Potential markets include automotive, computer, industrial, and cost sensitive consumer products. A description of each section of the device is given below with the representative block diagram shown in Figure 14.

Oscillator

The oscillator frequency is internally programmed to 72 kHz by capacitor C_T and a trimmed current source. The charge to discharge ratio is controlled to yield a 95% maximum duty cycle at the Switch Output. During the discharge of C_T , the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate high, disabling the output switch transistor. The nominal oscillator peak and valley thresholds are 4.1 V and 2.3 V respectively.

Pulse Width Modulator

The Pulse Width Modulator consists of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied into the inverting input. Output switch conduction is initiated when C_T is discharged to the oscillator valley voltage. As C_T charges to a voltage that exceeds the error amplifier output, the latch resets, terminating output transistor conduction for the duration of the oscillator ramp-up period. This PWM/Latch combination prevents multiple output pulses during a given oscillator clock cycle. Figures 7 and 15 illustrate the switch output duty cycle versus the compensation voltage.

Current Sense

The MC34167 series utilizes cycle-by-cycle current limiting as a means of protecting the output switch transistor from overstress. Each on cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch transistor current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp-up period.

The collector current is converted to a voltage by an internal trimmed resistor and compared against a reference by the Current Sense comparator. When the current limit threshold is reached, the comparator resets the PWM latch. The current limit threshold is typically set at 6.5 A.

Figure 10 illustrates switch output current limit threshold versus temperature.

Error Amplifier and Reference

A high gain Error Amplifier is provided with access to the inverting input and output. This amplifier features a typical dc voltage gain of 80 dB, and a unity gain bandwidth of 600 kHz with 70 degrees of phase margin (Figure 4). The noninverting input is biased to the internal 5.05 V reference and is not pinned out. The reference has an accuracy of $\pm 2.0\%$ at room temperature. To provide 5.0 V at the load, the reference is programmed 50 mV above 5.0 V to compensate for a 1.0% voltage drop in the cable and connector from the converter output. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input as shown in Figures 14 and 19. The equation for determining the output voltage with the divider network is:

$$V_{out} = 5.05 \left(\frac{R_2}{R_1} + 1 \right)$$

External loop compensation is required for converter stability. A simple low-pass filter is formed by connecting a resistor (R_2) from the regulated output to the inverting input, and a series resistor-capacitor (R_F , C_F) between Pins 1 and 5. The compensation network component values shown in each of the applications circuits were selected to provide stability over the tested operating conditions. The step-down converter (Figure 19) is the easiest to compensate for stability. The step-up (Figure 21) and voltage-inverting (Figure 23) configurations operate as continuous conduction flyback converters, and are more difficult to compensate. The simplest way to optimize the compensation network is to observe the response of the output voltage to a step load change, while adjusting R_F and C_F for critical damping. The final circuit should be verified for stability under four boundary conditions. These conditions are minimum and maximum input voltages, with minimum and maximum loads.

By clamping the voltage on the error amplifier output (Pin 5) to less than 150 mV, the internal circuitry will be placed into a low power standby mode, reducing the power supply current to 36 μ A with a 12 V supply voltage. Figure 11 illustrates the standby supply current versus supply voltage.

The Error Amplifier output has a 100 μ A current source pull-up that can be used to implement soft-start. Figure 18 shows the current source charging capacitor C_{SS} through a series diode. The diode disconnects C_{SS} from the feedback loop when the 1.0 M resistor charges it above the operating range of Pin 5.

Switch Output

The output transistor is designed to switch a maximum of 40 V, with a minimum peak collector current of 5.5 A. When configured for step-down or voltage-inverting applications, as in Figures 19 and 23, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency. Figure 9 shows that by clamping the emitter to 0.5 V, the collector current will be in the range of 100 μ A over temperature. A 1N5825 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit is fully

functional before the output stage is enabled. The internal reference voltage is monitored by the comparator which enables the output stage when V_{CC} exceeds 5.9 V. To prevent erratic output switching as the threshold is crossed, 0.9 V of hysteresis is provided.

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the latch is forced into a 'reset' state, disabling the output switch. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended to be used as a substitute for proper heatsinking.** The MC34167 is contained in a 5-lead TO-220 type package. The tab of the package is common with the center pin (Pin 3) and is normally connected to ground.

DESIGN CONSIDERATIONS

Do not attempt to construct a converter on wire-wrap or plug-in prototype boards. Special care should be taken to separate ground paths from signal currents and ground paths from load currents. All high current loops should be kept as short as possible using heavy copper runs to minimize ringing and radiated EMI. For best operation, a

tight component layout is recommended. Capacitors C_{in} , C_O , and all feedback components should be placed as close to the IC as physically possible. It is also imperative that the Schottky diode connected to the Switch Output be located as close to the IC as possible.

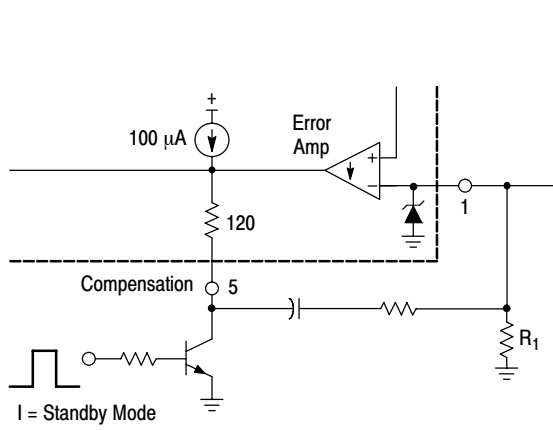


Figure 16. Low Power Standby Circuit

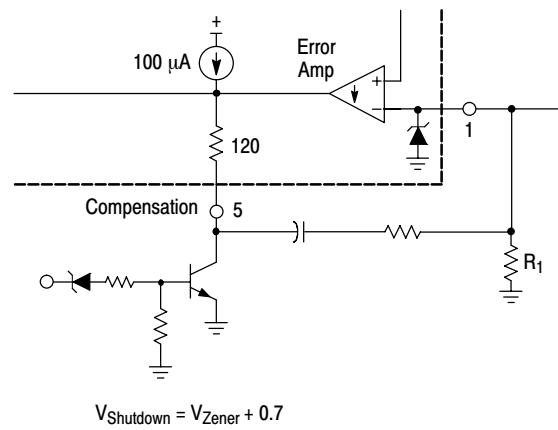


Figure 17. Over Voltage Shutdown Circuit

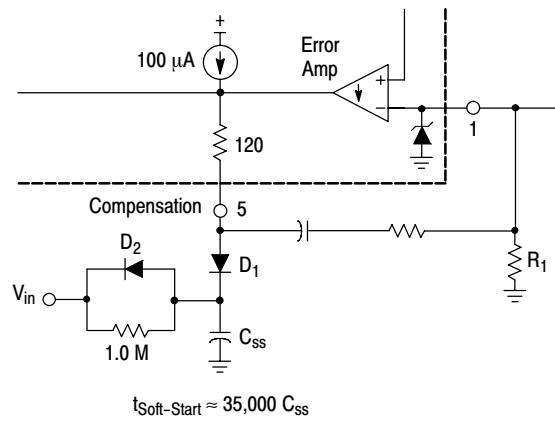
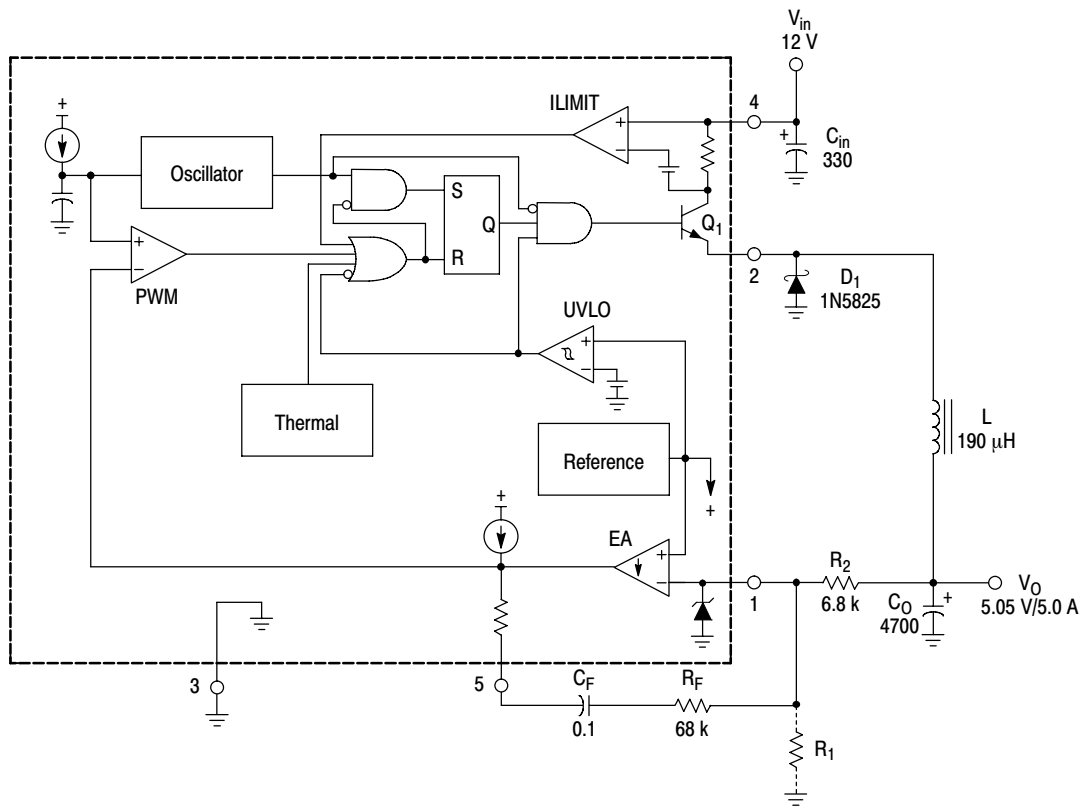


Figure 18. Soft-Start Circuit

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Test	Conditions	Results
Line Regulation	$V_{in} = 10 \text{ V to } 36 \text{ V}$, $I_O = 5.0 \text{ A}$	$4.0 \text{ mV} = \pm 0.039\%$
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 0.25 \text{ A to } 5.0 \text{ A}$	$1.0 \text{ mV} = \pm 0.01\%$
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 5.0 \text{ A}$	20 mV_{pp}
Short Circuit Current	$V_{in} = 12 \text{ V}$, $R_L = 0.1 \Omega$	6.5 A
Efficiency	$V_{in} = 12 \text{ V}$, $I_O = 5.0 \text{ A}$ $V_{in} = 24 \text{ V}$, $I_O = 5.0 \text{ A}$	78.9% 82.6%

L = Coilcraft M1496-A or General Magnetics Technology GMT-0223, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

The Step-Down Converter application is shown in Figure 19. The output switch transistor Q_1 interrupts the input voltage, generating a squarewave at the LC_O filter input. The filter averages the squarewaves, producing a dc output voltage that can be set to any level between V_{in} and V_{ref} by controlling the percent conduction time of Q_1 to that of the total oscillator cycle time. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input.

Figure 19. Step-Down Converter

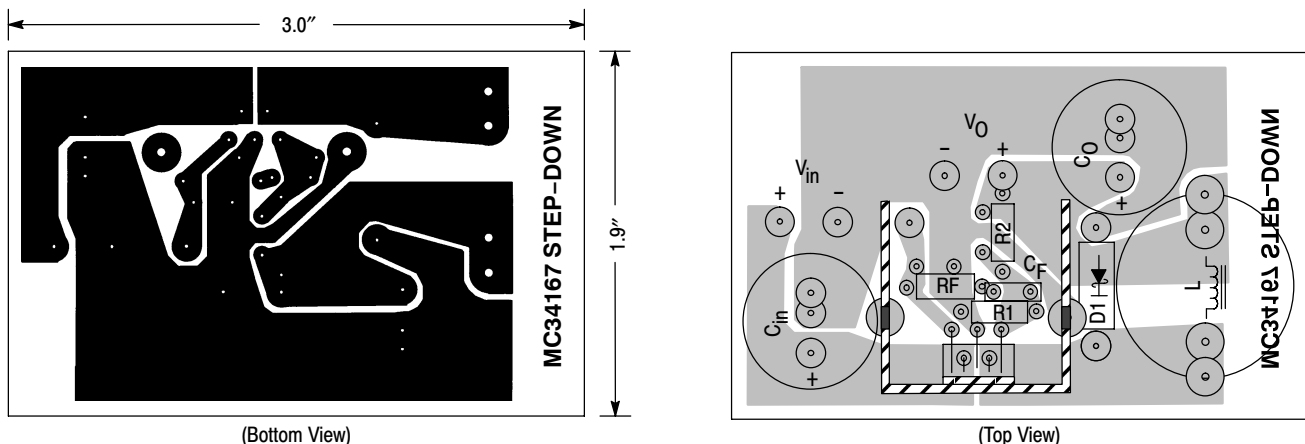
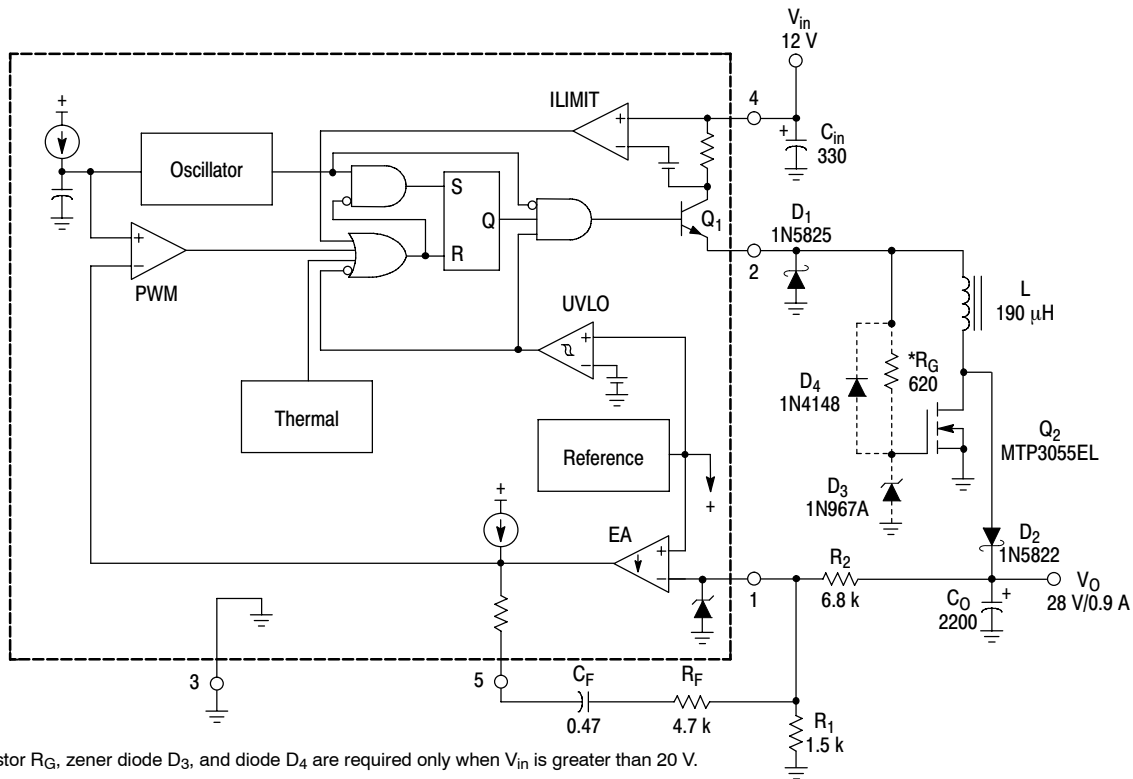


Figure 20. Step-Down Converter Printed Circuit Board and Component Layout

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*Gate resistor R_G , zener diode D_3 , and diode D_4 are required only when V_{in} is greater than 20 V.

Test	Conditions	Results
Line Regulation	$V_{in} = 10 \text{ V to } 24 \text{ V}$, $I_O = 0.9 \text{ A}$	$10 \text{ mV} = \pm 0.017\%$
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 0.1 \text{ A to } 0.9 \text{ A}$	$30 \text{ mV} = \pm 0.053\%$
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 0.9 \text{ A}$	140 mV_{pp}
Short Circuit Current	$V_{in} = 12 \text{ V}$, $R_L = 0.1 \Omega$	6.0 A
Efficiency	$V_{in} = 12 \text{ V}$, $I_O = 0.9 \text{ A}$ $V_{in} = 24 \text{ V}$, $I_O = 0.9 \text{ A}$	80.1% 87.8%

L = Coilcraft M1496-A or General Magnetics Technology GMT-0223, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.

Heatsink = Aavid Engineering Inc. MC34167: 5903B, or 5930B MTP3055EL: 5925B

Figure 21 shows that the MC34167 can be configured as a step-up/down converter with the addition of an external power MOSFET. Energy is stored in the inductor during the ON time of transistors Q_1 and Q_2 . During the OFF time, the energy is transferred, with respect to ground, to the output filter capacitor and load. This circuit configuration has two significant advantages over the basic step-up converter circuit. The first advantage is that output short circuit protection is provided by the MC34167, since Q_1 is directly in series with V_{in} and the load. Second, the output voltage can be programmed to be less than V_{in} . Notice that during the OFF time, the inductor forward biases diodes D_1 and D_2 , transferring its energy with respect to ground rather than with respect to V_{in} . When operating with V_{in} greater than 20 V, a gate protection network is required for the MOSFET. The network consists of components R_G , D_3 , and D_4 .

Figure 21. Step-Up/Down Converter

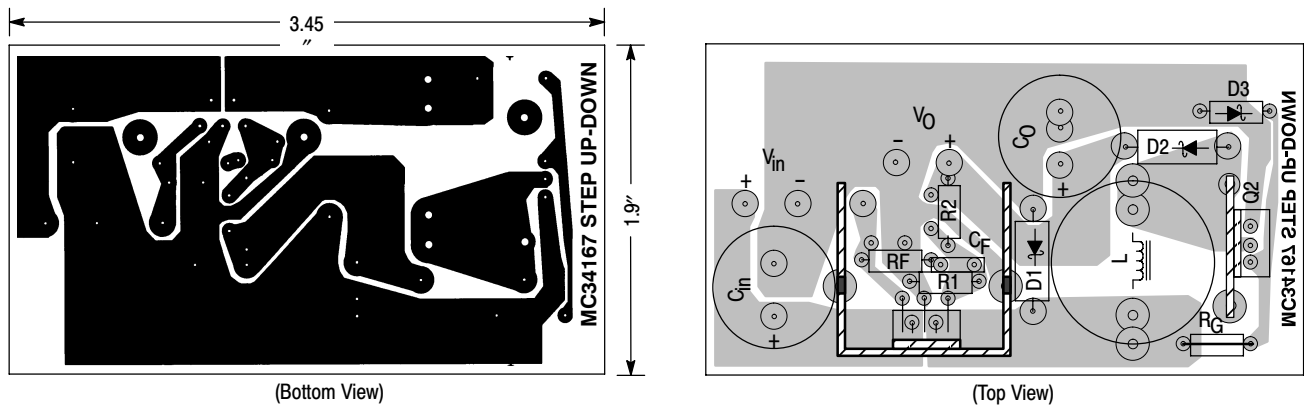
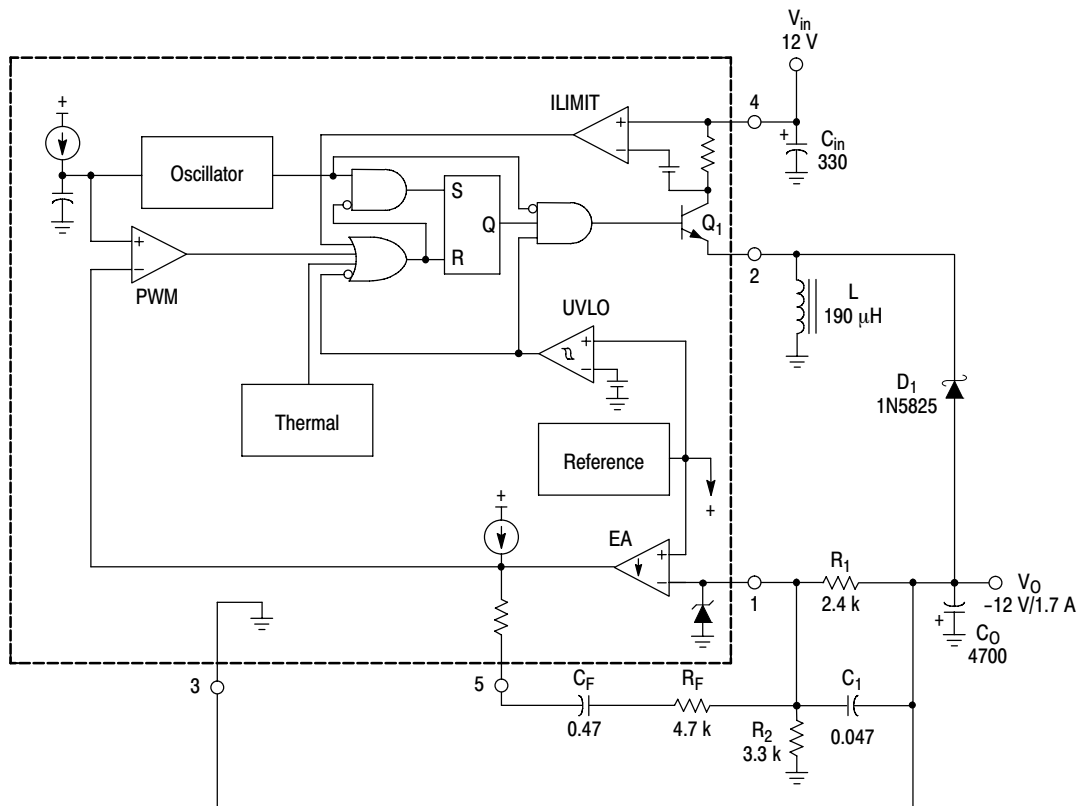


Figure 22. Step-Up/Down Converter Printed Circuit Board and Component Layout

MC34167, MC33167



Test	Conditions	Results
Line Regulation	$V_{in} = 10 \text{ V to } 24 \text{ V}$, $I_O = 1.7 \text{ A}$	$15 \text{ mV} = \pm 0.61\%$
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 0.1 \text{ A to } 1.7 \text{ A}$	$4.0 \text{ mV} = \pm 0.020\%$
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 1.7 \text{ A}$	78 mV_{pp}
Short Circuit Current	$V_{in} = 12 \text{ V}$, $R_L = 0.1 \Omega$	5.7 A
Efficiency	$V_{in} = 12 \text{ V}$, $I_O = 1.7 \text{ A}$ $V_{in} = 24 \text{ V}$, $I_O = 1.7 \text{ A}$	79.5% 86.2%

L = Coilcraft M1496-A or General Magnetics Technology GMT-0223, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core. Heatsink = Aavid Engineering Inc. 5903B, or 5930B.

Two potential problems arise when designing the standard voltage-inverting converter with the MC34167. First, the Switch Output emitter is limited to -1.5 V with respect to the ground pin and second, the Error Amplifier's noninverting input is internally committed to the reference and is not pinned out. Both of these problems are resolved by connecting the IC ground pin to the converter's negative output as shown in Figure 23. This keeps the emitter of Q_1 positive with respect to the ground pin and has the effect of reversing the Error Amplifier inputs. Note that the voltage drop across R_1 is equal to 5.05 V when the output is in regulation.

Figure 23. Voltage-Inverting Converter

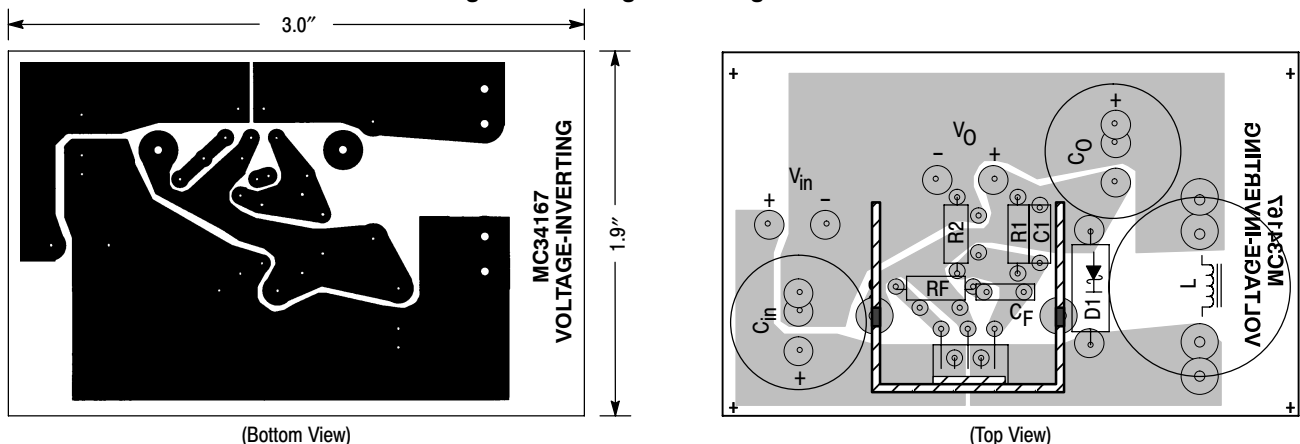


Figure 24. Voltage-Inverting Converter Printed Circuit Board and Component Layout

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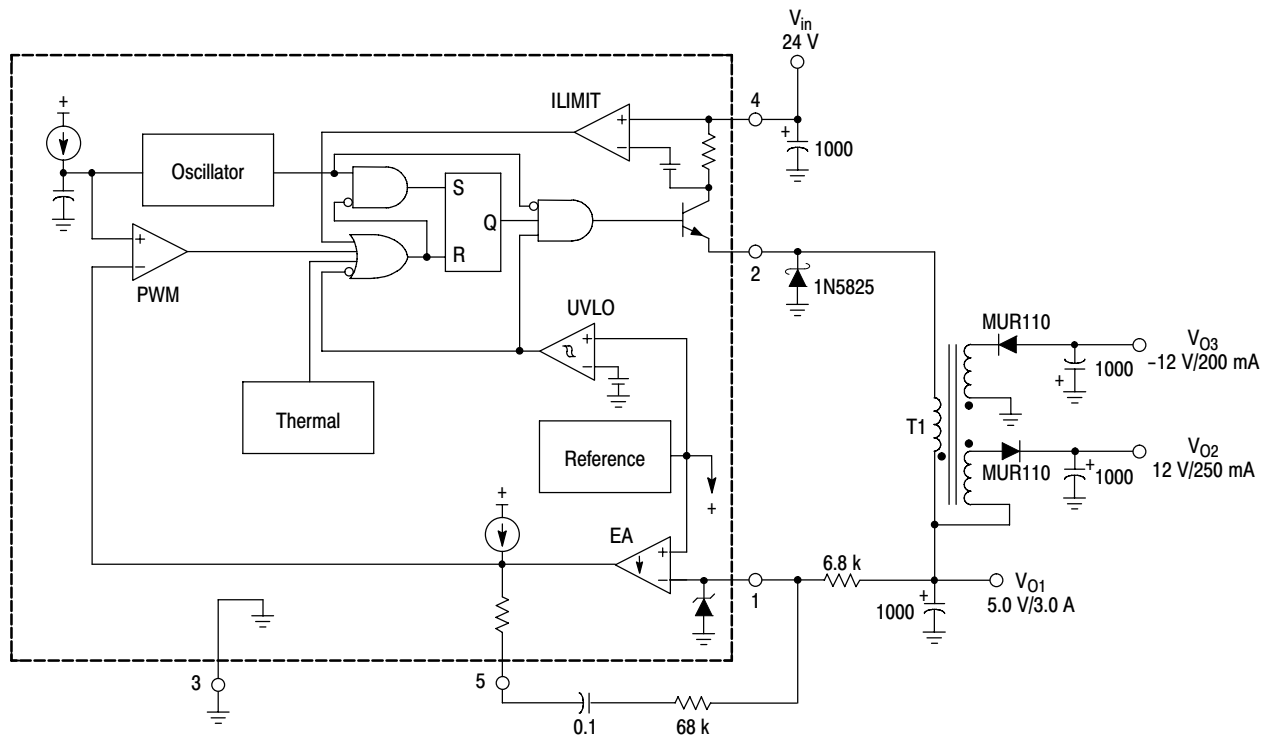


Figure 25. Triple Output Converter

Tests		Conditions	Results
Line Regulation	5.0 V 12 V -12 V	$V_{in} = 15 \text{ V to } 30 \text{ V}$, $I_{O1} = 3.0 \text{ A}$, $I_{O2} = 250 \text{ mA}$, $I_{O3} = 200 \text{ mA}$	3.0 mV = $\pm 0.029\%$ 572 mV = $\pm 2.4\%$ 711 mV = $\pm 2.9\%$
Load Regulation	5.0 V 12 V -12 V	$V_{in} = 24 \text{ V}$, $I_{O1} = 30 \text{ mA to } 3.0 \text{ A}$, $I_{O2} = 250 \text{ mA}$, $I_{O3} = 200 \text{ mA}$ $V_{in} = 24 \text{ V}$, $I_{O1} = 3.0 \text{ A}$, $I_{O2} = 100 \text{ mA to } 250 \text{ mA}$, $I_{O3} = 200 \text{ mA}$ $V_{in} = 24 \text{ V}$, $I_{O1} = 3.0 \text{ A}$, $I_{O2} = 250 \text{ mA}$, $I_{O3} = 75 \text{ mA to } 200 \text{ mA}$	1.0 mV = $\pm 0.009\%$ 409 mV = $\pm 1.5\%$ 528 mV = $\pm 2.0\%$
Output Ripple	5.0 V 12 V -12 V	$V_{in} = 24 \text{ V}$, $I_{O1} = 3.0 \text{ A}$, $I_{O2} = 250 \text{ mA}$, $I_{O3} = 200 \text{ mA}$	75 mV _{pp} 20 mV _{pp} 20 mV _{pp}
Short Circuit Current	5.0 V 12 V -12 V	$V_{in} = 24 \text{ V}$, $R_L = 0.1 \Omega$	6.5 A 2.7 A 2.2 A
Efficiency	TOTAL	$V_{in} = 24 \text{ V}$, $I_{O1} = 3.0 \text{ A}$, $I_{O2} = 250 \text{ mA}$, $I_{O3} = 200 \text{ mA}$	84.2%

T1 = Primary: Coilcraft M1496-A or General Magnetics Technology GMT-0223, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.

Secondary: V_{O2} – 69 turns of #26 AWG

V_{O3} – 104 turns of #28 AWG

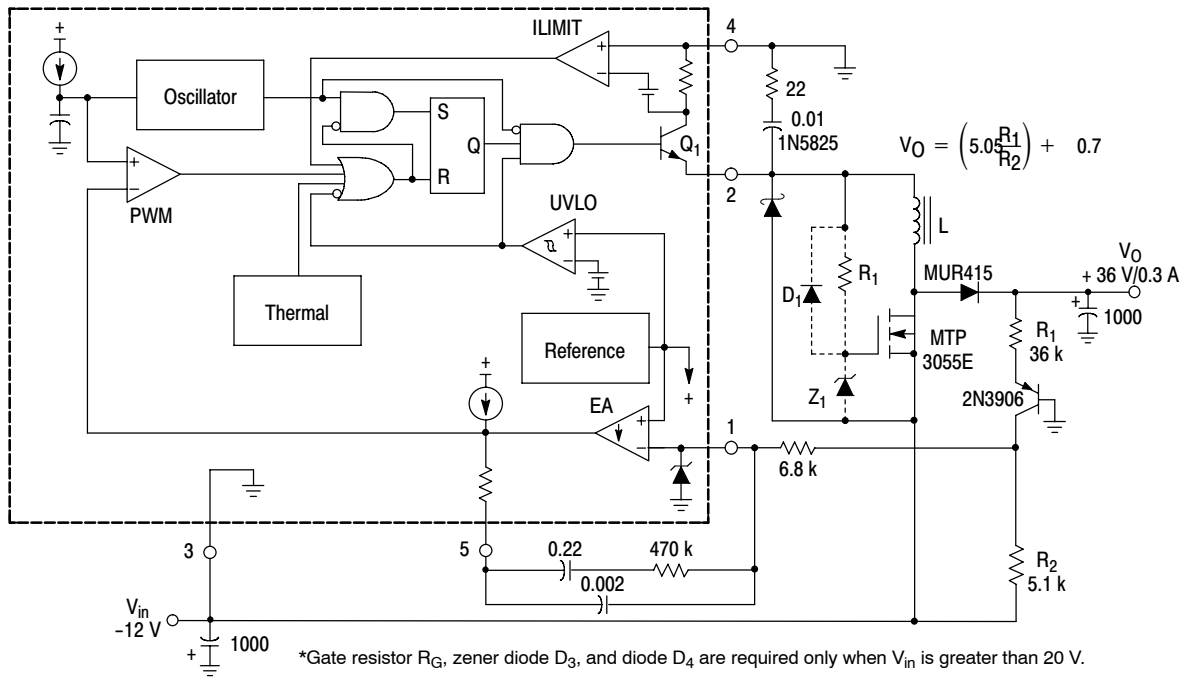
Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Multiple auxiliary outputs can easily be derived by winding secondaries on the main output inductor to form a transformer. The secondaries must be connected so that the energy is delivered to the auxiliary outputs when the Switch Output turns off. During the OFF time, the voltage across the primary winding is regulated by the feedback loop, yielding a constant Volts/Turn ratio. The number of turns for any given secondary voltage can be calculated by the following equation:

$$\# \text{ TURNS}_{(\text{SEC})} = \frac{V_{O(\text{SEC})} + V_{F(\text{SEC})}}{\left(\frac{V_{O(\text{PRI})} + V_{F(\text{PRI})}}{\# \text{ TURNS}_{(\text{PRI})}} \right)}$$

Note that the 12 V winding is stacked on top of the 5.0 V output. This reduces the number of secondary turns and improves load regulation. For best auxiliary regulation, the auxiliary outputs should be less than 33% of the total output power.

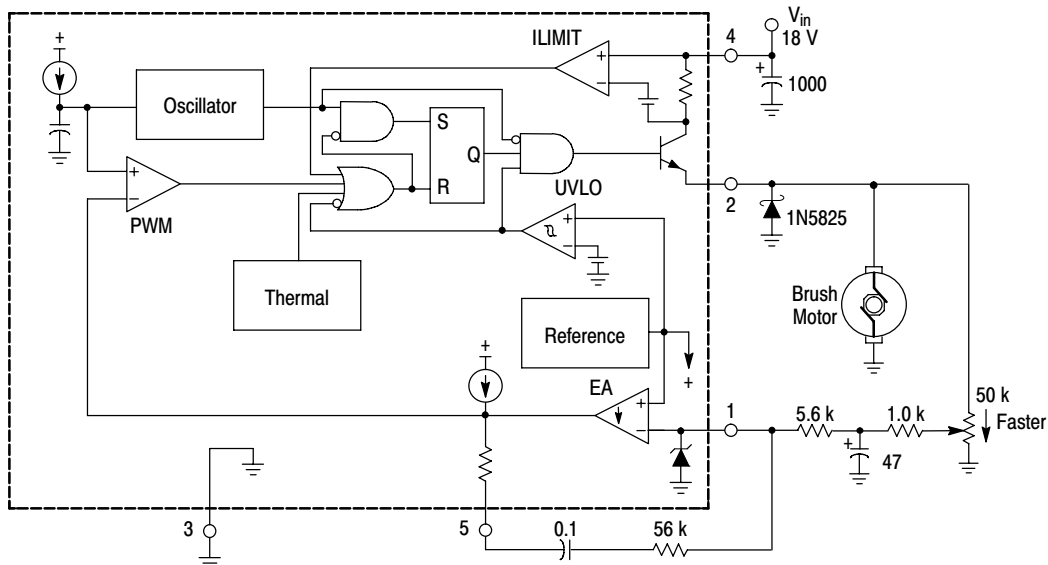
MC34167, MC33167



Test	Conditions	Results
Line Regulation	$V_{in} = -10\text{ V to } -20\text{ V}$, $I_O = 0.3\text{ A}$	266 mV $\pm$ 0.38%
Load Regulation	$V_{in} = -12\text{ V}$, $I_O = 0.03\text{ A to } 0.3\text{ A}$	7.90 mV $\pm$ 1.1%
Output Ripple	$V_{in} = -12\text{ V}$, $I_O = 0.3\text{ A}$	100 mV _{pp}
Efficiency	$V_{in} = -12\text{ V}$, $I_O = 0.3\text{ A}$	78.4%

L = General Magnetics Technology GMT-0223, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core. Heatsink = Aavid Engineering Inc. 5903B or 5930B

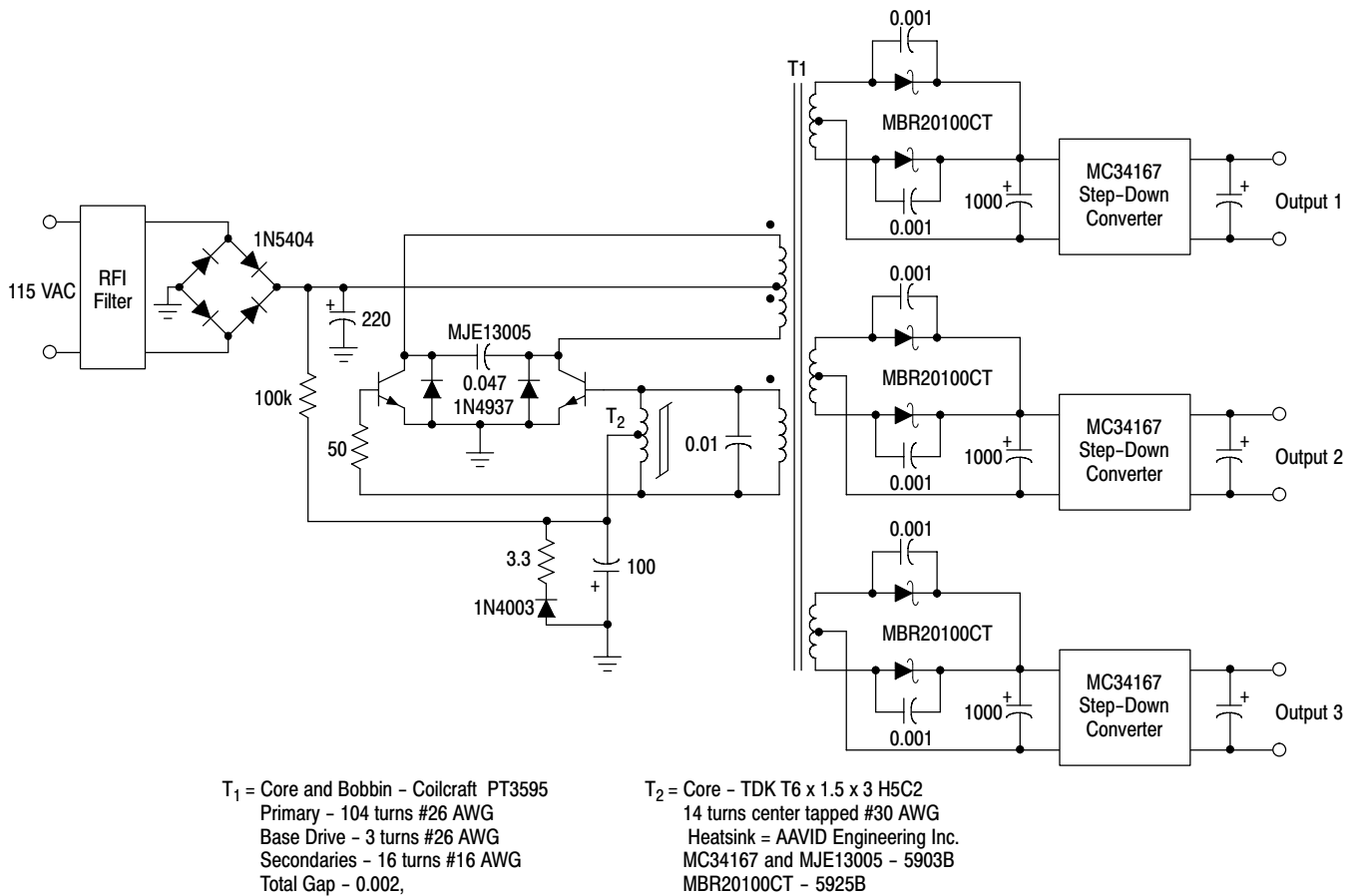
Figure 26. Negative Input/Positive Output Regulator



Test	Conditions	Results
Low Speed Line Regulation	$V_{in} = 12\text{ V to } 24\text{ V}$	1760 RPM $\pm$ 1%
High Speed Line Regulation	$V_{in} = 12\text{ V to } 24\text{ V}$	3260 RPM $\pm$ 6%

Figure 27. Variable Motor Speed Control with EMF Feedback Sensing

MC34167, MC33167



The MC34167 can be used cost effectively in off-line applications even though it is limited to a maximum input voltage of 40 V. Figure 28 shows a simple and efficient method for converting the AC line voltage down to 24 V. This preconverter has a total power rating of 125 W with a conversion efficiency of 90%. Transformer T_1 provides output isolation from the AC line and isolation between each of the secondaries. The circuit self-oscillates at 50 kHz and is controlled by the saturation characteristics of T_2 . Multiple MC34167 post regulators can be used to provide accurate independently regulated outputs for a distributed power system.

Figure 28. Off-Line Preconverter

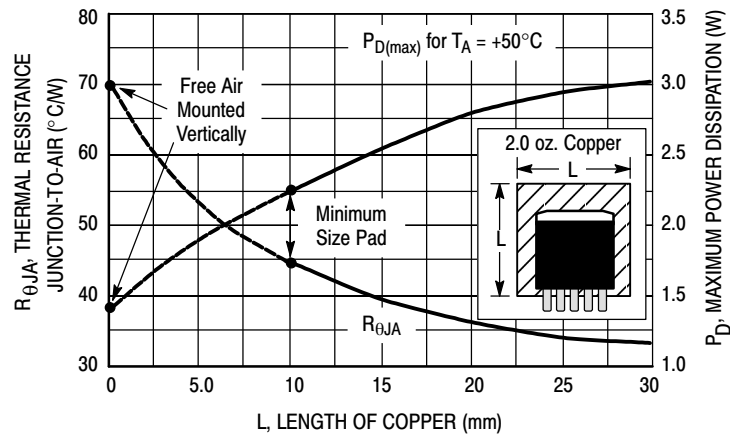


Figure 29. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

MC34167, MC33167

Table 1. Design Equations

Calculation	Step-Down	Step-Up/Down	Voltage-Inverting
$\frac{t_{on}}{t_{off}}$ (Notes 1, 2)	$\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_{F1} + V_{F2}}{V_{in} - V_{satQ1} - V_{satQ2}}$	$\frac{ V_{out} + V_F}{V_{in} - V_{sat}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc} \left(\frac{t_{on}}{t_{off}} + 1 \right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc} \left(\frac{t_{on}}{t_{off}} + 1 \right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc} \left(\frac{t_{on}}{t_{off}} + 1 \right)}$
Duty Cycle (Note 3)	$t_{on} f_{osc}$	$t_{on} f_{osc}$	$t_{on} f_{osc}$
$I_{L\ avg}$	I_{out}	$I_{out} \left(\frac{t_{on}}{t_{off}} + 1 \right)$	$I_{out} \left(\frac{t_{on}}{t_{off}} + 1 \right)$
$I_{pk(switch)}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$
L	$\left(\frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L} \right) t_{on}$	$\left(\frac{V_{in} - V_{satQ1} - V_{satQ2}}{\Delta I_L} \right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L} \right) t_{on}$
$V_{ripple(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8f_{osc}C_O} \right)^2 + (ESR)^2}$	$\left(\frac{t_{on}}{t_{off}} + 1 \right) \sqrt{\left(\frac{1}{f_{osc}C_O} \right)^2 + (ESR)^2}$	$\left(\frac{t_{on}}{t_{off}} + 1 \right) \sqrt{\left(\frac{1}{f_{osc}C_O} \right)^2 + (ESR)^2}$
V_{out}	$V_{ref} \left(\frac{R_2}{R_1} + 1 \right)$	$V_{ref} \left(\frac{R_2}{R_1} + 1 \right)$	$V_{ref} \left(\frac{R_2}{R_1} + 1 \right)$

1. V_{sat} – Switch Output source saturation voltage, refer to Figure 8.
2. V_F – Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.35 V.
3. Duty cycle is calculated at the minimum operating input voltage and must not exceed the guaranteed minimum $DC_{(max)}$ specification of 0.92.

The following converter characteristics must be chosen:

- V_{out} – Desired output voltage.
- I_{out} – Desired output current.
- ΔI_L – Desired peak-to-peak inductor ripple current. For maximum output current especially when the duty cycle is greater than 0.5, it is suggested that ΔI_L be chosen minimum current limit threshold of 5.5 A. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2 (I_{L\ avg})$. This will proportionally reduce the converter's output current capability.
- $V_{ripple(pp)}$ – Desired peak-to-peak output ripple voltage. For best performance, the ripple voltage should be kept to less than 2% of V_{out} . Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

MC34167, MC33167

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping [†]
MC33167D2T	$T_A = -40^\circ \text{ to } +85^\circ \text{C}$	D ² PAK (Surface Mount)	50 Units/Rail
MC33167T		TO-220 (Straight Lead)	
MC33167TG		TO-220 (Straight Lead) (Pb-Free)	50 Units/Rail
MC33167TH	$T_A = -40^\circ \text{ to } +85^\circ \text{C}$	TO-220 (Horizontal Mount)	50 Units/Rail
MC33167TV		TO-220 (Vertical Mount)	
MC33167TVG		TO-220 (Vertical Mount) (Pb-Free)	50 Units/Rail
MC34167D2T	$T_A = 0^\circ \text{ to } +70^\circ \text{C}$	D ² PAK (Surface Mount)	50 Units/Rail
MC34167T		TO-220 (Straight Lead)	
MC34167TH		TO-220 (Horizontal Mount)	
MC34167TV		TO-220 (Vertical Mount)	
MC34167TVG		TO-220 (Vertical Mount) (Pb-Free)	50 Units/Rail

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP1400A

100 mA, Fixed Frequency PWM Step-Up Micropower Switching Regulator

The NCP1400A series are micropower step-up DC to DC converters that are specifically designed for powering portable equipment from one or two cell battery packs. These devices are designed to startup with a cell voltage of 0.8 V and operate down to less than 0.2 V. With only four external components, this series allows a simple means to implement highly efficient converters that are capable of up to 100 mA of output current.

Each device consists of an on-chip fixed frequency oscillator, pulse width modulation controller, phase compensated error amplifier that ensures converter stability with discontinuous mode operation, soft-start, voltage reference, driver, and power MOSFET switch with current limit protection. Additionally, a chip enable feature is provided to power down the converter for extended battery life.

The NCP1400A device series are available in the Thin SOT23-5 package with seven standard regulated output voltages. Additional voltages that range from 1.8 V to 4.9 V in 100 mV steps can be manufactured.

Features

- Extremely Low Startup Voltage of 0.8 V
- Operation Down to Less than 0.2 V
- Only Four External Components for Simple Highly Efficient Converters
- Up to 100 mA Output Current Capability
- Fixed Frequency Pulse Width Modulation Operation
- Phase Compensated Error Amplifier for Stable Converter Operation
- Chip Enable Power Down Capability for Extended Battery Life
- Pb-Free Packages are Available

Typical Applications

- Cellular Telephones
- Pagers
- Personal Digital Assistants
- Electronic Games
- Digital Cameras
- Camcorders
- Handheld Instruments
- White LED Torch Light



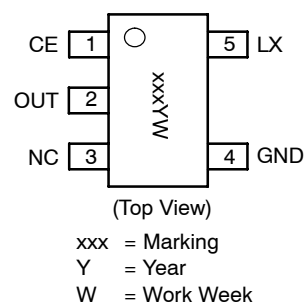
ON Semiconductor®

<http://onsemi.com>



THIN SOT23-5
SN SUFFIX
CASE 483

PIN CONNECTIONS AND MARKING DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 256 of this data sheet.

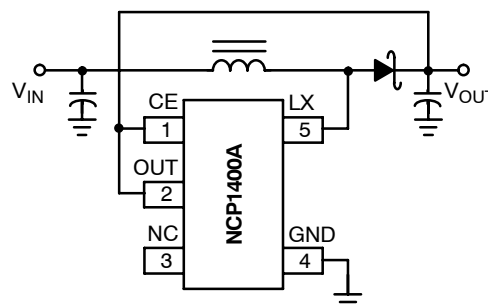


Figure 1. Typical Step-Up Converter Application

NCP1400A

ORDERING INFORMATION

Device	Output Voltage	Switching Frequency	Marking	Package	Shipping [†]
NCP1400ASN19T1	1.9 V	180 KHz	DAI	Thin SOT23-5	3000 / Tape & Reel (7 Inch Reel)
NCP1400ASN19T1G	1.9 V		DAI	Thin SOT23-5 (Pb-Free)	
NCP1400ASN22T1	2.2 V		DCN	Thin SOT23-5	
NCP1400ASN22T1G	2.2 V		DCN	Thin SOT23-5 (Pb-Free)	
NCP1400ASN25T1	2.5 V		DAV	Thin SOT23-5	
NCP1400ASN25T1G	2.5 V		DAV	Thin SOT23-5 (Pb-Free)	
NCP1400ASN27T1	2.7 V		DAA	Thin SOT23-5	
NCP1400ASN30T1	3.0 V		DAB		
NCP1400ASN33T1	3.3 V		DAJ		
NCP1400ASN38T1	3.8 V		DBK		
NCP1400ASN38T1G	3.8 V		DBK	Thin SOT23-5 (Pb-Free)	
NCP1400ASN45T1	4.5 V		DBL	Thin SOT23-5	
NCP1400ASN45T1G	4.5 V		DBL	Thin SOT23-5 (Pb-Free)	
NCP1400ASN50T1	5.0 V		DAD	Thin SOT23-5	
NCP1400ASN50T1G	5.0 V		DAD	Thin SOT23-5 (Pb-Free)	

NOTE: The ordering information lists seven standard output voltage device options. Additional devices with output voltage ranging from 1.8 V to 5.0 V in 100 mV increments can be manufactured. Contact your ON Semiconductor representative for availability.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 2)	V _{OUT}	-0.3 to 6.0	V
Input/Output Pins LX (Pin 5) LX Peak Sink Current	V _{LX} I _{LX}	-0.3 to 6.0 400	V mA
CE (Pin 1) Input Voltage Range Input Current Range	V _{CE} I _{CE}	-0.3 to 6.0 -150 to 150	V mA
Thermal Resistance Junction to Air	R _{θJA}	250	°C/W
Operating Ambient Temperature Range (Note 2)	T _A	-40 to +85	°C
Operating Junction Temperature Range	T _J	-40 to +125	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- This device series contains ESD protection and exceeds the following tests:
Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22-A114.
Machine Model (MM) ±200 V per JEDEC standard: JESD22-A115.
- The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

- Latchup Current Maximum Rating: ±150 mA per JEDEC standard: JESD78.
- Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.

NCP1400A

ELECTRICAL CHARACTERISTICS (For all values $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit

OSCILLATOR

Frequency ($V_{OUT} = V_{SET} \times 0.96$, Note 5)	f_{OSC}	144	180	216	kHz
Frequency Temperature Coefficient ($T_A = -40^\circ\text{C}$ to 85°C)	Δf	–	0.11	–	%/ $^\circ\text{C}$
Maximum PWM Duty Cycle ($V_{OUT} = V_{SET} \times 0.96$)	D_{MAX}	68	75	82	%
Minimum Startup Voltage ($I_O = 0$ mA)	V_{start}	–	0.8	0.95	V
Minimum Startup Voltage Temperature Coefficient ($T_A = -40^\circ\text{C}$ to 85°C)	ΔV_{start}	–	–1.6	–	mV/ $^\circ\text{C}$
Minimum Operation Hold Voltage ($I_O = 0$ mA)	V_{hold}	0.3	–	–	V
Soft-Start Time ($V_{OUT} > 0.8$ V)	t_{SS}	0.5	2.0	–	ms

LX (PIN 5)

LX Pin On-State Sink Current ($V_{LX} = 0.4$ V) Device Suffix: 19T1 22T1 25T1 27T1 30T1 33T1 38T1 45T1 50T1	I_{LX}	80 80 80 100 100 100 100 100 100 100	90 90 120 125 130 135 145 155 160	– – – – – – – – – –	mA
Voltage Limit ($V_{OUT} = V_{CE} = V_{SET} \times 0.96$, V_{LX} "L" Side)	V_{LXLIM}	0.65	0.8	1.0	V
Off-State Leakage Current ($V_{LX} = 5.0$ V, $T_A = -40^\circ\text{C}$ to 85°C)	I_{LKG}	–	0.5	1.0	μA

CE (PIN 1)

CE Input Voltage ($V_{OUT} = V_{SET} \times 0.96$) High State, Device Enabled Low State, Device Disabled	$V_{CE(high)}$ $V_{CE(low)}$	0.9 –	– –	– 0.3	V
CE Input Current (Note 6) High State, Device Enabled ($V_{OUT} = V_{CE} = 5.0$ V) Low State, Device Disabled ($V_{OUT} = 5.0$ V, $V_{CE} = 0$ V)	$I_{CE(high)}$ $I_{CE(low)}$	–0.5 –0.5	0 0.15	0.5 0.5	μA

5. V_{SET} means setting of output voltage.

6. CE pin is integrated with an internal 150 nA pullup current source.

NCP1400A

ELECTRICAL CHARACTERISTICS (continued) (For all values $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
TOTAL DEVICE					
Output Voltage ($V_{IN} = 0.7 \times V_{OUT}$, $I_O = 10\text{ mA}$) Device Suffix: 19T1 22T1 25T1 27T1 30T1 33T1 38T1 45T1 50T1	V_{OUT}	1.853 2.145 2.438 2.633 2.925 3.218 3.705 4.3875 4.875	1.9 2.2 2.5 2.7 3.0 3.3 3.8 4.5 5.0	1.948 2.255 2.563 2.768 3.075 3.383 3.895 4.6125 5.125	V
Output Voltage Temperature Coefficient ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) Device Suffix: 19T1 22T1 25T1 27T1 30T1 33T1 38T1 45T1 50T1	ΔV_{OUT}	– – – – – – – – –	100 100 100 100 100 100 150 150 150	– – – – – – – – –	ppm/ $^\circ\text{C}$
Operating Current 2 ($V_{OUT} = V_{CE} = V_{SET} + 0.5\text{ V}$, Note 5)	I_{DD2}	–	7.0	15	μA
Off-State Current ($V_{OUT} = 5.0\text{ V}$, $V_{CE} = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, Note 6)	I_{OFF}	–	0.6	1.5	μA
Operating Current 1 ($V_{OUT} = V_{CE} = V_{SET} \times 0.96$, $f_{OSC} = 180\text{ kHz}$) Device Suffix: 19T1 22T1 25T1 27T1 30T1 33T1 38T1 45T1 50T1	I_{DD1}	– – – – – – – – –	23 27 32 32 37 37 44 53 70	50 60 60 60 60 60 65 75 100	μA

5. V_{SET} means setting of output voltage.

6. CE pin is integrated with an internal 150 nA pullup current source.

NCP1400A

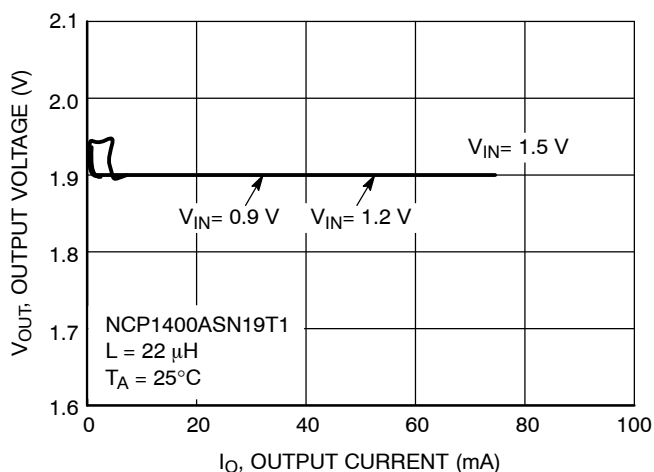


Figure 2. NCP1400ASN19T1 Output Voltage vs. Output Current

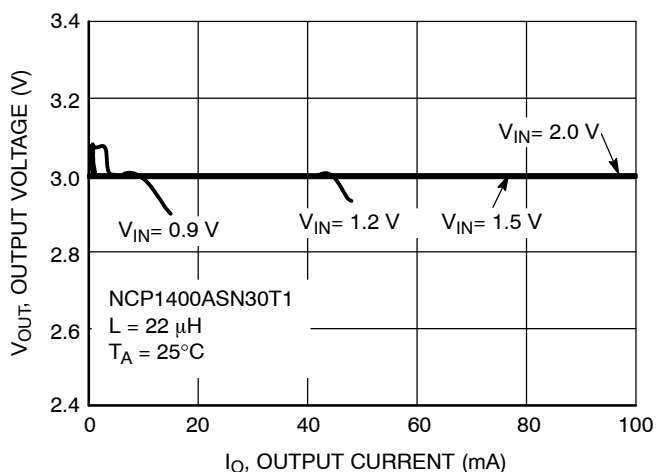


Figure 3. NCP1400ASN30T1 Output Voltage vs. Output Current

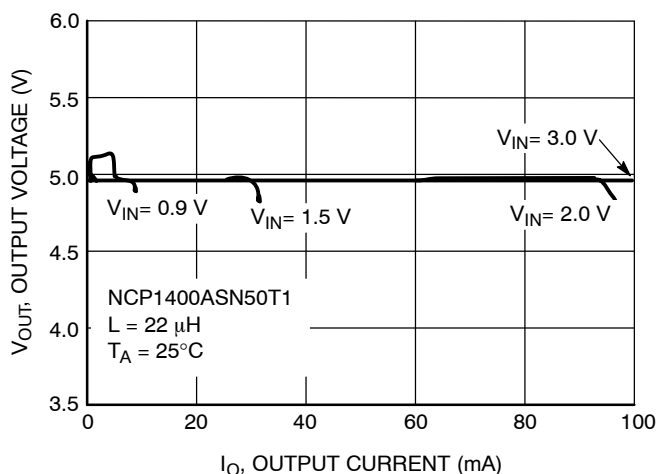


Figure 4. NCP1400ASN50T1 Output Voltage vs. Output Current

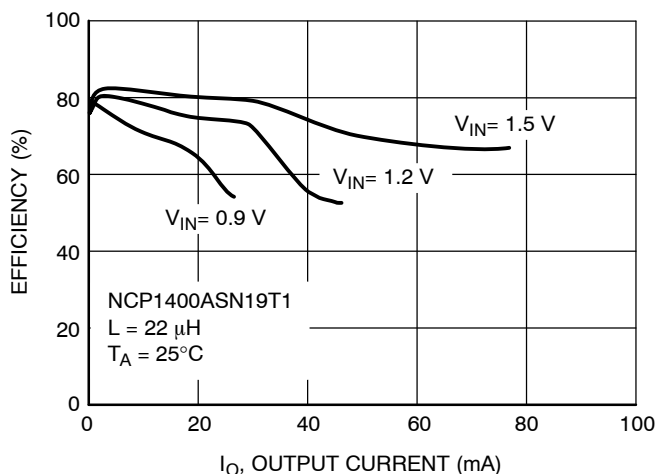


Figure 5. NCP1400ASN19T1 Efficiency vs. Output Current

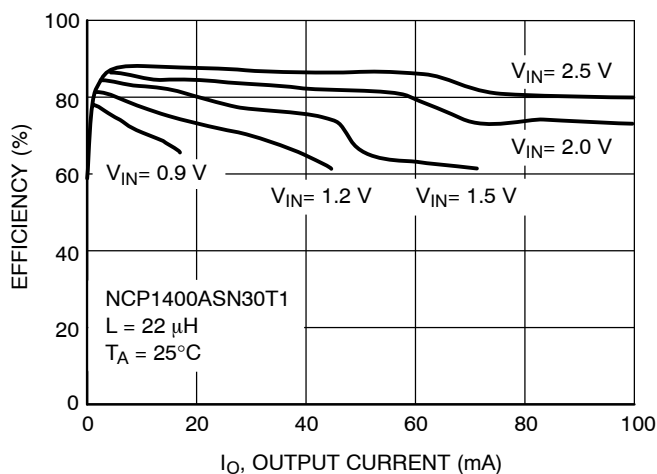


Figure 6. NCP1400ASN30T1 Efficiency vs. Output Current

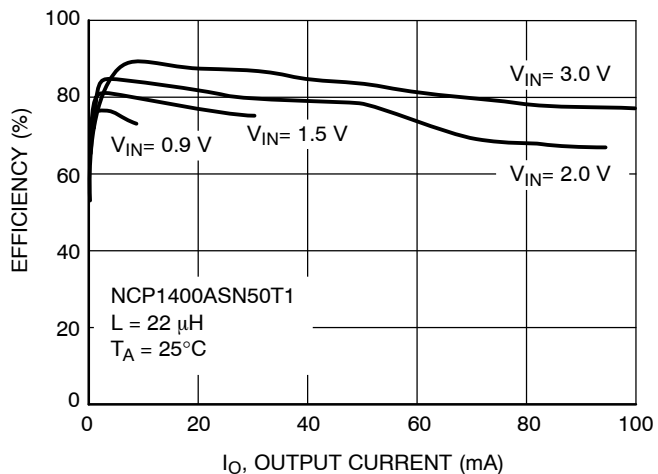


Figure 7. NCP1400ASN50T1 Efficiency vs. Output Current

NCP1400A

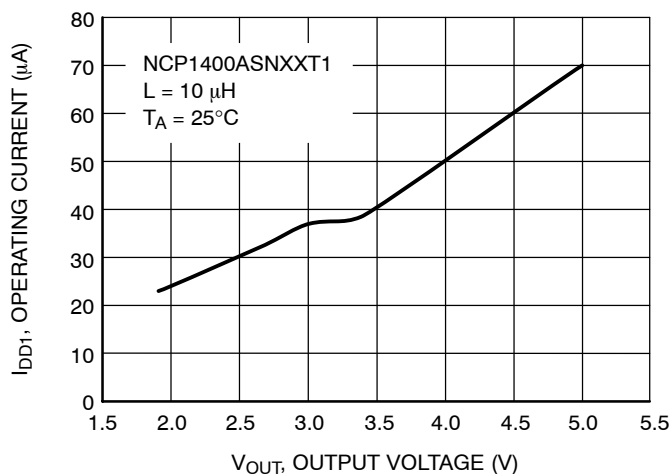


Figure 8. NCP1400ASNXXT1 Operating Current (I_{DD1}) vs. Output Voltage

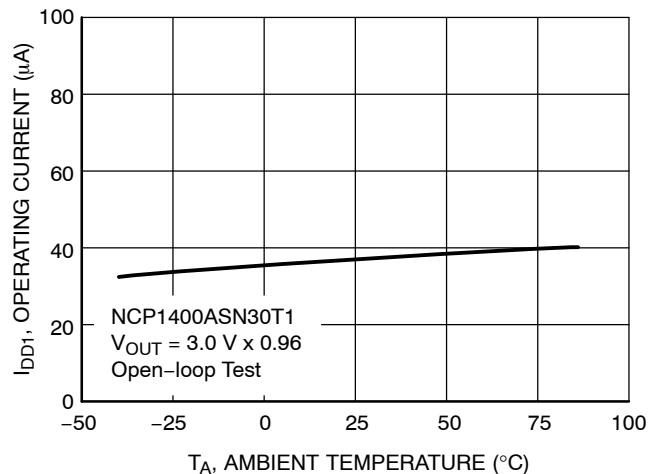


Figure 9. NCP1400ASN30T1 Current Consumption vs. Temperature

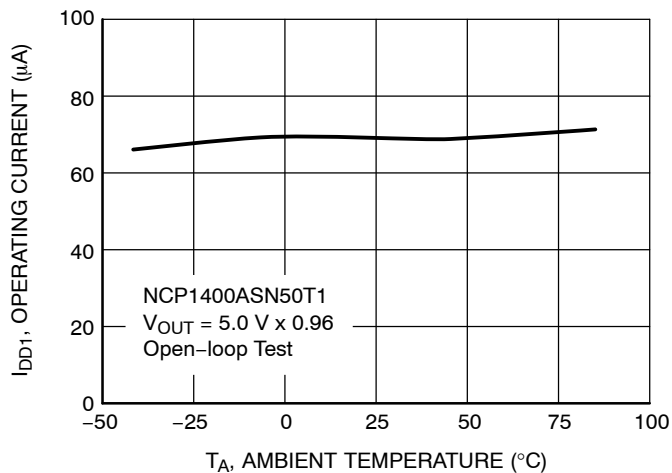


Figure 10. NCP1400ASN50T1 Current Consumption vs. Temperature

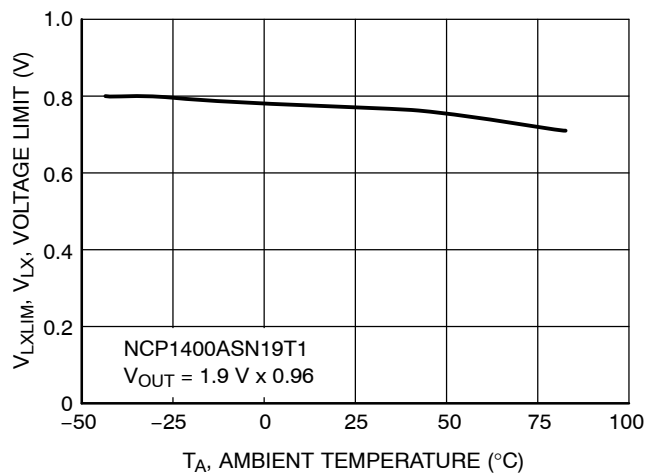


Figure 11. NCP1400ASN19T1 V_{LX} Voltage Limit vs. Temperature

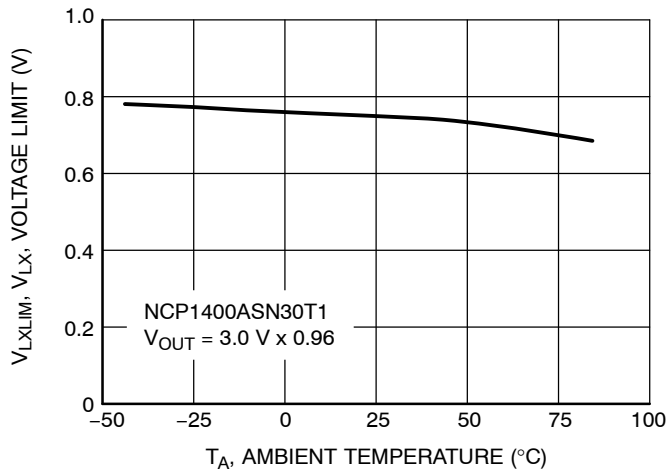


Figure 12. NCP1400ASN30T1 V_{LX} Voltage Limit vs. Temperature

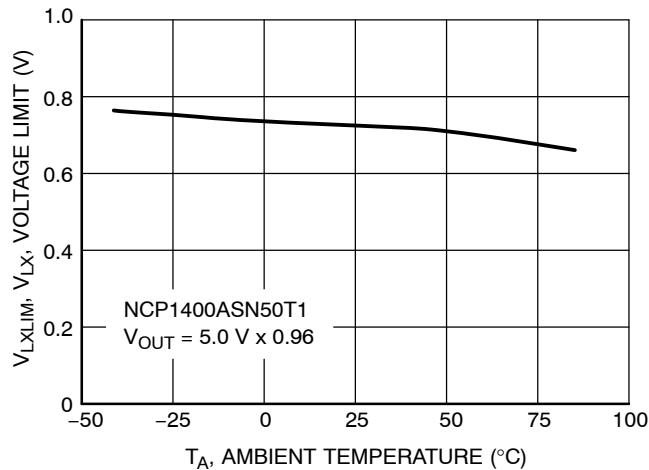


Figure 13. NCP1400ASN50T1 V_{LX} Voltage Limit vs. Temperature

NCP1400A

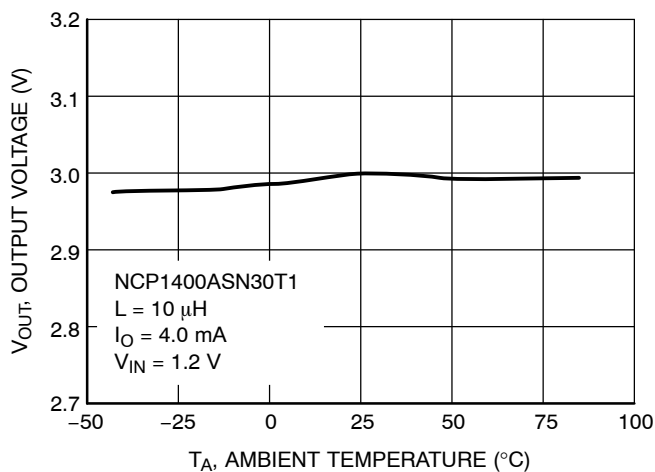


Figure 14. NCP1400ASN30T1 Output Voltage vs. Temperature

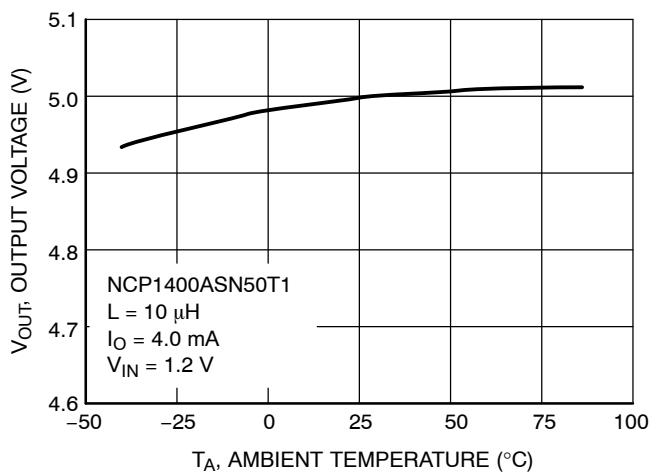


Figure 15. NCP1400ASN50T1 Output Voltage vs. Temperature

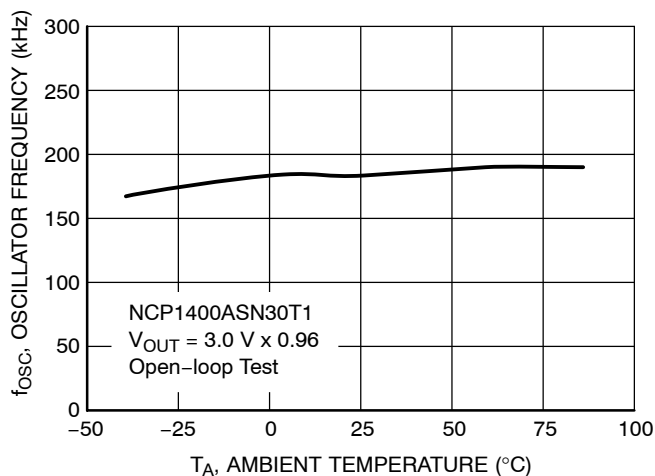


Figure 16. NCP1400ASN30T1 Oscillator Frequency vs. Temperature

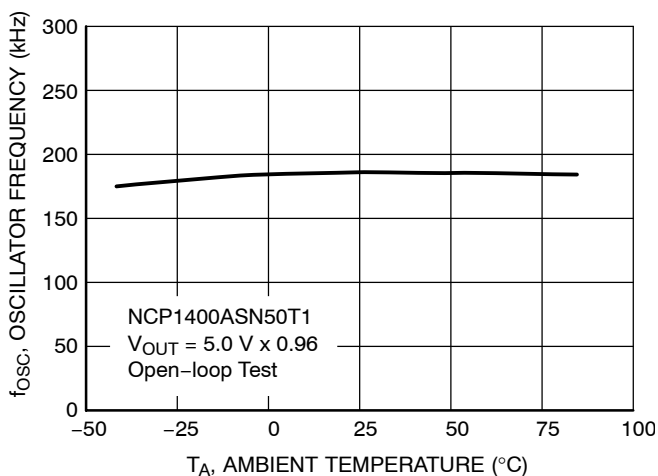


Figure 17. NCP1400ASN50T1 Oscillator Frequency vs. Temperature

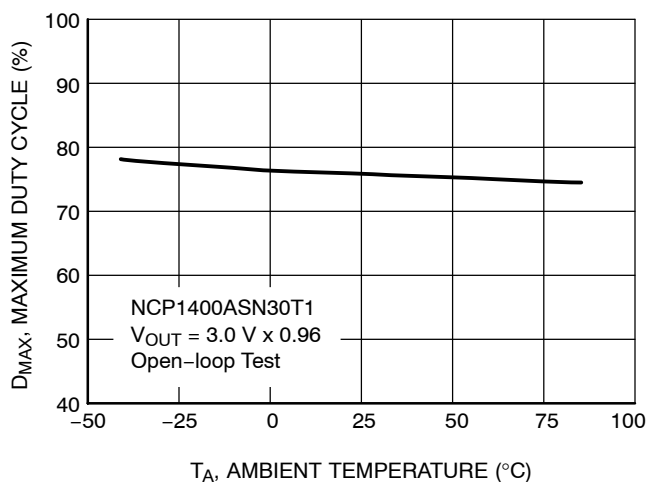


Figure 18. NCP1400ASN30T1 Maximum Duty Cycle vs. Temperature

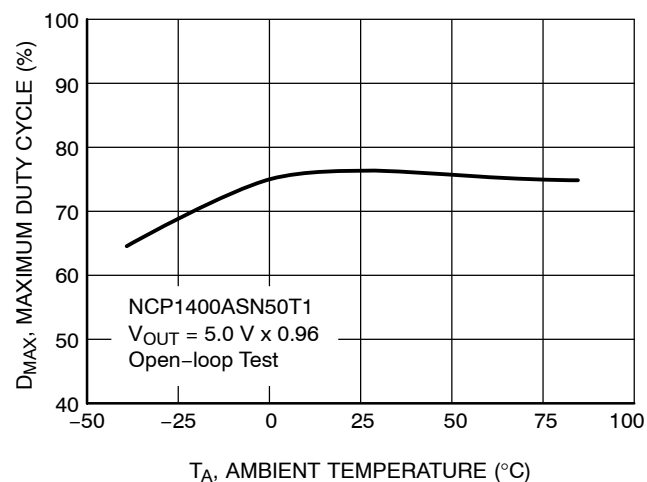


Figure 19. NCP1400ASN50T1 Maximum Duty Cycle vs. Temperature

NCP1400A

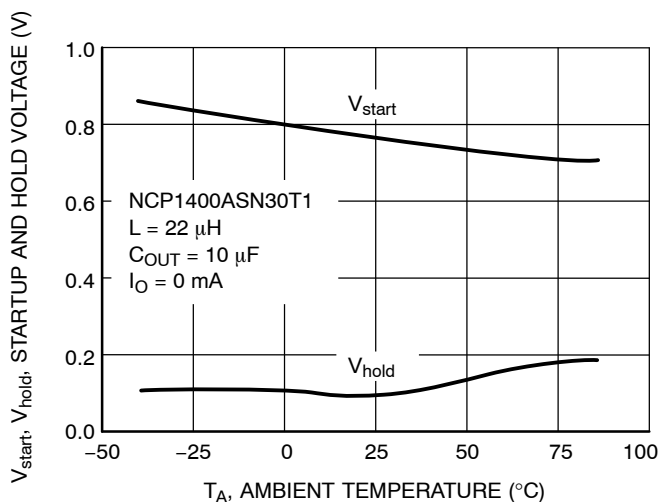


Figure 20. NCP1400ASN30T1 Startup/Hold Voltage vs. Temperature

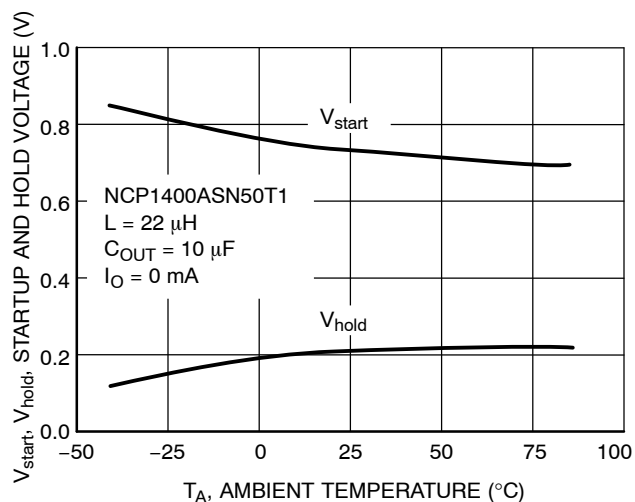


Figure 21. NCP1400ASN50T1 Startup/Hold Voltage vs. Temperature

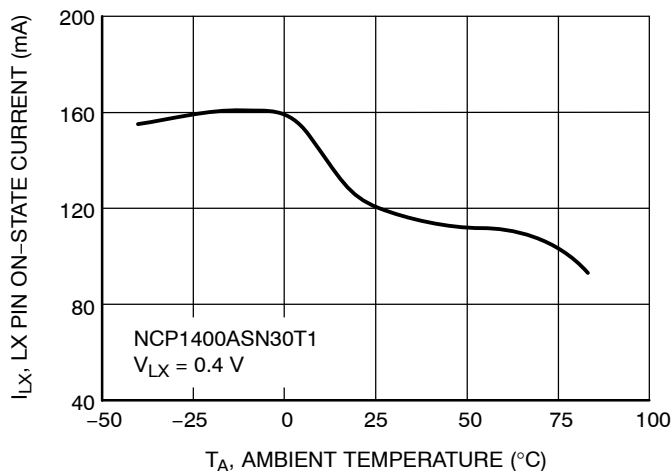


Figure 22. NCP1400ASN30T1 LX Pin On-State Current vs. Temperature

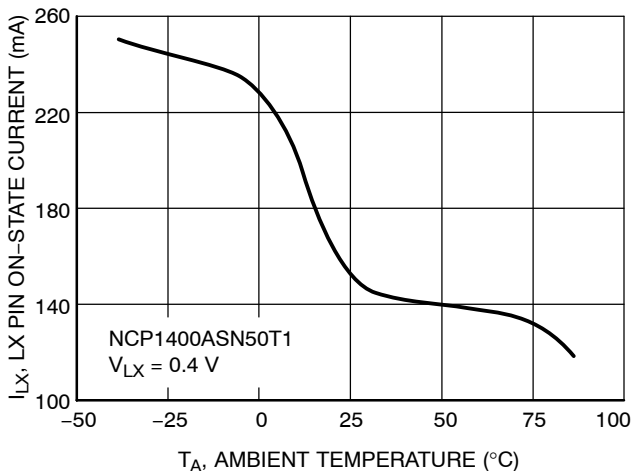


Figure 23. NCP1400ASN50T1 LX Pin On-State Current vs. Temperature

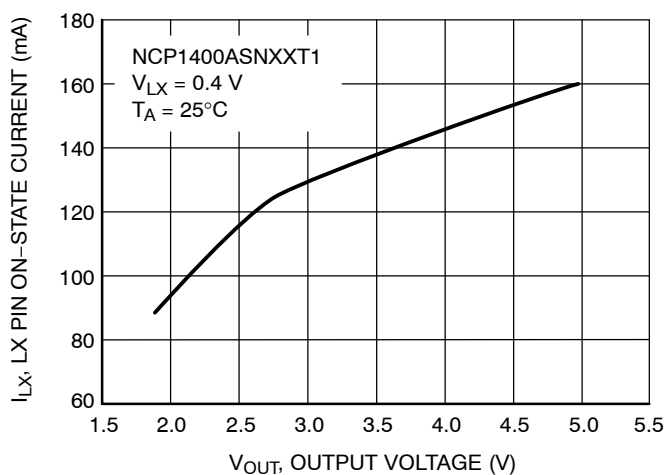


Figure 24. NCP1400ASNXXT1 LX Pin On-State Current vs. Output Voltage

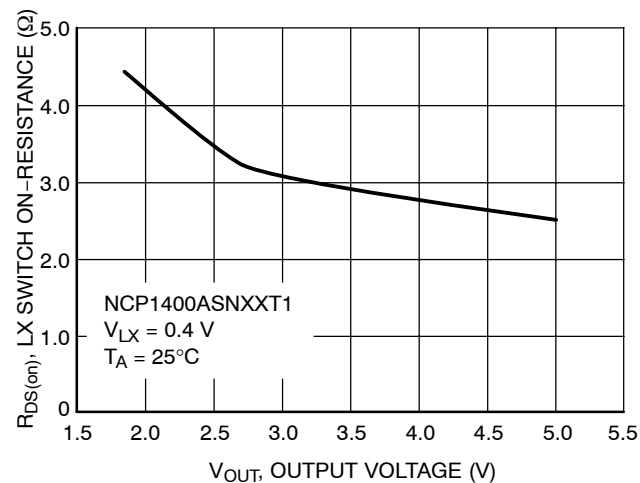


Figure 25. NCP1400ASNXXT1 LX Switch On-Resistance vs. Output Voltage

NCP1400A

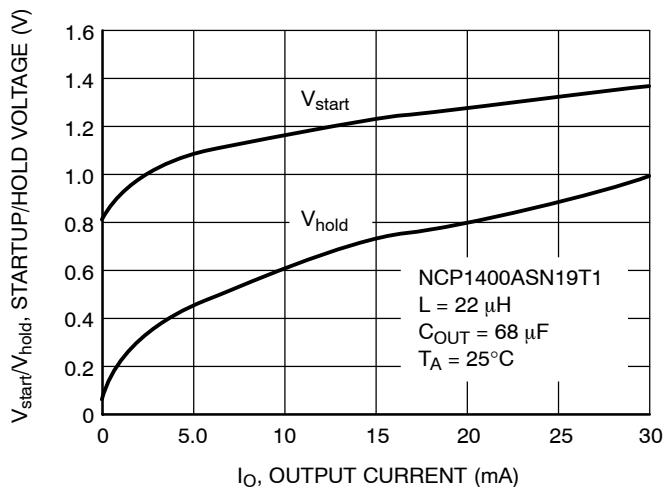


Figure 26. NCP1400ASN19T1 Operation Startup/Hold Voltage vs. Output Current

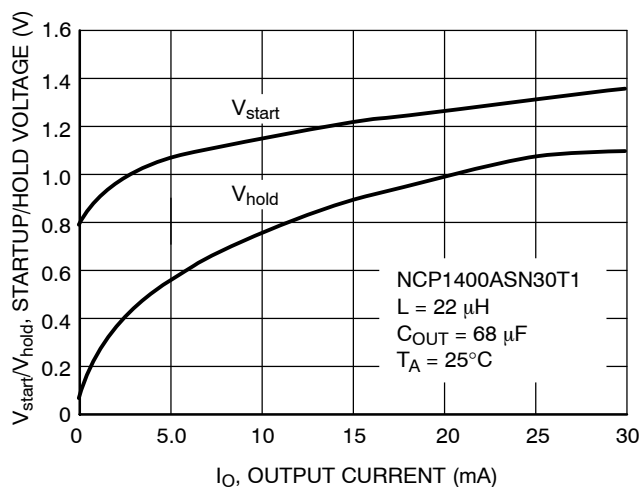


Figure 27. NCP1400ASN30T1 Operation Startup/Hold Voltage vs. Output Current

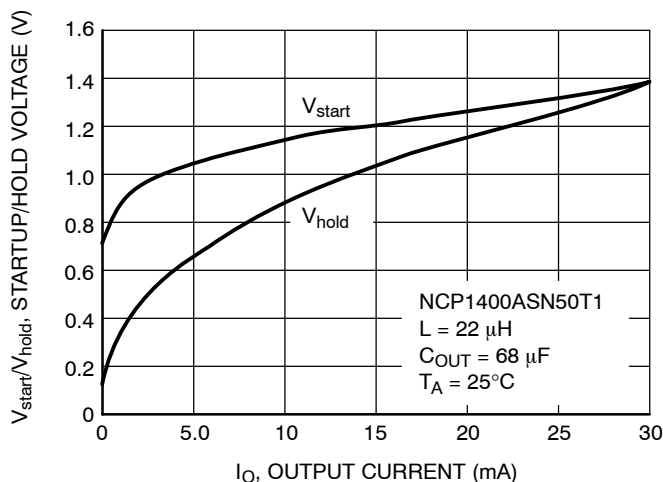


Figure 28. NCP1400ASN50T1 Operation Startup/Hold Voltage vs. Output Current

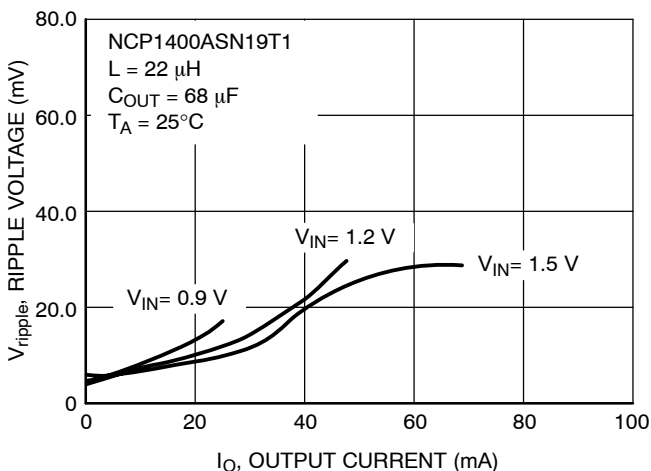


Figure 29. NCP1400ASN19T1 Ripple Voltage vs. Output Current

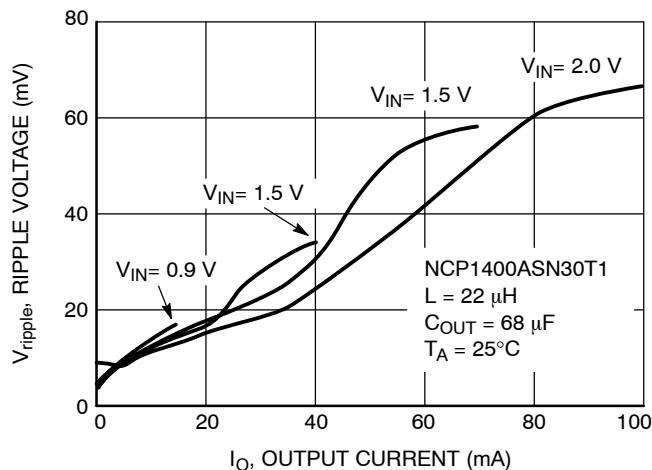


Figure 30. NCP1400ASN30T1 Ripple Voltage vs. Output Current

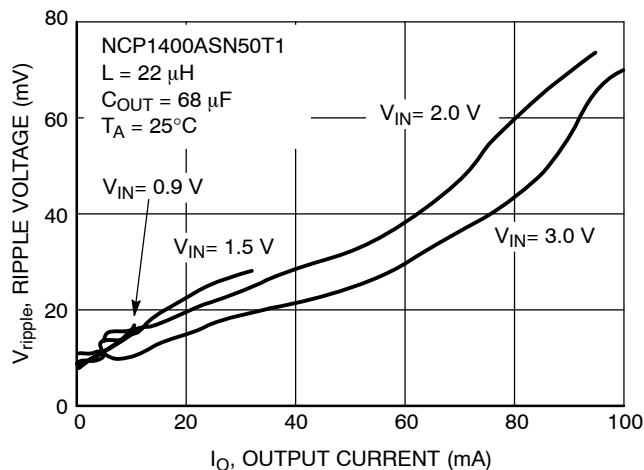
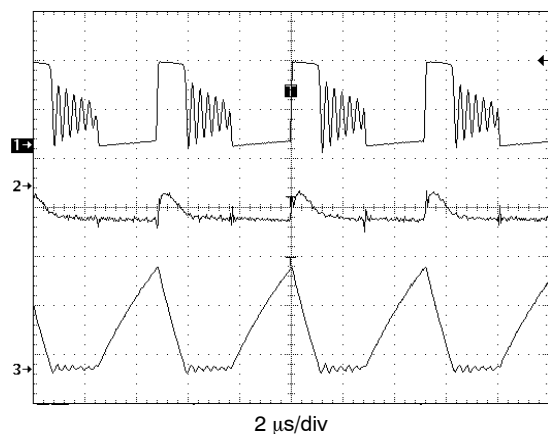


Figure 31. NCP1400ASN50T1 Ripple Voltage vs. Output Current

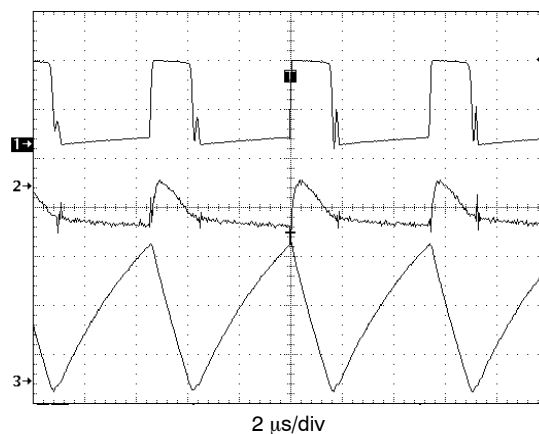
NCP1400A



$V_{OUT} = 3.0\text{ V}$, $V_{IN} = 1.2\text{ V}$, $I_O = 10\text{ mA}$, $L = 22\text{ }\mu\text{H}$, $C_{OUT} = 68\text{ }\mu\text{F}$

1. V_{LX} , 2.0 V/div
2. V_{OUT} , 20 mV/div, AC coupled
3. I_L , 100 mA/div

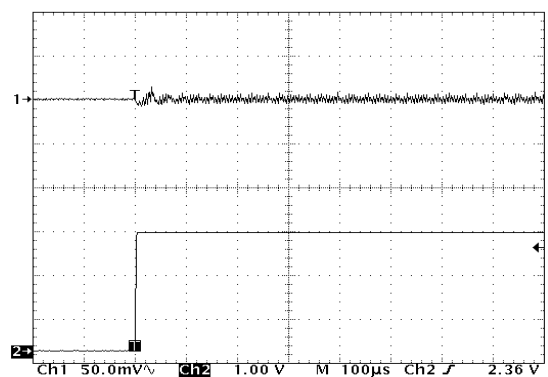
Figure 32. Operating Waveforms (Medium Load)



$V_{OUT} = 3.0\text{ V}$, $V_{IN} = 1.2\text{ V}$, $I_O = 25\text{ mA}$, $L = 22\text{ }\mu\text{H}$, $C_{OUT} = 68\text{ }\mu\text{F}$

1. V_{LX} , 2.0 V/div
2. V_{OUT} , 20 mV/div, AC coupled
3. I_L , 100 mA/div

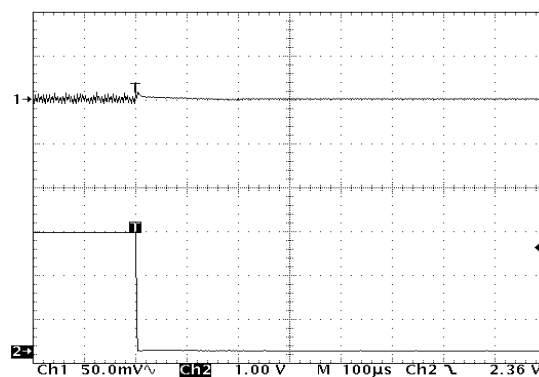
Figure 33. Operating Waveforms (Heavy Load)



$V_{IN} = 1.2\text{ V}$, $L = 22\text{ }\mu\text{H}$

1. $V_{OUT} = 1.9\text{ V}$ (AC coupled), 50 mV/div
2. $I_O = 3.0\text{ mA}$ to 30 mA

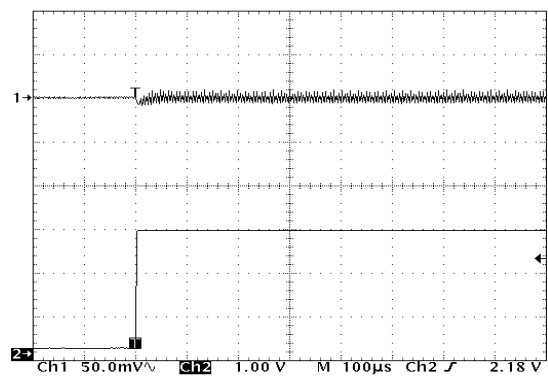
Figure 34. NCP1400ASN19T1 Load Transient Response



$V_{IN} = 1.2\text{ V}$, $L = 22\text{ }\mu\text{H}$

1. $V_{OUT} = 1.9\text{ V}$ (AC coupled), 50 mV/div
2. $I_O = 30\text{ mA}$ to 3.0 mA

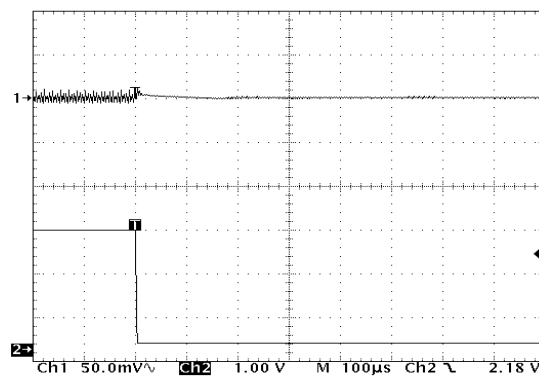
Figure 35. NCP1400ASN19T1 Load Transient Response



$V_{IN} = 1.5\text{ V}$, $L = 22\text{ }\mu\text{H}$

1. $V_{OUT} = 3.0\text{ V}$ (AC coupled), 50 mV/div
2. $I_O = 3.0\text{ mA}$ to 30 mA

Figure 36. NCP1400ASN30T1 Load Transient Response

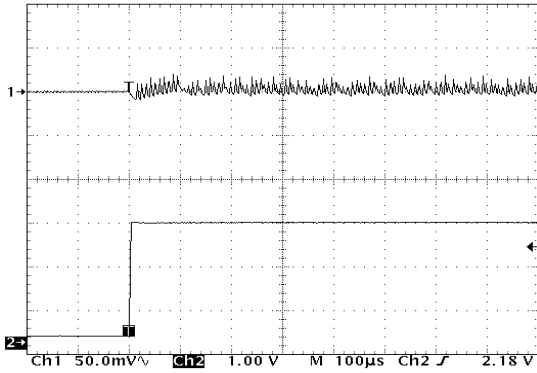


$V_{IN} = 1.5\text{ V}$, $L = 22\text{ }\mu\text{H}$

1. $V_{OUT} = 3.0\text{ V}$ (AC coupled), 50 mV/div
2. $I_O = 30\text{ mA}$ to 3.0 mA

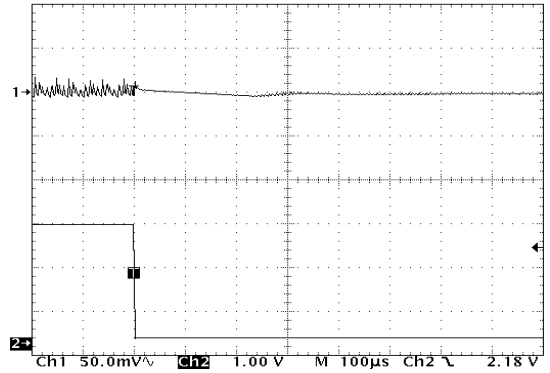
Figure 37. NCP1400ASN30T1 Load Transient Response

NCP1400A



$V_{IN} = 1.5 \text{ V}$, $L = 22 \mu\text{H}$
 1. $V_{OUT} = 5.0 \text{ V}$ (AC coupled), 50 mV/div
 2. $I_O = 3.0 \text{ mA}$ to 30 mA

**Figure 38. NCP1400ASN50T1
Load Transient Response**



$V_{IN} = 1.5 \text{ V}$, $L = 22 \mu\text{H}$
 1. $V_{OUT} = 5.0 \text{ V}$ (AC coupled), 50 mV/div
 2. $I_O = 30 \text{ mA}$ to 3.0 mA

**Figure 39. NCP1400ASN50T1
Load Transient Response**

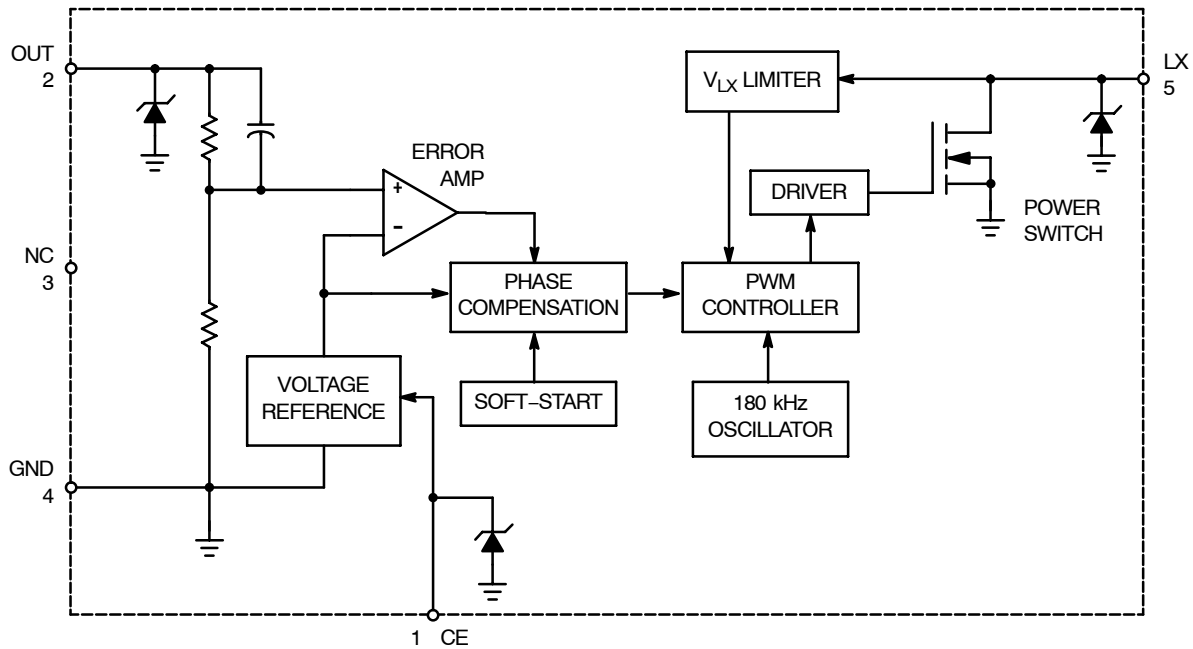


Figure 40. Representative Block Diagram

PIN FUNCTION DESCRIPTION

Pin #	Symbol	Pin Description
1	CE	Chip Enable Pin (1) The chip is enabled if a voltage equal to or greater than 0.9 V is applied. (2) The chip is disabled if a voltage less than 0.3 V is applied. (3) The chip is enabled if this pin is left floating.
2	OUT	Output voltage monitor pin and also the power supply pin for the device.
3	NC	No internal connection to this pin.
4	GND	Ground pin.
5	LX	External inductor connection pin to power switch drain.

DETAILED OPERATING DESCRIPTION

Operation

The NCP1400A series are monolithic power switching regulators optimized for applications where power drain must be minimized. These devices operate as fixed frequency, voltage mode boost regulator and is designed to operate in the discontinuous conduction mode. Potential applications include low powered consumer products and battery powered portable products.

The NCP1400A series are low noise fixed frequency voltage-mode PWM DC-DC converters, and consist of soft-start circuit, feedback resistor, reference voltage, oscillator, loop compensation network, PWM control circuit, current limit circuit and power switch. Due to the on-chip feedback resistor and loop compensation network, the system designer can get the regulated output voltage from 1.8 V to 5.0 V with a small number of external components. The quiescent current is typically 32 μA ($V_{\text{OUT}} = 2.7 \text{ V}$), and can be further reduced to about 1.5 μA when the chip is disabled ($V_{\text{CE}} < 0.3 \text{ V}$).

Soft-Start

There is a soft-start circuit in NCP1400A. When power is applied to the device, the soft-start circuit pumps up the output voltage to approximately 1.5 V at a fixed duty cycle, the level at which the converter can operate normally. What is more, the startup capability with heavy loads is also improved.

Oscillator

The oscillator frequency is internally set to 180 kHz at an accuracy of $\pm 20\%$ and with low temperature coefficient of $0.11\%/^{\circ}\text{C}$. Figures 16 and 17 illustrate oscillator frequency versus temperature.

Regulated Converter Voltage (V_{OUT})

The V_{OUT} is set by an internal feedback resistor network. This is trimmed to a selected voltage from 1.8 V to 5.0 V range in 100 mV steps with an accuracy of $\pm 2.5\%$. Note: When the duty cycle is less than about 12%, the regulator will skip switching cycles to maintain high efficiency at light loads. The regulated output will be raised by 3 to 4% under this condition.

Compensation

The device is designed to operate in discontinuous conduction mode. An internal compensation circuit was designed to guarantee stability over the full input/output voltage and full output load range. Stability cannot be guaranteed in continuous conduction mode.

Current Limit

The NCP1400A series utilizes cycle-by-cycle current limiting as a means of protecting the output switch MOSFET from overstress and preventing the small value inductor from saturation. Current limiting is implemented by monitoring the output MOSFET current build-up during conduction, and upon sensing an overcurrent conduction immediately turning off the switch for the duration of the oscillator cycle.

The voltage across the output MOSFET is monitored and compared against a reference by the VLX limiter. When the threshold is reached, a signal is sent to the PWM controller block to terminate the output switch conduction. The current limit threshold is typically set at 350 mA.

Enable/Disable Operation

The NCP1400A series offer IC shutdown mode by chip enable pin (CE pin) to reduce current consumption. An internal 150 nA pull-up current source tied the CE pin to OUT pin by default, i.e., user can float the pin CE for permanent "On". When voltage at pin CE is equal or greater than 0.9 V, the chip will be enabled, which means the regulator is in normal operation. When voltage at pin CE is less than 0.3 V, the chip is disabled, which means IC is shutdown.

Important: DO NOT apply a voltage between 0.3 V to 0.9 V to pin CE as this voltage will place the IC into an undefined state and the IC may drain excessive current from the supply.

APPLICATION CIRCUIT INFORMATION

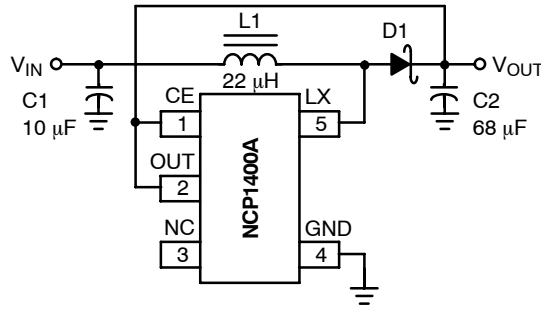


Figure 41. Typical Step-Up Converter Application

Step-up Converter Design Equations

General step-up DC-DC converter designed to operate in discontinuous conduction mode can be defined by:

Calculation	Equation
D	$\frac{t_{on}}{T}$
I_{PK}	$\frac{V_{in} t_{on}}{L}$
I_O	$\frac{(V_{in})^2 (t_{on})^2 f}{2L(V_{out} + V_F - V_{in})}$

- D – Duty cycle
 I_{PK} – Peak inductor current
 I_O – Desired dc output current
 V_{IN} – Nominal operating dc input voltage
 V_{OUT} – Desired dc output voltage
 V_F – Diode forward voltage
 Assume saturation voltage of the internal FET switch is negligible.

External Component Selection

Inductor

Inductance values between 18 µH and 27 µH are the best suitable values for NCP1400A. In general, smaller inductance values can provide larger peak inductor current and output current capability, and lower conversion efficiency, and vice versa. Select an inductor with smallest possible DCR, usually less than 1.0 Ω, to minimize loss. It is necessary to choose an inductor with saturation current greater than the peak current which the inductor will encounter in the application. The inductor selected should be able to handle the worst case peak inductor current without saturation.

Diode

The diode is the largest source of loss in DC-DC converters. The most importance parameters which affect their efficiency are the forward voltage drop, V_F , and the reverse recovery time, t_{rr} . The forward voltage drop creates a loss just by having a voltage across the device while a current flowing through it. The reverse recovery time generates a loss when the diode is reverse biased, and the current appears to actually flow backwards through the diode due to the minority carriers being swept from the P-N junction. A Schottky diode with the following characteristics is recommended:

- Small forward voltage, $V_F < 0.3 \text{ V}$
- Small reverse leakage current
- Fast reverse recovery time/switching speed
- Rated current larger than peak inductor current,
 $I_{rated} > I_{PK}$
- Reverse voltage larger than output voltage,
 $V_{reverse} > V_{OUT}$

Input Capacitor

The input capacitor can stabilize the input voltage and minimize peak current ripple from the source. The value of the capacitor depends on the impedance of the input source used. Small Equivalent Series Resistance (ESR) Tantalum or ceramic capacitor with value of 10 µF should be suitable.

Output Capacitor

The output capacitor is used for sustaining the output voltage when the internal MOSFET is switched on and smoothing the ripple voltage. Low ESR capacitor should be used to reduce output ripple voltage. In general, a 47 µF to 68 µF low ESR (0.15 Ω to 0.30 Ω) Tantalum capacitor should be appropriate.

NCP1400A

An evaluation board of NCP1400A has been made in the small size of 23 mm x 20 mm and is shown in Figures 42 and 43. Please contact your ON Semiconductor

representative for availability. The evaluation board schematic diagram, the artwork and the silkscreen of the surface mount PCB are shown below:

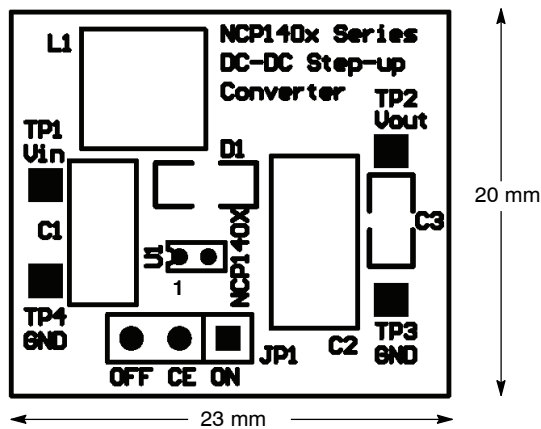


Figure 42. NCP1400A PWM Step-up DC-DC Converter Evaluation Board Silkscreen

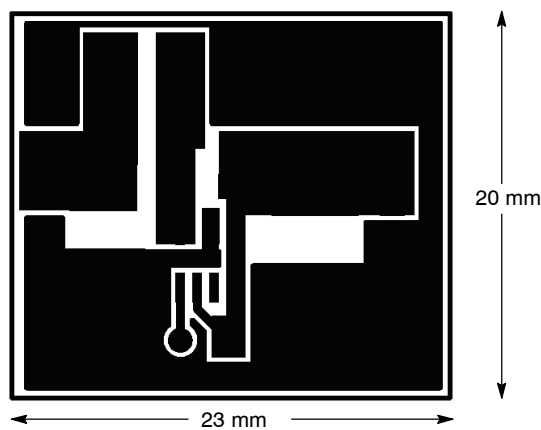


Figure 43. NCP1400A PWM Step-up DC-DC Converter Evaluation Board Artwork (Component Side)

NCP1400A

Components Supplier

Parts	Supplier	Part Number	Description	Phone
Inductor, L1	Sumida Electric Co. Ltd.	CR54-220MC	Inductor 22 μ H/1.11 A	(852) 2880-6688
Schottky Diode, D1	ON Semiconductor Corp.	MBR0520LT1	Schottky Power Rectifier	(852) 2689-0088
Output Capacitor, C2	KEMET Electronics Corp.	T494D686K010AS	Low ESR Tantalum Capacitor 68 μ F/10 V	(852) 2305-1168
Input Capacitor, C1	KEMET Electronics Corp.	T491C106K016AS	Low Profile Tantalum Capacitor 10 μ F/16 V	(852) 2305-1168

PCB Layout Hints

Grounding

One point grounding should be used for the output power return ground, the input power return ground, and the device switch ground to reduce noise as shown in Figure 44, e.g.: C2 GND, C1 GND, and U1 GND are connected at one point in the evaluation board. The input ground and output ground traces must be thick enough for current to flow through and for reducing ground bounce.

Power Signal Traces

Low resistance conducting paths should be used for the power carrying traces to reduce power loss so as to improve

efficiency (short and thick traces for connecting the inductor L can also reduce stray inductance), e.g. short and thick traces listed below are used in the evaluation board:

1. Trace from TP1 to L1
2. Trace from L1 to Lx pin of U1
3. Trace from L1 to anode pin of D1
4. Trace from cathode pin of D1 to TP2

Output Capacitor

The output capacitor should be placed close to the output terminals to obtain better smoothing effect on the output ripple.

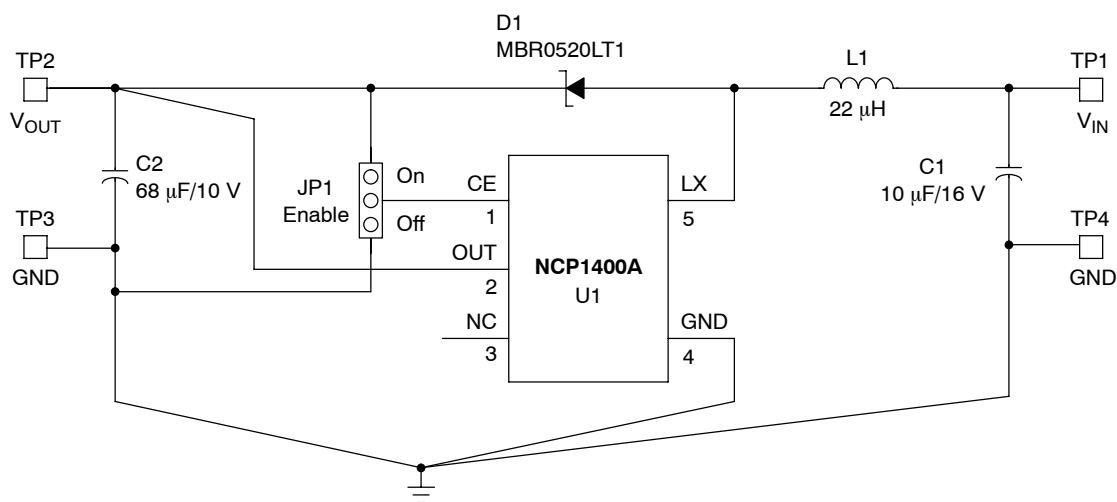


Figure 44. NCP1400A Evaluation Board Schematic Diagram

NCP1402

200 mA, PFM Step-Up Micropower Switching Regulator

The NCP1402 series are monolithic micropower step-up DC to DC converter that are specially designed for powering portable equipment from one or two cell battery packs. These devices are designed to startup with a cell voltage of 0.8 V and operate down to less than 0.3 V. With only three external components, this series allow a simple means to implement highly efficient converters that are capable of up to 200 mA of output current at $V_{in} = 2.0$ V, $V_{OUT} = 3.0$ V.

Each device consists of an on-chip PFM (Pulse Frequency Modulation) oscillator, PFM controller, PFM comparator, soft-start, voltage reference, feedback resistors, driver, and power MOSFET switch with current limit protection. Additionally, a chip enable feature is provided to power down the converter for extended battery life.

The NCP1402 device series are available in the Thin SOT-23-5 package with five standard regulated output voltages. Additional voltages that range from 1.8 V to 5.0 V in 100 mV steps can be manufactured.

Features

- Pb-Free Packages are Available
- Extremely Low Startup Voltage of 0.8 V
- Operation Down to Less than 0.3 V
- High Efficiency 85% ($V_{in} = 2.0$ V, $V_{OUT} = 3.0$ V, 70 mA)
- Low Operating Current of 30 μ A ($V_{OUT} = 1.9$ V)
- Output Voltage Accuracy $\pm 2.5\%$
- Low Converter Ripple with Typical 30 mV
- Only Three External Components Are Required
- Chip Enable Power Down Capability for Extended Battery Life
- Micro Miniature Thin SOT-23-5 Packages

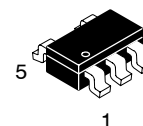
Typical Applications

- Cellular Telephones
- Pagers
- Personal Digital Assistants (PDA)
- Electronic Games
- Portable Audio (MP3)
- Camcorders
- Digital Cameras
- Handheld Instruments



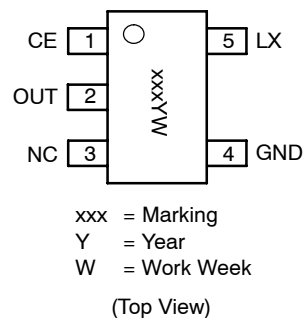
ON Semiconductor®

<http://onsemi.com>



SOT23-5
(TSOP-5, SC59-5)
SN SUFFIX
CASE 483

PIN CONNECTIONS AND MARKING DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 272 of this data sheet.

NCP1402

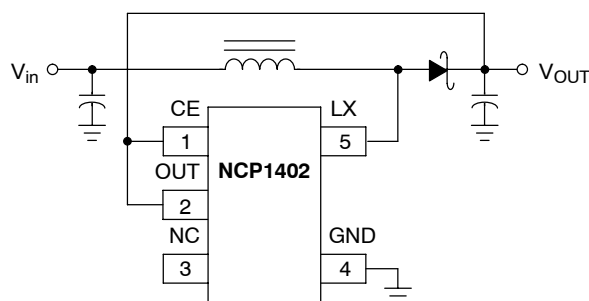


Figure 1. Typical Step-Up Converter Application

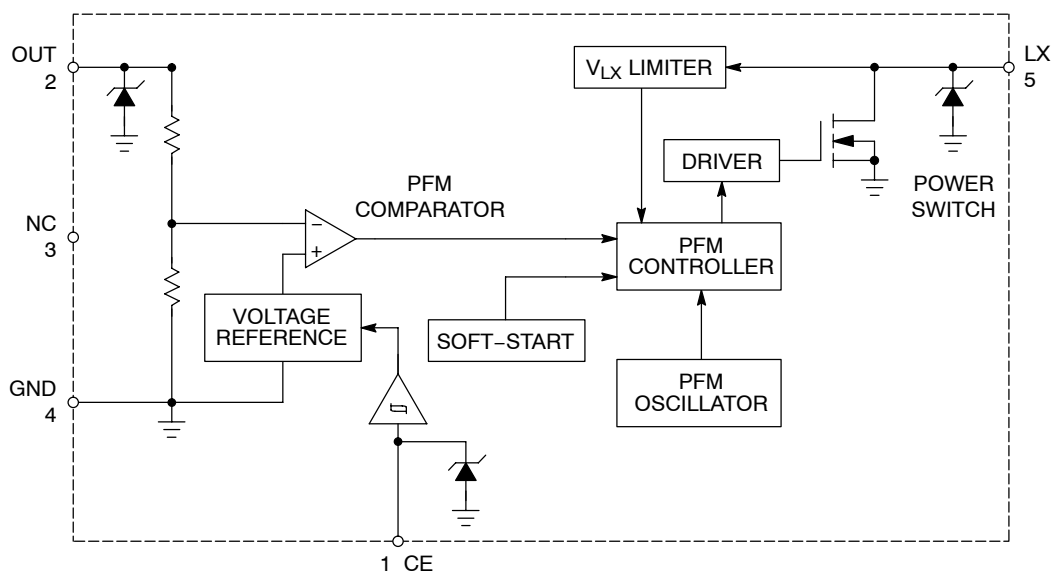


Figure 2. Representative Block Diagram

PIN FUNCTION DESCRIPTIONS

Pin #	Symbol	Pin Description
1	CE	Chip Enable pin (1) The chip is enabled if a voltage which is equal to or greater than 0.9 V is applied (2) The chip is disabled if a voltage which is less than 0.3 V is applied (3) The chip will be enabled if it is left floating
2	OUT	Output voltage monitor pin, also the power supply pin of the device
3	NC	No internal connection to this pin
4	GND	Ground pin
5	LX	External inductor connection pin to power switch drain

NCP1402

ORDERING INFORMATION

Device	Output Voltage	Device Marking	Package	Shipping [†]
NCP1402SN19T1	1.9 V	DAU	SOT23–5	3000 Units Per Reel
NCP1402SN27T1	2.7 V	DAE		
NCP1402SN30T1	3.0 V	DAF		
NCP1402SN33T1	3.3 V	DAG		
NCP1402SN33T1G	3.3 V	DAG	SOT23–5 (Pb–Free)	
NCP1402SN40T1	4.0 V	DCR	SOT23–5	
NCP1402SN50T1	5.0 V	DAH		
NCP1402SN50T1G	5.0 V	DAH	SOT23–5 (Pb–Free)	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: The ordering information lists five standard output voltage device options. Additional device with output voltage ranging from 1.8 V to 5.0 V in 100 mV increments can be manufactured. Contact your ON Semiconductor representative for availability.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 2)	V _{OUT}	6.0	V
Input/Output Pins LX (Pin 5) LX Peak Sink Current	V _{LX} I _{LX}	-0.3 to 6.0 400	V mA
CE (Pin 1) Input Voltage Range Input Current Range	V _{CE} I _{CE}	-0.3 to 6.0 -150 to 150	V mA
Thermal Resistance, Junction-to-Air	R _{θJA}	250	°C/W
Operating Ambient Temperature Range (Note 2)	T _A	-40 to +85	°C
Operating Junction Temperature Range	T _J	-40 to +125	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

NOTES:

- This device series contains ESD protection and exceeds the following tests:
Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22-A114.
Machine Model (MM) ±200 V per JEDEC standard: JESD22-A115.
- The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

- Latchup Current Maximum Rating: ±150 mA per JEDEC standard: JESD78.
- Moisture Sensitivity Level: MSL 1 per IPC/JEDEC standard: J-STD-020A.

NCP1402

ELECTRICAL CHARACTERISTICS (For all values $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Switch On Time (current limit not asserted)	t_{on}	3.6	5.5	7.6	μs
Switch Minimum Off Time	t_{off}	1.0	1.45	1.9	μs
Maximum Duty Cycle	D_{MAX}	70	78	85	%
Minimum Startup Voltage ($I_O = 0\text{ mA}$)	V_{start}	–	0.8	0.95	V
Minimum Startup Voltage Temperature Coefficient ($T_A = -40^\circ\text{C}$ to 85°C)	ΔV_{start}	–	–1.6	–	$\text{mV}/^\circ\text{C}$
Minimum Operation Hold Voltage ($I_O = 0\text{ mA}$)	V_{hold}	0.3	–	–	V
Soft-Start Time ($V_{OUT} > 0.8\text{ V}$)	t_{SS}	0.3	2.0	–	ms

LX (PIN 5)

Internal Switching N-Channel FET Drain Voltage	V_{LX}	–	–	6.0	V
LX Pin On-State Sink Current ($V_{LX} = 0.4\text{ V}$) Device Suffix:	I_{LX}				mA
19T1		110	145	–	
27T1		130	180	–	
30T1		130	190	–	
33T1		130	200	–	
40T1		130	210	–	
50T1		130	215	–	
Voltage Limit	V_{LXLIM}	0.45	0.65	0.9	V
Off-State Leakage Current ($V_{LX} = 6.0\text{ V}$, $T_A = -40^\circ\text{C}$ to 85°C)	I_{LKG}	–	0.5	1.0	μA

CE (PIN 1)

CE Input Voltage ($V_{OUT} = V_{SET} \times 0.96$) High State, Device Enabled Low State, Device Disabled	$V_{CE(high)}$ $V_{CE(low)}$	0.9 –	– –	– 0.3	V
CE Input Current (Note 6) High State, Device Enabled ($V_{OUT} = V_{CE} = 6.0\text{ V}$) Low State, Device Disabled ($V_{OUT} = 6.0\text{ V}$, $V_{CE} = 0\text{ V}$)	$I_{CE(high)}$ $I_{CE(low)}$	–0.5 –0.5	0 0.15	0.5 0.5	μA

TOTAL DEVICE

Output Voltage Device Suffix:	V_{OUT}				V
19T1		1.853	1.9	1.948	
27T1		2.632	2.7	2.768	
30T1		2.925	3.0	3.075	
33T1		3.218	3.3	3.383	
40T1		3.900	4.0	4.100	
50T1		4.875	5.0	5.125	
Output Voltage Temperature Coefficient ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) Device Suffix:	ΔV_{OUT}				$\text{ppm}/^\circ\text{C}$
19T1		–	150	–	
27T1		–	150	–	
30T1		–	150	–	
33T1		–	150	–	
40T1		–	150	–	
50T1		–	150	–	
Operating Current 2 ($V_{OUT} = V_{CE} = V_{SET} + 0.5\text{ V}$, Note 5)	I_{DD2}	–	13	15	μA
Off-State Current ($V_{OUT} = 5.0\text{ V}$, $V_{CE} = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, Note 6)	I_{OFF}	–	0.6	1.0	μA
Operating Current 1 ($V_{OUT} = V_{CE} = V_{SET} \times 0.96$) Device Suffix:	I_{DD1}				μA
19T1		–	30	50	
27T1		–	39	60	
30T1		–	42	60	
33T1		–	45	60	
40T1		–	55	100	
50T1		–	70	100	

5. V_{SET} means setting of output voltage.

6. CE pin is integrated with an internal $10\text{ M}\Omega$ pullup resistor.

NCP1402

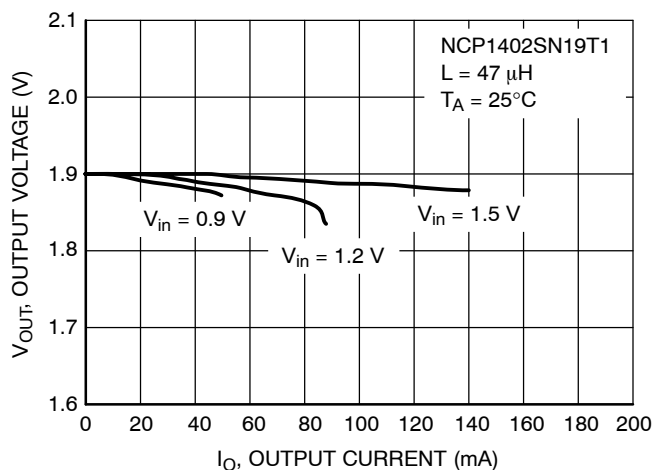


Figure 3. NCP1402SN19T1 Output Voltage vs. Output Current

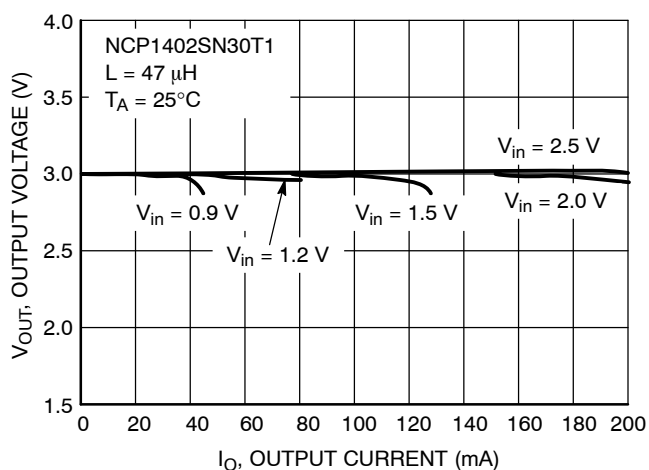


Figure 4. NCP1402SN30T1 Output Voltage vs. Output Current

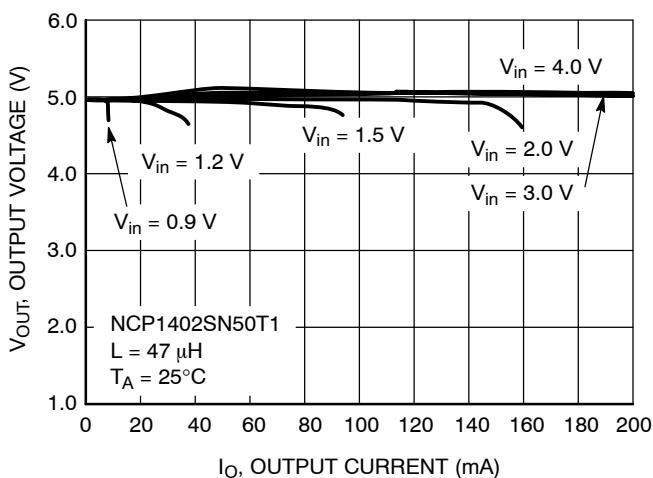


Figure 5. NCP1402SN50T1 Output Voltage vs. Output Current

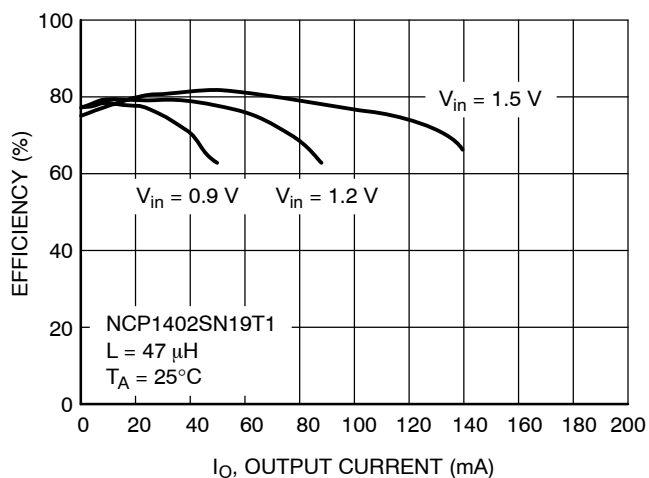


Figure 6. NCP1402SN19T1 Efficiency vs. Output Current

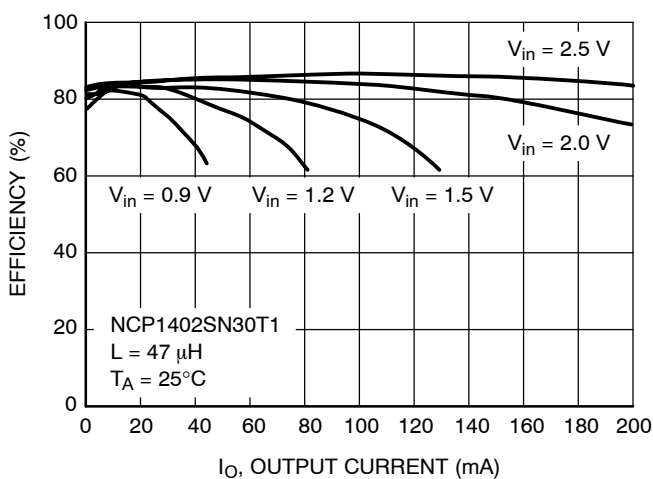


Figure 7. NCP1402SN30T1 Efficiency vs. Output Current

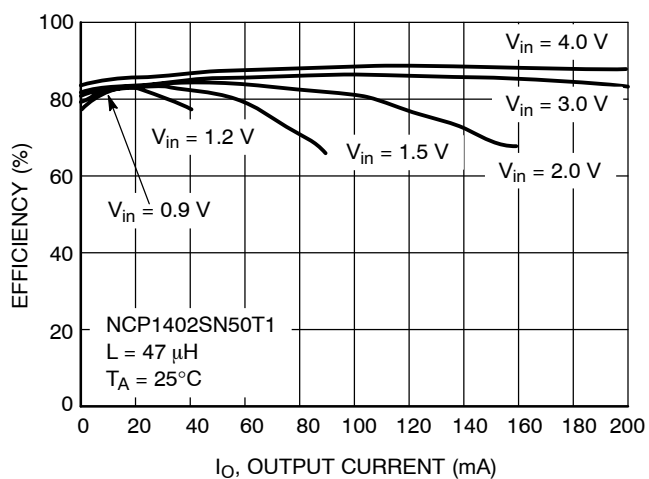


Figure 8. NCP1402SN50T1 Efficiency vs. Output Current

NCP1402

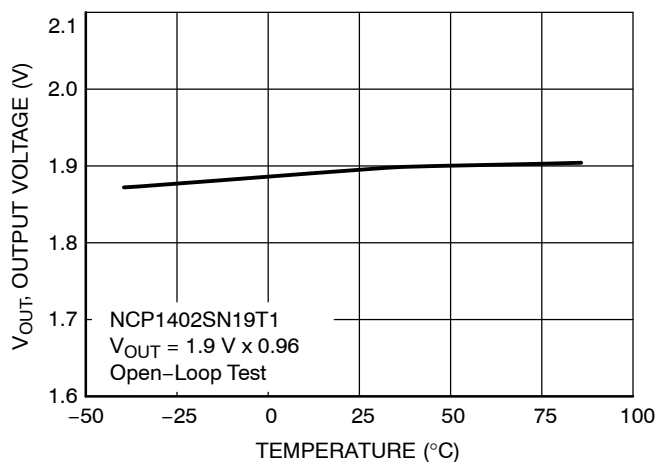


Figure 9. NCP1402SN19T1 Output Voltage vs. Temperature

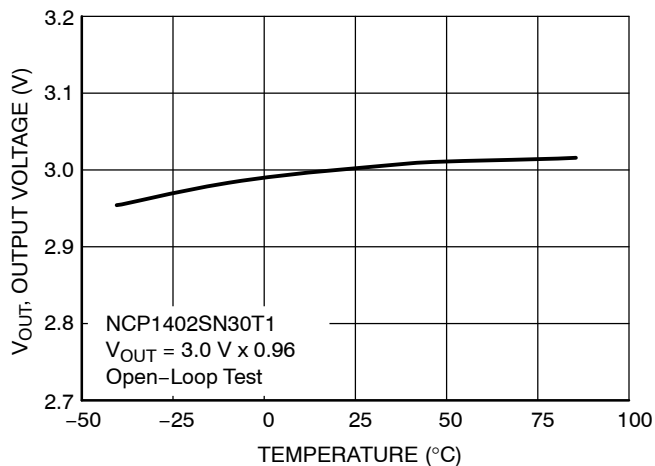


Figure 10. NCP1402SN30T1 Output Voltage vs. Temperature

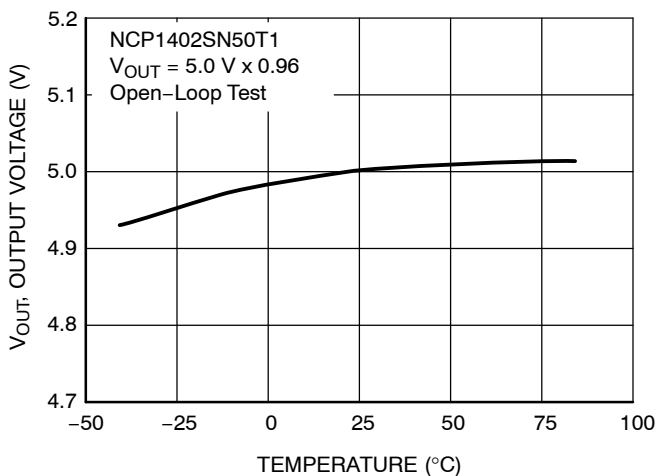


Figure 11. NCP1402SN50T1 Output Voltage vs. Temperature

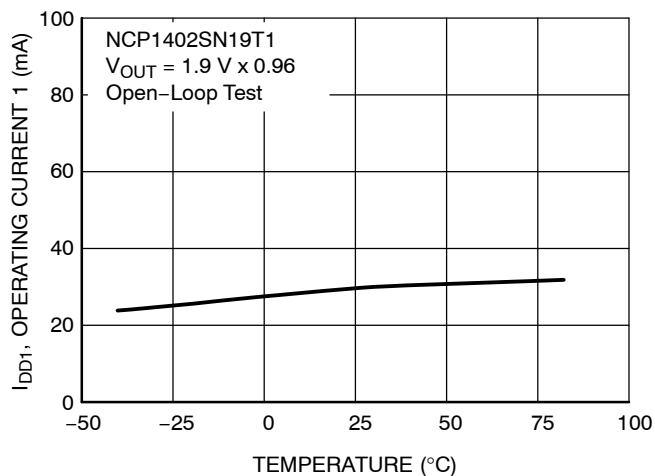


Figure 12. NCP1402SN19T1 Operating Current 1 vs. Temperature

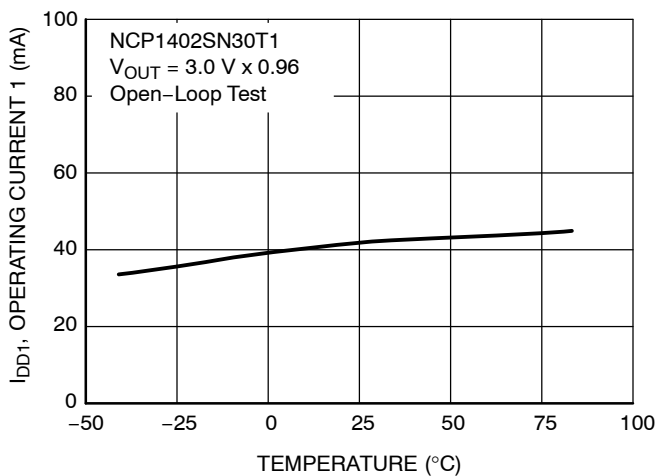


Figure 13. NCP1402SN30T1 Operating Current 1 vs. Temperature

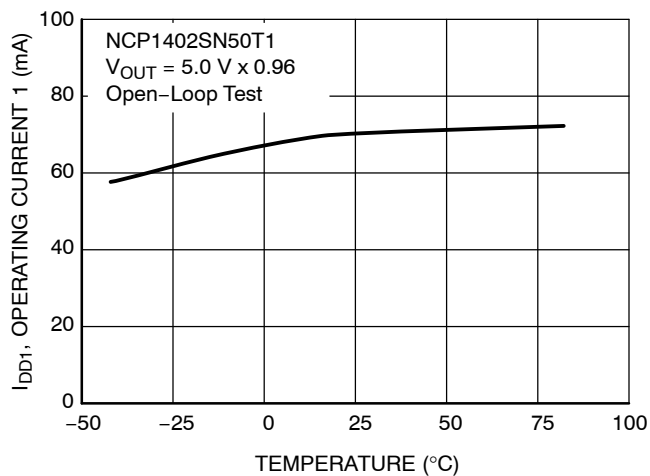


Figure 14. NCP1402SN50T1 Operating Current 1 vs. Temperature

NCP1402

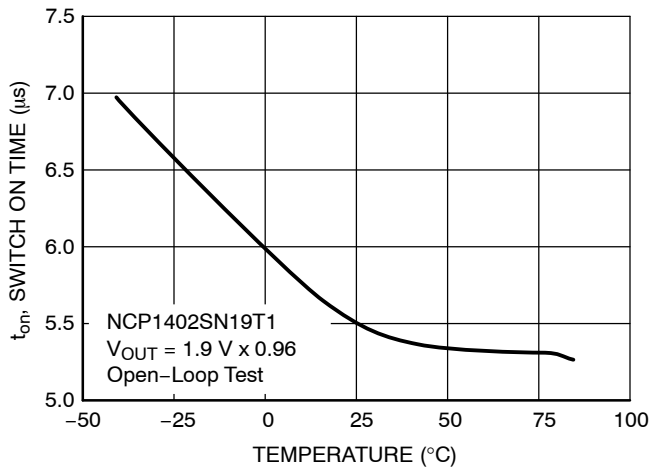


Figure 15. NCP1402SN19T1 Switch On Time vs. Temperature

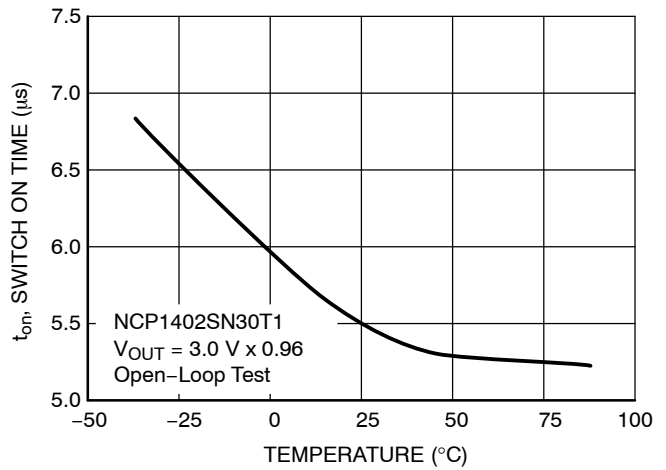


Figure 16. NCP1402SN30T1 Switch On Time vs. Temperature

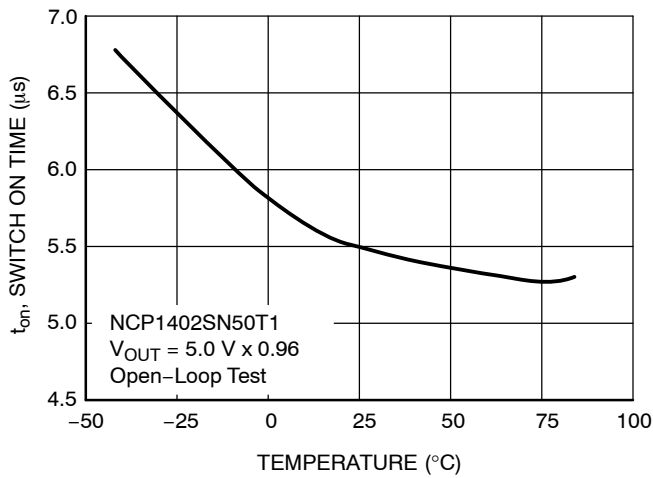


Figure 17. NCP1402SN50T1 Switch On Time vs. Temperature

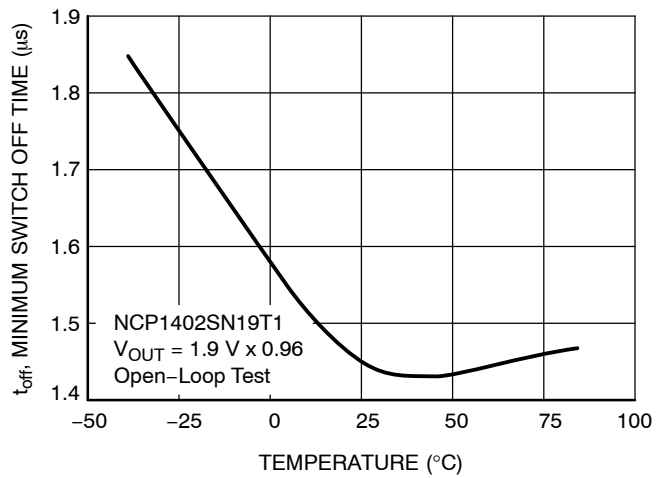


Figure 18. NCP1402SN19T1 Minimum Switch Off Time vs. Temperature

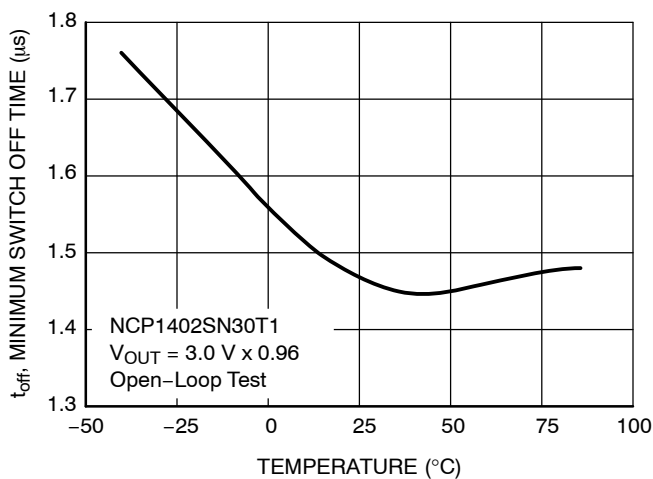


Figure 19. NCP1402SN30T1 Minimum Switch Off Time vs. Temperature

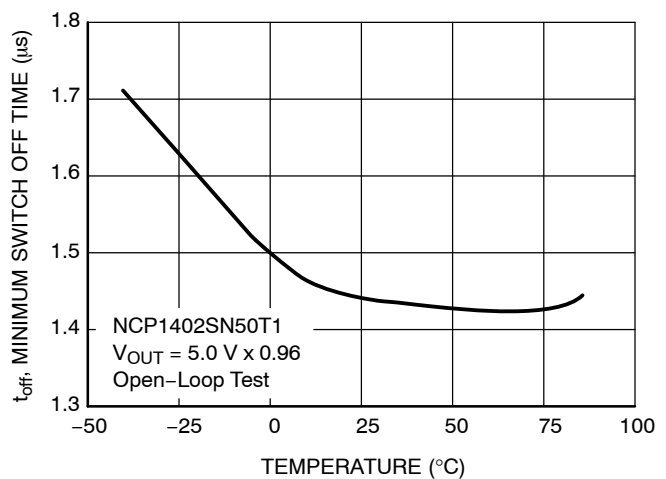


Figure 20. NCP1402SN50T1 Minimum Switch Off Time vs. Temperature

NCP1402

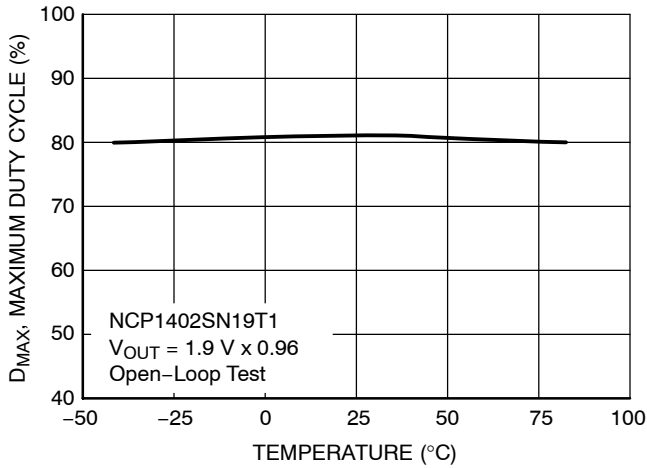


Figure 21. NCP1402SN19T1 Maximum Duty Cycle vs. Temperature

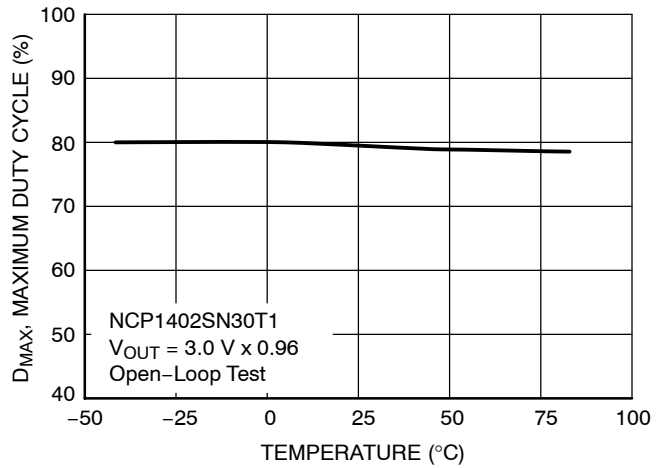


Figure 22. NCP1402SN30T1 Maximum Duty Cycle vs. Temperature

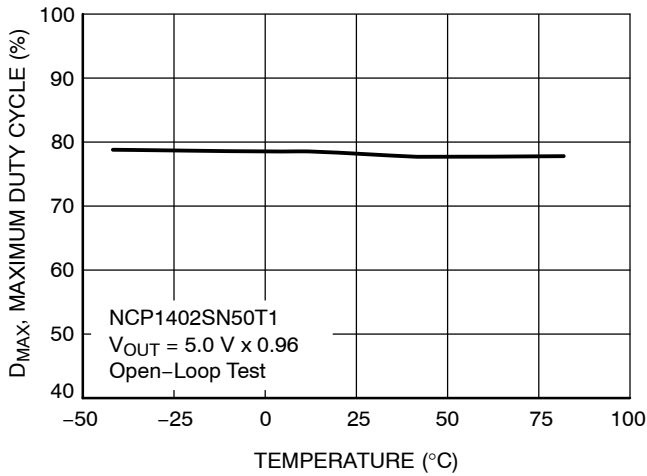


Figure 23. NCP1402SN50T1 Maximum Duty Cycle vs. Temperature

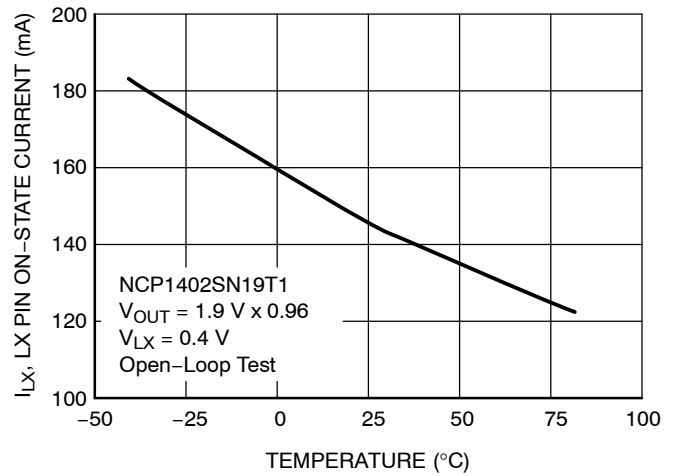


Figure 24. NCP1402SN19T1 LX Pin On-State Current vs. Temperature

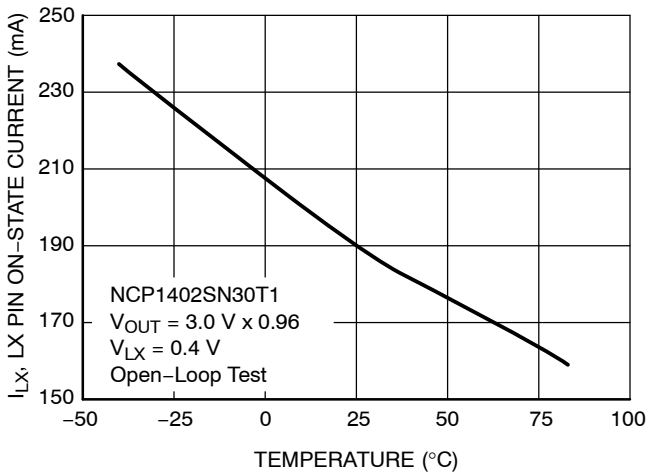


Figure 25. NCP1402SN30T1 LX Pin On-State Current vs. Temperature

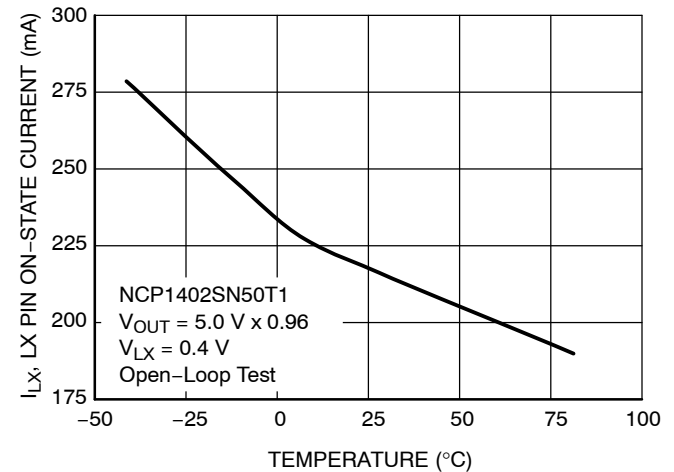


Figure 26. NCP1402SN50T1 LX Pin On-State Current vs. Temperature

NCP1402

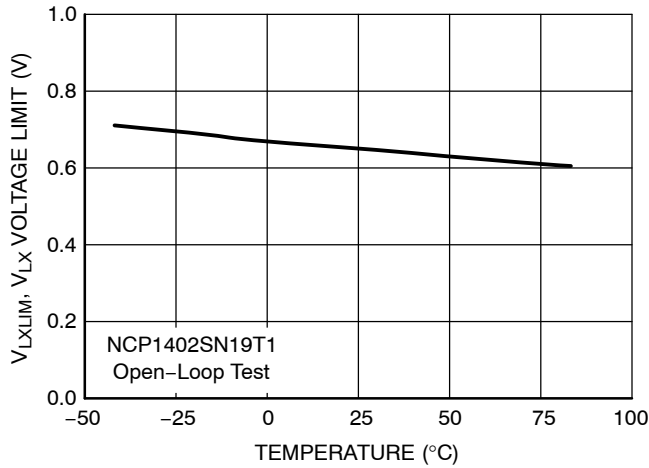


Figure 27. NCP1402SN19T1 V_{LX} Voltage Limit vs. Temperature

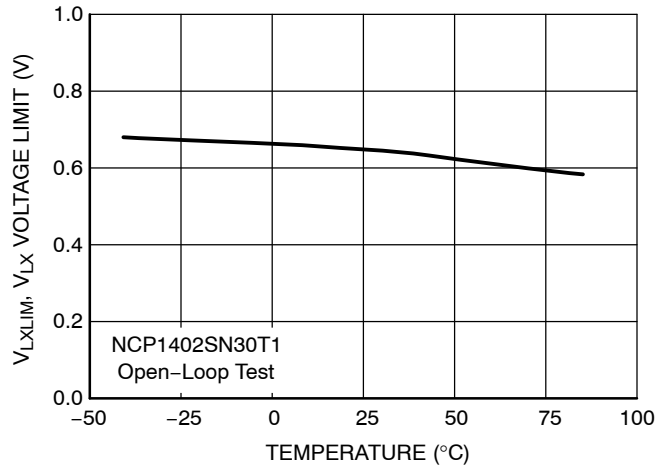


Figure 28. NCP1402SN30T1 V_{LX} Voltage Limit vs. Temperature

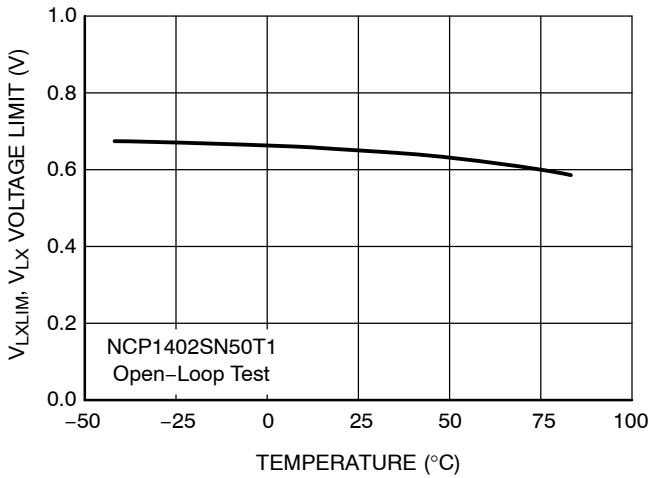


Figure 29. NCP1402SN50T1 V_{LX} Voltage Limit vs. Temperature

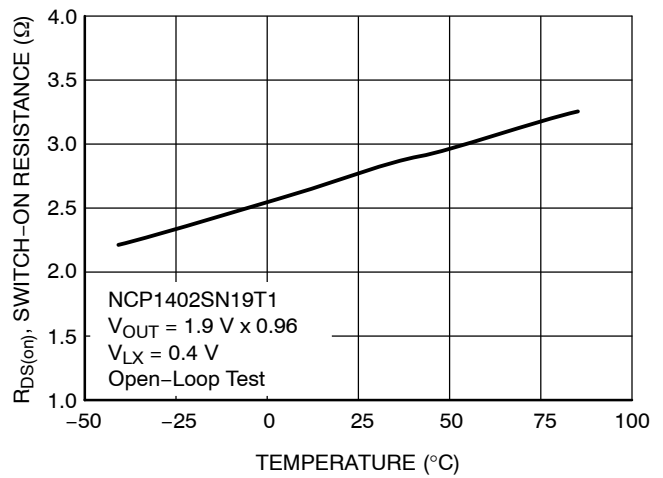


Figure 30. NCP1402SN19T1 Switch-on Resistance vs. Temperature

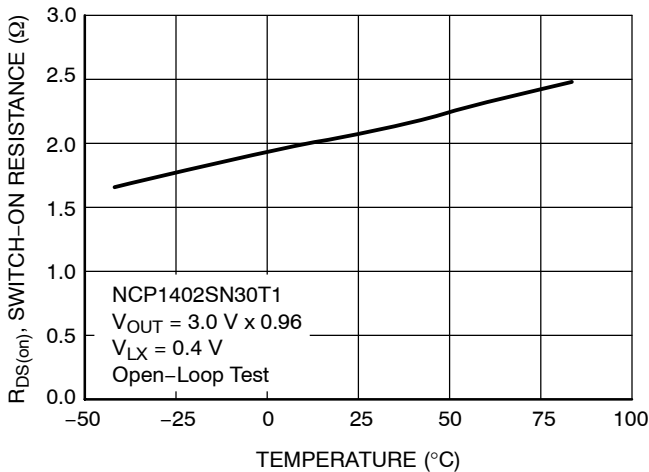


Figure 31. NCP1402SN30T1 Switch-on Resistance vs. Temperature

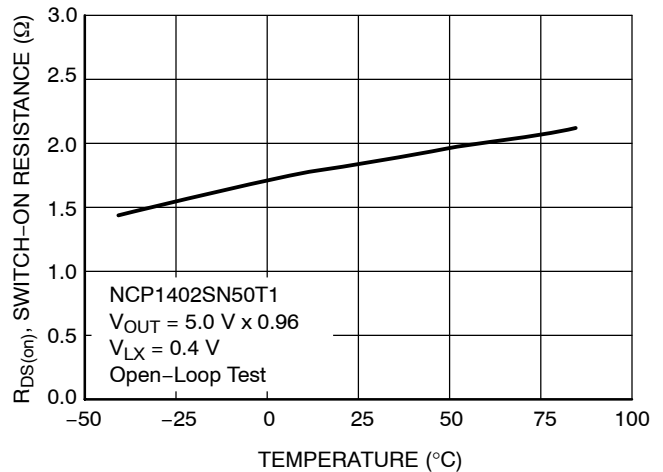


Figure 32. NCP1402SN50T1 Switch-on Resistance vs. Temperature

NCP1402

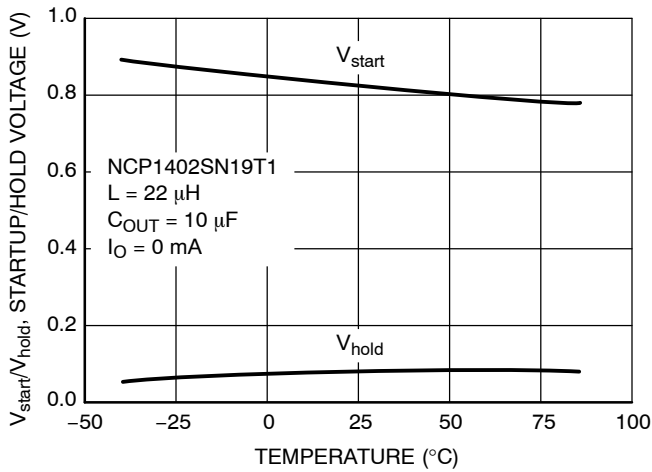


Figure 33. NCP1402SN19T1 Startup/Hold Voltage vs. Temperature

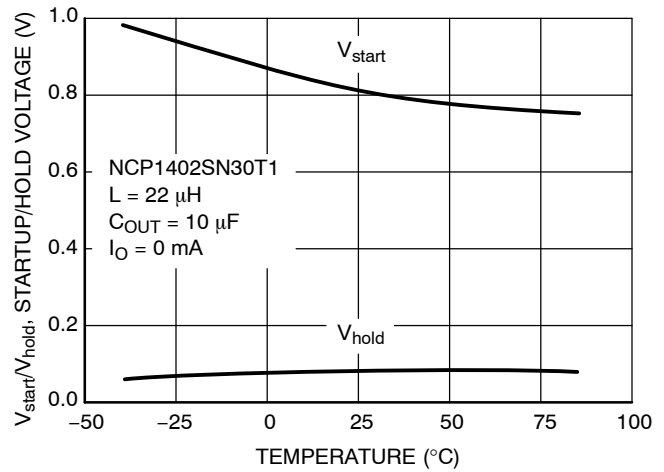


Figure 34. NCP1402SN30T1 Startup/Hold Voltage vs. Temperature

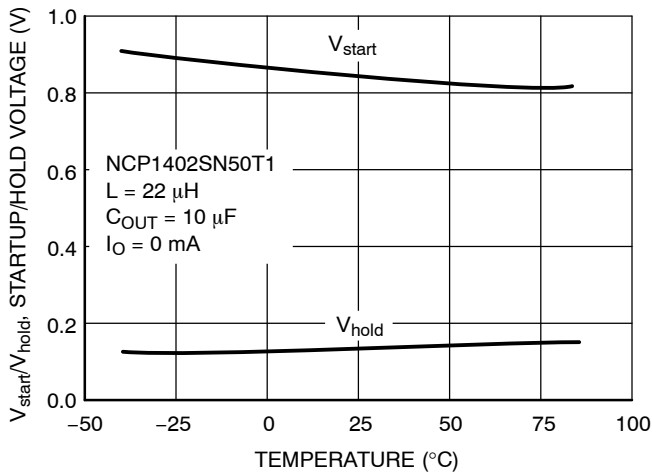


Figure 35. NCP1402SN50T1 Startup/Hold Voltage vs. Temperature

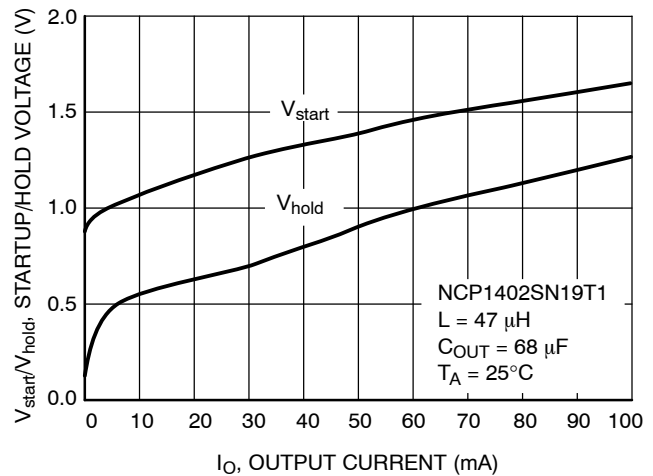


Figure 36. NCP1402SN19T1 Startup/Hold Voltage vs. Output Current

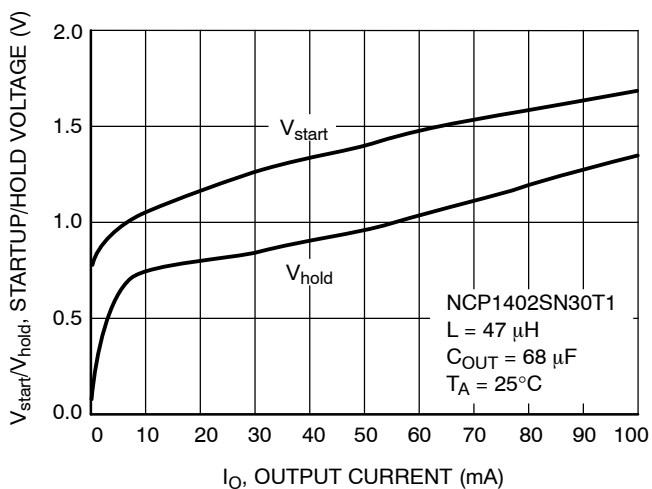


Figure 37. NCP1402SN30T1 Startup/Hold Voltage vs. Output Current

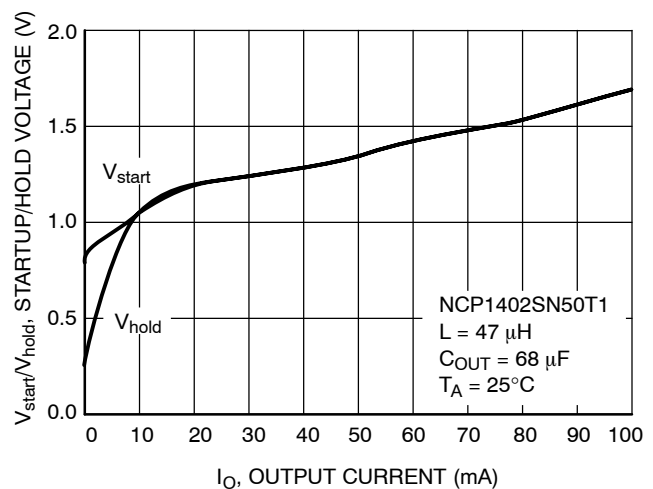
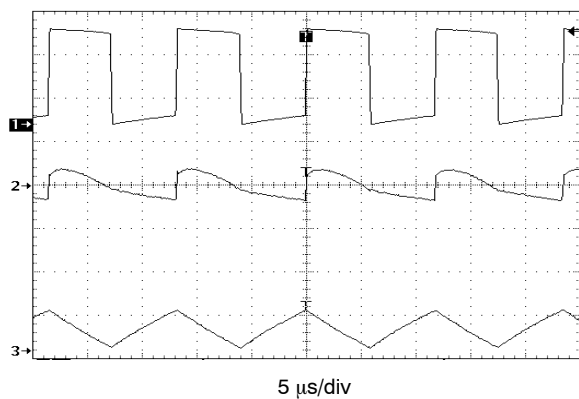


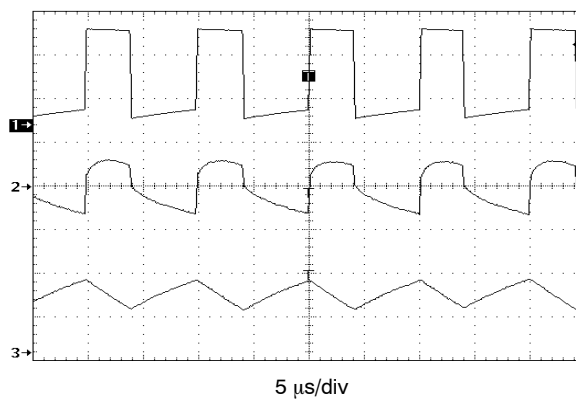
Figure 38. NCP1402SN50T1 Startup/Hold Voltage vs. Output Current

NCP1402



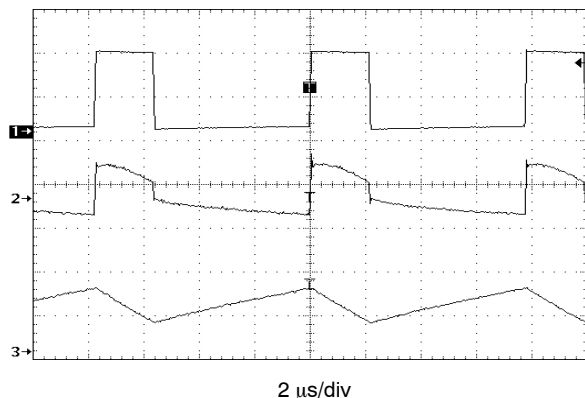
$V_{OUT} = 1.9 \text{ V}$, $V_{IN} = 1.2 \text{ V}$, $I_O = 30 \text{ mA}$, $L = 47 \mu\text{H}$, $C_{OUT} = 68 \mu\text{F}$
 1. V_{LX} , 1.0 V/div
 2. V_{OUT} , 20 mV/div, AC coupled
 3. I_L , 100 mA/div

Figure 39. NCP1402SN19T1 Operating Waveforms (Medium Load)



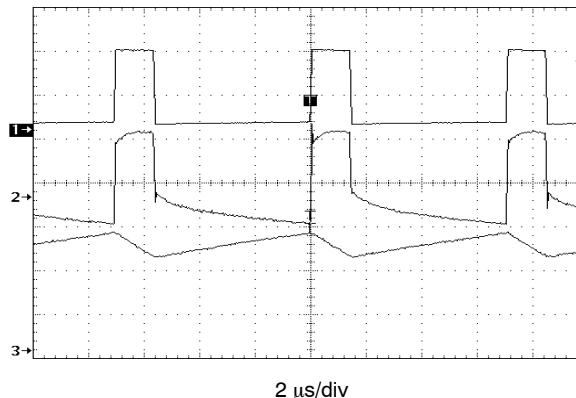
$V_{OUT} = 1.9 \text{ V}$, $V_{IN} = 1.2 \text{ V}$, $I_O = 70 \text{ mA}$, $L = 47 \mu\text{H}$, $C_{OUT} = 68 \mu\text{F}$
 1. V_{LX} , 1.0 V/div
 2. V_{OUT} , 20 mV/div, AC coupled
 3. I_L , 100 mA/div

Figure 40. NCP1402SN19T1 Operating Waveforms (Heavy Load)



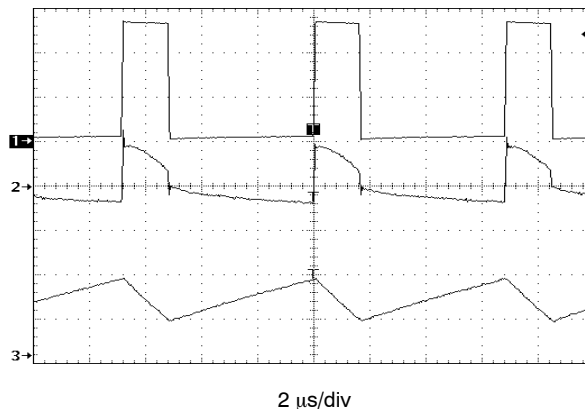
$V_{OUT} = 3.0 \text{ V}$, $V_{IN} = 1.2 \text{ V}$, $I_O = 30 \text{ mA}$, $L = 47 \mu\text{H}$, $C_{OUT} = 68 \mu\text{F}$
 1. V_{LX} , 2.0 V/div
 2. V_{OUT} , 20 mV/div, AC coupled
 3. I_L , 100 mA/div

Figure 41. NCP1402SN30T1 Operating Waveforms (Medium Load)



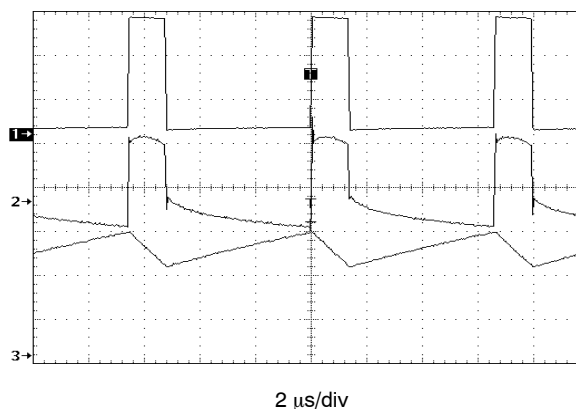
$V_{OUT} = 3.0 \text{ V}$, $V_{IN} = 1.2 \text{ V}$, $I_O = 70 \text{ mA}$, $L = 47 \mu\text{H}$, $C_{OUT} = 68 \mu\text{F}$
 1. V_{LX} , 2.0 V/div
 2. V_{OUT} , 20 mV/div, AC coupled
 3. I_L , 100 mA/div

Figure 42. NCP1402SN30T1 Operating Waveforms (Heavy Load)



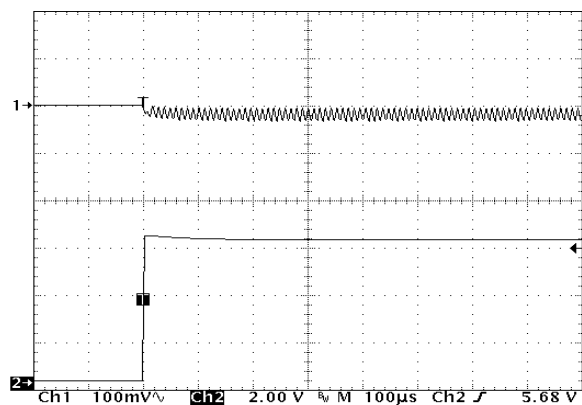
$V_{OUT} = 5.0 \text{ V}$, $V_{IN} = 1.5 \text{ V}$, $I_O = 30 \text{ mA}$, $L = 47 \mu\text{H}$, $C_{OUT} = 68 \mu\text{F}$
 1. V_{LX} , 2.0 V/div
 2. V_{OUT} , 20 mV/div, AC coupled
 3. I_L , 100 mA/div

Figure 43. NCP1402SN50T1 Operating Waveforms (Medium Load)



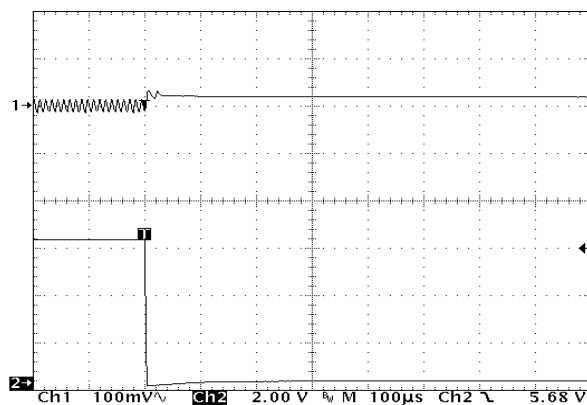
$V_{OUT} = 5.0 \text{ V}$, $V_{IN} = 1.5 \text{ V}$, $I_O = 60 \text{ mA}$, $L = 47 \mu\text{H}$, $C_{OUT} = 68 \mu\text{F}$
 1. V_{LX} , 2.0 V/div
 2. V_{OUT} , 20 mV/div, AC coupled
 3. I_L , 100 mA/div

Figure 44. NCP1402SN50T1 Operating Waveforms (Heavy Load)



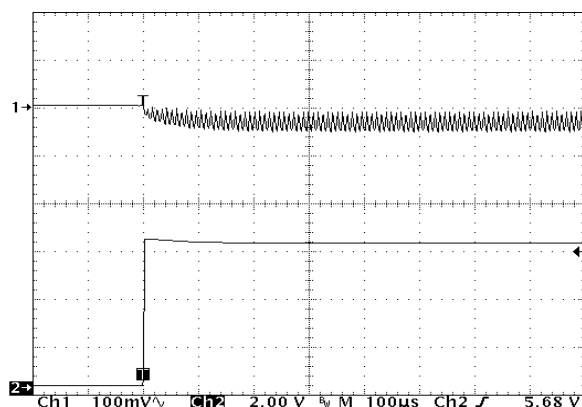
$V_{in} = 1.2 \text{ V}$, $L = 47 \mu\text{H}$, $C_{OUT} = 68 \mu\text{F}$
 1. $V_{OUT} = 1.9 \text{ V}$ (AC coupled), 100 mV/div
 2. $I_O = 0.1 \text{ mA}$ to 80 mA

Figure 45. NCP1402SN19T1 Load Transient Response



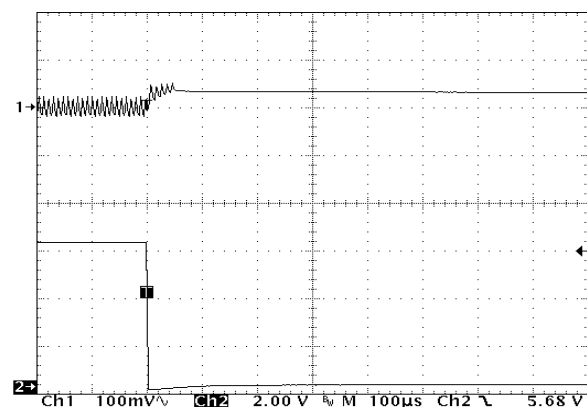
$V_{in} = 1.2 \text{ V}$, $L = 47 \mu\text{H}$, $C_{OUT} = 68 \mu\text{F}$
 1. $V_{OUT} = 1.9 \text{ V}$ (AC coupled), 100 mV/div
 2. $I_O = 80 \text{ mA}$ to 0.1 mA

Figure 46. NCP1402SN19T1 Load Transient Response



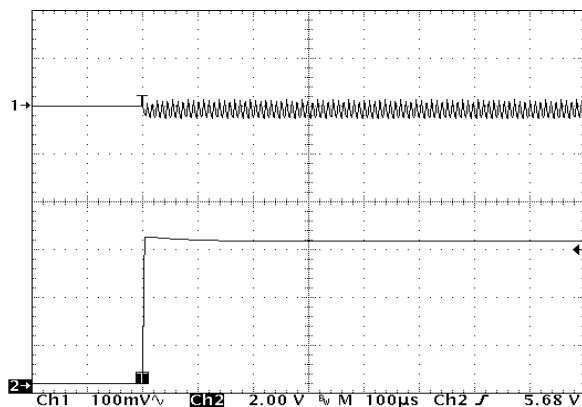
$V_{in} = 1.5 \text{ V}$, $L = 47 \mu\text{H}$, $C_{OUT} = 68 \mu\text{F}$
 1. $V_{OUT} = 3.0 \text{ V}$ (AC coupled), 100 mV/div
 2. $I_O = 0.1 \text{ mA}$ to 80 mA

Figure 47. NCP1402SN30T1 Load Transient Response



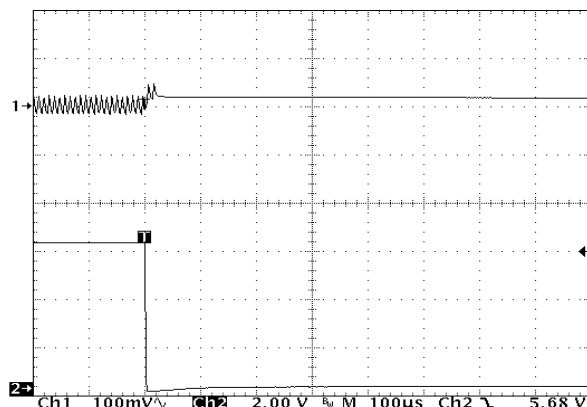
$V_{in} = 1.5 \text{ V}$, $L = 47 \mu\text{H}$, $C_{OUT} = 68 \mu\text{F}$
 1. $V_{OUT} = 3.0 \text{ V}$ (AC coupled), 100 mV/div
 2. $I_O = 80 \text{ mA}$ to 0.1 mA

Figure 48. NCP1402SN30T1 Load Transient Response



$V_{in} = 2.4 \text{ V}$, $L = 47 \mu\text{H}$, $C_{OUT} = 68 \mu\text{F}$
 1. $V_{OUT} = 5.0 \text{ V}$ (AC coupled), 100 mV/div
 2. $I_O = 0.1 \text{ mA}$ to 80 mA

Figure 49. NCP1402SN50T1 Load Transient Response



$V_{in} = 2.4 \text{ V}$, $L = 47 \mu\text{H}$, $C_{OUT} = 68 \mu\text{F}$
 1. $V_{OUT} = 5.0 \text{ V}$ (AC coupled), 100 mV/div
 2. $I_O = 80 \text{ mA}$ to 0.1 mA

Figure 50. NCP1402SN50T1 Load Transient Response

NCP1402

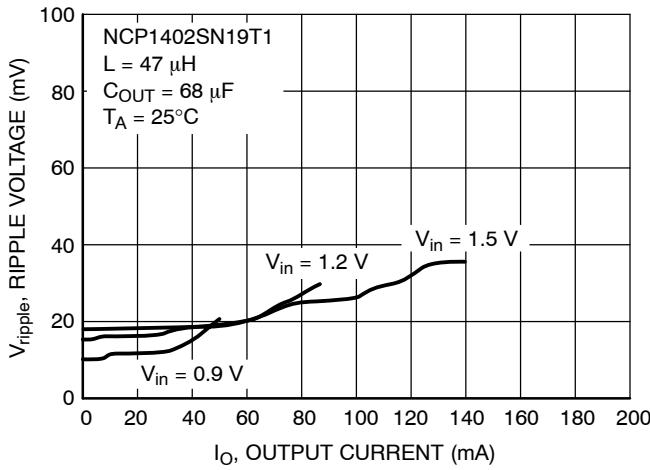


Figure 51. NCP1402SN19T1 Ripple Voltage vs. Output Current

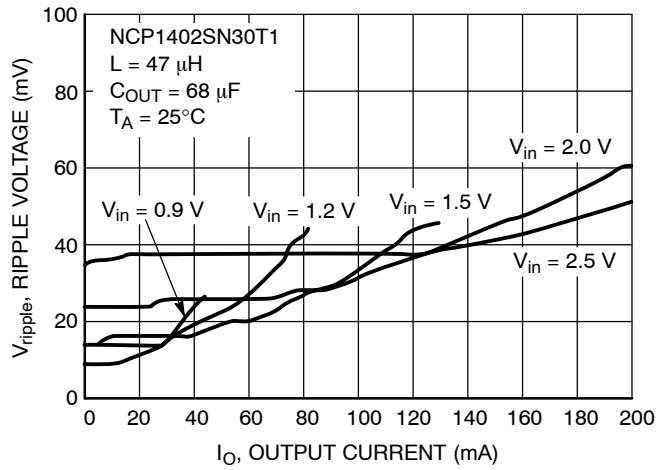


Figure 52. NCP1402SN30T1 Ripple Voltage vs. Output Current

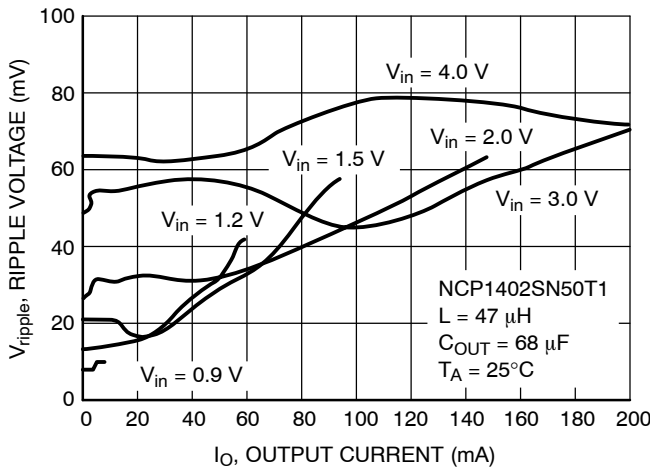


Figure 53. NCP1402SN50T1 Ripple Voltage vs. Output Current

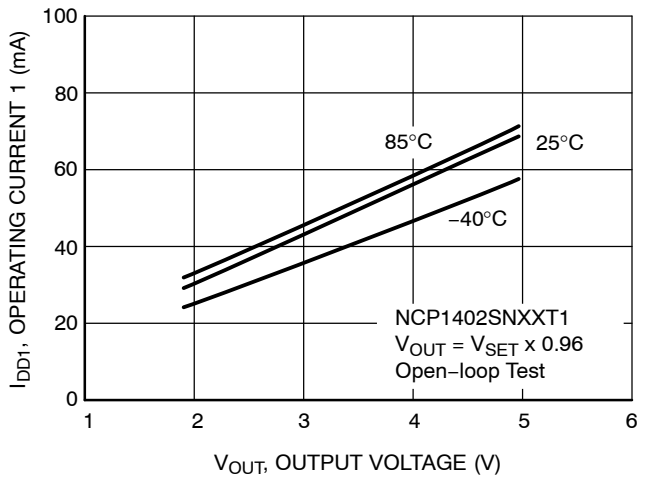


Figure 54. NCP1402SNXXT1 Operating Current I vs. Output Voltage

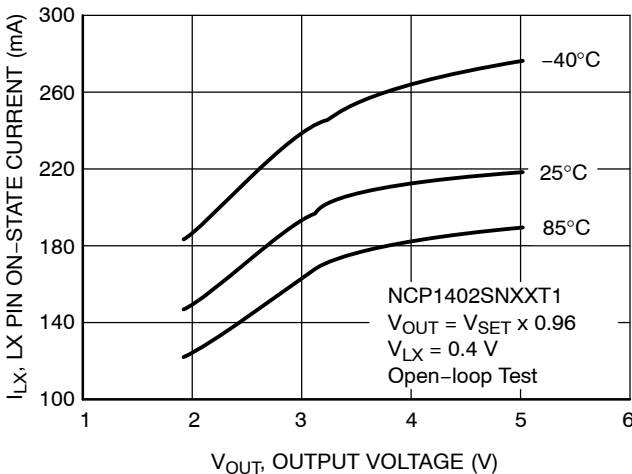


Figure 55. NCP1402SNXXT1 Pin On-state Current vs. Output Voltage

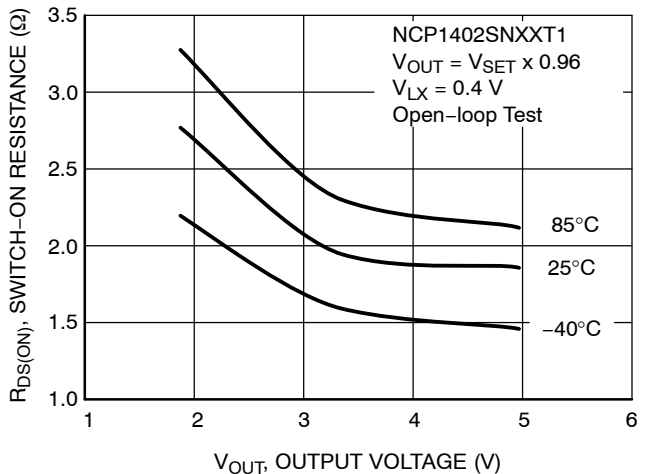


Figure 56. NCP1402SNXXT1 Switch-On Resistance vs. Output Voltage

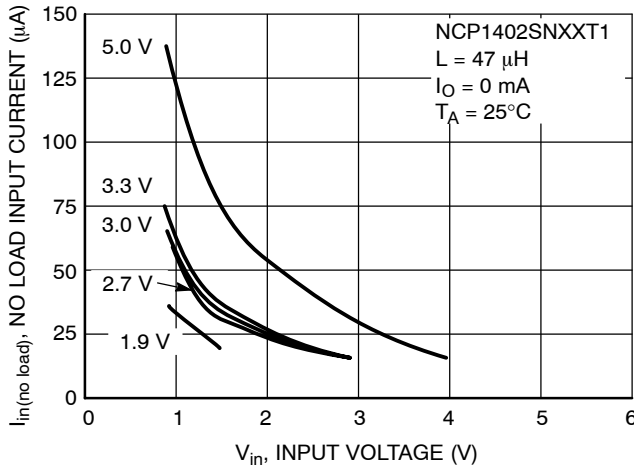


Figure 57. NCP1402SNXXT1 No Load Input Current vs. Input Voltage

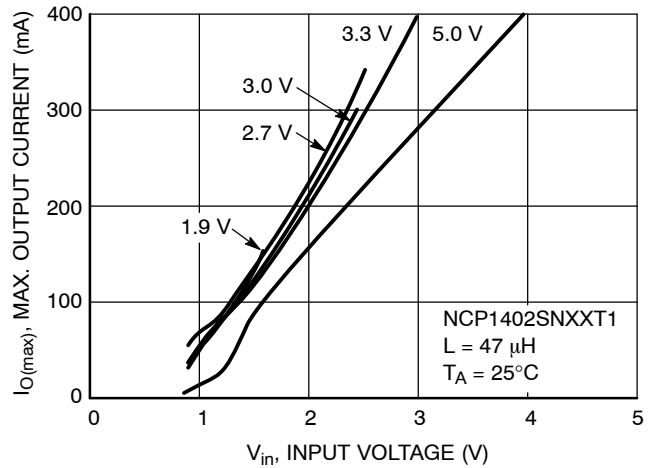


Figure 58. NCP1402SNXXT1 Maximum Output Current vs. Input Voltage

DETAILED OPERATING DESCRIPTION

Operation

The NCP1402 series are monolithic power switching regulators optimized for applications where power drain must be minimized. These devices operate as variable frequency, voltage mode boost regulators and designed to operate in continuous conduction mode. Potential applications include low powered consumer products and battery powered portable products.

The NCP1402 series are low noise variable frequency voltage-mode DC-DC converters, and consist of Soft-Start circuit, feedback resistor, reference voltage, oscillator, PFM comparator, PFM control circuit, current limit circuit and power switch. Due to the on-chip feedback resistor network, the system designer can get the regulated output voltage from 1.8 V to 5 V with a small number of external components. The operating current is typically 30 μ A ($V_{OUT} = 1.9$ V), and can be further reduced to about 0.6 μ A when the chip is disabled ($V_{CE} < 0.3$ V).

The NCP1402 operation can be best understood by examining the block diagram in Figure 2. PFM comparator monitors the output voltage via the feedback resistor. When the feedback voltage is higher than the reference voltage, the power switch is turned off. As the feedback voltage is lower than reference voltage and the power switch has been off for at least a period of minimum off-time decided by PFM oscillator, the power switch is then cycled on for a period of on-time also decided by PFM oscillator, or until current limit signal is asserted. When the power switch is on, current ramps up in the inductor, storing energy in the magnetic field. When the power switch is off, the energy in the magnetic field is transferred to output filter capacitor and the load. The output filter capacitor stores the charge while the inductor current is high, then holds up the output voltage until next switching cycle.

Important: DO NOT apply a voltage between 0.3 V and 0.9 V to pin CE as this is the CE pin's hysteresis voltage range. Clearly defined output states can only be obtained by applying voltage out of this range.

Soft-Start

There is a Soft-Start circuit in NCP1402. When power is applied to the device, the Soft-Start circuit pumps up the output voltage to approximately 1.5 V at a fixed duty cycle, the level at which the converter can operate normally. What is more, the startup capability with heavy loads is also improved.

Regulated Converter Voltage (V_{OUT})

The V_{OUT} is set by an internal feedback resistor network. This is trimmed to a selected voltage from 1.8 to 5.0 V range in 100 mV steps with an accuracy of $\pm 2.5\%$.

Current Limit

The NCP1402 series utilizes cycle-by-cycle current limiting as a means of protecting the output switch MOSFET from overstress and preventing the small value inductor from saturation. Current limiting is implemented by monitoring the output MOSFET current build-up during conduction, and upon sensing an overcurrent conduction immediately turning off the switch for the duration of the oscillator cycle.

The voltage across the output MOSFET is monitored and compared against a reference by the VLX limiter. When the threshold is reached, a signal is sent to the PFM controller block to terminate the power switch conduction. The current limit threshold is typically set at 350 mA.

Enable / Disable Operation

The NCP1402 series offer IC shut-down mode by chip enable pin (CE pin) to reduce current consumption. An internal pullup resistor tied the CE pin to OUT pin by default i.e. user can float the pin CE for permanent "On". When voltage at pin CE is equal or greater than 0.9 V, the chip will be enabled, which means the regulator is in normal operation. When voltage at pin CE is less than 0.3 V, the chip is disabled, which means IC is shutdown.

APPLICATIONS CIRCUIT INFORMATION

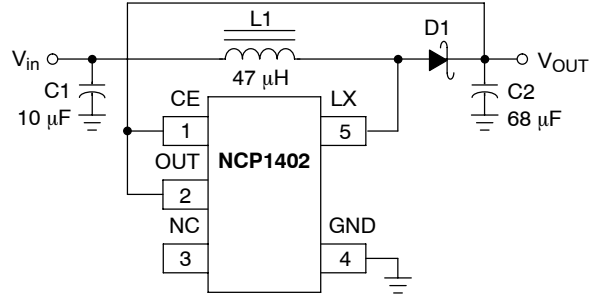


Figure 59. Typical Application Circuit

Step-up Converter Design Equations

NCP1402 step-up DC-DC converter designed to operate in continuous conduction mode can be defined by:

Calculation	Equation
L	$\leq M \left(\frac{V_{in}^2}{V_{OUT} I_{Omax}} \right)$
I_{PK}	$\frac{(V_{in} - V_S)t_{on}}{L} + I_{min}$
I_{min}	$\frac{(t_{on} + t_{off})I_O}{t_{off}} - \frac{(V_{in} - V_S)t_{on}}{2L}$
t_{off}	$\frac{(V_{in} - V_S)t_{on}}{(V_{OUT} + V_F - V_{in})}$
ΔQ	$(I_L - I_O)t_{off}$
V_{ripple}	$\approx \frac{\Delta Q}{C_{OUT}} + (I_L - I_O)ESR$

*NOTES:

- I_{PK} – Peak inductor current
- I_{min} – Minimum inductor current
- I_O – Desired dc output current
- I_{Omax} – Desired maximum dc output current
- I_L – Average inductor current
- V_{in} – Nominal operating dc input voltage
- V_{OUT} – Desired dc output voltage
- V_F – Diode forward voltage
- V_S – Saturation voltage of the internal FET switch
- ΔQ – Charge stores in the C_{OUT} during charging up
- V_{ripple} – Output ripple voltage
- ESR – Equivalent series resistance of the output capacitor
- M – An empirical factor, when $V_{OUT} \geq 3.0 V$,
 $M = 8 \times 10^{-6}$, otherwise $M = 5.3 \times 10^{-6}$.

EXTERNAL COMPONENT SELECTION

Inductor

The NCP1402 is designed to work well with a 47 µH inductor in most applications. 47 µH is a sufficiently low value to allow the use of a small surface mount coil, but large

enough to maintain low ripple. Low inductance values supply higher output current, but also increase the ripple and reduce efficiency. Note that values below 27 µH is not recommended due to NCP1402 switch limitations. Higher inductor values reduce ripple and improve efficiency, but also limit output current.

The inductor should have small DCR, usually less than 1 Ω to minimize loss. It is necessary to choose an inductor with saturation current greater than the peak current which the inductor will encounter in the application.

Diode

The diode is the main source of loss in DC-DC converters. The most importance parameters which affect their efficiency are the forward voltage drop, V_F , and the reverse recovery time, t_{rr} . The forward voltage drop creates a loss just by having a voltage across the device while a current flowing through it. The reverse recovery time generates a loss when the diode is reverse biased, and the current appears to actually flow backwards through the diode due to the minority carriers being swept from the P-N junction. A Schottky diode with the following characteristics is recommended:

- Small forward voltage, $V_F < 0.3 V$
- Small reverse leakage current
- Fast reverse recovery time/ switching speed
- Rated current larger than peak inductor current,
 $I_{rated} > I_{PK}$
- Reverse voltage larger than output voltage,
 $V_{reverse} > V_{OUT}$

Input Capacitor

The input capacitor can stabilize the input voltage and minimize peak current ripple from the source. The value of the capacitor depends on the impedance of the input source used. Small Equivalent Series Resistance (ESR) Tantalum or ceramic capacitor with value of 10 µF should be suitable.

NCP1402

Output Capacitor

The output capacitor is used for sustaining the output voltage when the internal MOSFET is switched on and smoothing the ripple voltage. Low ESR capacitor should be used to reduce output ripple voltage. In general, a 47 μ F to 68 μ F low ESR (0.15 Ω to 0.30 Ω) Tantalum capacitor should be appropriate. For applications where space is a critical factor, two parallel 22 μ F low profile SMD ceramic capacitors can be used.

An evaluation board of NCP1402 has been made in the size of 23 mm x 20 mm only, as shown in Figures 60 and 61. Please contact your ON Semiconductor representative for availability. The evaluation board schematic diagram, the artwork and the silkscreen of the surface mount PCB are shown below:

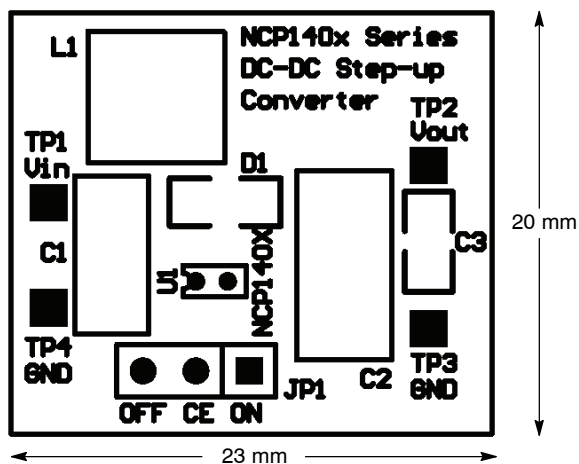


Figure 60. NCP1402 PFM Step-Up DC-DC Converter Evaluation Board Silkscreen

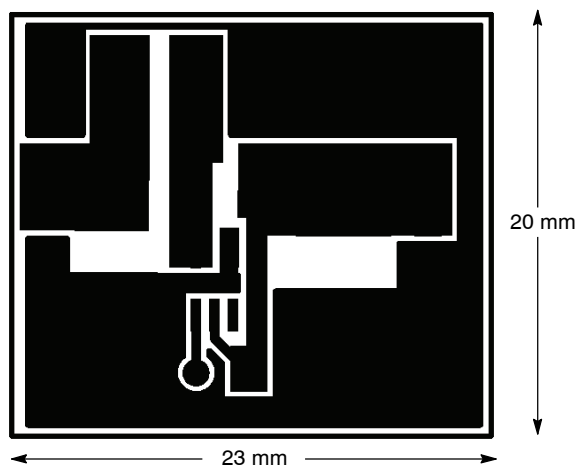


Figure 61. NCP1402 PFM Step-Up DC-DC Converter Evaluation Board Artwork (Component Side)

NCP1402

Components Supplier

Parts	Supplier	Part Number	Description	Phone
Inductor, L1	Sumida Electric Co. Ltd.	CD54-470L	Inductor 47 μ H / 0.72 A	(852)-2880-6688
Schottky Diode, D1	ON Semiconductor Corp.	MBR0520LT1	Schottky Power Rectifier	(852)-2689-0088
Output Capacitor, C2	KEMET Electronics Corp.	T494D686K010AS	Low ESR Tantalum Capacitor 68 μ F / 10 V	(852)-2305-1168
Input Capacitor, C1	KEMET Electronics Corp.	T491C106K016AS	Low Profile Tantalum Capacitor 10 μ F / 16 V	(852)-2305-1168

PCB Layout Hints

Grounding

One point grounding should be used for the output power return ground, the input power return ground, and the device switch ground to reduce noise as shown in Figure 62, e.g.: C2 GND, C1 GND, and U1 GND are connected at one point in the evaluation board. The input ground and output ground traces must be thick enough for current to flow through and for reducing ground bounce.

Power Signal Traces

Low resistance conducting paths should be used for the power carrying traces to reduce power loss so as to improve

efficiency (short and thick traces for connecting the inductor L can also reduce stray inductance), e.g.: short and thick traces listed below are used in the evaluation board:

1. Trace from TP1 to L1
2. Trace from L1 to Lx pin of U1
3. Trace from L1 to anode pin of D1
4. Trace from cathode pin of D1 to TP2

Output Capacitor

The output capacitor should be placed close to the output terminals to obtain better smoothing effect on the output ripple.

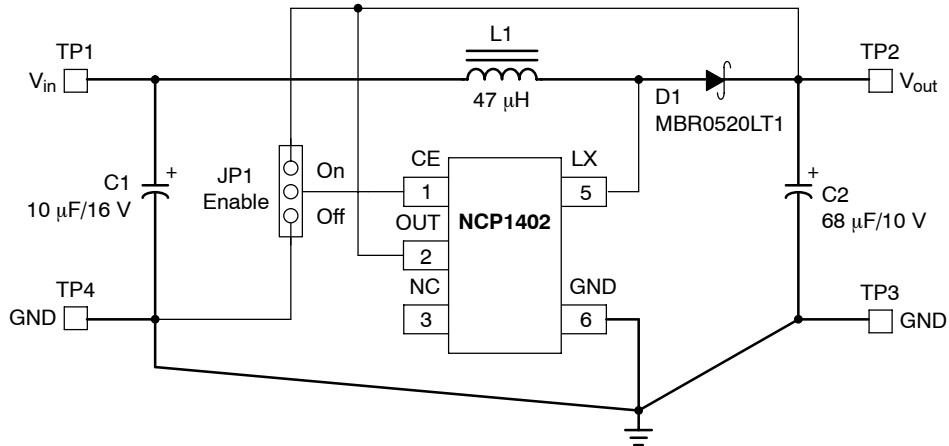


Figure 62. NCP1402 Evaluation Board Schematic Diagram

NCP1403

15 V/50 mA PFM Step-Up DC-DC Converter

The NCP1403 is a monolithic PFM step-up DC-DC converter. This device is designed to boost a single Lithium or two cell AA/AAA battery voltage up to 15 V (with internal MOSFET) output for handheld applications. A pullup Chip Enable feature is built with this device to extend battery-operating life. Besides, the device can also be incorporated in step-down, and voltage-inverting configurations. This device is available in space-saving TSOP-5 package.

Features

- 82% Efficiency at $V_{OUT} = 15\text{ V}$, $I_{OUT} = 50\text{ mA}$, $V_{IN} = 5.0\text{ V}$
- 78% Efficiency at $V_{OUT} = 15\text{ V}$, $I_{OUT} = 30\text{ mA}$, $V_{IN} = 3.6\text{ V}$
- Low Operating Current of $19\text{ }\mu\text{A}$ (No Switching)
- Low Shutdown Current of $0.3\text{ }\mu\text{A}$
- Low Startup Voltage of 1.3 V Typical at 0 mA
- Output Voltage up to 15 V with Built-in 16 V MOSFET Switch
- PFM Switching Frequency up to 300 kHz
- Chip Enable
- Low Profile and Minimum External Parts
- Micro Miniature TSOP-5 Package

Typical Applications

- LCD Bias
- Personal Digital Assistants (PDA)
- Digital Still Camera
- Handheld Games
- Hand-held Instrument



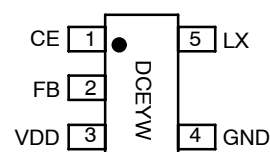
ON Semiconductor®

<http://onsemi.com>



**TSOP-5
CASE 483
SN SUFFIX**

PIN CONNECTIONS AND MARKING DIAGRAM



(Top View)

DCE = Device Marking

Y = Year

W = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NCP1403SNT1	TSOP-5	3000/Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP1403

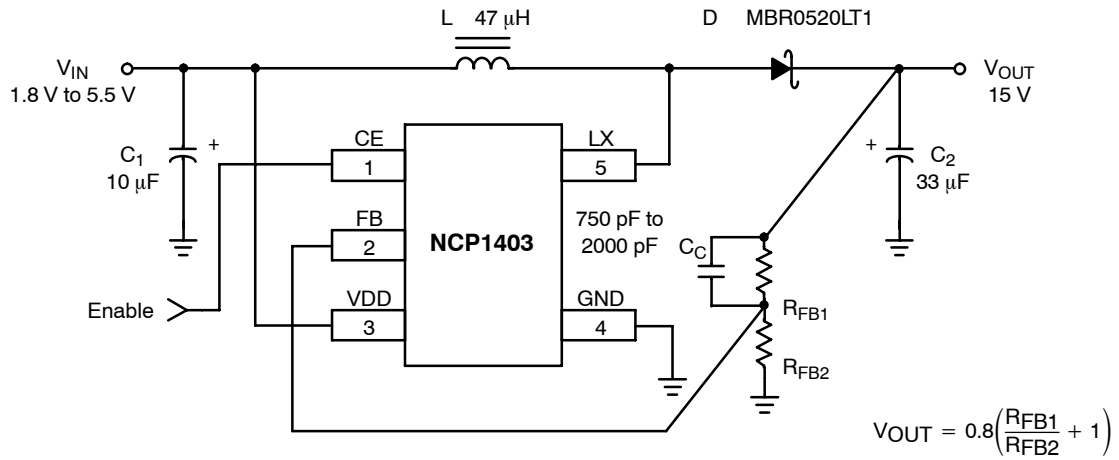


Figure 63. Typical Step-Up Application Circuit 1

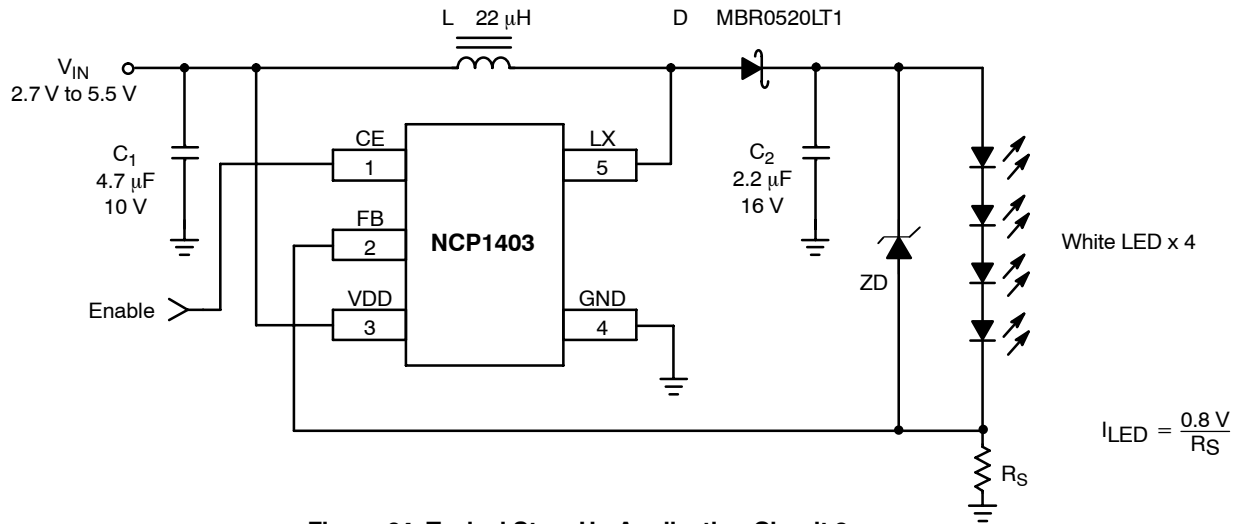


Figure 64. Typical Step-Up Application Circuit 2

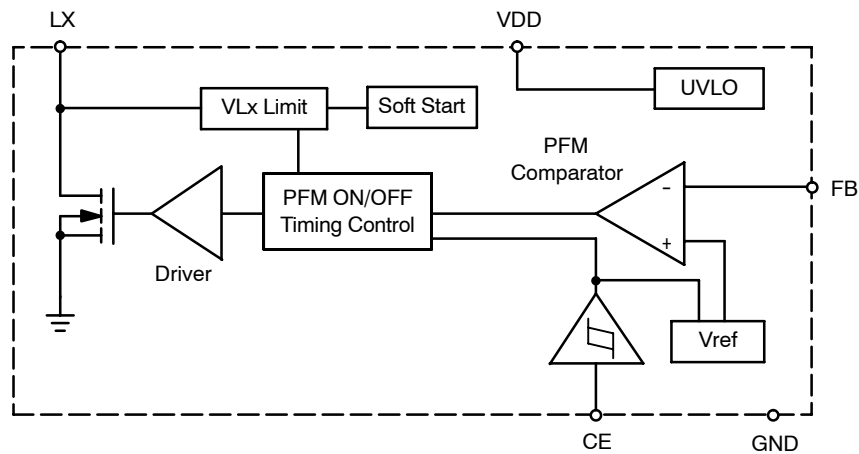


Figure 65. Representative Block Diagram

PIN FUNCTION DESCRIPTIONS

Pin	Symbol	Description
1	CE	Chip Enable Pin 1. The chip is enabled if a voltage which is equal to or greater than 0.9 V is applied. 2. The chip is disabled if a voltage which is less than 0.3 V is applied. 3. The chip will be enabled if it is left floating.
2	FB	PFM comparator inverting input, and is connected to off-chip resistor divider which sets output voltage.
3	VDD	Power supply pin for internal circuit.
4	GND	Ground pin.
5	LX	External inductor connection pin.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 3)	V_{DD}	-0.3 to 6.0	V
Input/Output Pin LX (Pin 5) LX Peak Sink Current FB (Pin 2)	V_{LX} I_{LX} V_{FB}	-0.3 to 16.0 600 -0.3 to 6.0	V mA V
CE (Pin 1) Input Voltage Range Input Current Range	V_{CE} I_{CE}	-0.3 to 6.0 150	V mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$ Thermal Resistance Junction-to-Air	P_D $R_{\theta JA}$	500 250	mW $^\circ\text{C/W}$
Operating Ambient Temperature Range	T_A	-40 to +85	$^\circ\text{C}$
Operating Junction Temperature Range	T_J	-40 to +150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

7. This device series contains ESD protection and exceeds the following tests:
Human Body Model (HBM) ± 2.0 kV per JEDEC standard: JESD22-A114 for all pins except LX pin.
Human Body Model (HBM) ± 1.5 kV for LX pin.
Machine Model (MM) ± 200 V per JEDEC standard: JESD22-A115 for all pins.
8. Latchup Current Maximum Rating: ± 150 mA per JEDEC standard: JESD78.
9. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.

NCP1403

ELECTRICAL CHARACTERISTICS ($V_{OUT} = 15\text{ V}$, $T_A = 25^\circ\text{C}$, for min/max values unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON/OFF TIMING CONTROL					
Minimum Off Time ($V_{DD} = 3.0\text{ V}$, $V_{FB} = 0\text{ V}$)	t_{off}	0.8	1.3	1.5	μs
Maximum On Time (Current not asserted)	t_{on}	4.0	6.0	8.4	μs
Maximum Duty Cycle	D_{MAX}	75	83	91	%
Minimum Startup Voltage ($I_{OUT} = 0\text{ mA}$)	V_{start}	–	1.3	1.8	V
Minimum Startup Voltage Temperature Coefficient ($T_A = -40\text{ to }+85^\circ\text{C}$)	DV_{start}	–	1.6	–	$\text{mV}/^\circ\text{C}$
Minimum Supply Voltage ($I_{OUT} = 0\text{ mA}$)	V_{hold}	–	1.2	1.7	V
Soft-Start Time	t_{SS}	0.5	10	–	ms
LX (PIN 5)					
Internal Switch Voltage (Note 10)	V_{LX}	0.5	–	16	V
LX Pin On-State Sink Current ($V_{LX} = 0.4\text{ V}$, $V_{DD} = 3.0\text{ V}$)	I_{LX}	100	130	–	mA
Voltage Limit (When V_{LX} reaches V_{LXLIM} , the LX switch is turned off by the LX switch protection circuit)	V_{LXLIM}	0.55	0.75	1.0	V
Off-State Leakage Current ($V_{LX} = 16\text{ V}$)	I_{LKG}	–	0.1	1.0	μA
CE (PIN 1)					
CE Input Voltage ($V_{DD} = 3.0\text{ V}$, $V_{FB} = 0\text{ V}$)					
High State, Device Enabled	$V_{CE(high)}$	0.9	–	–	V
Low State, Device Enabled	$V_{CE(low)}$	–	–	0.3	V
CE Input Current					
High State, Device Enabled ($V_{DD} = V_{CE} = 5.5\text{ V}$)	$I_{CE(high)}$	–0.5	0	0.5	μA
Low State, Device Enabled ($V_{DD} = 5.5\text{ V}$, $V_{CE} = V_{FB} = 0\text{ V}$)	$I_{CE(low)}$	–0.5	–0.1	0.5	μA
TOTAL DEVICE					
Supply Voltage	V_{DD}	1.2	–	5.5	V
Feedback Voltage	V_{FB}	0.76	0.8	0.84	V
Feedback Pin Bias Current ($V_{FB} = 0.8\text{ V}$)	I_{FB}	–	15	30	nA
Operating Current 1 ($V_{FB} = 0\text{ V}$, $V_{DD} = V_{CE} = 3.0\text{ V}$)	I_{DD1}	–	130	200	μA
Operating Current 2 ($V_{DD} = V_{CE} = V_{FB} = 3.0\text{ V}$, Not switching)	I_{DD2}	–	19	25	μA
Off-state Current ($V_{DD} = 5.0\text{ V}$, $V_{CE} = 0\text{ V}$, internal 100 nA pullup current source)	I_{OFF}	–	0.3	0.8	μA

10. Recommend maximum V_{OUT} up to 15 V.

TYPICAL CHARACTERISTICS

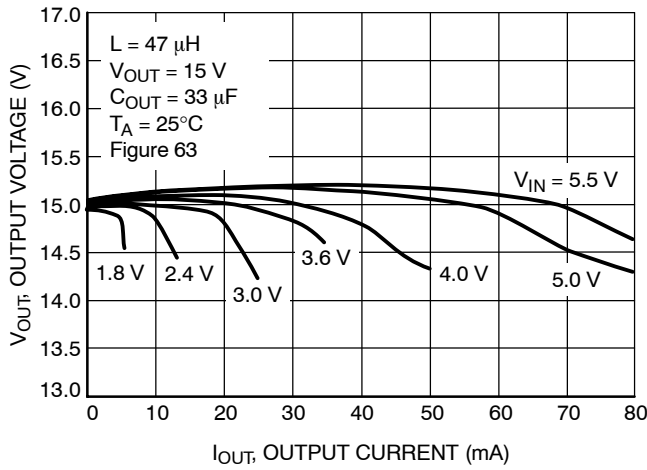


Figure 66. Output Voltage versus Output Current ($V_{OUT} = 15\text{ V}$)

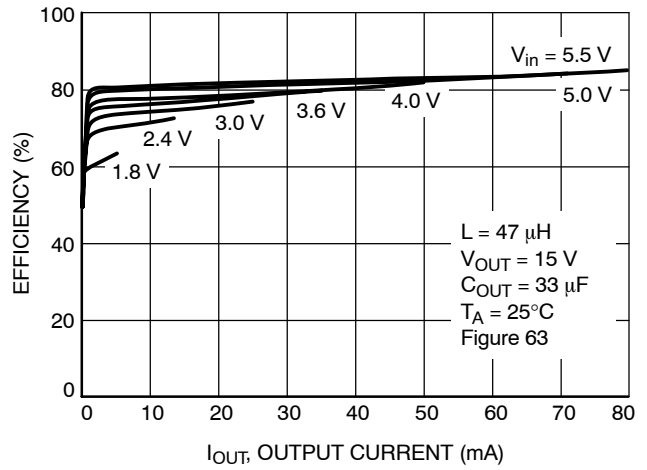


Figure 67. Efficiency versus Output Current ($V_{OUT} = 15\text{ V}$)

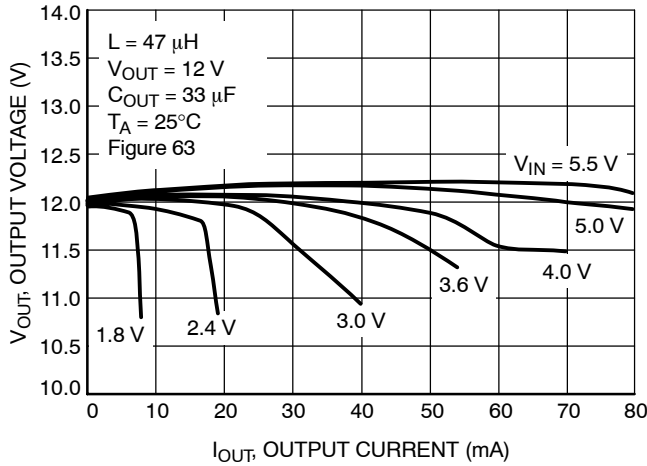


Figure 68. Output Voltage versus Output Current ($V_{OUT} = 12\text{ V}$)

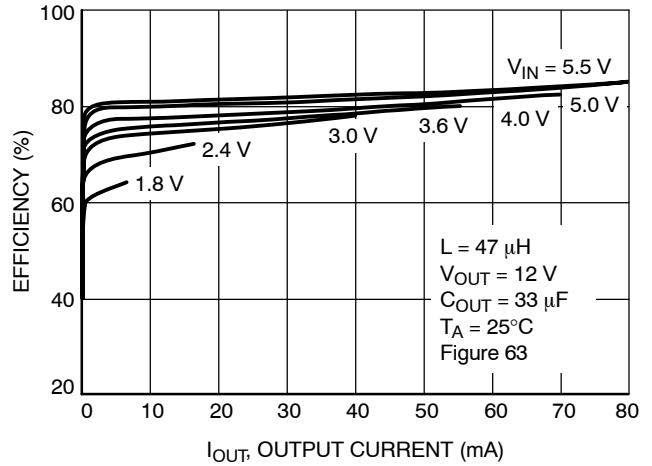


Figure 69. Efficiency versus Output Current ($V_{OUT} = 12\text{ V}$)

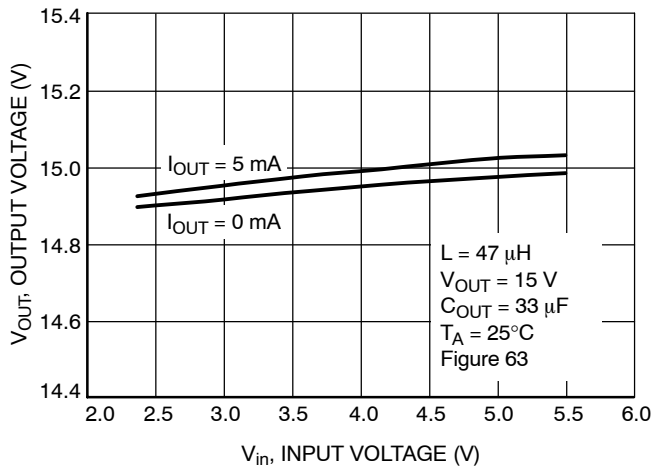


Figure 70. Output Voltage versus Input Voltage ($V_{OUT} = 15\text{ V}$)

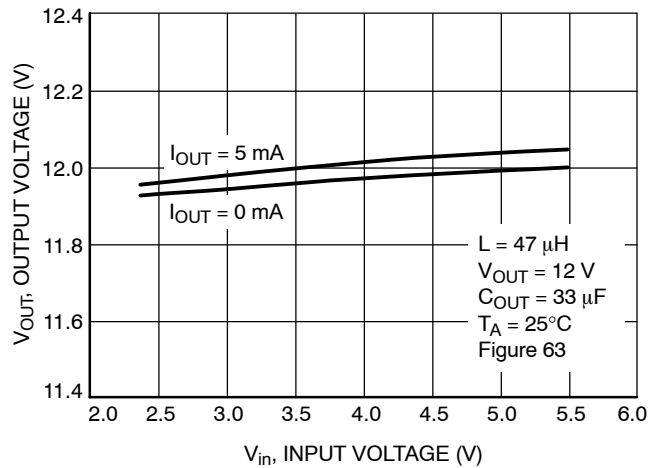


Figure 71. Output Voltage versus Input Voltage ($V_{OUT} = 12\text{ V}$)

TYPICAL CHARACTERISTICS

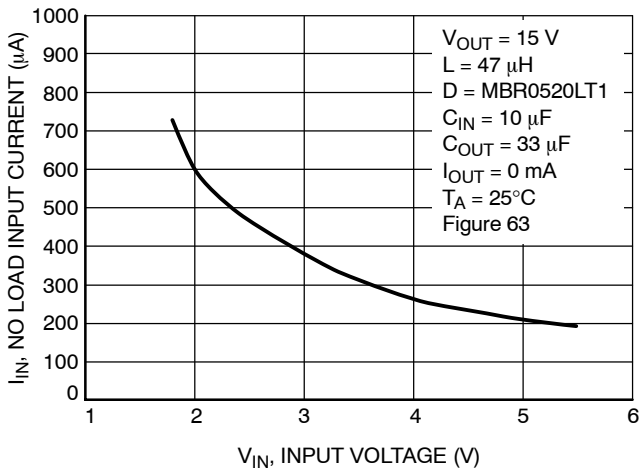


Figure 72. No Load Input Current versus Input Voltage

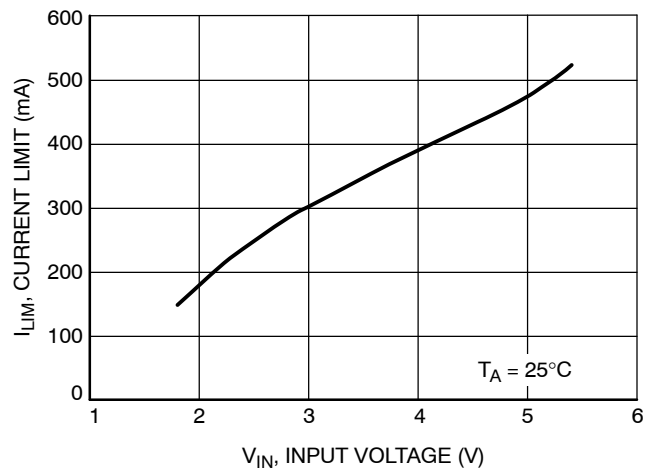


Figure 73. Current Limit versus Input Voltage

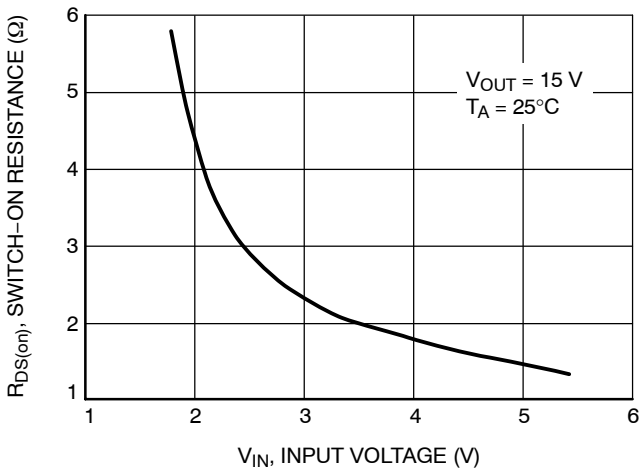


Figure 74. Switch-On Resistance versus Input Voltage

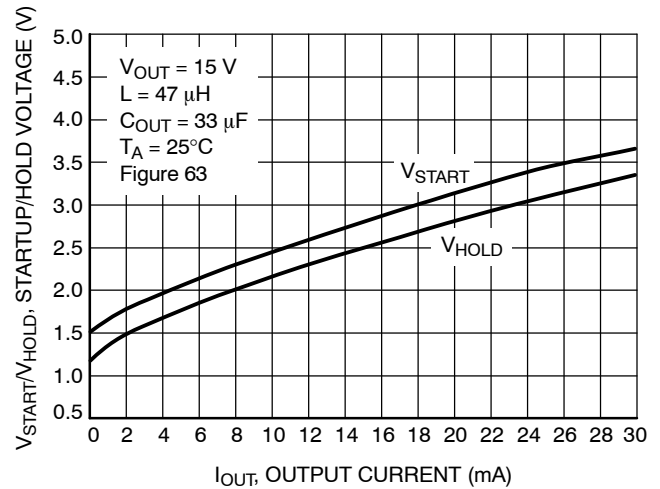


Figure 75. Startup/Hold Voltage versus Output Current

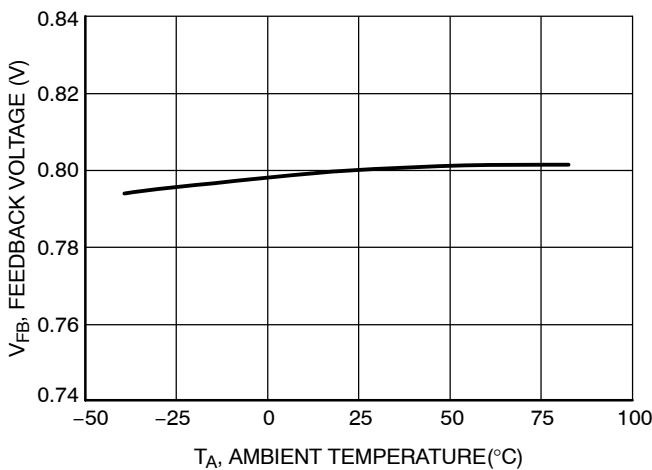


Figure 76. Feedback Voltage versus Ambient Temperature

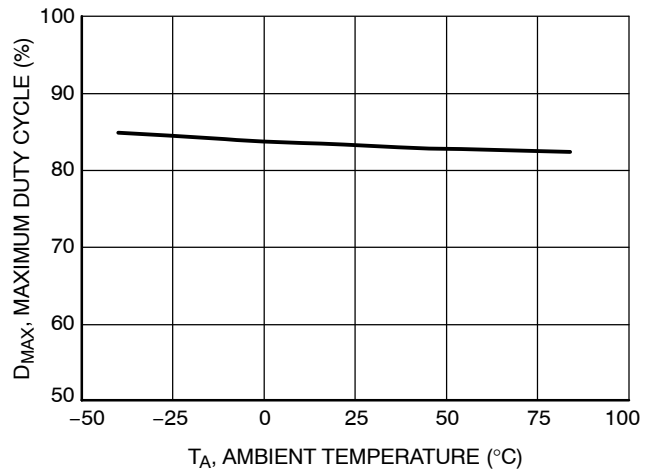


Figure 77. Maximum Duty Cycle versus Ambient Temperature

TYPICAL CHARACTERISTICS

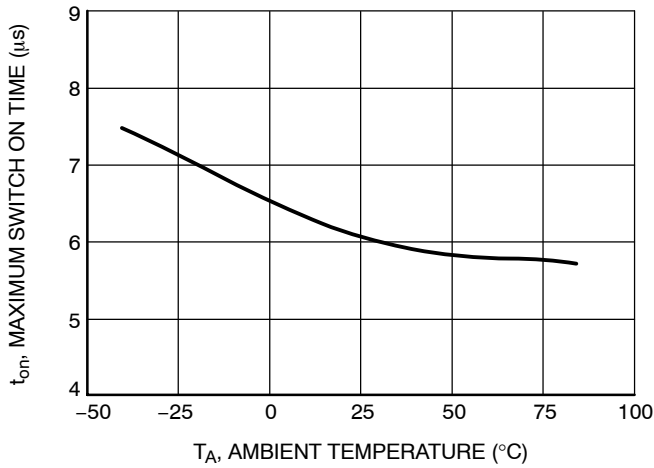


Figure 78. Maximum Switch On Time

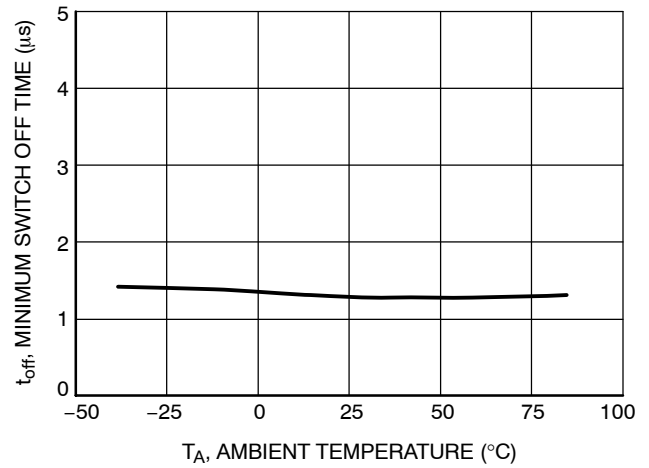


Figure 79. Minimum Switch Off Time

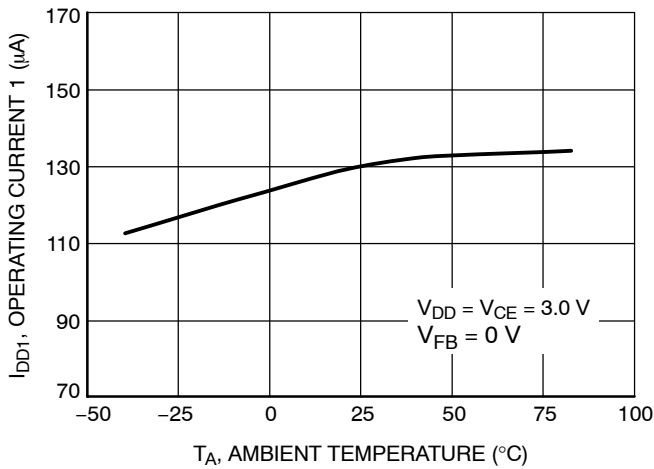


Figure 80. Operating Current 1 versus Ambient Temperature

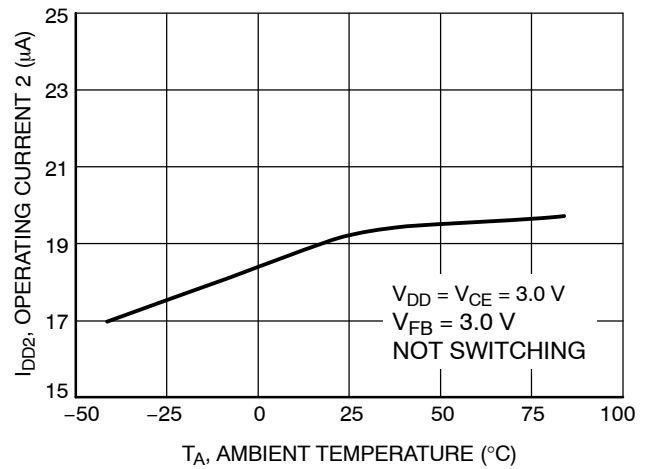


Figure 81. Operating Current 2 versus Ambient Temperature

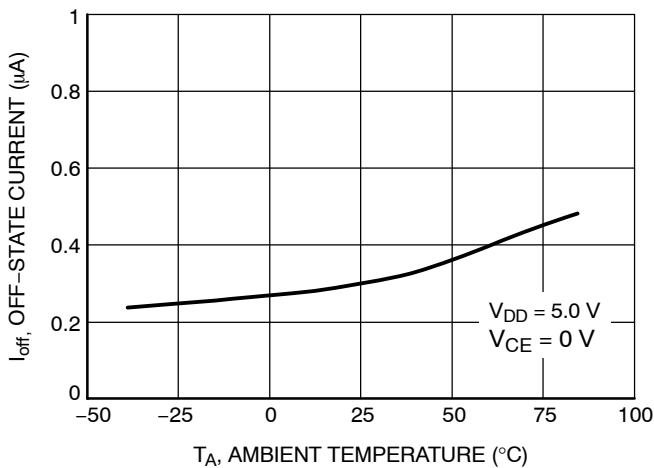


Figure 82. Off-State Current versus Ambient Temperature

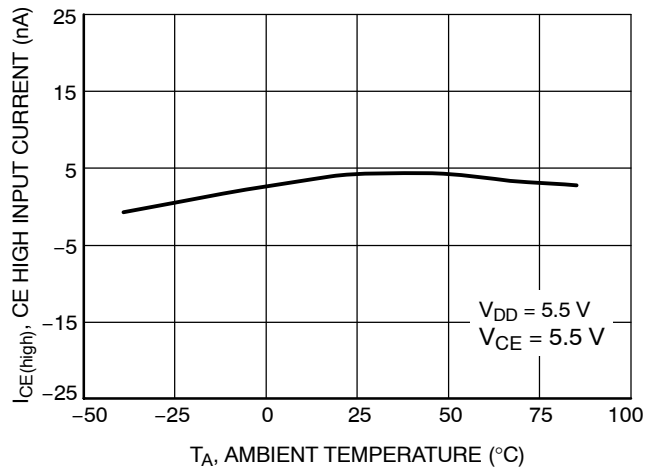
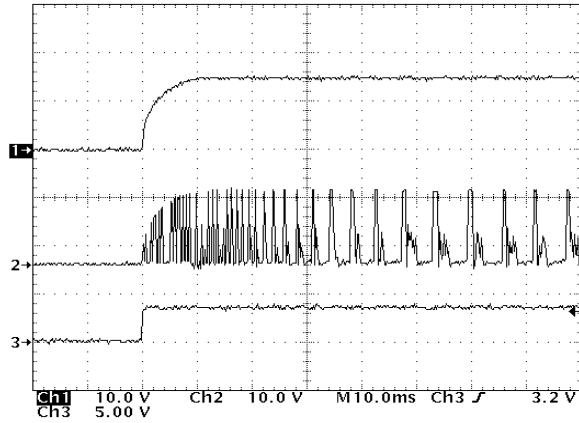


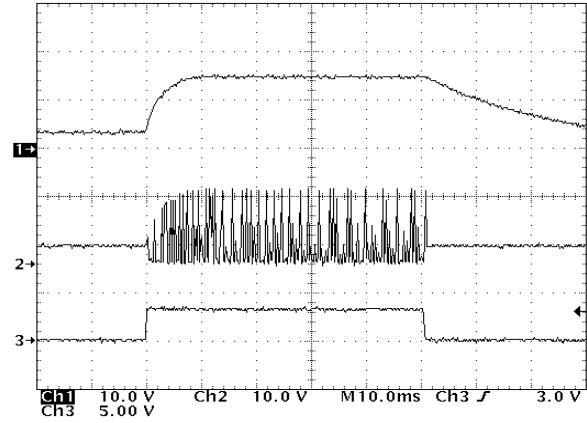
Figure 83. CE High Input Current versus Ambient Temperature

TYPICAL CHARACTERISTICS



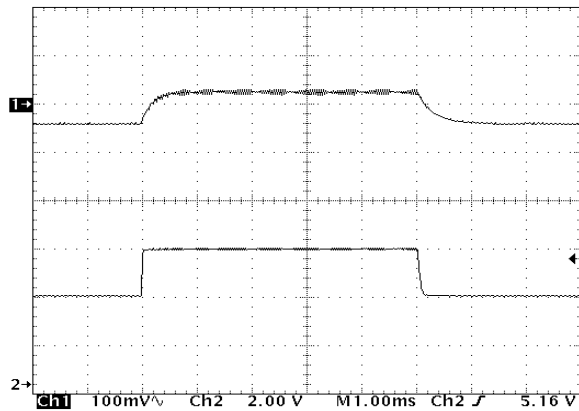
- $L = 47\ \mu\text{H}$, $C_{\text{IN}} = 10\ \mu\text{F}$, $C_{\text{OUT}} = 33\ \mu\text{F}$, $I_{\text{OUT}} = 20\ \text{mA}$
1. $V_{\text{OUT}} = 15\ \text{V}$, 10 V/div
 2. V_{LX} , 10 V/div
 3. $V_{\text{IN}} = 0\ \text{V}$ to 3.6 V, 5 V/div

Figure 84. Startup Waveforms



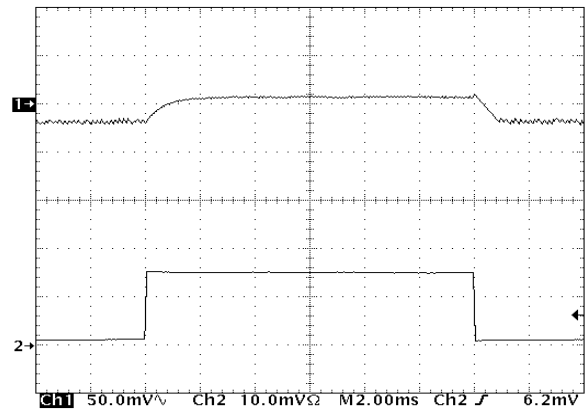
- $L = 47\ \mu\text{H}$, $C_{\text{IN}} = 10\ \mu\text{F}$, $C_{\text{OUT}} = 33\ \mu\text{F}$, $V_{\text{IN}} = 3.6\ \text{V}$, $I_{\text{OUT}} = 20\ \text{mA}$
1. $V_{\text{OUT}} = 15\ \text{V}$, 10 V/div
 2. V_{LX} , 10 V/div
 3. $V_{\text{CE}} = 0\ \text{V}$ to 3.3 V, 5 V/div

Figure 85. Chip Enable Waveforms



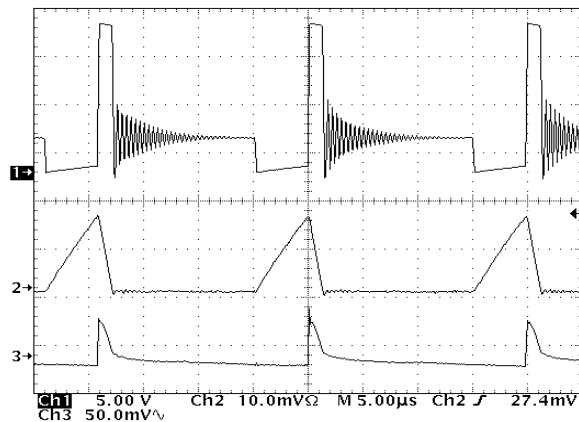
- $L = 47\ \mu\text{H}$, $C_{\text{IN}} = 10\ \mu\text{F}$, $C_{\text{OUT}} = 33\ \mu\text{F}$, $I_{\text{OUT}} = 10\ \text{mA}$
1. $V_{\text{OUT}} = 15\ \text{V}$ (AC Coupled), 100 mV/div
 2. $V_{\text{IN}} = 3.6\ \text{V}$ to 5.5 V, 2.0 V/div

Figure 86. Line Transient Response



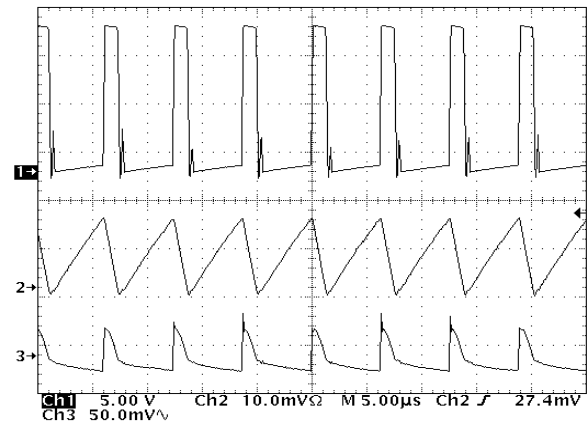
- $L = 47\ \mu\text{H}$, $C_{\text{IN}} = 10\ \mu\text{F}$, $C_{\text{OUT}} = 33\ \mu\text{F}$, $V_{\text{IN}} = 3.6\ \text{V}$
1. $V_{\text{OUT}} = 15\ \text{V}$ (AC Coupled), 50 mV/div
 2. $I_{\text{OUT}} = 1.0\ \text{mA}$ to 15 mA, 10 mA/div

Figure 87. Load Transient Response



- $L = 47\ \mu\text{H}$, $C_{\text{IN}} = 10\ \mu\text{F}$, $C_{\text{OUT}} = 33\ \mu\text{F}$, $V_{\text{IN}} = 3.6\ \text{V}$, $V_{\text{OUT}} = 15\ \text{V}$, $I_{\text{OUT}} = 10\ \text{mA}$
1. V_{LX} , 5.0 V/div
 2. I_{L} , 200 mA/div
 3. V_{ripple} , 50 mV/div

Figure 88. Operating Waveforms (Medium Load)



- $L = 47\ \mu\text{H}$, $C_{\text{IN}} = 10\ \mu\text{F}$, $C_{\text{OUT}} = 33\ \mu\text{F}$, $V_{\text{IN}} = 3.6\ \text{V}$, $V_{\text{OUT}} = 15\ \text{V}$, $I_{\text{OUT}} = 30\ \text{mA}$
1. V_{LX} , 5.0 V/div
 2. I_{L} , 200 mA/div
 3. V_{ripple} , 50 mV/div

Figure 89. Operating Waveforms (Heavy Load)

DETAILED OPERATING DESCRIPTION

Operation

The NCP1403 is monolithic DC-DC switching converter optimized for single Lithium or two cells AA/AAA size batteries powered portable products.

The NCP1403 device consists of startup circuit, chip enable circuit, PFM comparator, voltage reference, PFM on/off timing control circuit, driver, current limit circuit, and open-drain MOSFET switch. The device operating current is typically 130 μA , and can be further reduced to about 0.3 μA when the chip is disabled ($V_{\text{CE}} < 0.3 \text{ V}$).

The operation of NCP1403 can be best understood by referring to the block diagram and typical application circuit 1 in Figures 65 and 63. The PFM comparator monitors the output voltage via the external feedback resistor divider by comparing the feedback voltage with the reference voltage. When the feedback voltage is lower than the reference voltage, the PFM control and driver circuit turns on the N-Channel MOSFET switch and the current ramps up in the inductor. The switch will remain on for the maximum on-time, 6.0 μs , or until the current limit is reached, whichever occurs first. The MOSFET switch is then turned off and energy stored in the inductor will be discharged to the output capacitor and load through the Schottky diode. The MOSFET switch will be turned off for at least the minimum off-time, 1.3 μs , and will remain off if the feedback voltage is higher than the reference voltage and output capacitor will be discharged to sustain the output current, until the feedback voltage is again lower than reference voltage. This switching cycle is then repeated to attain voltage regulation.

Soft Start

There is a soft start circuit in NCP1403. When power is applied to the device, the soft start circuit pumps up the output voltage to approximately 1.5 V at a fixed duty cycle, the level at which the converter can operate normally. With the soft start circuit, the output voltage overshoot is minimized and the startup capability with heavy loads is also improved.

ON/OFF Timing Control

The maximum on-time is typically 6.0 μs , whereas, the minimum off-time is typically 1.3 μs . Owing to the current limit circuit, the on-time can be shorter. The switching frequency can be up to 300 kHz.

Voltage Reference and Output Voltage

The internal voltage reference is trimmed to 0.8 V at an accuracy of $\pm 5.0\%$. The voltage reference is connected to the non-inverting input of the PFM comparator and the inverting input of the PFM comparator is connected to the FB pin. The output voltage can be set by connected an external resistor voltage divider from the V_{OUT} to the FB pin. With the internal 16 V MOSFET switch, the output voltage can be set between V_{IN} to 15 V.

LX Limit

The LX Limit is a current limit feature which is achieved by monitoring the voltage at the LX pin during the MOSFET switch turn-on period. When the switch is turned on, current ramps up in the inductor, and the voltage at the LX pin will increase according to the Ohm's Law due to the On-state resistance of the MOSFET. When the V_{LX} is greater than 0.75 V, the switch will be turned off. With the current limit circuit, saturation of inductor is prevented and output voltage overshoot during startup can also be minimized.

N-Channel MOSFET Switch

The NCP1403 is built-in with a 16 V open drain N-Channel MOSFET switch which allows high output voltage up to 15 V to be generated from simple step-up topology.

Enable / Disable Operation

The NCP1403 offers IC shut-down mode by the chip enable pin (CE pin) to reduce current consumption. An internal 100 nA pullup current source tied the CE pin to OUT pin by default i.e. user can float the pin CE for permanent "ON". When voltage at pin CE is equal to or greater than 0.9 V, the chip will be enabled, which means the device is in normal operation. When voltage at pin CE is less than 0.3 V, the chip is disabled, which means IC is shutdown. During shutdown, the IC supply current reduces to 0.3 μA and LX pin enters high impedance state. However, the input remains connected to the output through the inductor and the Schottky diode, keeping the output voltage to one diode forward voltage drop below the input voltage.

APPLICATIONS CIRCUIT INFORMATION

External Component Selection

Inductor

The NCP1403 is designed to work well with a range of inductance values, the actual inductance value depends on the specific application, output current, efficiency, and output ripple voltage. For step up conversion, the device works well with inductance ranging from 22 μ H to 47 μ H. Inductor with small DCR, usually less than 1.0 Ω , should be used to minimize loss. It is necessary to choose an inductor with saturation current greater than the peak switching current in the application.

If 22 μ H inductance is used, lower profile surface mount inductor can be selected for the same current rating. Moreover, it permits the converter to switch at higher frequency up to 300 kHz since the inductor current will ramp up faster and hit the current limit at a shorter time for smaller inductance value. However, current output are slightly lower because the off-time is limited by the minimum off-time. If 47 μ H inductance is selected, higher efficiency and output current capability are achieved, but the converter will switch at a lower frequency and the inductor size will be slightly larger for the same current rating.

For lower inductance value, the inductor current ramp-down time will be shorter than the minimum off-time. Consequently, the converter can only operate in discontinuous conduction mode and lower output current can be generated. For higher inductance value, if the inductance is sufficiently large, the maximum on-time will expire before the current limit is reached. As a result, the available output power and output current are reduced. Besides, instability may occur when operation enters CCM.

To ensure the current limit is reached before the maximum on-time expires, L can be selected according to the inequality below:

$$L \leq \frac{(V_{IN} - V_S)}{I_{LIM}} \cdot t_{on(MAX)}$$

where $V_S = 0.75$ V which is the MOSFET saturation voltage, and I_{LIM} is the current limit which can be referred to in Figure 73, and $t_{on(MAX)} = 6.0$ μ s.

If the above condition is satisfied, $I_{PK} = I_{LIM}$; where I_{PK} is the peak inductor current. Then, step-up converter with inductor satisfy the following condition will operate in DCM only,

$$\frac{I_{LIM} \cdot L}{(V_{OUT} + V_D - V_{IN})} \leq t_{off(MIN)}$$

If the $I_{PK} = I_{LIM}$, step-up converter with inductor satisfy the following condition will operate in CCM at maximum output current,

$$\frac{I_{LIM} \cdot L}{(V_{OUT} + V_D - V_{IN})} > t_{off(MIN)}$$

where V_D is the Schottky diode forward voltage drop, $t_{off(MIN)} = 1.3$ μ s.

For step-up converter operates in DCM only, the maximum output current can be calculated from the equation below:

$$I_{OUT(MAX)} = \frac{(I_{LIM})^2 L}{2(V_{OUT} + V_D - V_{IN}) \left(\left(\frac{I_{LIM} \times L}{V_{IN} - V_S} \right) + t_{off(MIN)} \right)}$$

For step-up converter operates in CCM, the maximum output current can be calculated from the equation below:

$$I_{OUT(MAX)} = \left(I_{LIM} - \frac{(V_{OUT} + V_D - V_{IN}) t_{off(MIN)}}{2L} \right) \cdot \frac{(V_{IN} - V_S)}{(V_{OUT} + V_D - V_S)}$$

Diode

The diode is the main source of loss in DC-DC converters. The most importance parameters which affect their efficiency are the forward voltage drop, V_F , and the reverse recovery time, t_{rr} . The forward voltage drop creates a loss just by having a voltage across the device while a current flowing through it. The reverse recovery time generates a loss when the diode is reverse biased, and the current appears to actually flow backwards through the diode due to the minority carriers being swept from the P-N junction. A Schottky diode with the following characteristics is recommended:

1. Small forward voltage, $V_F < 0.3$ V
2. Small reverse leakage current
3. Fast reverse recovery time / switching speed
4. Rated current larger than peak inductor current,
 $I_{rated} > I_{PK}$
5. Reverse voltage larger than output voltage,
 $V_{reverse} > V_{OUT}$

Input Capacitor

The input capacitor can stabilize the input voltage and minimize peak current ripple from the source. The value of the capacitor depends on the impedance of the input source used. Small ESR (Equivalent Series Resistance) Tantalum or ceramic capacitor with value of 10 μ F should be suitable.

Output Capacitor

The output capacitor is used for sustaining the output voltage when no current is delivering from the input, and smoothing the ripple voltage. Low ESR Tantalum capacitor should be used to reduce output ripple voltage since the output ripple voltage is dominated by the ESR value of the Tantalum capacitor. In general, a 22 μ F to 47 μ F low ESR (0.2 Ω to 0.4 Ω) Tantalum capacitor should be appropriate. The output ripple voltage can be approximately given by the following equation:

$$V_{ripple} \approx (I_{PK} - I_{OUT}) \cdot ESR$$

Feedback Resistors

Choose the R_{FB2} value from the range 10 k Ω to 200 k Ω for positive output voltage. The value of R_{FB1} can then be calculated from the equation below:

$$R_{FB1} = R_{FB2} \left(\frac{V_{OUT}}{0.8} - 1 \right)$$

1% tolerance resistors should be used for both R_{FB1} and R_{FB2} for better V_{OUT} accuracy.

Output Voltage Higher than 15 V

NCP1403 can be used to generate output voltage higher than 15 V by adding an external high voltage N-Channel MOSFET in series with the internal MOSFET switch as shown in Figure 95. The drain-to-source breakdown voltage of the external MOSFET must be at least 1 V higher than the output voltage. The diode D1 helps the external MOSFET to turn off and ensures that most of the voltage across the external MOSFET during the switch-off period. Since the high voltage external MOSFET is in series with the internal MOSFET, higher break down voltage is achieved but the current capability is not increased.

There is an alternative application circuit shown in Figure 97 which can output voltage up to 30 V. For this circuit, a diode-capacitor charge-pump voltage doubler constructed by D2, D3 and C1 is added. During the internal MOSFET switch-on time, the LX pin is shorted to ground and D2 will charge up C1 to the stepped up voltage at the cathode of D1. During the MOSFET switch-off time, the voltage at V_{OUT} will be almost equal to the double of the voltage at the cathode of D1. The V_{OUT} is monitored by the FB pin via the resistor divider and can be set by the resistor values. Since the maximum voltage at the cathode of D1 is 15 V, the maximum V_{OUT} is 30 V. The value of C1 can be in the range of 0.47 µF to 2.2 µF.

Negative Voltage Generation

The NCP1403 can be used to produce a negative voltage output by adding a diode-capacitor charge-pump circuit (D2, D3, and C1) to the LX pin as shown in Figure 94. The feedback voltage resistor divider is still connected to the positive output to monitor the positive output voltage and a small value capacitor is used at C2. When the internal MOSFET switches off, the voltage at the LX pin charges up the capacitor through diode D2. When the MOSFET switches on, the capacitor C1 is effectively connected like a reversed battery and C1 discharges the stored charges through the R_{ds(on)} of the internal MOSFET and D3 to charge up C_{OUT} and builds up a negative voltage at V_{OUT}. Since the negative voltage output is not directly monitored by the NCP1403, the output load regulation of the negative output is not as good as the standard positive output circuit. The resistance values of the resistors of the voltage divider can be one-tenth of those used in the positive output circuit in order to improve the regulation at light load.

For the application circuit in Figure 98, it is actually the combination of the application circuits in Figures 94 and 95.

Step-Down Converter

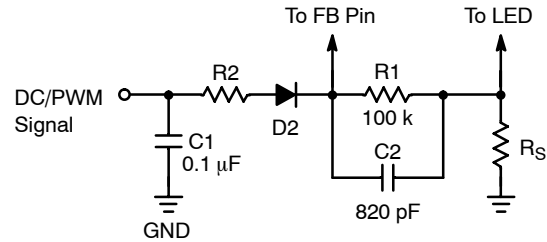
NCP1403 can be configured as a simple step-down converter by using the open-drain LX pin to drive an external P-Channel MOSFET as shown in Figure 96. The resistor R_{GS} is used to switch off the P-Channel MOSFET during the switch-off period. Too small resistance value should not be used for R_{GS}, otherwise, the efficiency will be reduced.

White LED Driver

The NCP1403 can be used as a constant current LED driver which can drive up to 4 white LEDs in series as shown in Figure 64. The LED current can be set by the resistance value of R_S. The desired LED current can be calculated by the equation below:

$$I_{LED} = \frac{0.8}{R_S}$$

Moreover, the brightness of the LEDs can be adjusted by a DC voltage or a PWM signal with an additional circuit illustrated below:



With this additional circuit, the maximum LED current is set by the above equation. The value of R₂ can be obtained by the following equation:

$$R_2 = \frac{V_{MAX} - V_D - 0.8}{\left(\frac{(I_{LED(MAX)} - I_{LED(MIN)}) R_S}{R_1} \right)}$$

V_{MAX} is the maximum voltage of the control signal, V_D is the diode forward voltage, I_{LED(MAX)} is the maximum LED current and I_{LED(MIN)} is the minimum LED current. If a PWM control signal is used, the signal frequency from 4 kHz to 40 kHz can be applied.

In case the LEDs fail, the feedback voltage will become zero. The NCP1403 will then switch at maximum duty cycle and result in a high output voltage which will cause the LX pin voltage to exceed its maximum rating. A Zener diode can be added across the output and FB pin to limit the voltage at the LX pin. The Zener voltage should be higher than the total forward voltage of the LED string.

PCB Layout Hints

The schematic, PCB trace layout, and component placement of the step-up DC-DC converter demonstration board are shown in Figure 90 to Figure 93 for PCB layout design reference.

Grounding

One point grounding should be used for the output power return ground, the input power return ground, and the device switch ground to reduce noise. The input ground and output ground traces must be thick and short enough for current to flow through. A ground plane should be used to reduce ground bounce.

NCP1403

Power Signal Traces

Low resistance conducting paths should be used for the power carrying traces to reduce power loss so as to improve efficiency (short and thick traces for connecting the inductor L can also reduce stray inductance). Besides, the length and area of all the traces with connection to the LX pin should be minimized. e.g., short and thick traces listed below should be used in the PCB:

1. Trace from V_{IN} to L
2. Trace from L to LX pin of the IC
3. Trace from L to anode pin of Schottky diode
4. Trace from cathode pin of Schottky diode to V_{OUT} .

External Feedback Resistors

Feedback resistors should be located as close to the FB pin as possible to minimize noise picked up by the FB pin. The ground connection of the feedback resistor divider should be connected directly to the GND pin.

Input Capacitor

The input capacitor should be located close to both the V_{IN} to the inductor and the V_{DD} pin of the IC.

Output Capacitor

The output capacitor should be placed close to the output terminals to obtain better smoothing effect on output ripple voltage.

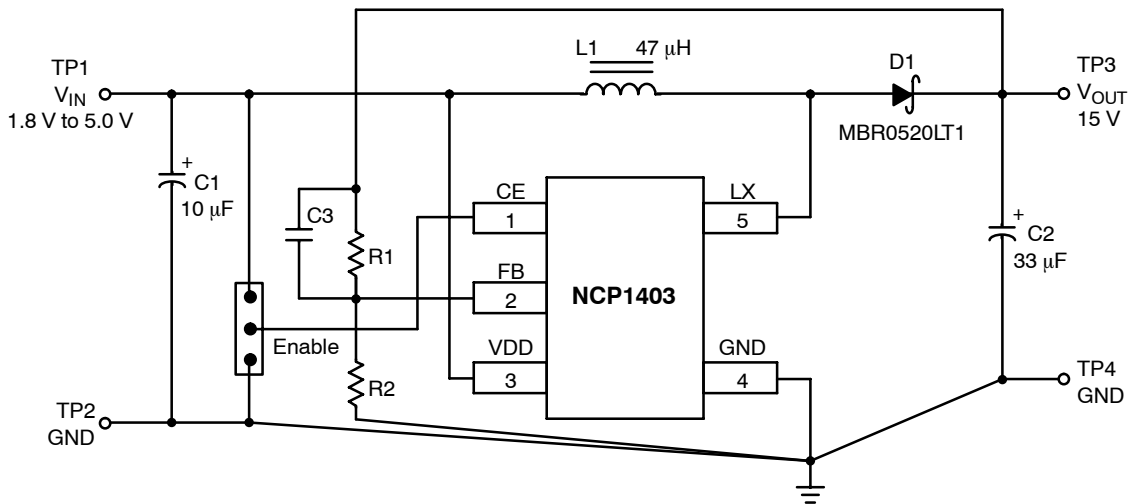


Figure 90. Step-Up Converter Demonstration Board Schematic

NCP1403

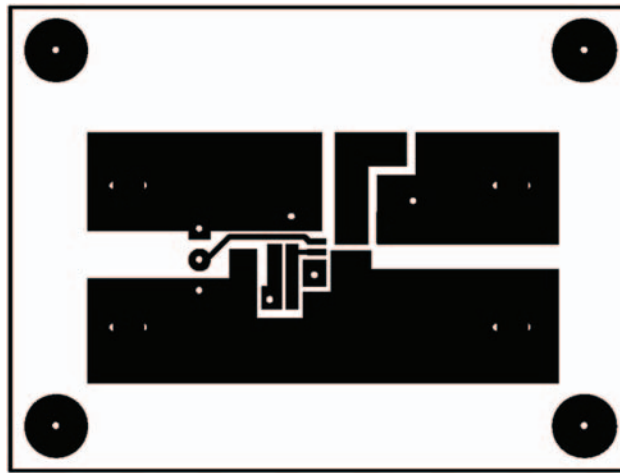


Figure 91. Step-Up Converter Demonstration Board Top Layer Copper

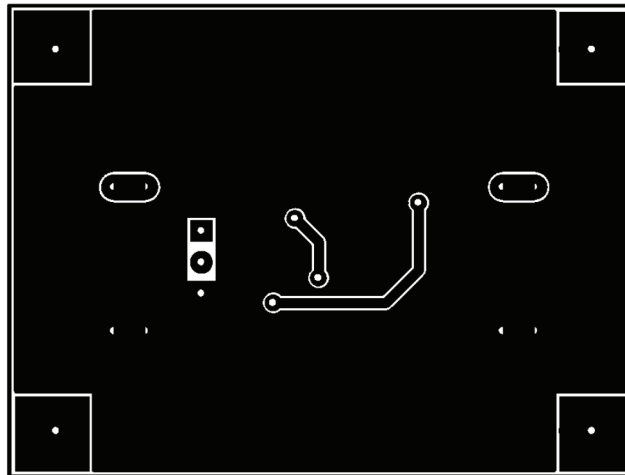


Figure 92. Step-Up Converter Demonstration Board Bottom Layer Copper

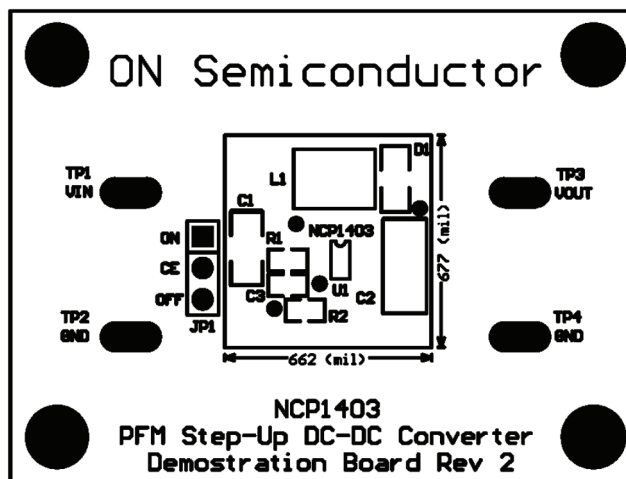


Figure 93. Step-Up Converter Demonstration Board Top Layer Component Silkscreen

NCP1403

Components Supplier

Parts	Supplier	Part Number	Description	Phone
L1	Sumida Electric Co. Ltd.	CD43-470KC	Inductor 47 μ H	(852) 2880-6688
D1	ON Semiconductor	MBR0520LT1	Schottky Power Rectifier	(852) 2689-0088
C1	Kemet Electronics Corp.	T494A106K010AS	Low ESR Tantalum Capacitor 10 μ F/10 V	(852) 2305-1168
C2	Kemet Electronics Corp.	T494C336K016AS	Low ESR Tantalum Capacitor 33 μ F/16 V	(852) 2305-1168

OTHER APPLICATIONS

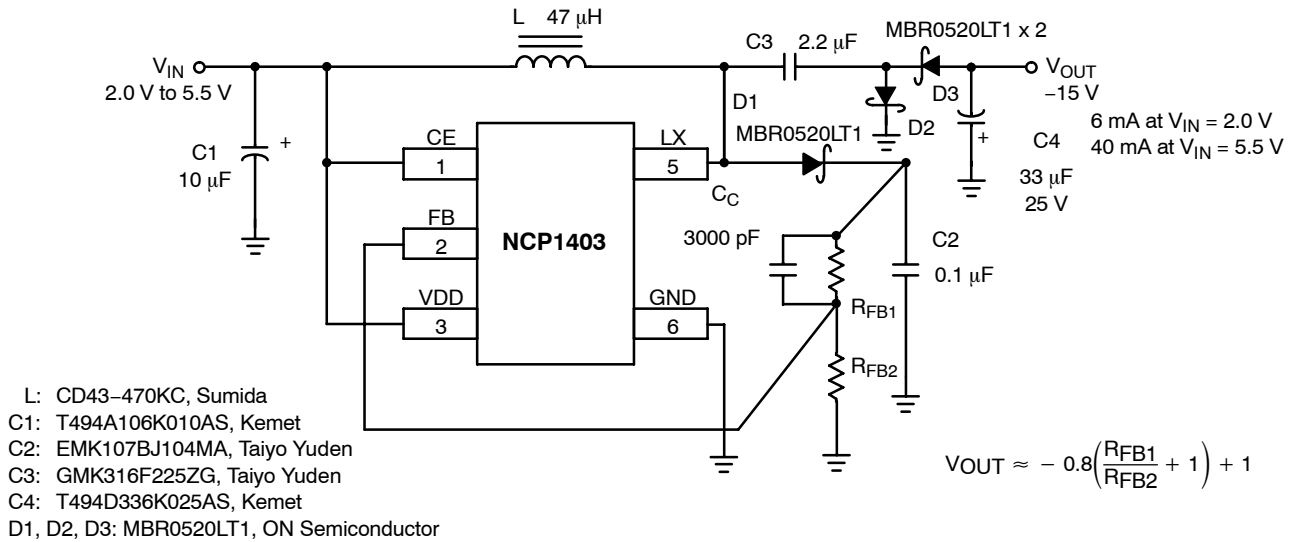


Figure 94. Positive-to-Negative Output Converter for Negative LCD Bias

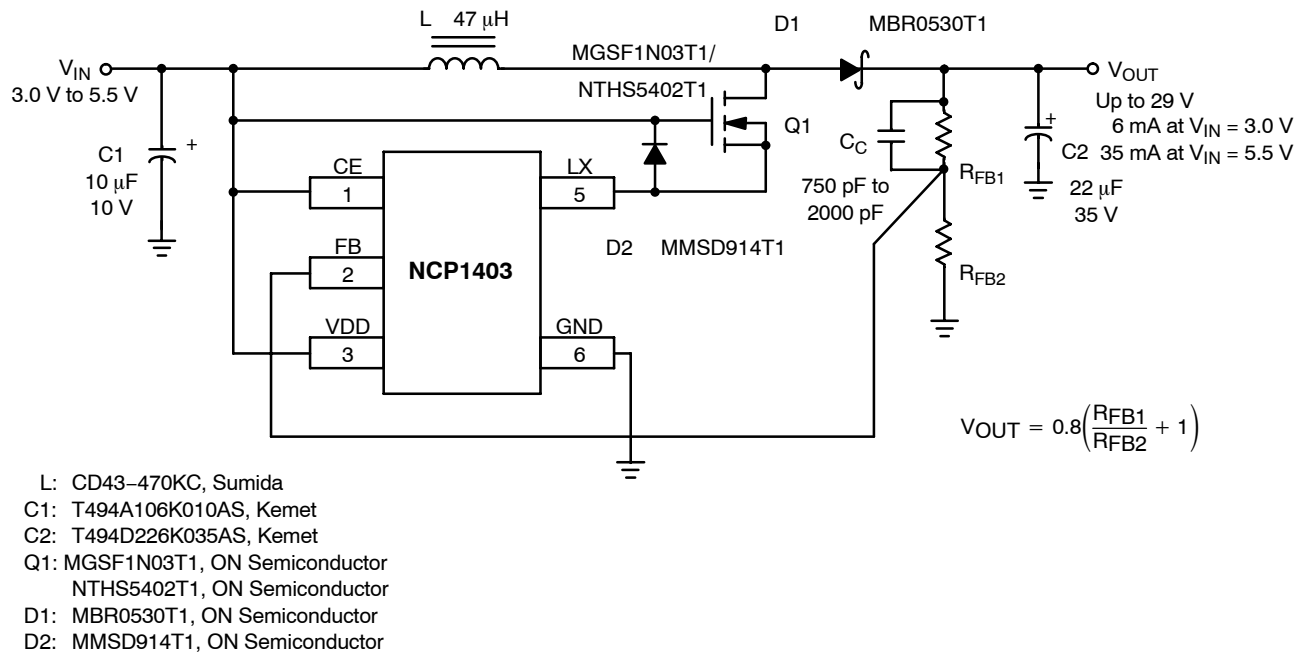


Figure 95. Step-Up DC-DC Converter with 29 V Output Voltage

NCP1403

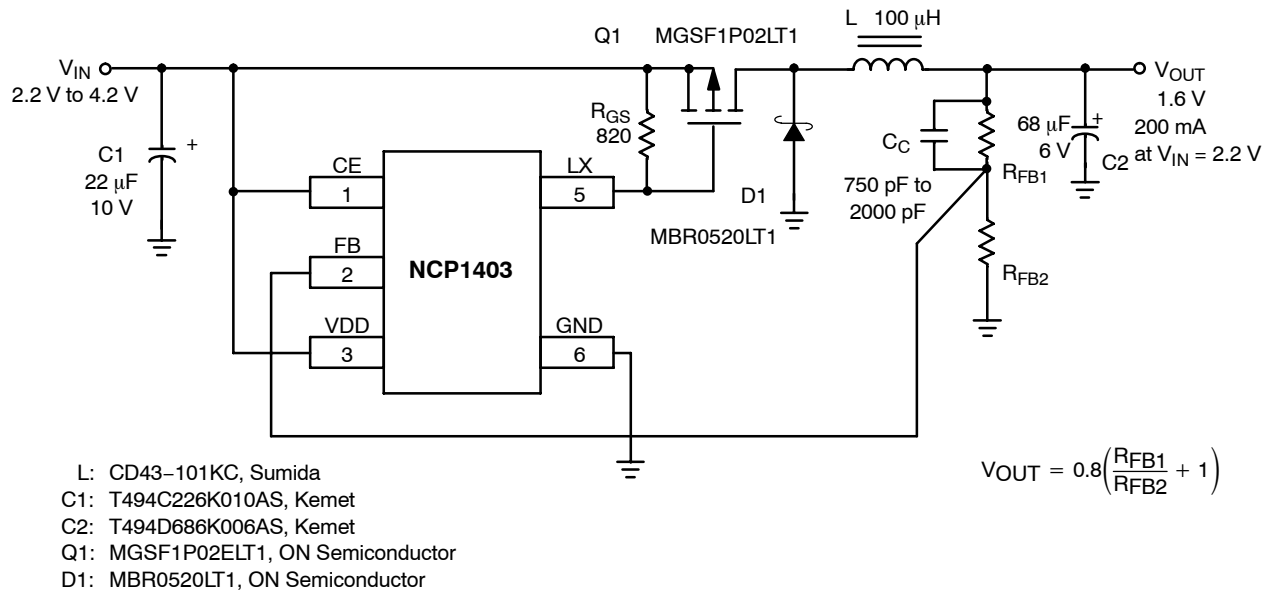


Figure 96. Step-down DC-DC Converter with 1.6 V Output Voltage for DSP Circuit

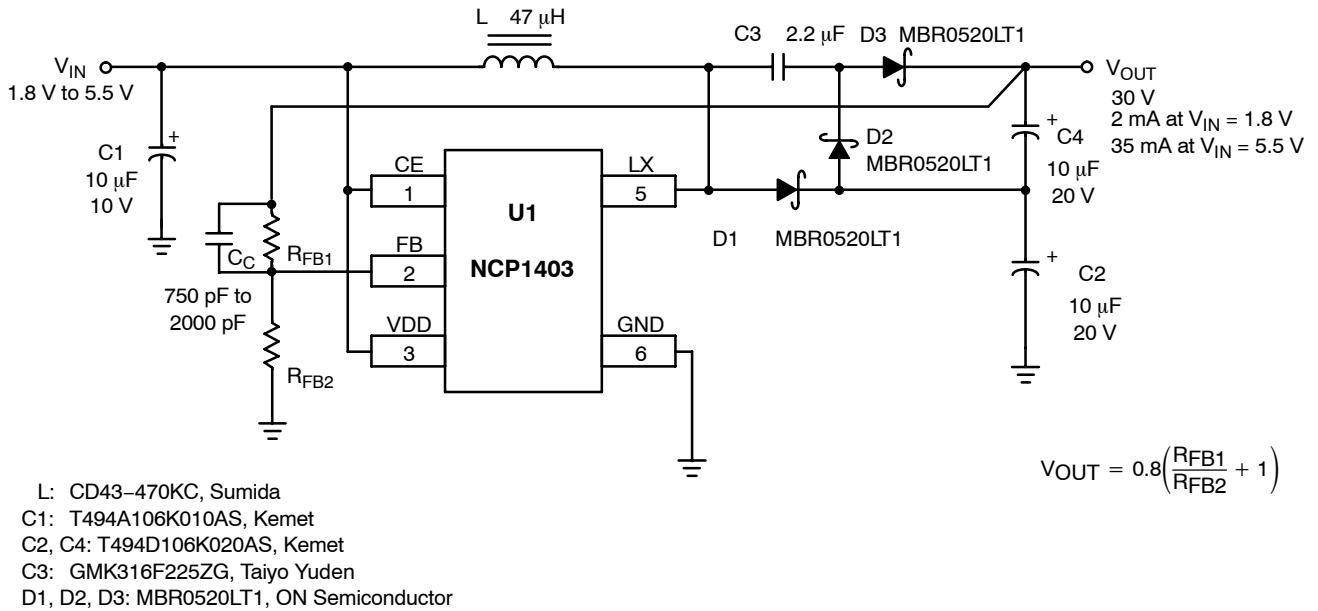
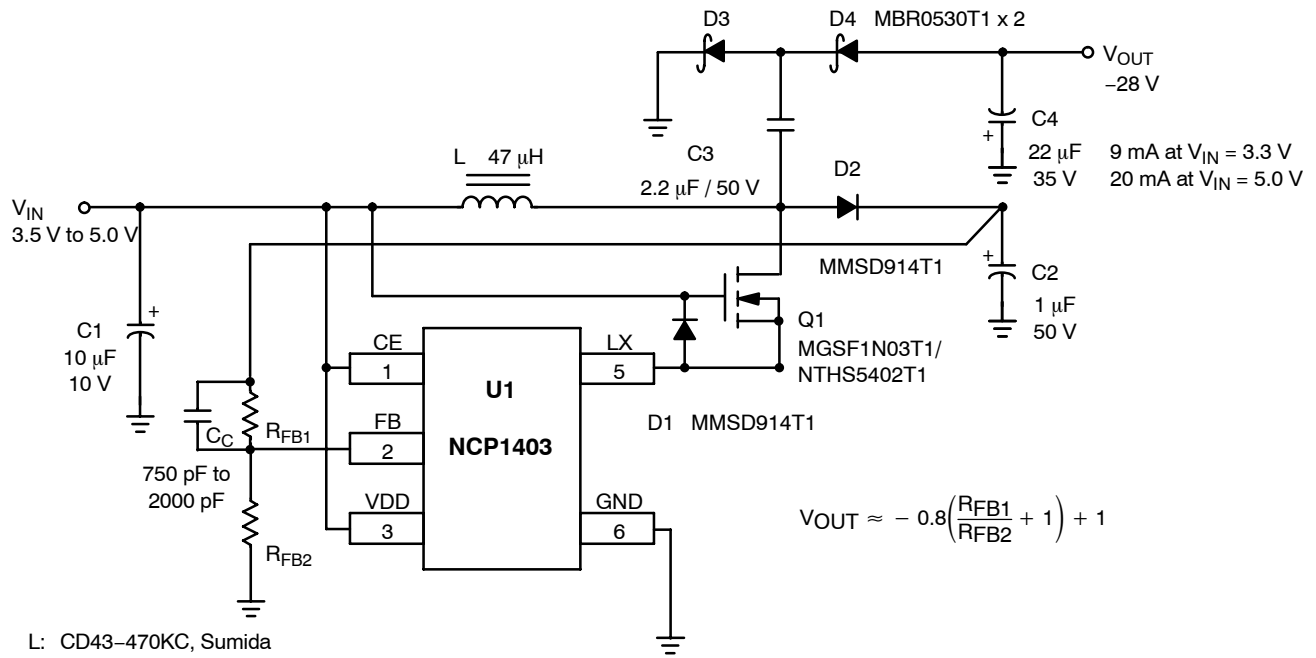


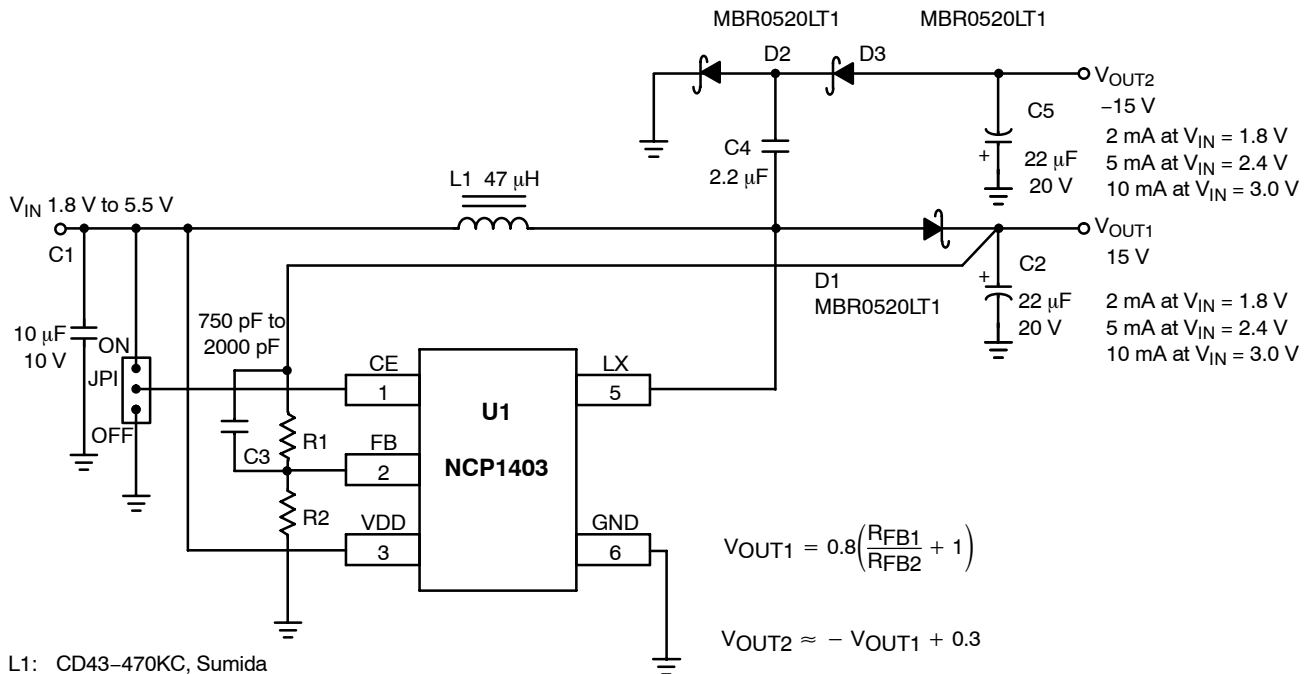
Figure 97. Step-Up DC-DC Converter with 30 V Output Voltage

NCP1403



- L: CD43-470KC, Sumida
 C1: T494A106K010AS, Kemet
 C2: UMK212F105ZG, Taiyo Yuden
 C3: GMK316F225ZG, Taiyo Yuden
 C4: T494D226K035AS, Kemet
 Q1: MGSF1N03T1, ON Semiconductor/
 NTHS5402T1, ON Semiconductor
 D1, D2: MMSD914T1, ON Semiconductor
 D3, D4: MBR0530T1, ON Semiconductor

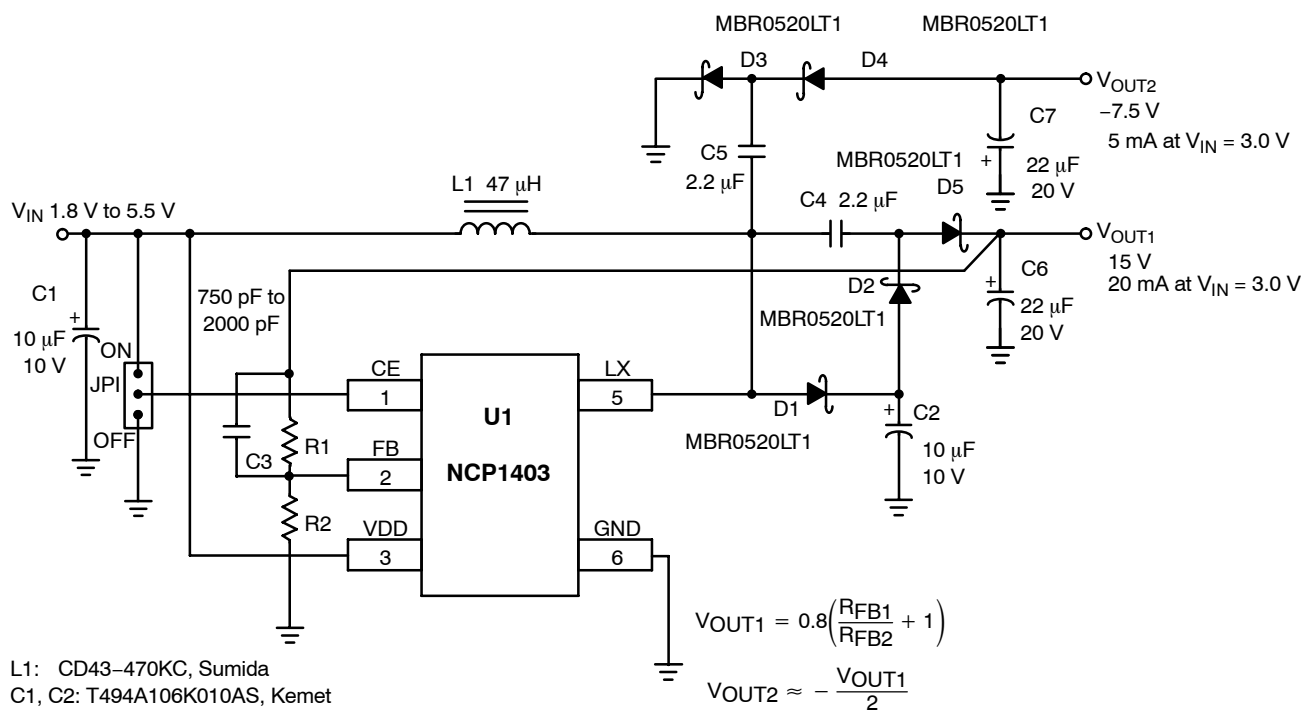
Figure 98. Voltage Inverting DC-DC Converter with -28 V Output Voltage



- L1: CD43-470KC, Sumida
 C1: T494A106K010AS, Kemet
 C2, C5: T494C226K020AS, Kemet
 C3: UMK107B102KZ, Taiyo Yuden
 C4: TMK316BJ225ML, Taiyo Yuden
 D1, D2, D3: MBR0520LT1, ON Semiconductor
 R1: 390 kΩ
 R2: 22 kΩ

Figure 99. +15 V, -15 V Outputs Converter for LCD Bias Supply

NCP1403



- L1: CD43-470KC, Sumida
 C1, C2: T494A106K010AS, Kemet
 C3: UMK107B102KZ, Taiyo Yuden
 C4, C5: TMK316BJ225ML, Taiyo Yuden
 C6, C7: T494C226K020AS, Kemet
 D1, D2, D3, D4, D5: MBR0520LT1, ON Semiconductor
 R1: 390 kΩ
 R2: 22 kΩ

Figure 100. +15 V, -7.5 V Outputs Converter for CCD Supply Circuit

NCP1406

25 V/25 mA PFM Step-Up DC-DC Converter

The NCP1406 is a monolithic PFM step-up DC-DC converter. This device is designed to boost single Lithium or two cells AA/AAA battery voltage up to 25 V (with internal MOSFET) output for handheld applications. A pullup Chip Enable feature is built-in with this device to extend battery-operating life. In addition to standard boost converter topologies, this device can be configured for voltage-inverting and step-down applications. This device is available in space-saving TSOP-5 package. With its small footprint, the device is also ideal for generating a boosted voltage from a 3.3 V or 5.0 V power rail.

Features

- 85% Efficiency at $V_{OUT} = 25\text{ V}$, $I_{OUT} = 25\text{ mA}$, $V_{IN} = 5.0\text{ V}$
- Low Operating Current of 15 μA (Not Switching)
- Low Shutdown Current of 0.3 μA
- Low Startup Voltage of 1.8 V Typical at 0 mA
- Output Voltage up to 25 V with Built-in 26 V MOSFET Switch
- PFM Switching Frequency up to 1.0 MHz
- Chip Enable
- Output Voltage Soft-Start
- Feedback Pin Open/Short Circuit Protection
- Input Undervoltage Lockout
- Thermal Shutdown
- Low Profile and Minimum External Parts
- Micro Miniature TSOP-5 Package
- Pb-Free Package is Available

Typical Applications

- LCD Bias
- White LED Driver
- OLED Driver
- Personal Digital Assistants (PDA)
- Digital Still Camera
- Cellular Telephone
- Hand-Held Games
- Hand-Held Instrument



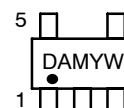
ON Semiconductor®

<http://onsemi.com>



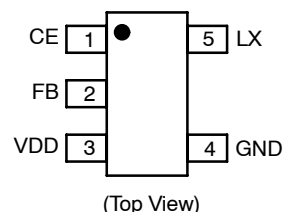
TSOP-5/SOT23-5/SC59-5
SN SUFFIX
CASE 483

MARKING DIAGRAM



DAM = Device Marking
Y = Year
W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP1406SNT1	TSOP-5	3000 Tape & Reel
NCP1406SNT1G	TSOP-5 (Pb-Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NCP1406

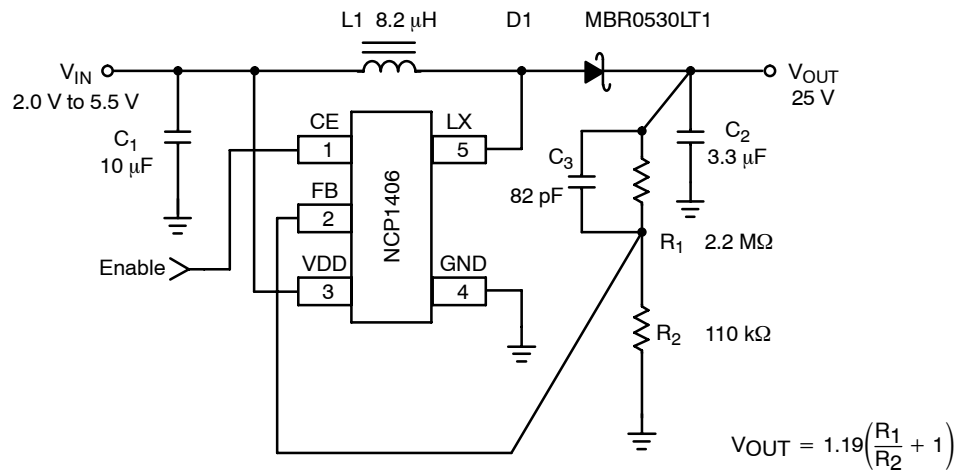


Figure 1. Typical 25 V Step-Up Application Circuit

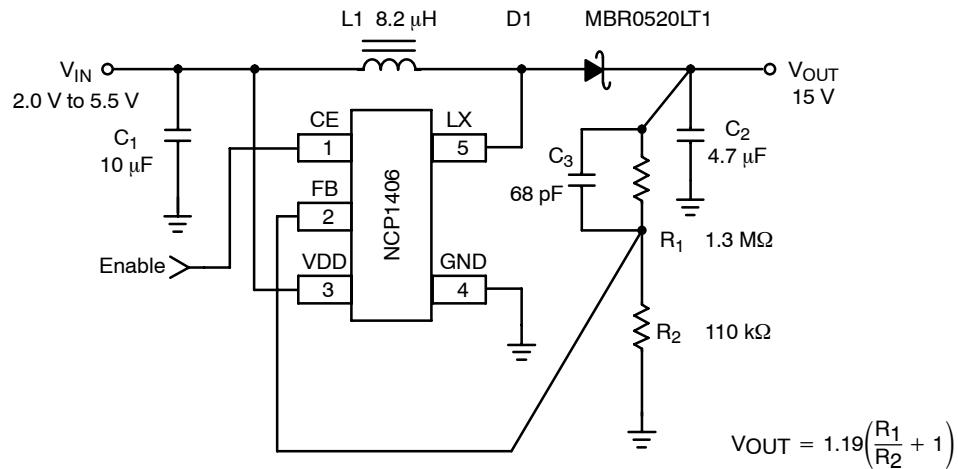


Figure 2. Typical 15 V Step-Up Application Circuit

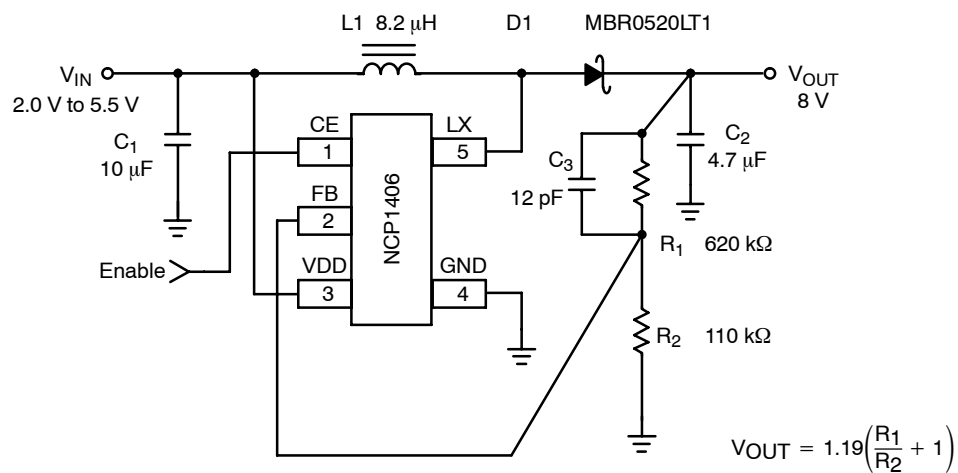


Figure 3. Typical 8.0 V Step-Up Application Circuit

NCP1406

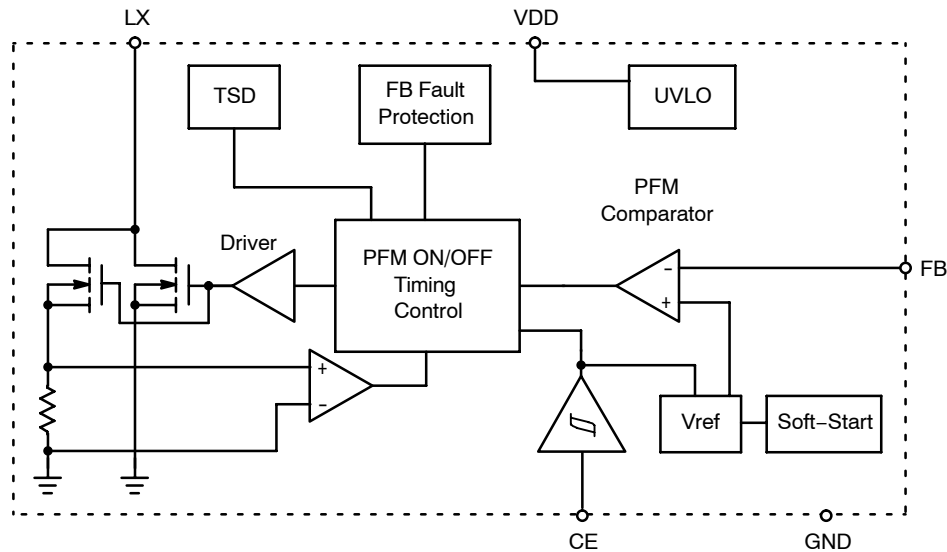


Figure 4. Representative Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	CE	Chip Enable Pin (1) The chip is enabled if a voltage which is equal to or greater than 0.9 V is applied. (2) The chip is disabled if a voltage which is less than 0.3 V is applied. (3) The chip will be enabled if it is left floating.
2	FB	PFM comparator inverting input, and is connected to off-chip resistor divider which sets output voltage.
3	VDD	Power supply pin for internal circuit.
4	GND	Ground pin.
5	LX	External inductor connection pin.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 3)	VDD	-0.3 to 6.0	V
Input/Output Pin LX (Pin 5) LX Peak Sink Current FB (Pin 2)	V_{LX} I_{LX} V_{FB}	-0.3 to 27 1.5 -0.3 to 6.0	V A V
CE (Pin 1) Input Voltage Range	V_{CE}	-0.3 to 6.0	V
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$ Thermal Resistance, Junction-to-Air	P_D $R_{\theta JA}$	500 250	mW $^\circ\text{C/W}$
Operating Ambient Temperature Range	T_A	-40 to +85	$^\circ\text{C}$
Operating Junction Temperature Range	T_J	-40 to +150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

11. This device series contains ESD protection and exceeds the following tests:

Human Body Model (HBM) ± 2.0 kV per JEDEC standard: JESD22-A114 for all pins.

Machine Model (MM) ± 200 V per JEDEC standard: JESD22-A115 for all pins.

12. Latchup Current Maximum Rating: ± 150 mA per JEDEC standard: JESD78.

13. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.

NCP1406

DISSIPATION RATINGS

Package	Power Rating @T _A ≤ 25°C	Derating Factor @T _A > 25°C	Power Rating @T _A = 70°C	Power Rating @T _A = 85°C
TSOP-5	500 mW	4.0 mW/°C	320 mW	260 mW

ELECTRICAL CHARACTERISTICS (V_{OUT} = 25 V, T_A = -40°C to +85°C for min/max values, typical values are at T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit

ON/OFF TIMING CONTROL

Minimum Off Time (V _{DD} = 3.0 V, V _{FB} = 0 V)	t _{off}	0.08	0.13	0.20	μs
Maximum On Time (Current Not Asserted)	t _{on}	0.58	0.90	1.40	μs
Maximum Duty Cycle	D _{MAX}	84	90	96	%
Minimum Startup Voltage (I _{OUT} = 0 mA)	V _{start}	–	1.8	2.0	V
Minimum Startup Voltage Temperature Coefficient (T _A = -40 to +85°C)	ΔV _{start}	–	1.6	–	mV/°C
Minimum Hold Voltage (I _{OUT} = 0 mA)	V _{hold}	–	1.7	1.9	V
Soft-Start Time	t _{SS}	–	3.0	8.0	ms

LX (PIN 5)

Internal Switch Voltage (Note 14) (Note 15)	V _{LX}	–	–	26	V
LX Pin On-State Resistance (V _{LX} = 0.4 V, V _{DD} = 5.0 V)	R _{sw(on)}	–	0.7	–	Ω
Current Limit (When I _{LX} reaches I _{LIM} , the LX switch is turned off by the LX switch protection circuit) (Note 15)	I _{LIM}	–	0.80	–	A
Off-State Leakage Current (V _{LX} = 26 V)	I _{LKG}	–	0.1	1.0	μA

CE (PIN 1)

CE Input Voltage (V _{DD} = 3.0 V, V _{FB} = 0 V) High State, Device Enabled Low State, Device Disabled	V _{CE(high)} V _{CE(low)}	0.9 –	– –	– 0.3	V V
CE Input Current High State, Device Enabled (V _{DD} = V _{CE} = 5.5 V) Low State, Device Disabled (V _{DD} = 5.5 V, V _{CE} = V _{FB} = 0 V)	I _{CE(high)} I _{CE(low)}	– –500	10 –150	500 –	nA nA

TOTAL DEVICE

Supply Voltage	V _{DD}	1.4	–	5.5	V
Undervoltage Lockout (V _{DD} Falling)	V _{UVLO}	–	1.0	1.3	V
Feedback Voltage T _A = 25°C T _A = -40 to +85°C	V _{FB}	1.178 1.170	1.190 1.190	1.202 1.210	V
Feedback Pin Bias Current (V _{FB} = 1.19 V)	I _{FB}	–	15	45	nA
Operating Current 1 (V _{FB} = 0 V, V _{DD} = V _{CE} = 3.0 V, Maximum Duty Cycle)	I _{DD1}	–	0.7	1.5	mA
Operating Current 2 (V _{DD} = V _{CE} = V _{FB} = 3.0 V, Not Switching)	I _{DD2}	–	15	25	μA
Off-State Current (V _{DD} = 5.0 V, V _{CE} = 0 V)	I _{OFF}	–	0.3	1.3	μA
Thermal Shutdown (Note 15)	T _{SD}	–	140	–	°C
Thermal Shutdown Hysteresis (Note 15)	T _{SDHYS}	–	10	–	°C

14. Recommended maximum V_{OUT} up to 25 V.

15. Guaranteed by design, not tested.

TYPICAL CHARACTERISTICS

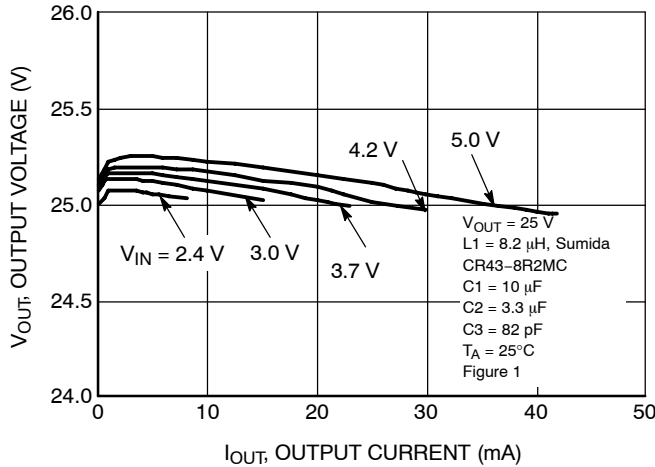


Figure 5. Output Voltage versus Output Current
($V_{OUT} = 25\text{ V}$, $L = 8.2\text{ }\mu\text{H}$)

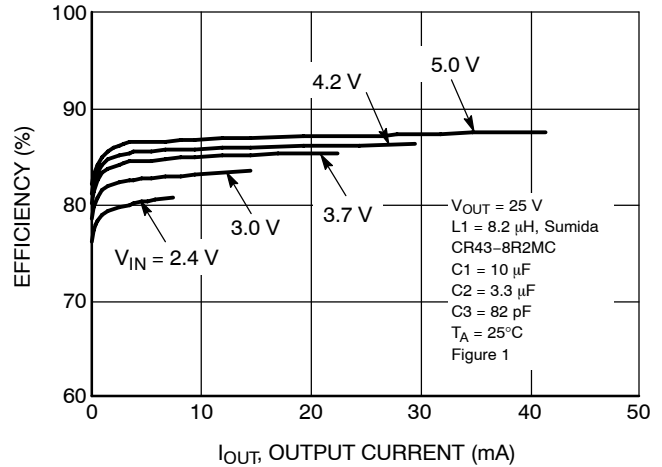


Figure 6. Efficiency versus Output Current
($V_{OUT} = 25\text{ V}$, $L = 8.2\text{ }\mu\text{H}$)

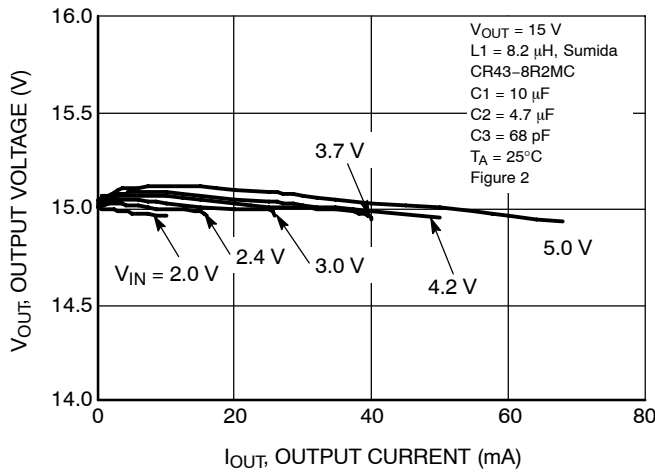


Figure 7. Output Voltage versus Output Current
($V_{OUT} = 15\text{ V}$, $L = 8.2\text{ }\mu\text{H}$)

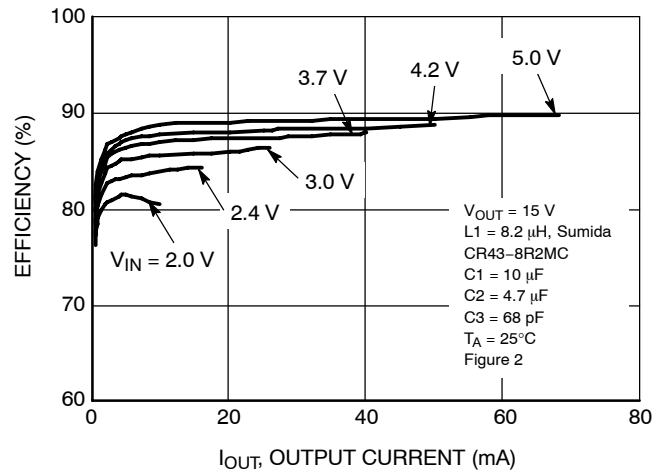


Figure 8. Efficiency versus Output Current
($V_{OUT} = 15\text{ V}$, $L = 8.2\text{ }\mu\text{H}$)

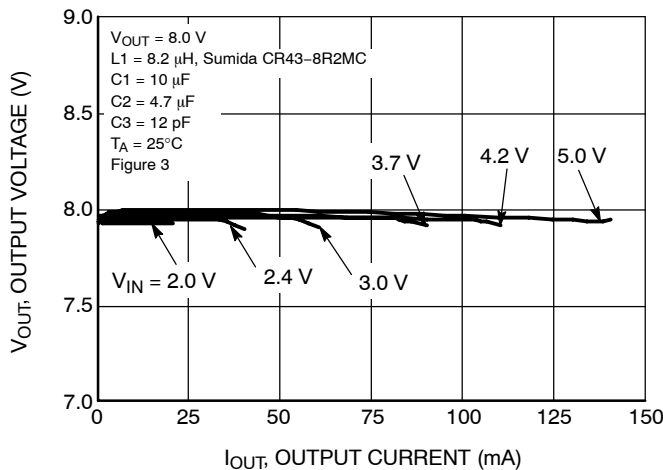


Figure 9. Output Voltage versus Output Current
($V_{OUT} = 8.0\text{ V}$, $L = 8.2\text{ }\mu\text{H}$)

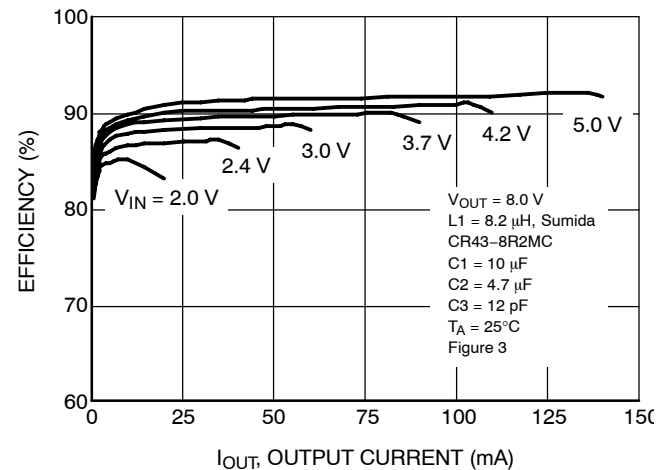


Figure 10. Efficiency versus Output Current
($V_{OUT} = 8.0\text{ V}$, $L = 8.2\text{ }\mu\text{H}$)

TYPICAL CHARACTERISTICS

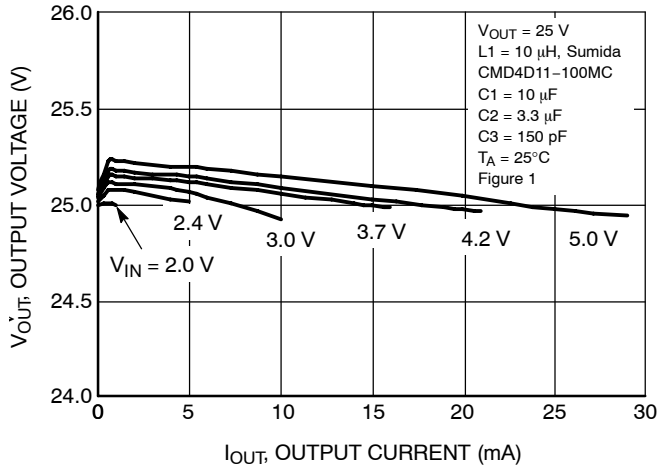


Figure 11. Output Voltage versus Output Current
 ($V_{OUT} = 25\text{ V}$, $L = 10\text{ }\mu\text{H}$)

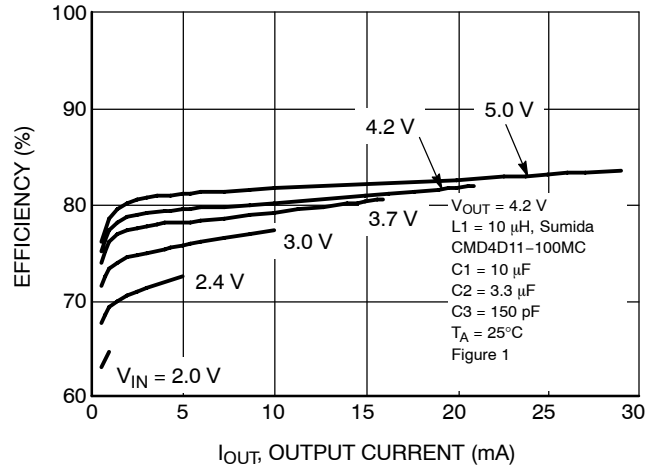


Figure 12. Efficiency versus Output Current
 ($V_{OUT} = 25\text{ V}$, $L = 10\text{ }\mu\text{H}$)

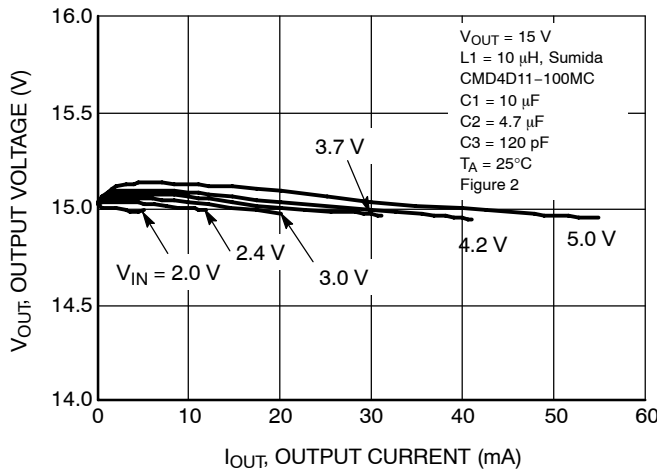


Figure 13. Output Voltage versus Output Current
 ($V_{OUT} = 15\text{ V}$, $L = 10\text{ }\mu\text{H}$)

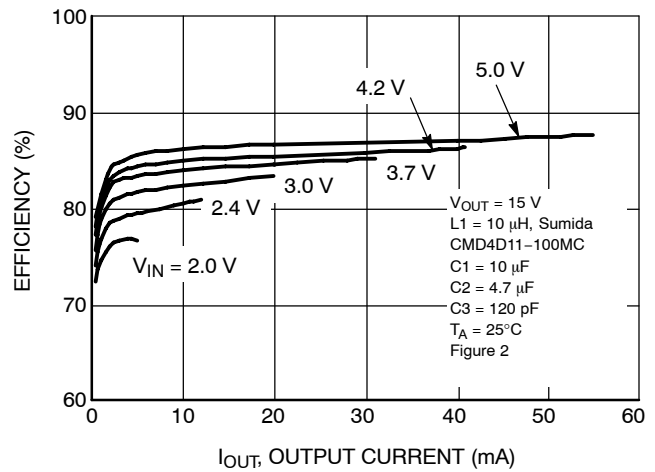


Figure 14. Efficiency versus Output Current
 ($V_{OUT} = 15\text{ V}$, $L = 10\text{ }\mu\text{H}$)

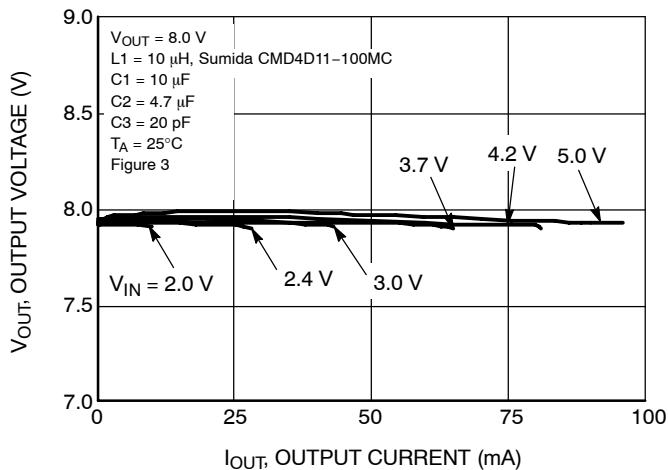


Figure 15. Output Voltage versus Output Current
 ($V_{OUT} = 8.0\text{ V}$, $L = 10\text{ }\mu\text{H}$)

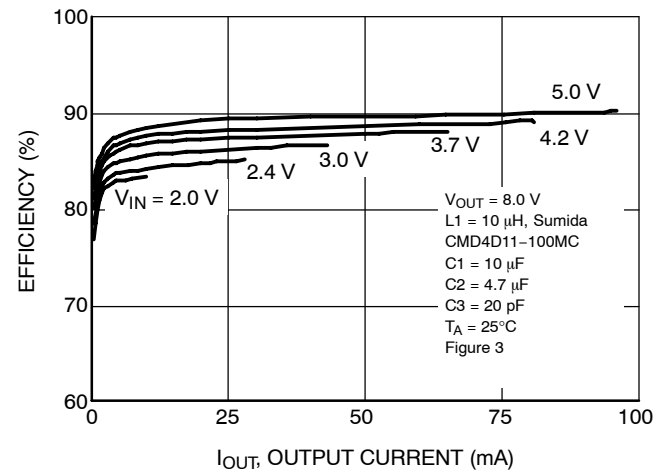


Figure 16. Efficiency versus Output Current
 ($V_{OUT} = 8.0\text{ V}$, $L = 10\text{ }\mu\text{H}$)

TYPICAL CHARACTERISTICS

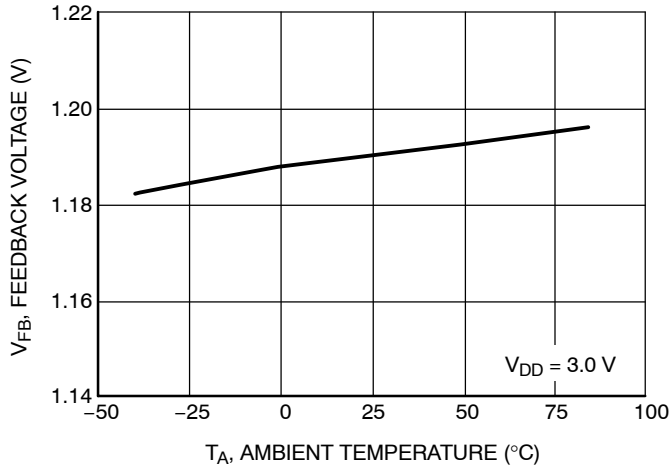


Figure 17. Feedback Voltage versus Ambient Temperature

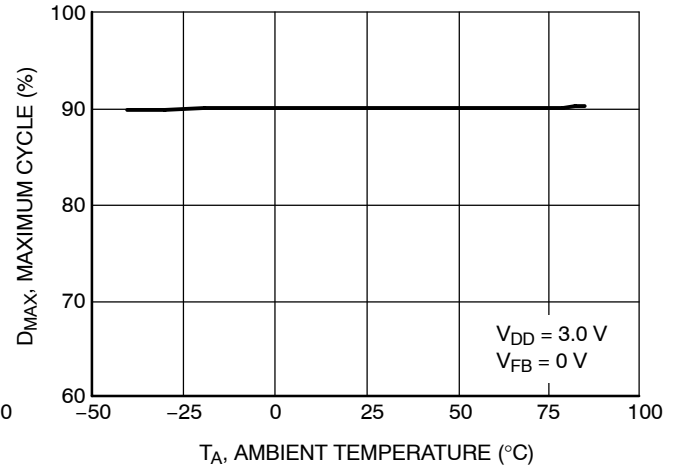


Figure 18. Maximum Duty Cycle versus Ambient Temperature

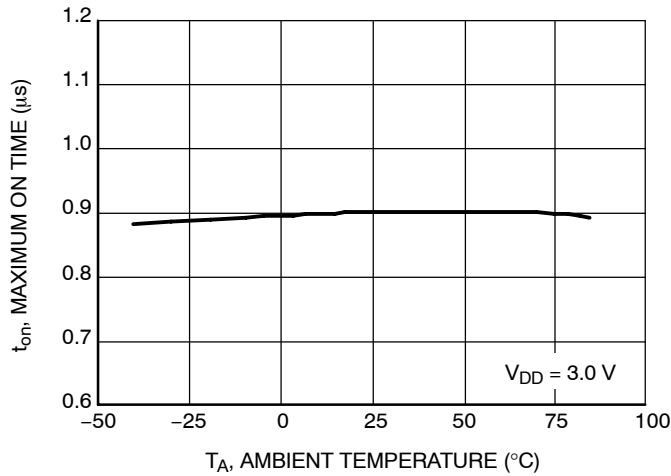


Figure 19. Maximum On Time versus Ambient Temperature

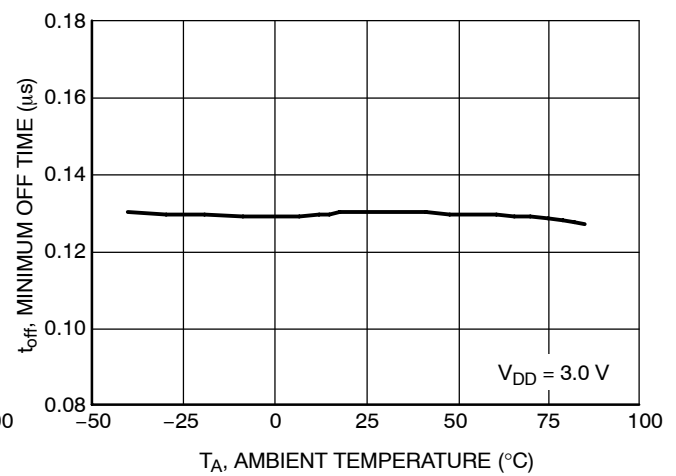


Figure 20. Minimum Off Time versus Ambient Temperature

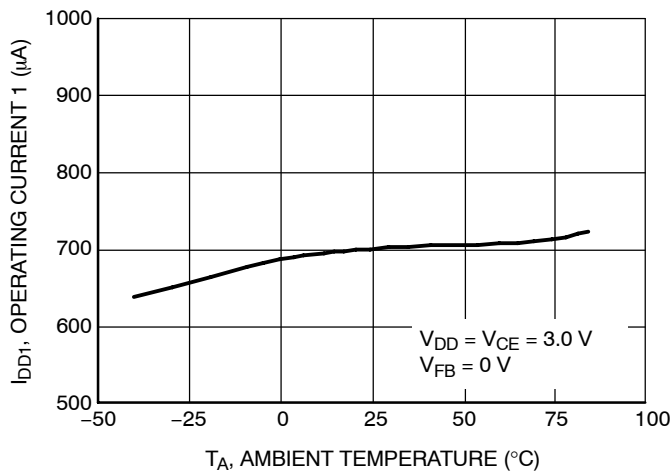


Figure 21. Operating Current 1 versus Ambient Temperature

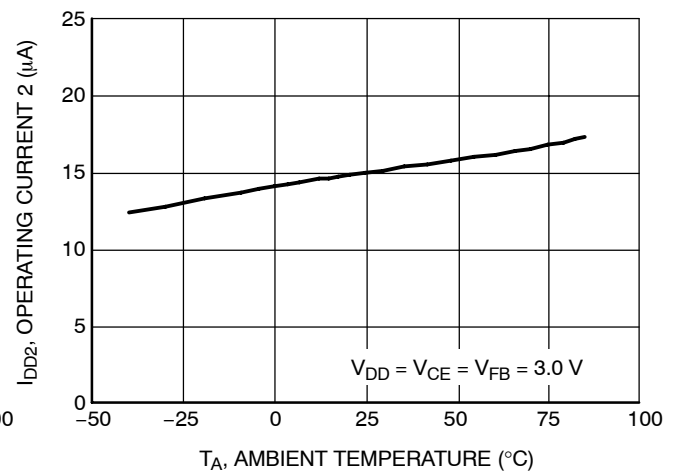


Figure 22. Operating Current 2 versus Ambient Temperature

TYPICAL CHARACTERISTICS

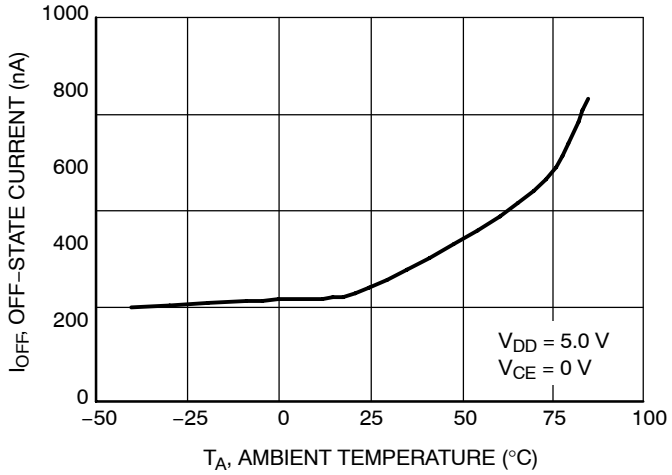


Figure 23. Off-State Current versus Ambient Temperature

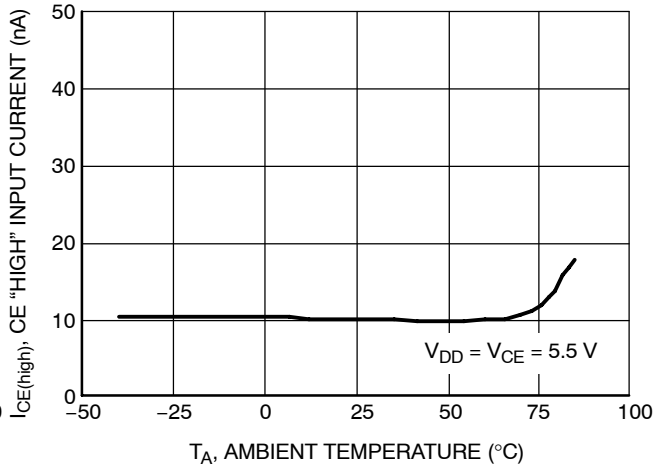


Figure 24. CE "High" Input Current versus Ambient Temperature

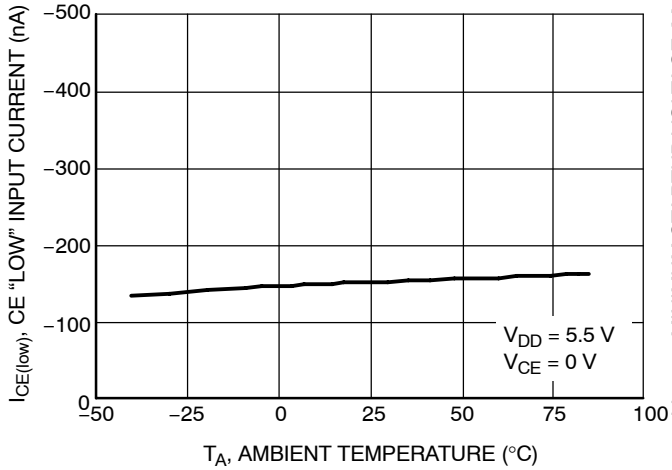


Figure 25. CE "Low" Input Current versus Ambient Temperature

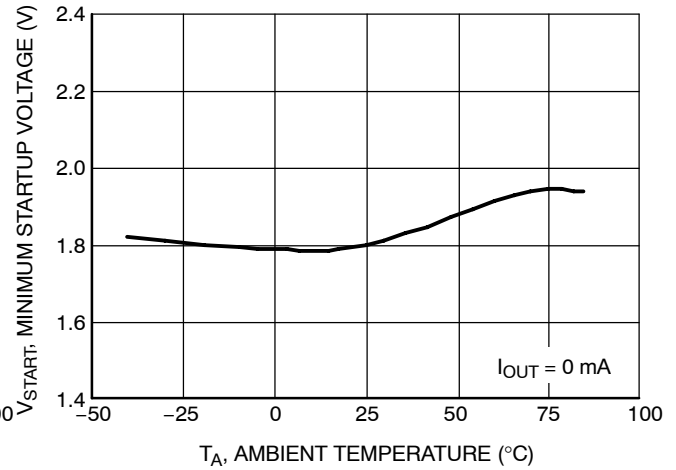


Figure 26. Minimum Startup Voltage versus Ambient Temperature

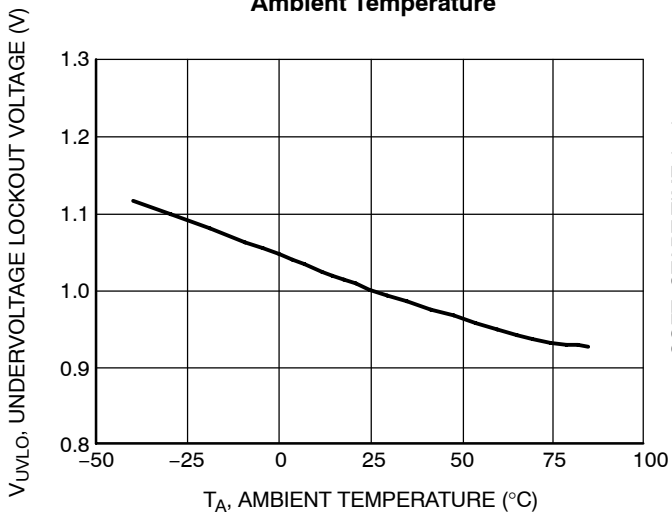


Figure 27. Undervoltage Lockout Voltage versus Ambient Temperature

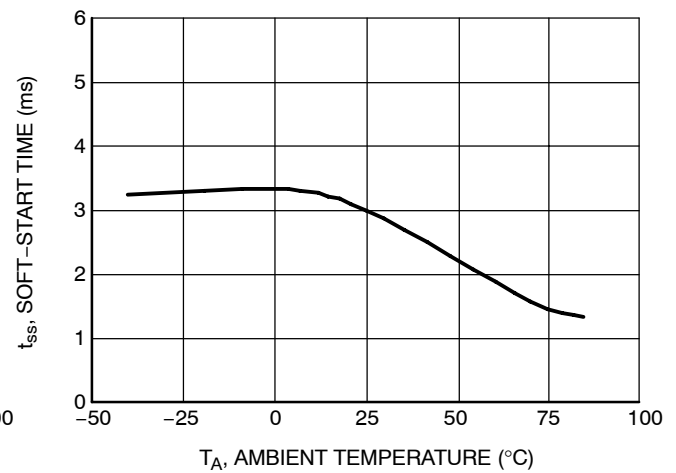


Figure 28. Soft-start Time versus Ambient Temperature

TYPICAL CHARACTERISTICS

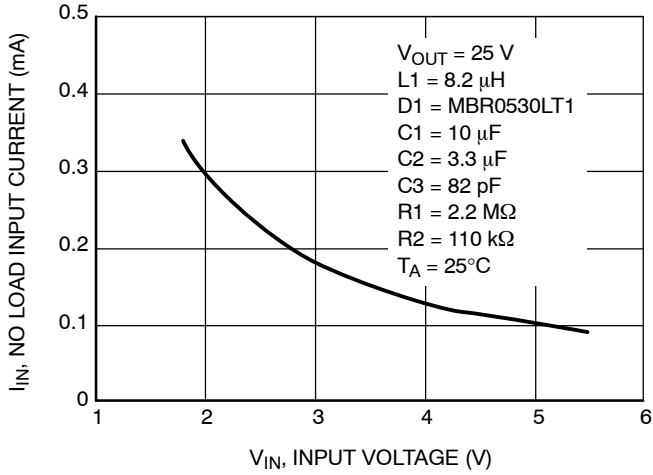


Figure 29. No Load Input Current versus Input Voltage

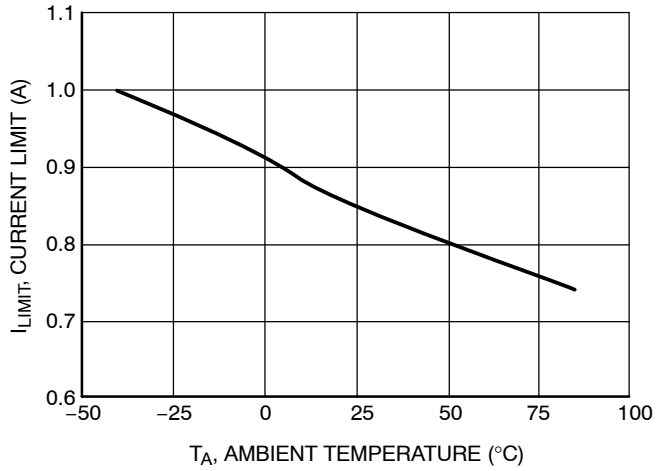


Figure 30. Current Limit versus Ambient Temperature

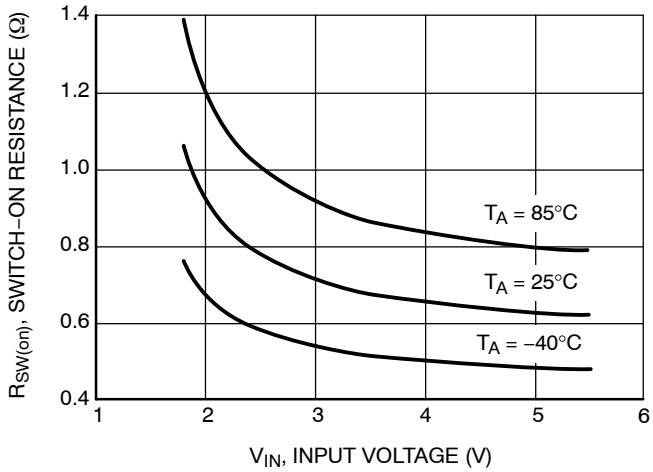


Figure 31. Switch-ON Resistance versus Input Voltage

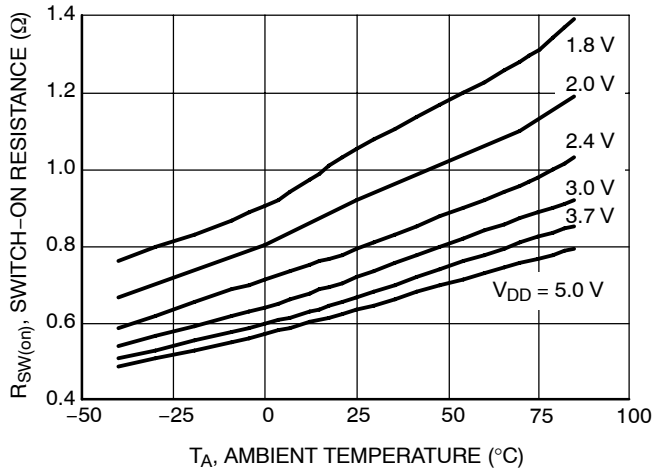


Figure 32. Switch-ON Resistance versus Ambient Temperature

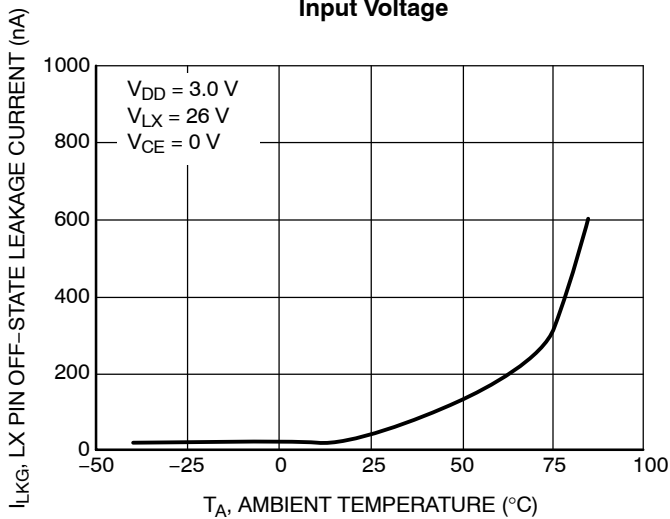


Figure 33. LX Pin Off-State Leakage Current versus Ambient Temperature

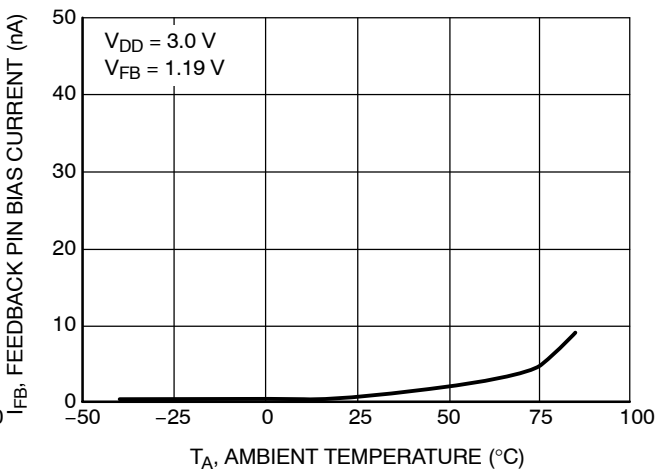
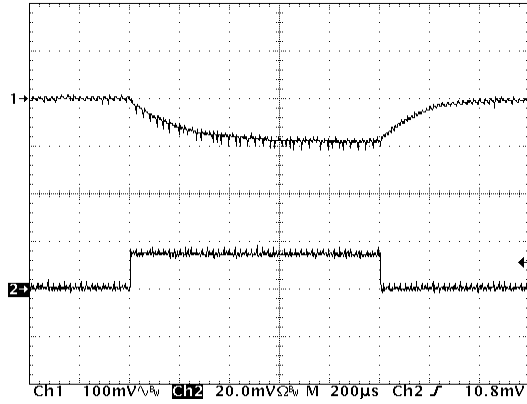
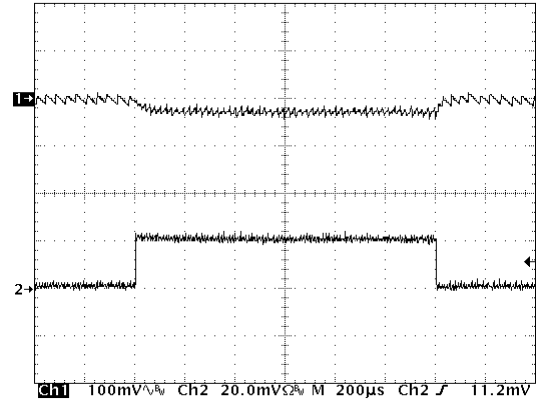


Figure 34. Feedback Pin Bias Current versus Ambient Temperature

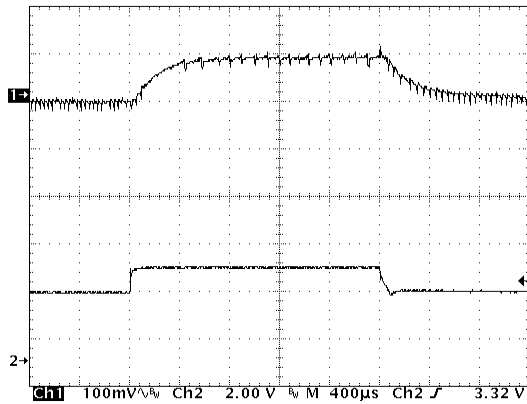
TYPICAL CHARACTERISTICS



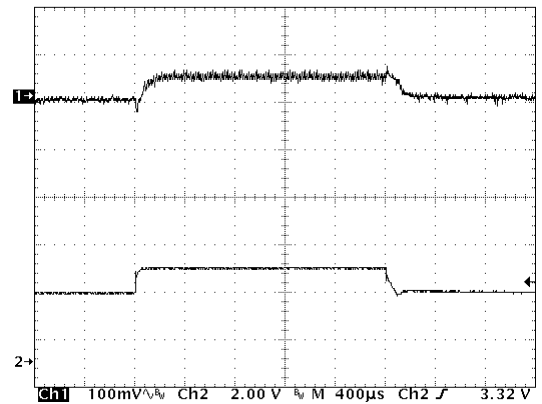
L1 = 8.2 μ H, C1 = 10 μ F, C2 = 3.3 μ F, V_{IN} = 3.7 V
 1. V_{OUT} = 25 V (AC Coupled), 100 mV/div
 2. I_{OUT} = 1.0 mA to 15 mA, 20 mA/div

Figure 35. Load Transient Response (V_{OUT} = 25 V)

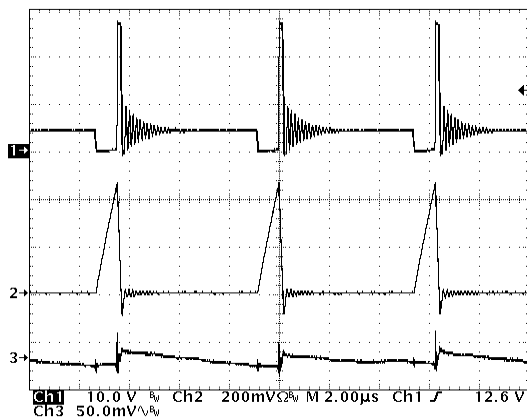
L1 = 8.2 μ H, C1 = 10 μ F, C2 = 4.7 μ F, V_{IN} = 3.7 V
 1. V_{OUT} = 15 V (AC Coupled), 100 mV/div
 2. I_{OUT} = 1.0 mA to 20 mA, 20 mA/div

Figure 36. Load Transient Response (V_{OUT} = 15 V)

L1 = 8.2 μ H, C1 = 10 μ F, C2 = 3.3 μ F, I_{OUT} = 15 mA
 1. V_{OUT} = 25 V (AC Coupled), 100 mV/div
 2. V_{IN} = 3.0 V to 4.0 V, 2.0 V/div

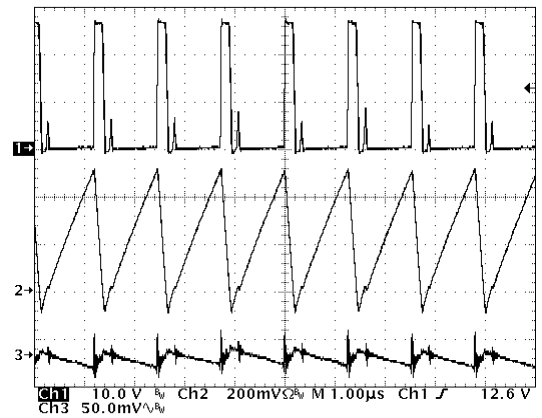
Figure 37. Line Transient Response (V_{OUT} = 25 V)

L1 = 8.2 μ H, C1 = 10 μ F, C2 = 4.7 μ F, I_{OUT} = 15 mA
 1. V_{OUT} = 15 V (AC Coupled), 100 mV/div
 2. V_{IN} = 3.0 V to 4.0 V, 2.0 V/div

Figure 38. Line Transient Response (V_{OUT} = 15 V)

L1 = 8.2 μ H, C1 = 10 μ F, C2 = 3.3 μ F, V_{IN} = 4.2 V,
 V_{OUT} = 25 V, I_{OUT} = 5.0 mA
 1. V_{LX} , 10 V/div
 2. I_L , 200 mA/div
 3. V_{ripple} , 50 mV/div

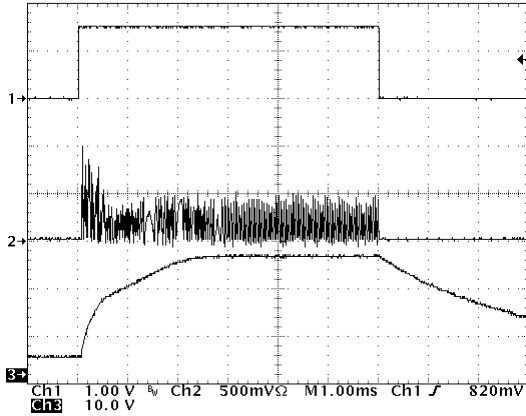
Figure 39. Operating Waveforms (Light Load)



L1 = 8.2 μ H, C1 = 10 μ F, C2 = 3.3 μ F, V_{IN} = 4.2 V,
 V_{OUT} = 25 V, I_{OUT} = 30 mA
 1. V_{LX} , 10 V/div
 2. I_L , 200 mA/div
 3. V_{ripple} , 50 mV/div

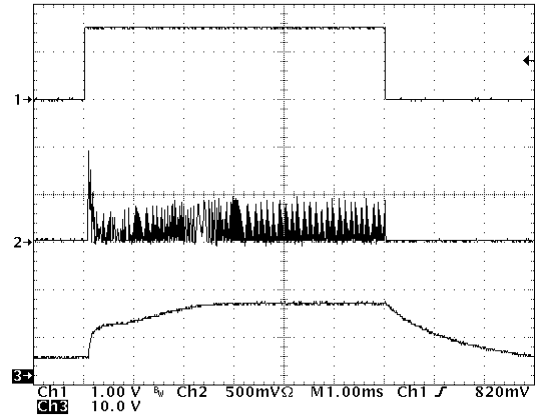
Figure 40. Operating Waveforms (Heavy Load)

TYPICAL CHARACTERISTICS



L1 = 8.2 μ H, C1 = 10 μ F, C2 = 3.3 μ F, V_{IN} = 4.2 V,
 I_{OUT} = 20 mA
 1. V_{CE} , 0 V to 1.0 V to 0 V, 1.0 V/div
 2. I_L , 500 mA/div
 3. V_{OUT} , 10 mV/div

Figure 41. Startup/Shutdown Waveforms
 (V_{OUT} = 25 V)



L1 = 8.2 μ H, C1 = 10 μ F, C2 = 4.7 μ F, V_{IN} = 4.2 V,
 I_{OUT} = 25 mA
 1. V_{CE} , 0 V to 1.0 V to 0 V, 1.0 V/div
 2. I_L , 500 mA/div
 3. V_{OUT} , 10 mV/div

Figure 42. Startup/Shutdown Waveforms
 (V_{OUT} = 15 V)

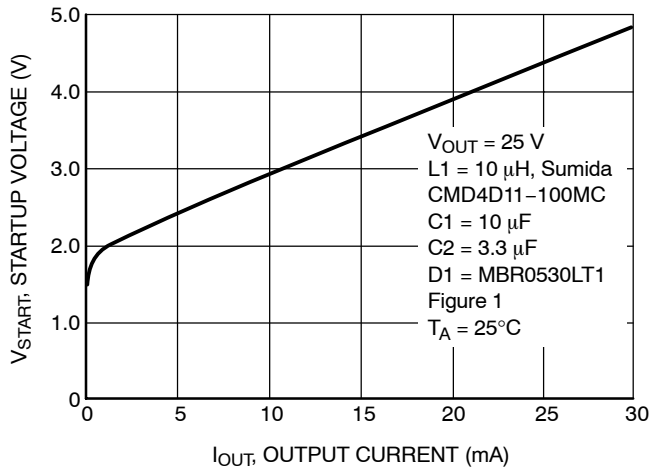


Figure 43. Startup Voltage versus Input Voltage
 (V_{OUT} = 25 V)

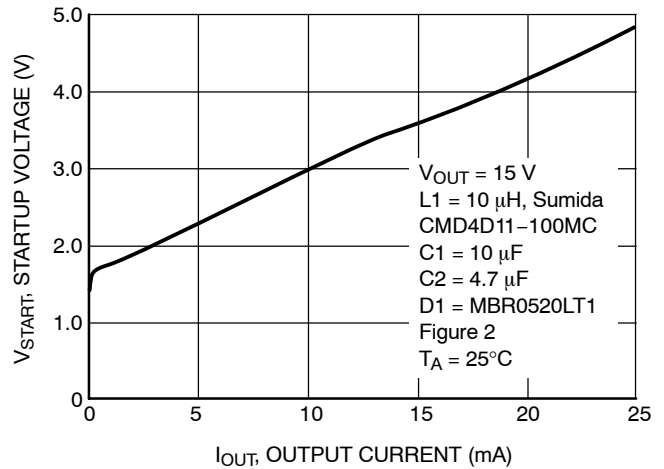


Figure 44. Startup Voltage versus Input Voltage
 (V_{OUT} = 15 V)

DETAILED OPERATING DESCRIPTION

Operation

The NCP1406 is a monolithic DC–DC switching converter optimized for single Lithium or two cells AA/AAA size batteries powered portable products.

The NCP1406 device consists of soft–start circuit, chip enable circuit, PFM comparator, voltage reference, PFM on/off timing control circuit, driver, current limit circuit, open–drain MOSFET switch, input voltage UVLO, thermal shutdown, and feedback pin short–circuit/open–circuit protection. The device operating current is typically 15 μA , and can be further reduced to about 0.3 μA when the chip is disabled ($V_{\text{CE}} < 0.3 \text{ V}$).

The operation of NCP1406 can be best understood by referring to the block diagram and typical application circuit in Figures 1 and 4. The PFM comparator monitors the output voltage via the external feedback resistor divider by comparing the feedback voltage with the reference voltage. When the feedback voltage is lower than the reference voltage, the PFM control and driver circuit turns on the N–Channel MOSFET switch and the current ramps up in the inductor. The switch will remain on for the maximum on–time, 0.90 μs , or until the current limit is reached, whichever occurs first. The MOSFET switch is then turned off and energy stored in the inductor will be discharged to the output capacitor and load through the Schottky diode. The MOSFET switch will be turned off for at least the minimum off–time, 0.13 μs , and will remain off if the feedback voltage is higher than the reference voltage and output capacitor will be discharged to sustain the output current, until the feedback voltage is again lower than reference voltage. This switching cycle is then repeated to attain voltage regulation.

Soft–Start

There is a soft–start circuit in NCP1406. When power is applied to the device, the soft–start circuit limits the device to switch at a small duty cycle initially, the duty cycle is then increased gradually until the output voltage is in regulation. With the soft–start circuit, the output voltage over–shoot is minimized and the startup capability with heavy loads is also improved.

ON/OFF Timing Control

The maximum on–time is typically 0.90 μs , whereas, the minimum off–time is typically 0.13 μs . The switching frequency can be up to 1.0 MHz.

Voltage Reference and Output Voltage

The internal bandgap voltage reference is trimmed to 1.19 V at an accuracy of $\pm 1.0\%$ at 25°C. The voltage reference is connected to the non–inverting input of the PFM comparator and the inverting input of the PFM comparator is connected to the FB pin. The output voltage can be set by connected an external resistor voltage divider from the V_{OUT} to the FB pin. With the internal 26 V MOSFET switch, the output voltage can be set between V_{IN} to 25 V.

Current Limit

The current limit circuit limits the maximum current flowing through the LX pin to typical 0.80 A during the MOSFET switch turn–on period. When the current limit is exceeded, the switch will be turned off. With the current limit circuit, the peak inductor current is limited to the current limit, saturation of inductor is prevented and output voltage over–shoot during startup can also be minimized.

N–Channel MOSFET Switch

The NCP1406 is built–in with a 26 V open drain N–Channel MOSFET switch which allows high output voltage up to 25 V to be generated from simple step–up topology.

Input Voltage Undervoltage Lockout

There is an undervoltage lockout circuit continuously monitoring the voltage at the VDD pin. The device will be disabled if the VDD pin voltage drops below the UVLO threshold voltage.

FB Pin Short–Circuit/Open–Circuit Protection

With the FB protection circuit, the drain–to–source leakage current of the N–Ch MOSFET is sensed. When the FB pin connection is shorted or opened, the converter switches at maximum duty cycle, the peak of V_{LX} and the V_{OUT} will build up, and the leakage current will increase. When the leakage current increases to a certain level, the converter will stop switching with the protection circuit. Therefore, the peak of V_{LX} will stop increasing at a certain level before the N–Ch MOSFET is damaged immediately. However, the sensing of the leakage current is not very accurate and cannot be too close to the normal 26 V maximum operating condition. Therefore, the V_{LX} is around 30 V to 40 V during a FB pin protection fault.

Thermal Shutdown

When the chip junction temperature exceeds 140°C, the entire IC is shutdown. The IC will resume operation when the junction temperature drops below 130°C.

Enable/Disable Operation

The NCP1406 offers IC shutdown mode by the chip enable pin (CE pin) to reduce current consumption. An internal 150 nA pullup current source ties the CE pin to the VDD pin by default. Therefore, the user can float the CE pin for permanent “ON”. When the voltage at the CE pin is equal to or greater than 0.9 V, the chip will be enabled, which means the device is in normal operation. When the voltage at the CE pin is less than 0.3 V, the chip is disabled, which means IC is shutdown. During shutdown, the IC supply current reduces to 0.3 μA and the LX pin enters high impedance state. However, the input remains connected to the output through the inductor and the Schottky diode, keeping the output voltage one diode forward voltage drop below the input voltage.

APPLICATIONS CIRCUIT INFORMATION

External Component Selection

Inductor

The NCP1406 is designed to work well with a range of inductance values; the actual inductance value depends on the specific application, output current, efficiency, and output ripple voltage. For step-up conversion, the device works well with inductance ranging from 1.0 μH to 47 μH . In general, an inductor with small DCR, usually less than 1.0 Ω , should be used to minimize loss. It is necessary to choose an inductor with saturation current greater than the peak switching current in the application.

NCP1406 is designed to operate in discontinuous conduction mode (DCM). Stable operation in continuous conduction mode is not guaranteed. For each switching cycle, if the internal MOSFET is switched on, it will be switched off only when either the maximum on-time, t_{on} , of typical 0.9 μs is reached or the inductor current limit of 0.8 A is met, whichever is earlier. Therefore, the designer can choose to use either the maximum on-time or the current limit to turn off the MOSFET switch. If the goal is targeted to minimize output ripple voltage, the maximum on-time of 0.9 μs should be used to turn off the MOSFET; however, the maximum output current will be reduced. If we target to maximize the output current, the current limit should be chosen to turn off the MOSFET, but this method will result in a larger output ripple voltage.

If the maximum on-time is used to turn off the MOSFET in order to achieve a smaller output ripple voltage, it is critical to ensure that the maximum on-time has been reached before the current limit is met. To ensure this condition is met, the inductance L should be selected according to the following inequality:

$$L > \frac{V_{\text{IN}}}{I_{\text{LIM}}} \times t_{\text{on(max)}}$$

Where V_{IN} is the input voltage, I_{LIM} is the current limit which is typically 0.8 A, and $t_{\text{on(max)}}$ is the maximum on-time which is typically 0.9 μs .

The maximum output current under this maximum on-time control can be calculated from the equation below:

$$I_{\text{OUT(max)}} = \frac{2}{2L(V_{\text{OUT}} + V_{\text{D}})} \times \frac{V_{\text{IN}} \times t_{\text{on(max)}}}{\eta}$$

Where V_{IN} is the input voltage, $t_{\text{on(max)}}$ is the maximum on-time which is typically 0.9 μs , L is the selected inductance, V_{OUT} is the desired output voltage, V_{D} is the Schottky diode forward voltage, and η is the conversion efficiency which can be assumed typically 80% for better margin for estimation.

The above equation for calculating $I_{\text{OUT(max)}}$ is for DCM mode operation only. In fact, the operation can go beyond the critical conduction mode if the current loading further

increases above the maximum output current in DCM mode. However, stable operation in continuous conduction mode is hard to achieve, and double pulsing or group pulsing will occur which will lead to much larger inductor current ripple and result in larger output ripple voltage.

If the current limit is used to turn off the MOSFET in order to maximize the output current, it is critical to make sure that the current limit has been reached before the maximum on-time is met. To ensure this condition is met, the inductance L should be selected according to the following inequality:

$$L < \frac{V_{\text{IN}}}{I_{\text{LIM}}} \times t_{\text{on(max)}}$$

Since there is 100 ns internal propagation delay between the time the current limit is reached and the time the MOSFET is switched off, the actual peak inductor current can be obtained from the equation below:

$$I_{\text{PK}} = I_{\text{LIM}} + \frac{V_{\text{IN}}}{L} \times 100 \text{ ns}$$

Where I_{LIM} is the current limit which is typically 0.8 A, V_{IN} is the input voltage, L is the selected inductance.

Then the maximum output current under the current limit control can be calculated by the equation below:

$$I_{\text{OUT(max)}} = \frac{V_{\text{IN}} \times I_{\text{PK}}}{2(V_{\text{OUT}} + V_{\text{D}})} \times \eta$$

This method can achieve larger maximum output current in DCM mode. Since the current limit is reached in each switching cycle, the inductor current ripple is larger resulting in larger output voltage ripple. Two ceramic capacitors in parallel can be used at the output to keep the output ripple small.

Diode

The diode is the main source of loss in DC-DC converters. The key parameters which affect their efficiency are the forward voltage drop, V_{D} , and the reverse recovery time, t_{rr} . The forward voltage drop creates a loss just by having a voltage across the device while a current flowing through it. The reverse recovery time generates a loss when the diode is reverse biased, and the current appears to actually flow backwards through the diode due to the minority carriers being swept from the P-N junction. A Schottky diode with the following characteristics is recommended:

5. Small forward voltage, $V_{\text{D}} < 0.3 \text{ V}$.
6. Small reverse leakage current.
7. Fast reverse recovery time/switching speed.
8. Rated current larger than peak inductor current, $I_{\text{rated}} > I_{\text{PK}}$.
9. Reverse voltage larger than output voltage, $V_{\text{reverse}} > V_{\text{OUT}}$.

Input Capacitor

The input capacitor stabilizes the input voltage and minimizes peak current ripple from the power source. The capacitor should be connected directly to the inductor pin where the input voltage is applied in order to effectively smooth the input current ripple and voltage due to the inductor current ripple. The input capacitor is also used to decouple the high frequency noise from the VDD supply to the internal control circuit; therefore, the capacitor should be placed close to the VDD pin. For some particular applications, separate decoupling capacitors should be provided and connected directly to the VDD pin for better decoupling effect. A larger input capacitor can better reduce ripple current at the input. By reducing the ripple current at the input, the converter efficiency can be improved. In general, a 4.7 μ F to 22 μ F ceramic input capacitor is sufficient for most applications. X5R and X7R type ceramic capacitors are recommended due to their good capacitance tolerance and stable temperature behavior.

Output Capacitor

The output capacitor is used for sustaining the output voltage when no current is delivering from the input, and smoothing the ripple voltage. Ceramic capacitors should be used for the output capacitor due to their low ESR at high switching frequency and low profile in physical size. In general, a 3.3 μ F to 22 μ F ceramic capacitor should be appropriate for most applications. X5R and X7R type ceramic capacitors are recommended due to their good capacitance tolerance and temperature coefficient, while Y5V type ceramic capacitors are not recommended since both their capacitance tolerance and temperature coefficient are too large. The output voltage ripple and switching frequency at nominal load current can be calculated by the following equations:

$$V_{\text{ripple}} = \frac{I_{\text{OUT}}}{C_{\text{OUT}}} \left(\frac{1}{f_{\text{SW}}(\text{Load})} - \frac{I_{\text{PK}} \times L}{V_{\text{OUT}} + V_{\text{D}} - V_{\text{IN}}} \right) - (I_{\text{PK}} - I_{\text{OUT}}) \times \text{ESR}$$

$$f_{\text{SW}}(\text{Load}) = \frac{2I_{\text{OUT}}(V_{\text{OUT}} + V_{\text{D}} - V_{\text{IN}})}{I_{\text{PK}} \times L}$$

Where I_{OUT} is the nominal load current, C_{OUT} is the selected output capacitance, I_{PK} is the peak inductor current, L is the selected inductance, V_{OUT} is the output voltage, V_{D} is the Schottky diode forward voltage, V_{IN} is the input voltage, ESR is the ESR of the output capacitor.

Feedback Resistors

To achieve better efficiency at light load, a high impedance feedback resistor divider should be used. Choose the lower resistor R_2 value from the range of 10 k Ω to 200 k Ω . The value of the upper resistor R_1 can then be calculated from the equation below:

$$R_1 = R_2 \left(\frac{V_{\text{OUT}}}{1.19} - 1 \right)$$

1% tolerance resistors should be used for both R_1 and R_2 for better V_{OUT} accuracy.

Feedforward Capacitor

A feedforward capacitor is required to add across the upper feedback resistor to avoid double pulsing or group pulsing at the switching node which will cause larger inductor ripple current and higher output voltage ripple. With adequate feedforward capacitance, evenly distributed single pulses at the switching node can be achieved. The range of the capacitor value is from 5.0 pF to 200 pF for most applications. For NCP1406, the lower the switching frequency, the larger the feedforward capacitance is needed; besides, the higher the output voltage, the larger the feedforward capacitance is required. For the initial trial value of the feedforward capacitor, the following equation can be used; however, the actual value needs fine tuning:

$$C_{\text{FF}} \approx \frac{1}{2 \times \pi \times \frac{f_{\text{SW}}(\text{Load})}{20} \times R_1}$$

Output Voltage Higher than 25 V

The NCP1406 can be used to generate output voltage higher than 25 V by adding an external high voltage N-Ch MOSFET in series with the internal MOSFET switch as shown in Figure 51. The drain-to-source breakdown voltage of the external MOSFET must be at least 1.0 V higher than the output voltage. The diode D2 connected across the gate and the source of the external MOSFET helps the external MOSFET to turn off and ensures that most of the voltage drops across the external MOSFET during the switch-off period. Since the high voltage external MOSFET is in series with the internal MOSFET, higher break down voltage is achieved but the current capability is not increased.

There is an alternative application circuit shown in Figure 53 which can output voltage up to 30 V. For this circuit, a diode-capacitor charge-pump voltage doubler constructed by D2, D3 and C1 is added. During the internal MOSFET switch-on time, the LX pin is shorted to ground and D2 will charge up C1 to the stepped up voltage at the cathode of D1. During the MOSFET switch-off time, the voltage at V_{OUT} will be almost equal to the double of the voltage at the cathode of D1. The V_{OUT} is monitored by the FB pin via the resistor divider and can be set by the resistor values. Since the maximum voltage at the cathode of D1 is 15 V, the maximum V_{OUT} is 30 V. The value of C1 can be in the range of 0.47 μ F to 2.2 μ F.

Negative Voltage Generation

The NCP1406 can be used to produce a negative voltage output by adding a diode-capacitor charge-pump circuit (D2, D3, and C1) to the LX pin as shown in Figure 50. The feedback voltage resistor divider is still connected to the positive output to monitor the positive output voltage and a small value capacitor is used at C2. When the internal MOSFET switches off, the voltage at the LX pin charges up the capacitor through diode D2. When the MOSFET

switches on, the capacitor C1 is effectively connected like a reversed battery and C1 discharges the stored charge through the $R_{DS(on)}$ of the internal MOSFET and D3 to charge up C_{OUT} and builds up a negative voltage at V_{OUT} . Since the negative voltage output is not directly monitored by the NCP1406, the output load regulation of the negative output is not as good as the standard positive output circuit. The resistance values of the resistors of the voltage divider can be one-tenth of those used in the positive output circuit in order to improve the regulation at light load.

The application circuit in Figure 54, is actually the combination of the application circuits in Figures 50 and 51.

Step-Down Converter

NCP1406 can be configured as a simple step-down converter by using the open-drain LX pin to drive an external P-Ch MOSFET as shown in Figure 52. The resistor R_{GS} is used to switch off the P-Ch MOSFET during the switch-off period. Too small a resistance value should not be used for R_{GS} , otherwise, the efficiency will be reduced. R_{GS} should be in the range of 510 Ω to 5.1 k Ω .

White LED Driver

The NCP1406 can be used as a constant current LED driver which can drive up to 6 white LEDs in series as shown in Figure 57. The LED current can be set by the resistance value of R_S . The desired LED current can be calculated by the equation below:

$$I_{LED} = \frac{1.19}{R_S}$$

Moreover, the brightness of the LEDs can be adjusted by a DC voltage or a PWM signal with an additional circuit illustrated below:

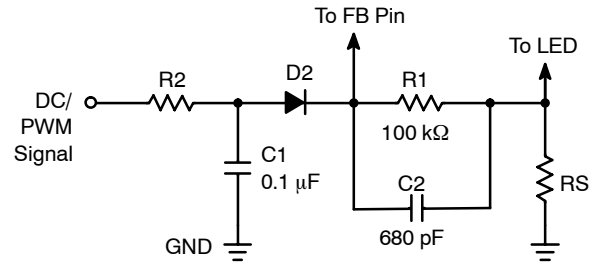


Figure 45.

With this additional circuit, the maximum LED current is set by the above equation. The value of R_2 can be obtained by the following equation:

$$R_2 = \frac{V_{MAX} \times D_{CTL(MAX)} - V_D - 1.19}{\left(\frac{(I_{LED(MAX)} - I_{LED(MIN)}) \times R_S}{R_1} \right)}$$

V_{MAX} is the maximum voltage of the control signal, $D_{CTL(MAX)}$ is the maximum duty cycle of the control signal, V_D is the diode forward voltage, $I_{LED(MAX)}$ is the maximum LED current and $I_{LED(MIN)}$ is the minimum LED current. If a PWM control signal is used, the signal frequency can be in the range of 5.0 kHz to 30 kHz. It is recommended to keep the input PWM frequency about 15 kHz to avoid generating audio noise.

PCB Layout Guidelines

PCB layout is very important for switching converter performance. All the converter's external components should be placed close to the IC. The schematic, PCB trace layout, and component placement of the step-up DC-DC converter demonstration board are shown in Figure 46 to Figure 49 for PCB layout design reference. The following guidelines should be observed:

1. Grounding

Single-point grounding should be used for the output power return ground, the input power return ground, and the device switch ground to reduce noise. The input ground and output ground traces must be thick and short enough for current to flow through. A ground plane should be used to reduce ground bounce.

2. Power Traces

Low resistance conducting paths (short and thick traces) should be used for the power carrying traces to reduce power loss so as to improve efficiency (short and thick

traces for connecting the inductor L can also reduce stray inductance). The path between C1, L1, D1, and C2 should be kept short. The trace from L to LX pin of the IC should also be kept short.

3. External Feedback Components

Feedback resistors R1 and R2, and feedforward capacitor C3 should be located as close to the FB pin as possible to minimize noise picked up by the FB pin. The ground connection of the feedback resistor divider should be connected directly to the GND pin.

4. Input Capacitor

The input capacitor should be located close to both the input to the inductor and the VDD pin of the IC.

5. Output Capacitor

The output capacitor should be placed close to the output terminals to obtain better smoothing effect on output ripple voltage.

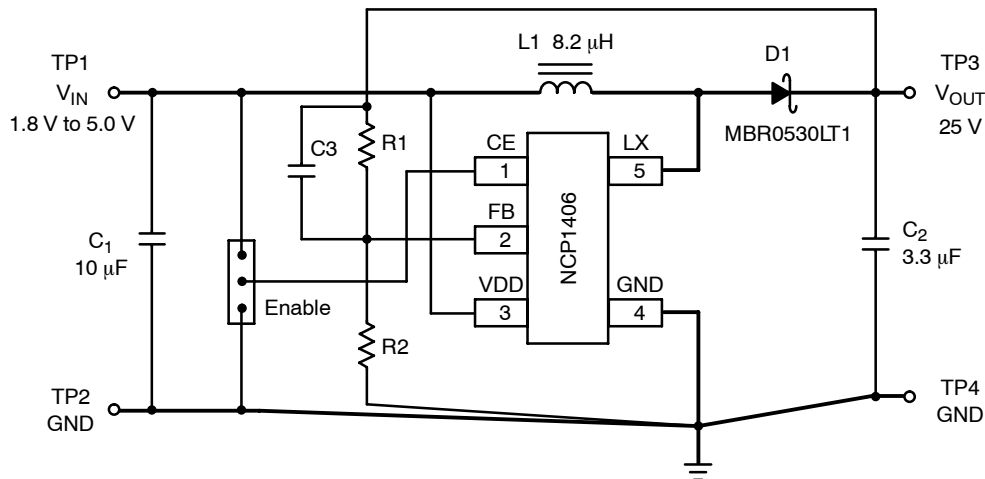


Figure 46. Step-Up Converter Demonstration Board Schematic

NCP1406

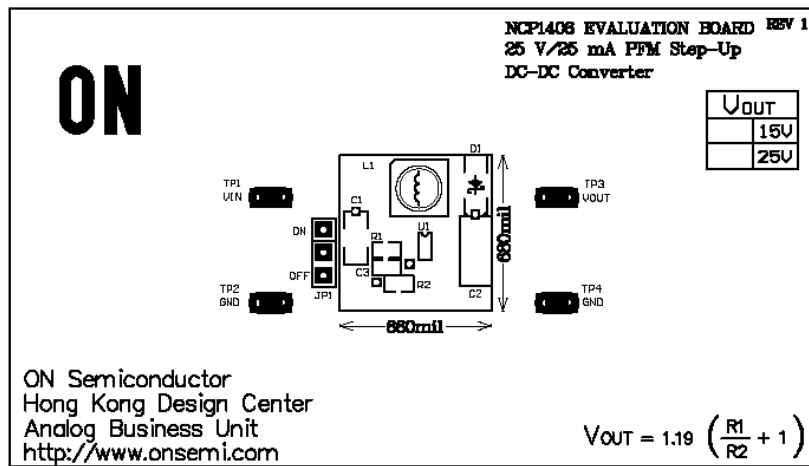


Figure 47. Step-Up Converter Demonstration Board Top Layer Component Silkscreen

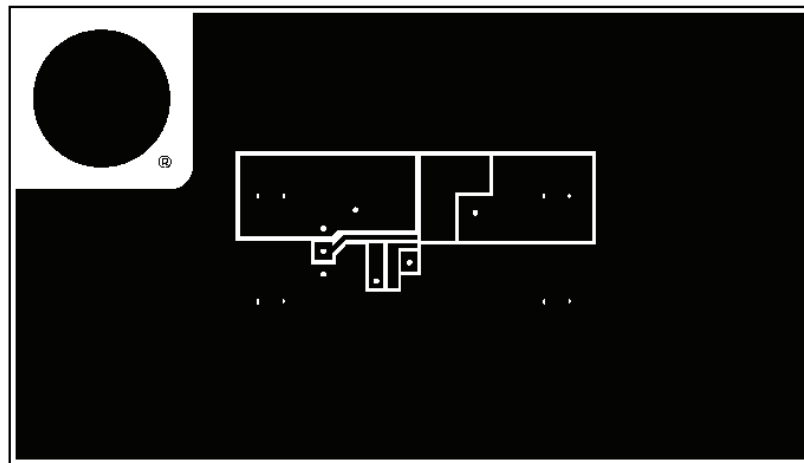


Figure 48. Step-Up Converter Demonstration Board Top Layer Copper

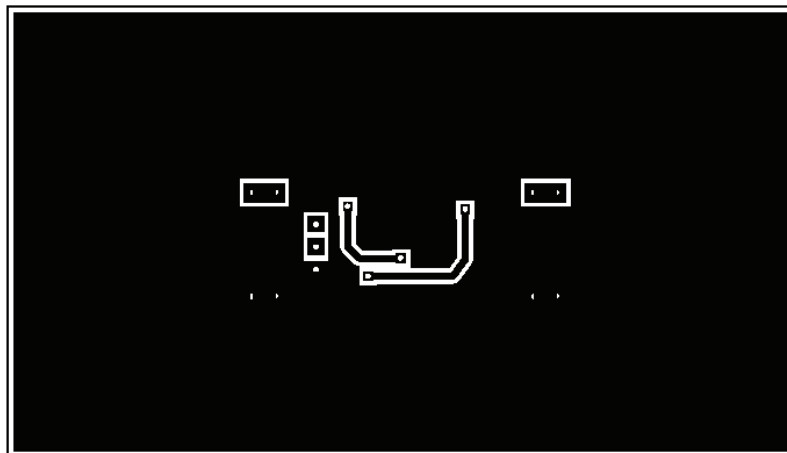


Figure 49. Step-Up Converter Demonstration Board Bottom Layer Copper

Components Supplier

Output Voltage	Parts	Supplier	Part Number	Description	Website
15 V	C1	Panasonic	ECJ2FB0J106M	Ceramic Capacitor 0805 10 μ F/6.3 V	www.panasonic.com
	C2	Panasonic	ECJ3YB1E475M	Ceramic Capacitor 1206 4.7 μ F/25 V	www.panasonic.com
	C3	Panasonic	ECJ1VC1H560K	Ceramic Capacitor 0603 56 pF/50 V	www.panasonic.com
	D1	ON Semiconductor	MBR0520LT1	Schottky Power Rectifier 20 V/500 mA	www.onsemi.com
	L1	Sumida Electric Co. Ltd	CMD4D11-100MC	Inductor 10 μ H 1.2 mm Low Profile	www.sumida.com
	R1	Panasonic	ERJ3GEYJ135V	Resistor 0603 1.3 M Ω	www.panasonic.com
	R2	Panasonic	ERJ3GEYJ114V	Resistor 0603 110 k Ω	www.panasonic.com
	U1	ON Semiconductor	NCP1406SNT1	25 V Step-up DC-DC Converter	www.onsemi.com
25 V	C1	Panasonic	ECJ2FB0J106M	Ceramic Capacitor 0805 10 μ F/6.3 V	www.panasonic.com
	C2	Panasonic	ECJ5YB1H335M	Ceramic Capacitor 1812 3.3 μ F/50 V	www.panasonic.com
	C3	Panasonic	ECJ1VC1H151K	Ceramic Capacitor 0603 150 pF/50 V	www.panasonic.com
	D1	ON Semiconductor	MBR0530LT1	Schottky Power Rectifier 30 V/500 mA	www.onsemi.com
	L1	Sumida Electric Co. Ltd	CMD4D11-100MC	Inductor 10 μ H 1.2 mm Low Profile	www.sumida.com
	R1	Panasonic	ERJ3GEYJ225V	Resistor 0603 2.2 M Ω	www.panasonic.com
	R2	Panasonic	ERJ3GEYJ114V	Resistor 0603 110 k Ω	www.panasonic.com
	U1	ON Semiconductor	NCP1406SNT1	25 V Step-up DC-DC Converter	www.onsemi.com

OTHER APPLICATION CIRCUITS

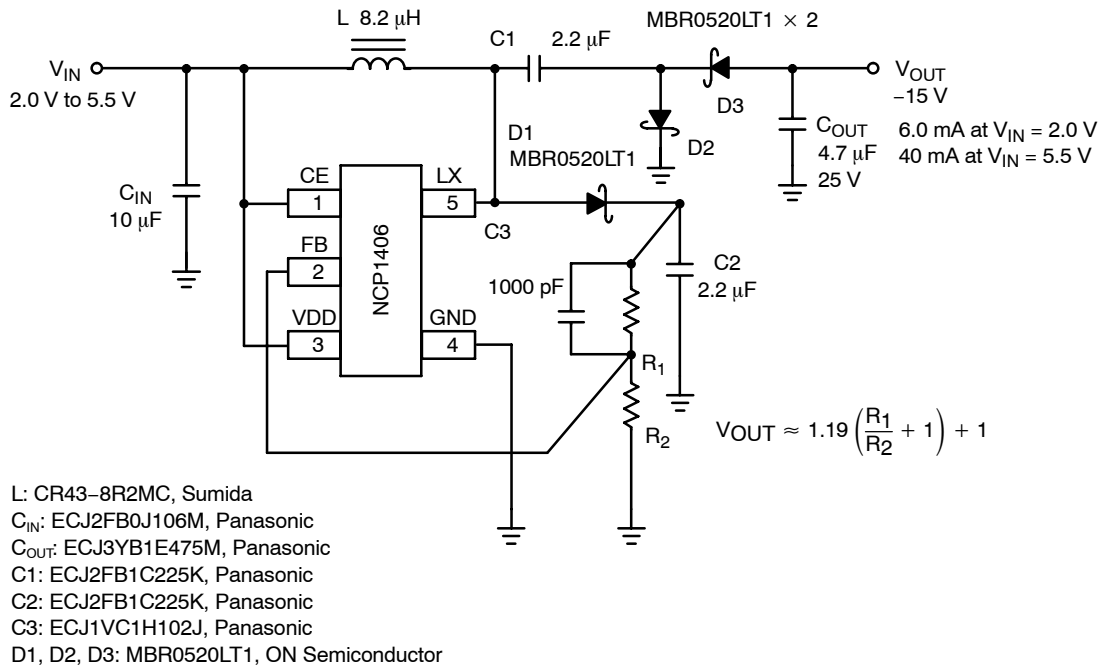


Figure 50. Positive-to-Negative Output Converter for Negative LCD Bias

NCP1406

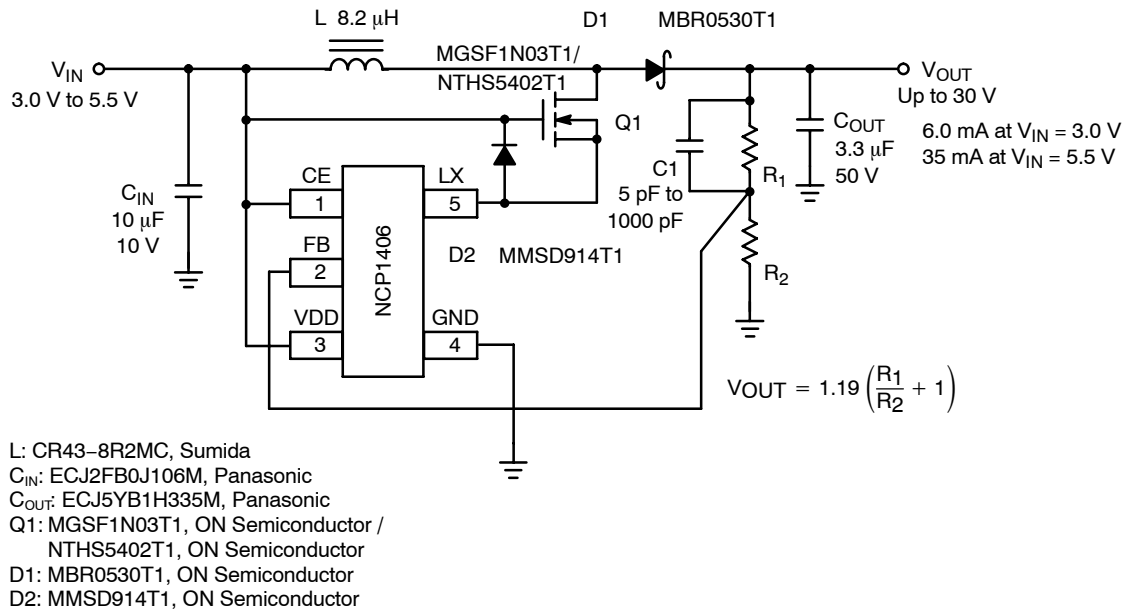


Figure 51. Step-Up DC-DC Converter with 30 V Output Voltage

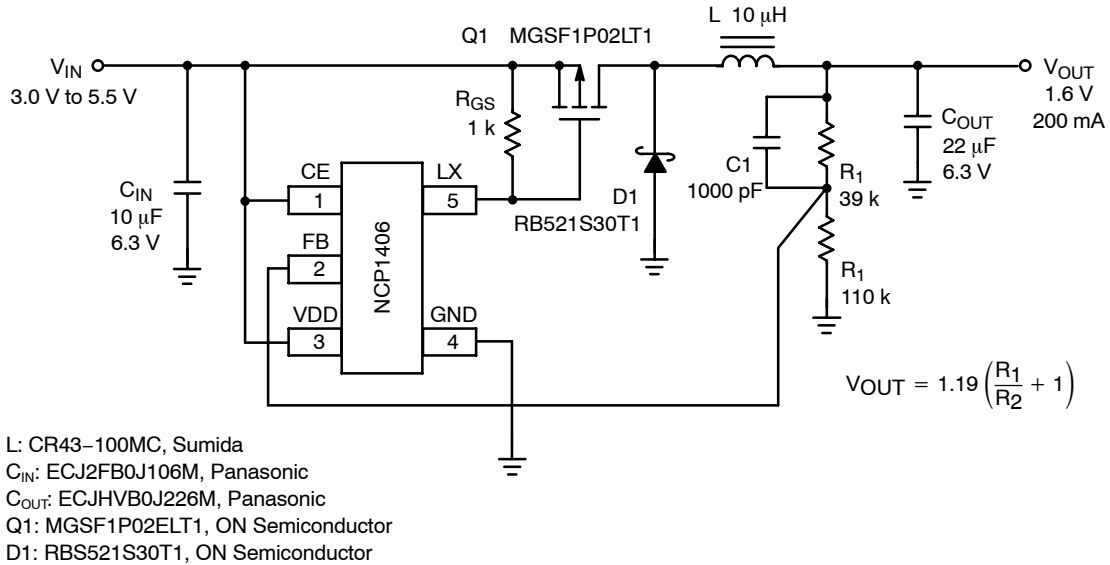
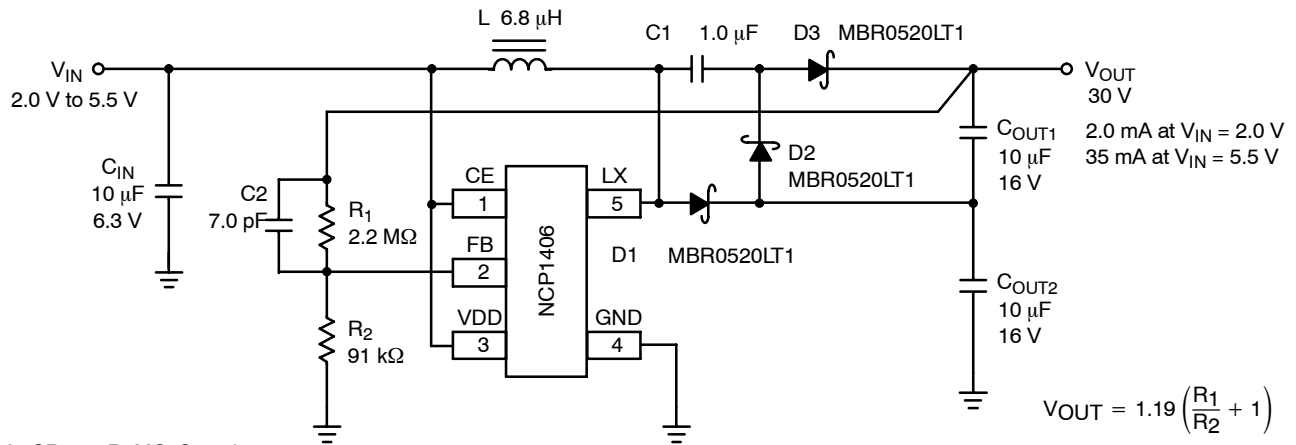


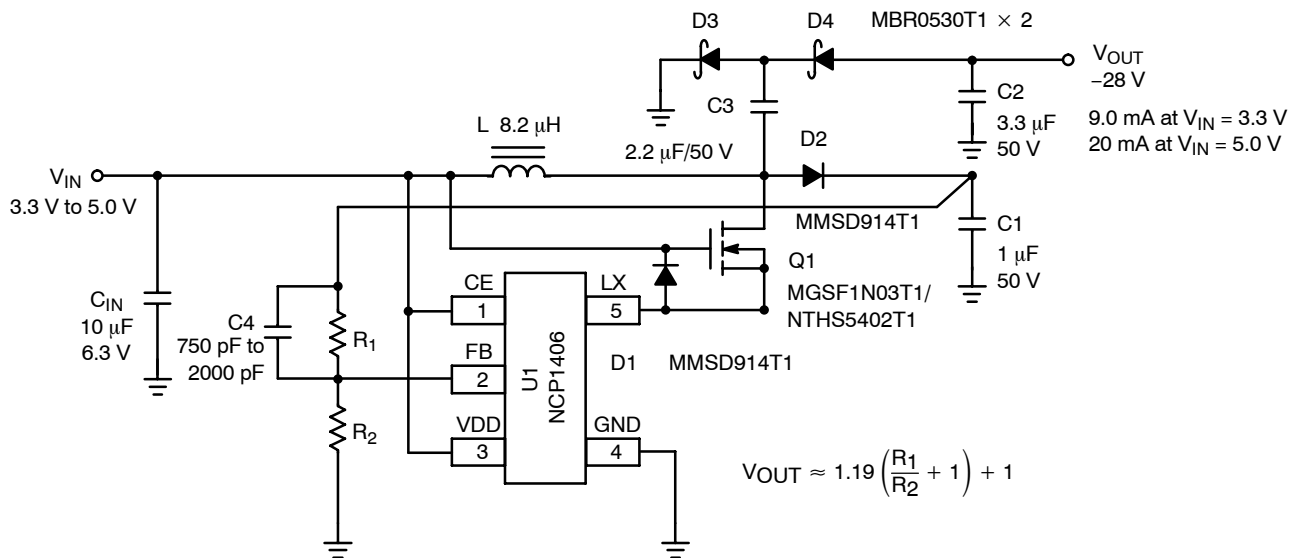
Figure 52. Step-Down DC-DC Converter with 1.6 V Output Voltage for DSP Circuit

NCP1406



L: CR43-6R8MC, Sumida
 C_{IN} : ECJ2FB0J106M, Panasonic
 C_{OUT1} , C_{OUT2} : ECJ3YB1C106M, Panasonic
 $C1$: ECJ2FB1C225K, Panasonic
 $D1$, $D2$, $D3$: MBR0520LT1, ON Semiconductor

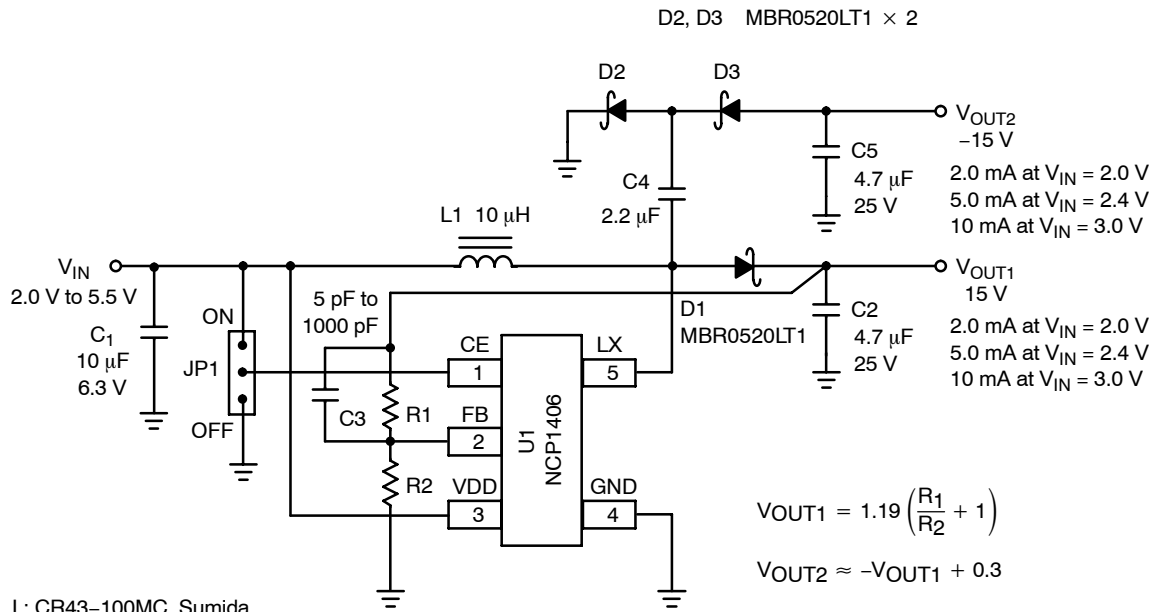
Figure 53. Step-Up DC-DC Converter with 30 V Output Voltage



L: CR43-8R2MC, Sumida
 C_{IN} : ECJ2FB0J106M, Panasonic
 $C1$: ECJGV1C105M, Panasonic
 $C2$: ECJ5YB1H335M, Panasonic
 $C3$: ECJ4YB1H105M, Panasonic
 $Q1$: MGSF1N03T1, ON Semiconductor /
 NTHS5402T1, ON Semiconductor
 $D1$, $D2$: MMSD914T1, ON Semiconductor
 $D3$, $D4$: MBR0530T1, ON Semiconductor

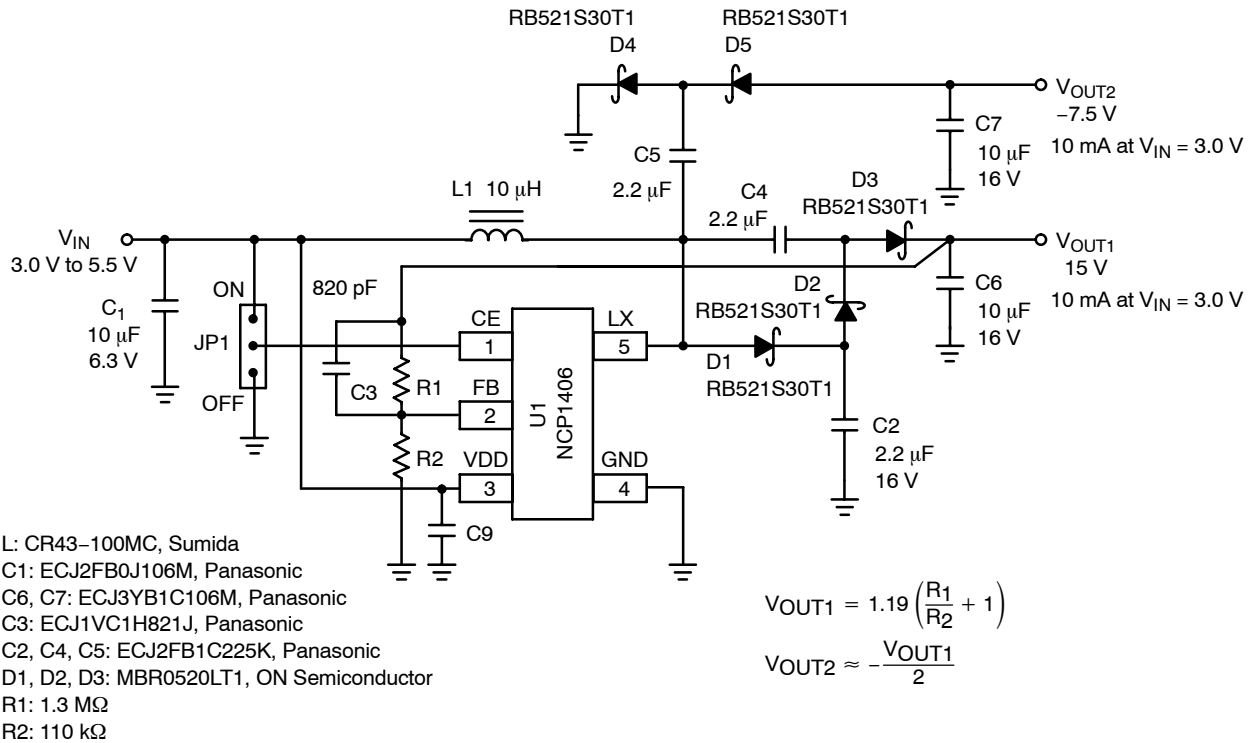
Figure 54. Voltage Inverting DC-DC Converter with -28 V Output Voltage

NCP1406



L: CR43-100MC, Sumida
 C1: ECJ2FB0J106M, Panasonic
 C2, C5: ECJ3YB1E475M, Panasonic
 C3: ECJ1VC1H102J, Panasonic
 C4: ECJ2FB1C225K, Panasonic
 D1, D2, D3: MBR0520LT1, ON Semiconductor
 R1: 1.3 MΩ
 R2: 110 kΩ

Figure 55. +15 V, -15 V Outputs Converter for LCD Bias Supply



L: CR43-100MC, Sumida
 C1: ECJ2FB0J106M, Panasonic
 C6, C7: ECJ3YB1C106M, Panasonic
 C3: ECJ1VC1H821J, Panasonic
 C2, C4, C5: ECJ2FB1C225K, Panasonic
 D1, D2, D3: MBR0520LT1, ON Semiconductor
 R1: 1.3 MΩ
 R2: 110 kΩ

Figure 56. +15 V, -7.5 V Outputs Converter for CCD Supply Circuit

NCP1406

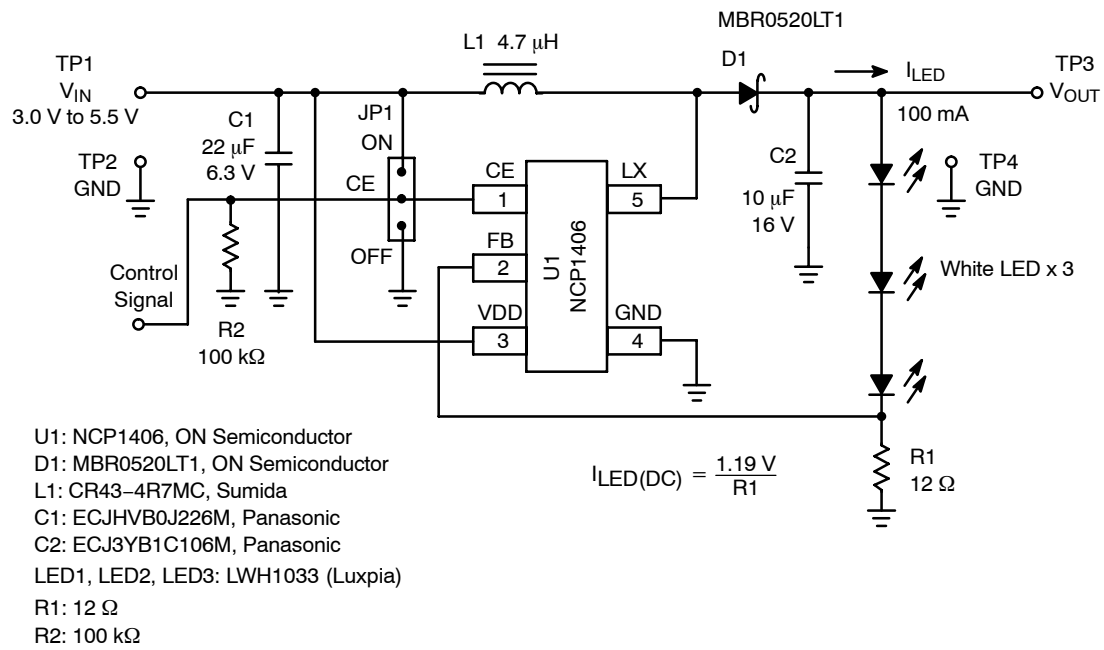


Figure 57. White LEDs Driver Circuit

NCP1410

250 mA Sync-Rect PFM Step-Up DC-DC Converter with Low-Battery Detector

NCP1410 is a monolithic micropower high frequency Boost (step-up) voltage switching converter IC specially designed for battery operated hand-held electronic products up to 250 mA loading. It integrates Synchronous Rectifier for improving efficiency as well as eliminating the external Schottky Diode. High switching frequency (up to 600 kHz) allows low profile inductor and output capacitor being used. Low-Battery Detector, Logic-Controlled Shutdown and Cycle-by-Cycle Current Limit provide value-added features for various battery-operated applications. With all these functions ON, the device quiescent supply current is only 9.0 μ A typical. This device is available in space saving compact Micro8™ package.

Features

- High Efficiency up to 92%
- Very Low Device Quiescent Supply Current of 9.0 μ A Typical
- Allows use of Small Size Inductor and Capacitor
- Built-in Synchronous Rectifier (PFET) Eliminates One External Schottky Diode
- High Switching Frequency (up to 600 kHz) Allows Use of Small Size Inductor and Capacitor
- High Accuracy Reference Output, 1.19 V $\pm$ 0.6% @ 25°C, can supply more than 2.5 mA when $V_{OUT} \geq 3.3$ V
- 1.0 V Startup at No Load Guaranteed
- Output Voltage from 1.5 V to 5.5 V Adjustable
- Output Current up to 250 mA @ $V_{in} = 2.5$ V, $V_{out} = 3.3$ V
- Logic-Controlled Shutdown
- Open Drain Low-Battery Detector Output
- 1.0 A Cycle-by-Cycle Current Limit
- Low Profile and Minimum External Parts
- Compact Micro8 Package
- Pb-Free Package is Available

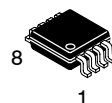
Typical Applications

- Personal Digital Assistant (PDA)
- Handheld Digital Audio Product
- Camcorders and Digital Still Camera
- Hand-held Instrument
- Conversion from One or Two NiMH or NiCd, or One Li-ion Cell to 3.3 V/5.0 V



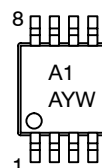
ON Semiconductor®

<http://onsemi.com>



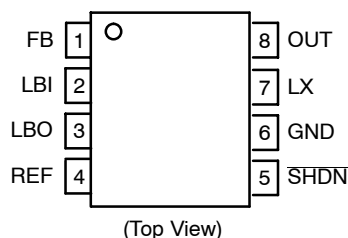
Micro8™
DM SUFFIX
CASE 846A

MARKING DIAGRAM



A1 = Device Marking
A = Assembly Location
Y = Year
W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP1410DMR2	Micro8	4000 Tape & Reel
NCP1410DMR2G	Micro8 (Pb-Free)	4000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP1410

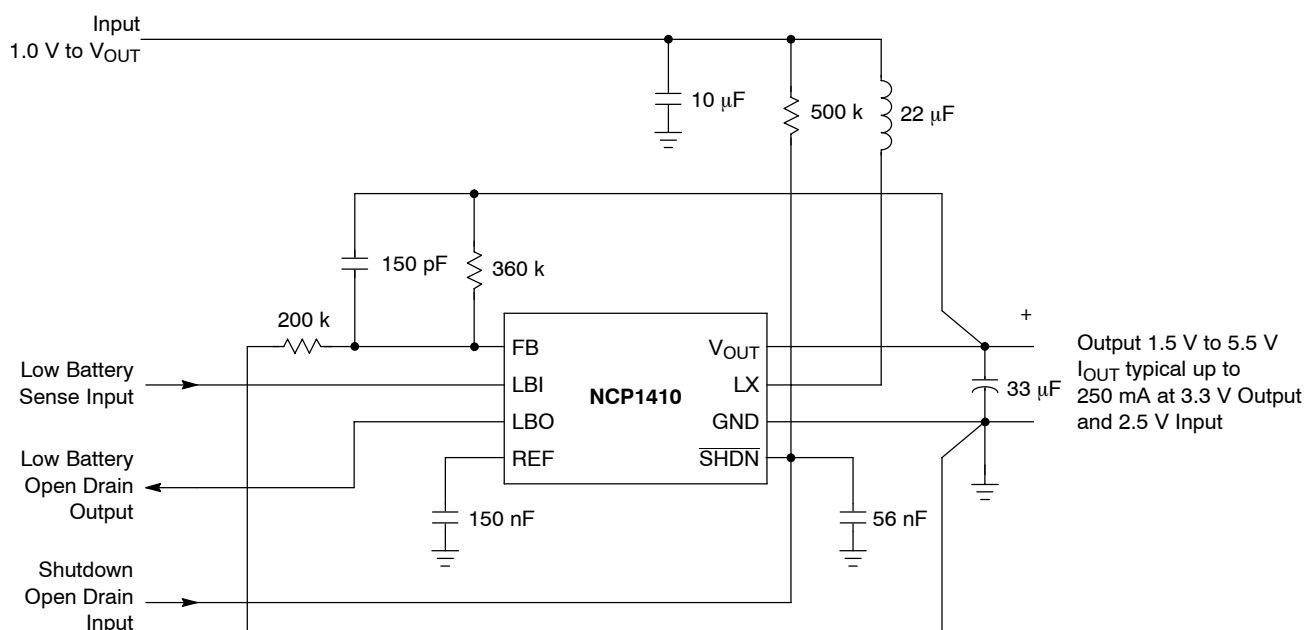


Figure 1. Typical Operating Circuit

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Device Power Supply (Pin 8)	V_{OUT}	-0.3 to 6.0	V
Input/Output Pins (Pin 1–5, Pin 7)	V_{IO}	-0.3 to 6.0	V
Thermal Characteristics – Micro8 Plastic Package Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$ Thermal Resistance Junction to Air	P_D $R_{\theta JA}$	520 240	mW $^\circ\text{C/W}$
Operating Junction Temperature Range	T_J	-40 to +150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- This device series contains ESD protection and exceeds the following tests:
Human Body Model (HBM) ± 2.0 kV per JEDEC standard: JESD22-A114.
Machine Model Method (MM) ± 200 V per JEDEC standard: JESD22-A115.
- The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_J(\text{max}) - T_A}{R_{\theta JA}}$$

- Latchup Current Maximum Rating: ± 150 mA per JEDEC standard: JESD78.
- Moisture Sensitivity Level: MSL 1 per IPC/JEDEC standard: J-STD-020A.

NCP1410

ELECTRICAL CHARACTERISTICS ($V_{OUT} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ for typical value, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for min/max values unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Voltage	V_{IN}	1.0	–	5.5	V
Output Voltage Range (Adjusted by external feedback)	V_{OUT}	V_{IN}	–	5.5	V
Reference Voltage ($C_{REF} = 150\text{ nF}$, under no loading, $T_A = 25^\circ\text{C}$)	V_{REF_NL}	1.183	1.190	1.197	V
Reference Voltage ($C_{REF} = 150\text{ nF}$, under no loading, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$)	$V_{REF\_NL\_A}$	1.178	–	1.202	V
Reference Voltage Temperature Coefficient	TC_{VREF}	–	0.03	–	mV/ $^\circ\text{C}$
Reference Voltage Load Current ($V_{OUT} = 3.3\text{ V}$, $V_{REF} = V_{REF\_NL} \pm 1.5\%$, $C_{REF} = 1.0\text{ }\mu\text{F}$) (Note 5)	I_{REF}	2.5	–	–	mA
Reference Voltage Load Regulation ($V_{OUT} = 3.3\text{ V}$, $I_{REF} = 0$ to $100\text{ }\mu\text{A}$, $C_{REF} = 1.0\text{ }\mu\text{F}$)	V_{REF_LOAD}	–	0.015	1.0	mV
Reference Voltage Line Regulation (V_{OUT} from 1.5 V to 5.5 V , $C_{REF} = 1.0\text{ }\mu\text{F}$)	V_{REF_LINE}	–	0.03	1.0	mV/V
FB, LBI Input Threshold ($I_{LOAD} = 0\text{ mA}$)	V_{FB} , V_{LBI}	1.174	1.190	1.200	V
N-FET ON Resistance	$R_{DS(ON)-N}$		0.6		Ω
P-FET ON Resistance	$R_{DS(ON)-P}$		0.9		Ω
LX Switch Current Limit (NFET)	I_{LIM}	–	1.0	–	A
Operating Current into OUT ($V_{FB} = 1.4\text{ V}$, i.e. No switching, $V_{OUT} = 3.3\text{ V}$)	I_Q	–	9.0	14	μA
Shutdown Current into OUT ($\overline{\text{SHDN}} = \text{GND}$)	I_{SD}	–	0.05	1.0	μA
LX Switch MAX. ON-Time ($V_{FB} = 1.0\text{ V}$, $V_{OUT} = 3.3\text{ V}$)	t_{ON}	1.2	1.4	1.8	μs
LX Switch MIN. OFF-Time ($V_{FB} = 1.0\text{ V}$, $V_{OUT} = 3.3\text{ V}$)	t_{OFF}	0.25	0.31	0.37	μs
FB Input Current	I_{FB}	–	1.5	9.0	nA
LBI Input Current	I_{LBI}	–	1.5	8.0	nA
LBO Low Output Voltage ($V_{LBI} = 0$, $I_{SINK} = 1.0\text{ mA}$)	V_{LBO_L}	–	–	0.05	V
$\overline{\text{SHDN}}$ Input Current	$I_{\overline{\text{SHDN}}}$	–	1.5	8.0	nA
$\overline{\text{SHDN}}$ Input Threshold, Low	$V_{\overline{\text{SHDN}}\_L}$	–	–	0.3	V
$\overline{\text{SHDN}}$ Input Threshold, High	$V_{\overline{\text{SHDN}}\_H}$	0.6	–	–	V

5. Loading capability increases with V_{OUT} .

PIN FUNCTION DESCRIPTIONS

Pin #	Symbol	Pin Description
1	FB	Output Voltage Feedback Input.
2	LBI	Low-Battery Detector Input.
3	LBO	Open-Drain Low-Battery Detector Output. Output is LOW when V_{LBI} is $< 1.178\text{ V}$. LBO is high impedance during shutdown.
4	REF	1.190 V Reference Voltage Output, bypass with 150 nF capacitor if this pin is not loaded, bypass with $1.0\text{ }\mu\text{F}$ if this pin is loaded up to 2.5 mA @ $V_{OUT} = 3.3\text{ V}$.
5	$\overline{\text{SHDN}}$	Shutdown Input. HIGH ($> 0.6\text{ V}$) = operating; LOW ($< 0.3\text{ V}$) = shutdown.
6	GND	Ground.
7	LX	N-Channel and P-Channel Power MOSFET Drain Connection.
8	OUT	Power Output. OUT provides bootstrap power to the IC.

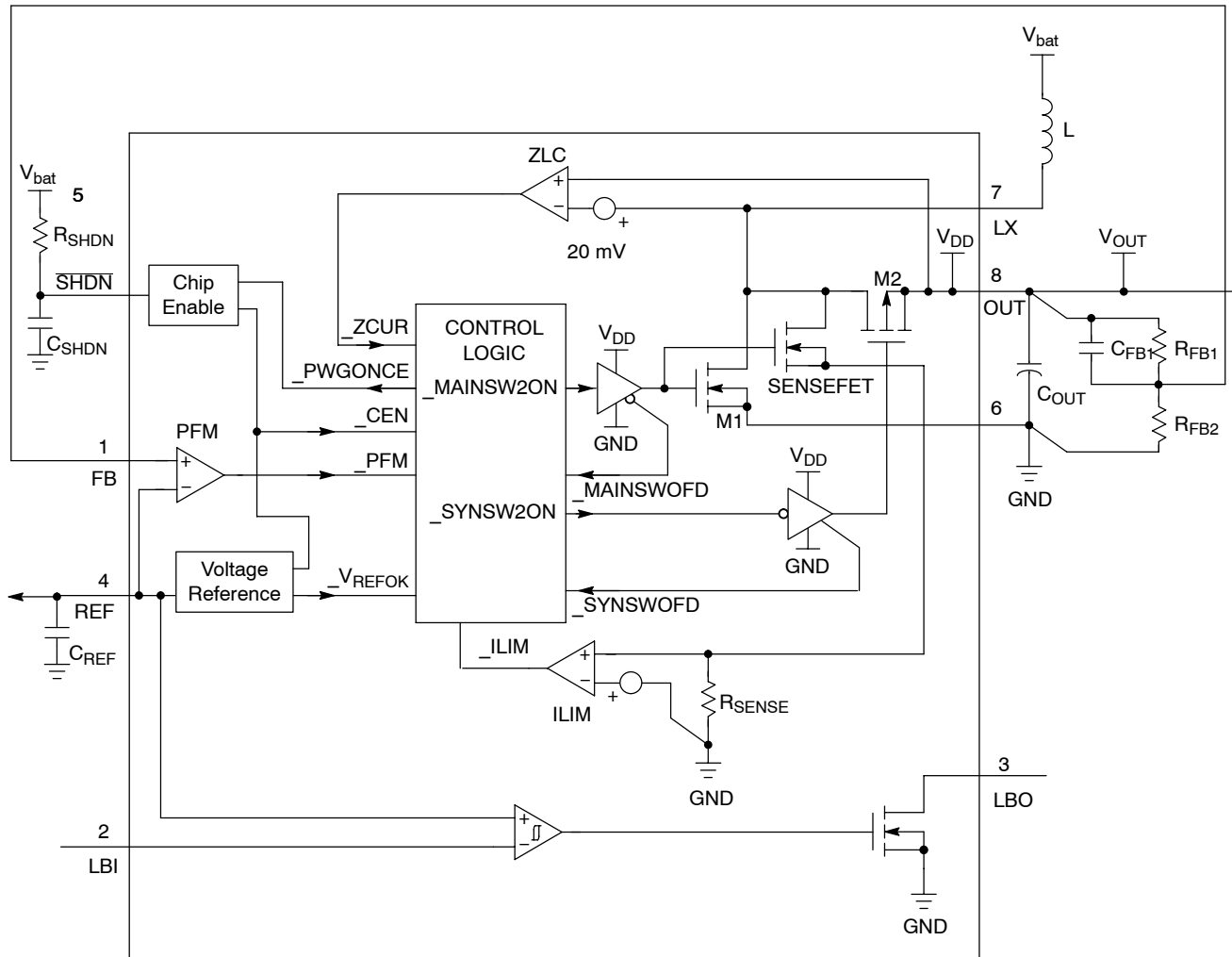


Figure 2. Simplified Functional Diagram

TYPICAL OPERATING CHARACTERISTICS

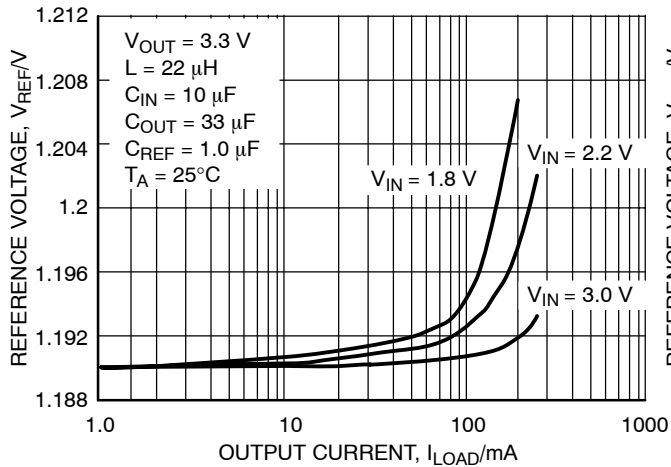


Figure 3. Reference Voltage vs. Output Current

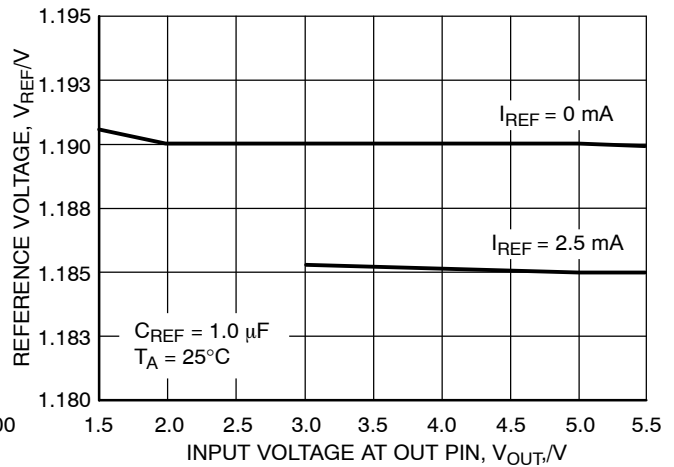


Figure 4. Reference Voltage vs. Input Voltage at OUT pin

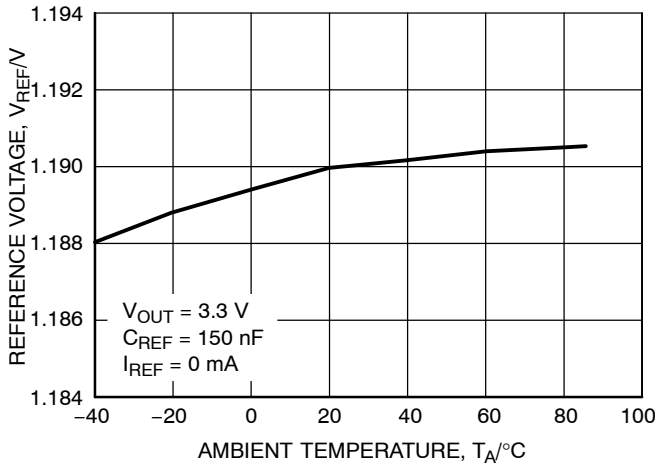


Figure 5. Reference Voltage vs. Temperature

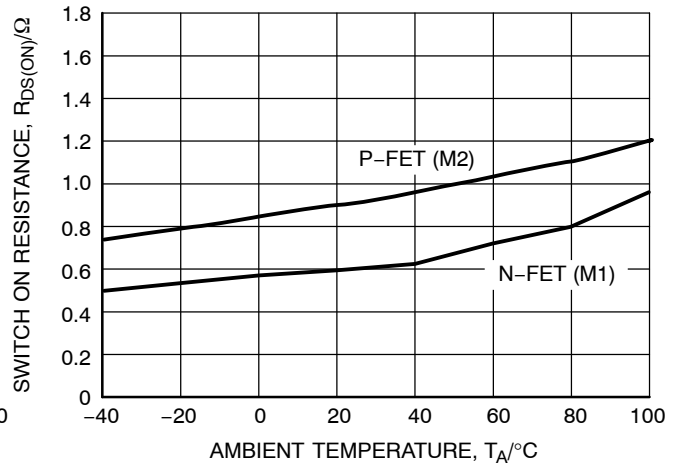


Figure 6. Switch ON Resistance vs. Temperature

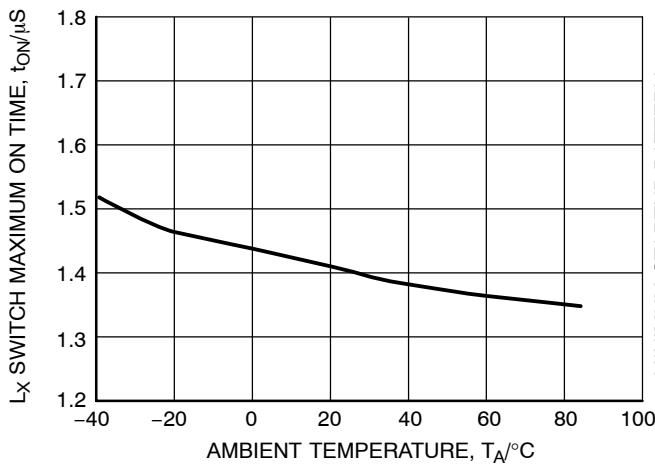


Figure 7. L_X Switch Maximum ON Time vs. Temperature

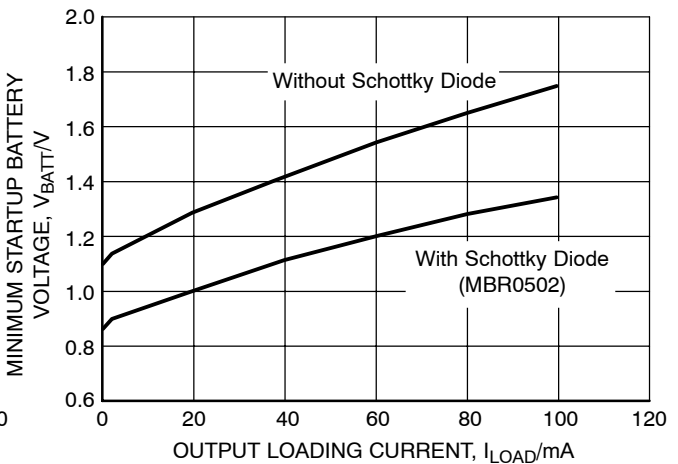


Figure 8. Minimum Startup Battery Voltage vs. Loading Current

TYPICAL OPERATING CHARACTERISTICS

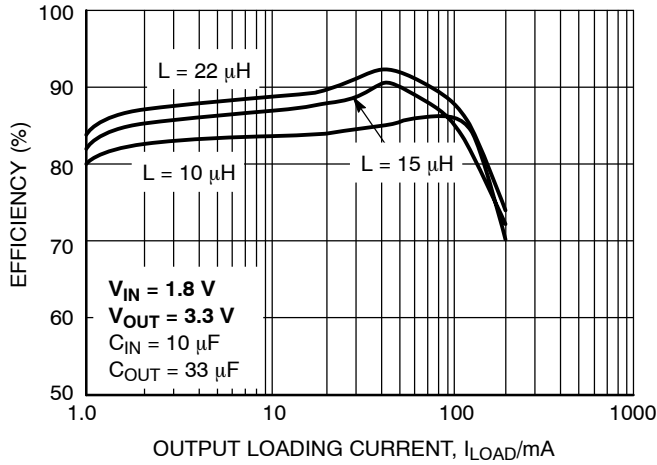


Figure 9. Efficiency vs. Load Current

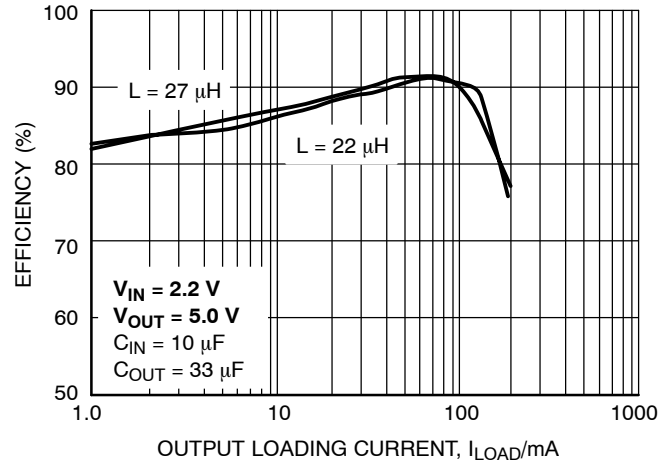


Figure 10. Efficiency vs. Load Current

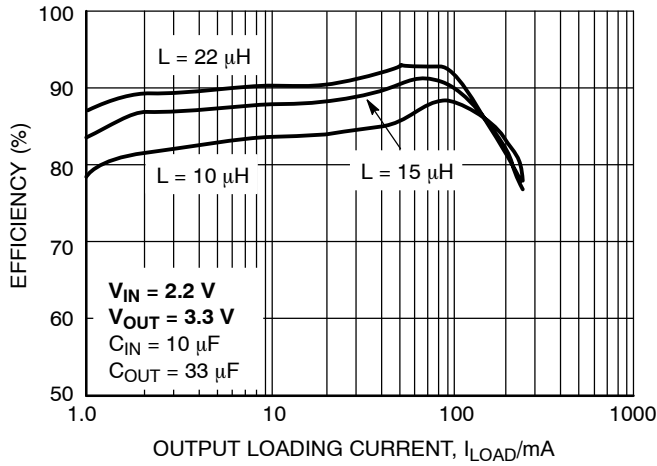


Figure 11. Efficiency vs. Load Current

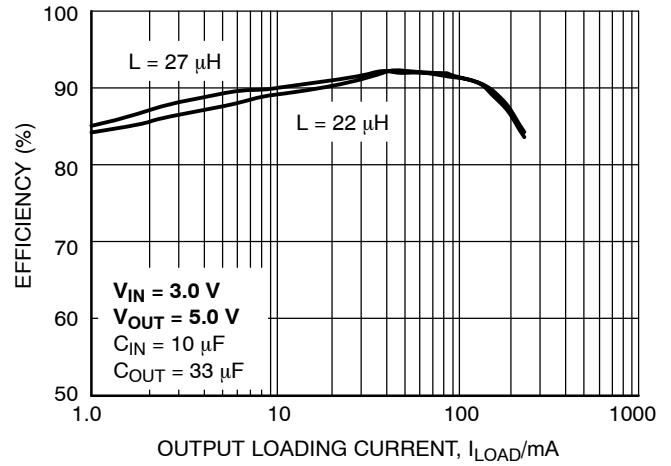


Figure 12. Efficiency vs. Load Current

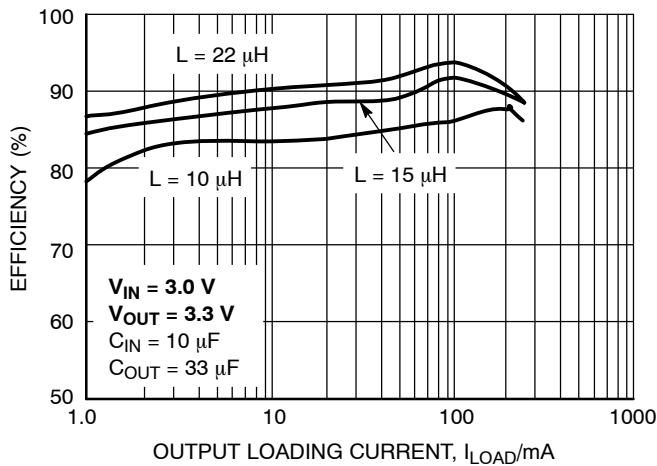


Figure 13. Efficiency vs. Load Current

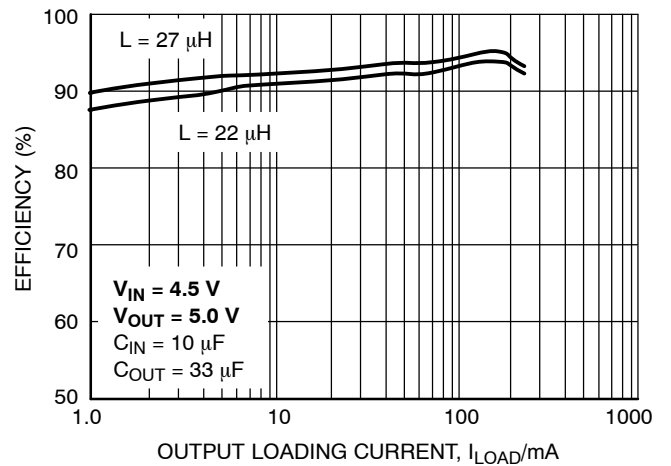


Figure 14. Efficiency vs. Load Current

TYPICAL OPERATING CHARACTERISTICS

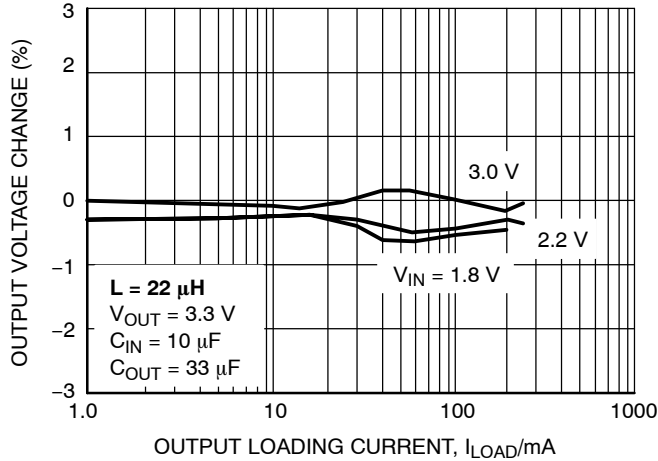


Figure 15. Output Voltage Change vs. Load Current

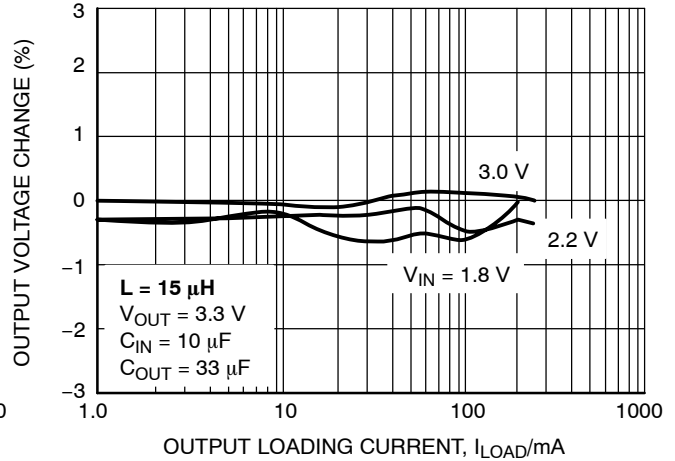


Figure 16. Output Voltage Change vs. Load Current

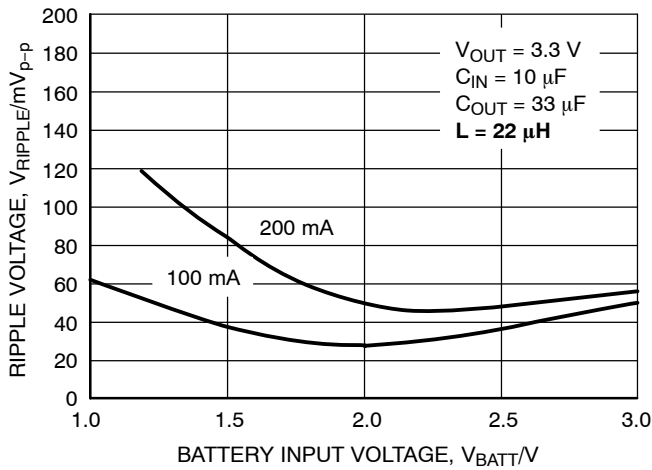


Figure 17. Output Ripple Voltage vs. Battery Input Voltage

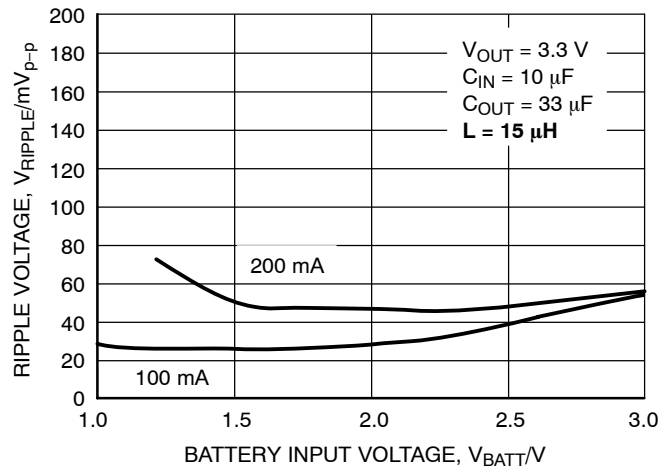


Figure 18. Output Ripple Voltage vs. Battery Input Voltage

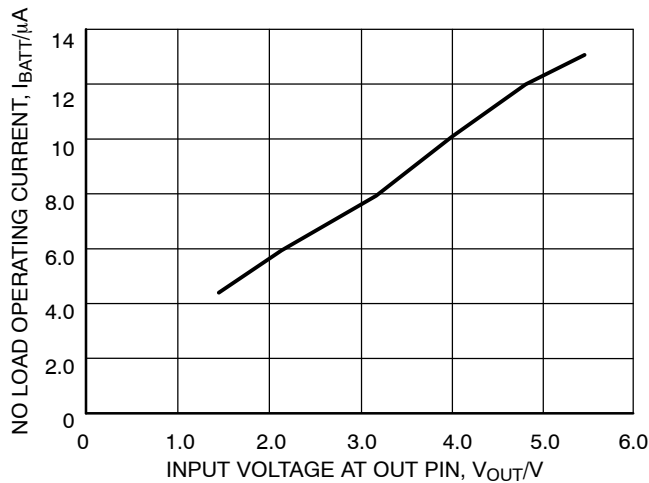


Figure 19. No Load Operating Current vs. Input Voltage at OUT Pin

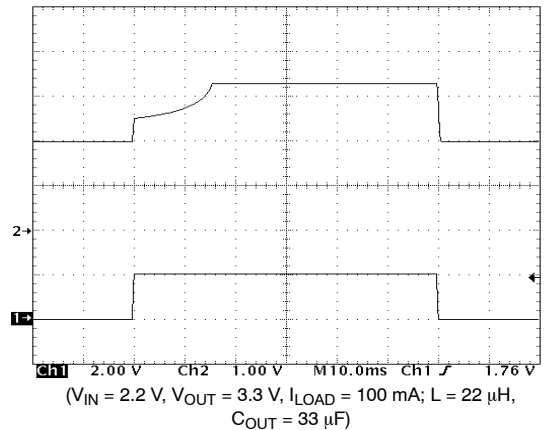
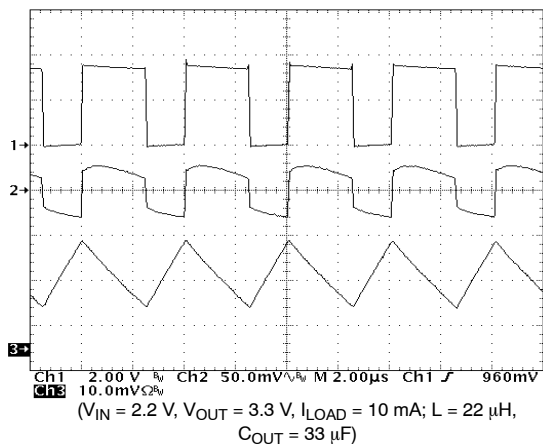


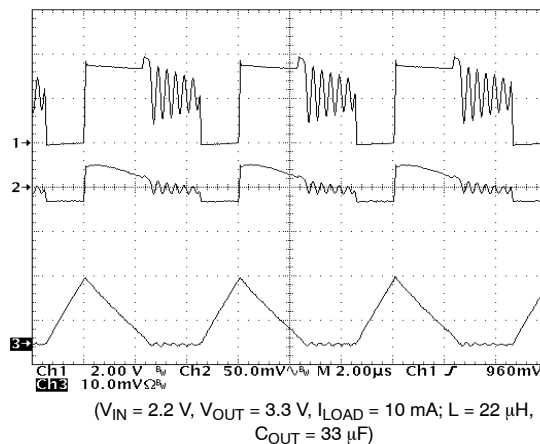
Figure 20. Startup Transient Response

TYPICAL OPERATING CHARACTERISTICS



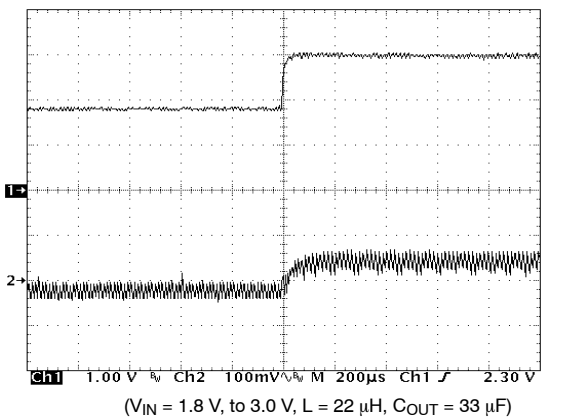
Upper Trace: Voltage at L_X pin, 2.0 V/Division
Middle Trace: Output Voltage Ripple, 50 mV/Division
Lower Trace: Inductor Current, I_L , 100 mA/Division

Figure 21. Continuous Conduction Mode Switching Waveform



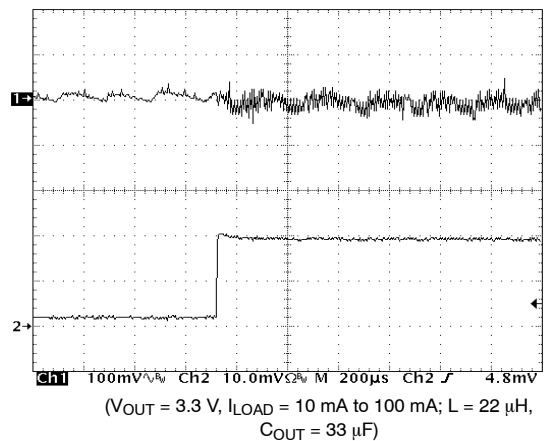
Upper Trace: Voltage at L_X pin, 2.0 V/Division
Middle Trace: Output Voltage Ripple, 50 mV/Division
Lower Trace: Inductor Current, I_L , 100 mA/Division

Figure 22. Discontinuous Conduction Mode Switching Waveform



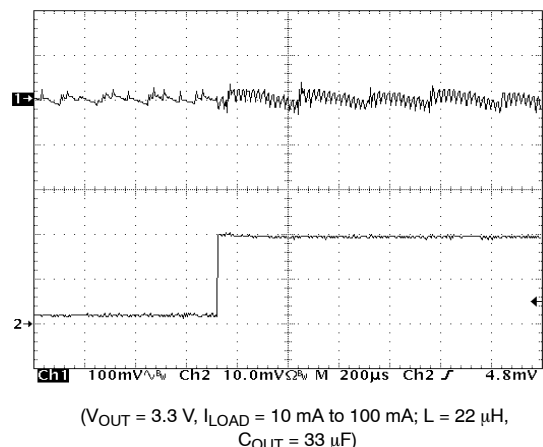
Upper Trace: Battery Voltage, V_{IN} , 1.0 V/Division
Lower Trace: Output Voltage Ripple, 100 mV/Division

Figure 23. Line Transient Response for $V_{OUT} = 3.3$ V



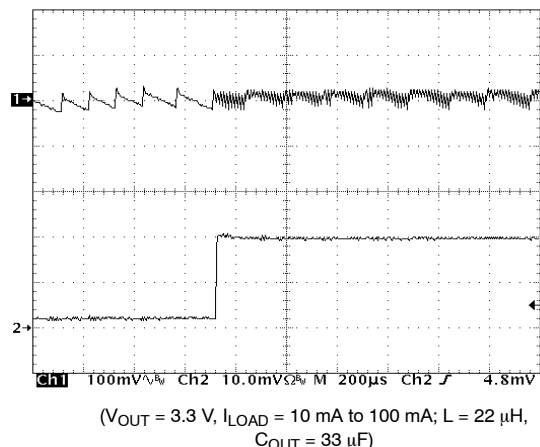
Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Load Current, I_{LOAD} , 50 mA/Division

Figure 24. Load Transient Response for $V_{IN} = 1.8$ V



Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Load Current, I_{LOAD} , 50 mA/Division

Figure 25. Load Transient Response for $V_{IN} = 2.4$ V



Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Load Current, I_{LOAD} , 50 mA/Division

Figure 26. Load Transient Response for $V_{IN} = 3.3$ V

DETAILED OPERATION DESCRIPTIONS

NCP1410 is a monolithic micropower high frequency step-up voltage switching converter IC specially designed for battery operated hand-held electronic products up to 250 mA loading. It integrates Synchronous Rectifier for improving efficiency as well as eliminating the external Schottky Diode. High switching frequency (up to 600 kHz) allows low profile inductor and output capacitor being used. Low-Battery Detector, Logic-Controlled Shutdown and Cycle-by-Cycle Current Limit provide value-added features for various battery-operated application. With all these functions ON, the quiescent supply current is only 9.0 μ A typical. This device is available in a compact Micro8 package.

PFM Regulation Scheme

From the simplified Functional Diagram (Figure 2), the output voltage is divided down and fed back to pin 1 (FB). This voltage goes to the non-inverting input of the PFM comparator whereas the comparator's inverting input is connected to REF. A switching cycle is initiated by the falling edge of the comparator, at the moment, the main switch (M1) is turned ON. After the maximum ON-time (typical 1.4 μ S) elapses or the current limit is reached, M1 is turned OFF, and the synchronous switch (M2) is turned ON. The M1 OFF time is not less than the minimum OFF-time (typical 0.31 μ S), this is to ensure energy transfer from the inductor to the output capacitor. If the regulator is operating at continuous conduction mode (CCM), M2 is turned OFF just before M1 is supposed to be ON again. If the regulator is operating at discontinuous conduction mode (DCM), which means the coil current will decrease to zero before the next cycle, M1 is turned OFF as the coil current is almost reaching zero. The comparator (ZLC) with fixed offset is dedicated to sense the voltage drop across M2 as it is conducting, when the voltage drop is below the offset, the ZLC comparator output goes HIGH, and M2 is turned OFF. Negative feedback of closed loop operation regulates voltage at pin 1 (FB) equal to the internal voltage reference (1.190 V).

Synchronous Rectification

Synchronous Rectifier is used to replace Schottky Diode for eliminating the conduction loss contributed by forward voltage of the latter. Synchronous Rectifier is normally realized by powerFET with gate control circuitry which, however, involved relative complicated timing concerns.

As main switch M1 is being turned OFF, if the synchronous switch M2 is just turned ON with M1 not being completed turned OFF, current will be shunt from the output bulk capacitor through M2 and M1 to ground. This power loss lowers overall efficiency. So a certain amount of dead time is introduced to make sure M1 is completely OFF before M2 is being turned ON.

When the main regulator is operating in CCM, as M2 is being turned OFF, and M1 is just turned ON with M2 not being completed OFF, the above mentioned situation will occur. So dead time is introduced to make sure M2 is completed OFF before M1 is being turned ON.

When the regulator is operating in DCM, as coil current is dropped to zero, M2 is supposed to be OFF. Fail to do so, reverse current will flow from the output bulk capacitor through M2 and then the inductor to the battery input. It causes damage to the battery. So the ZLC comparator comes with fixed offset voltage to switch M2 OFF before any reverse current builds up. However, if M2 is switch OFF too early, large residue coil current flows through the body diode of M2 and increases conduction loss. Therefore, determination on the offset voltage is essential for optimum performance.

With the implementation of synchronous rectification, efficiency can be as high as 92%. For single cell input voltage, use an external Schottky diode such as MBR0520 connected from pin 7 to pin 8 to ensure start-up.

Cycle-by-Cycle Current Limit

From Figure 2, SENSEFET is applied to sample the coil current as M1 is ON. With that sample current flowing through a sense resistor, sense-voltage is developed. Threshold detector (ILIM) detects whether the sense-voltage is higher than preset level. If it happens, detector output signifies the CONTROL LOGIC to switch OFF M1, and M1 can only be switched ON as next cycle starts after the minimum OFF-time (typical 0.31 μ S). With properly sizing of SENSEFET and sense resistor, the peak coil current limit is set at 1.0 A typically.

Voltage Reference

The voltage at REF is set typically at +1.190 V. It can output up to 2.5 mA with load regulation $\pm 1.5\%$, at V_{OUT} equal to 3.3 V. If V_{OUT} is increased, the REF load capability can also be increased. A bypass capacitor of 0.15 μ F is required for proper operation when REF is not loaded. If REF is loaded, 1.0 μ F capacitor at REF is needed.

Shutdown

The IC is shutdown when the voltage at pin 5 ($\overline{SHDN}$) is pulled lower than 0.3 V. During shutdown, M1 and M2 are both switched OFF, however, the body diode of M2 allows current flow from battery to the output, the IC internal circuit will consume less than 0.05 μ A current typically. If the pin 5 voltage is pull higher than 0.6 V, for example, by a resistor connected to VIN, the IC is enabled, and the internal circuit will only consume 9.0 μ A current typically from the OUT pin. Refer to Figure 2, the product of R_{SHDN} and C_{SHDN} must be larger than (500 k $\cdot$ 56 nF, i.e. 28 msec). This is to provide reset pulse for startup as battery is plugged in.

Low-Battery Detection

A comparator with 30 mV hysteresis is applied to perform the low-battery detection function. When pin 2 (LBI) is at a voltage, which can be defined by a resistor divider from the battery voltage, lower than the internal reference voltage, 1.190 V, the comparator output will cause a 50 Ohm low side switch to be turned ON. It will pull down the voltage at pin 3 (LBO) which has a hundreds kilo-Ohm of pull-high resistance. If the pin 2 voltage is higher than 1.190 V + 30 mV, the comparator output will cause the 50 Ohm low side switch to be turned OFF, pin 3 will become high impedance, and its voltage will be pulled high by the external resistor.

APPLICATIONS INFORMATION

Output Voltage Setting

The output voltage of the converter is determined by the external feedback network comprised of R_{FB1} and R_{FB2} and the relationship is given by:

$$V_{OUT} = 1.190 \text{ V} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where R_{F2} and R_{F1} are the upper and lower feedback resistors respectively.

Low Battery Detect Level Setting

The Low Battery Detect Voltage of the converter is determined by the external divider network comprised of R_{LB1} and R_{LB2} and the relationship is given by:

$$V_{LB} = 1.190 \text{ V} \times \left(1 + \frac{R_{LB1}}{R_{LB2}}\right)$$

where R_{LB1} and R_{LB2} are the upper and lower divider resistors respectively.

Inductor Selection

The NCP1410 is tested to produce optimum performance with a 22 μH inductor at $V_{IN} = 3 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$ supplying output current up to 250 mA. For other input/output requirements, inductance in the range 10 μH to 47 μH can be used according to end application specifications. Selecting an inductor is a compromise between output current capability and tolerable output voltage ripple. Of course, the first thing we need to obey is to keep the peak inductor current below its saturation limit at maximum current and the I_{LIM} of the device. In NCP1410, I_{LIM} is set at 1 A. As a rule of thumb, low inductance values supply higher output current, but also increase the ripple at output and reducing efficiency, on the other hand, high inductance values can improve output ripple and efficiency, however it also limit the output current capability at the same time. One other parameter of the inductor is its DC resistance, this resistance can introduce unwanted power loss and hence reduce overall efficiency, the basic rule is selecting an inductor with lowest DC resistance within the board space limitation of the end application.

Capacitors Selection

In all switching mode boost converter applications, both the input and output terminals sees pulsating voltage/current waveforms. The currents flowing into and out of the capacitors multiplying with the Equivalent Series Resistance (ESR) of the capacitor producing ripple voltage at the terminals. During the syn-rect switch off cycle, the charges stored in the output capacitor is used to sustain the output load current. Load current at this period and the ESR combined and reflected as ripple at the output terminals. For all cases, the lower the capacitor ESR, the lower the ripple voltage at output. As a general guide line, low ESR capacitors should be used. Ceramic capacitors have the lowest ESR, but low ESR tantalum capacitors can also be used as a cost effective substitute.

Optional Startup Schottky Diode for Low Battery Voltage

In general operation, no external Schottky diode is required, however, in case you are intended to operate the device close to 1 V level, a Schottky diode connected between the LX and OUT pins as shown in Figure 27 can help during startup of the converter. The effect of the additional Schottky was shown in Figure 8.

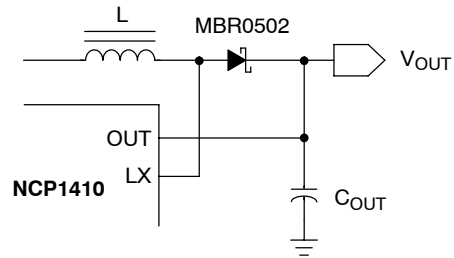


Figure 27. Schottky Device Between LX and OUT Pins

PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise and unwanted feedback that can affect the performance of the converter. Hints in the following paragraphs, can be used as guidelines in most situations.

Grounding

Star-ground connection should be used to connect the output power return ground, the input power return ground and the device power ground together at one point. All high current running paths must be thick enough for current flowing through and producing insignificant voltage drop along the path. Feedback signal path must be separated with the main current path and sensing directly at the anode of the output capacitor.

NCP1410

Components Placement

Power components, i.e. input capacitor, inductor and output capacitor, must be placed as close together as possible. All connecting traces must be short, direct and thick. High current flowing and switching paths must be kept away from the feedback (FB, pin 1) terminal to avoid unwanted injection of noise into the feedback path.

Feedback Network

Feedback of the output voltage must be a separate trace detached from the power path. External feedback network must be placed very close to the feedback (FB, pin 1) pin and sensing the output voltage directly at the anode of the output capacitor.

TYPICAL APPLICATION CIRCUIT

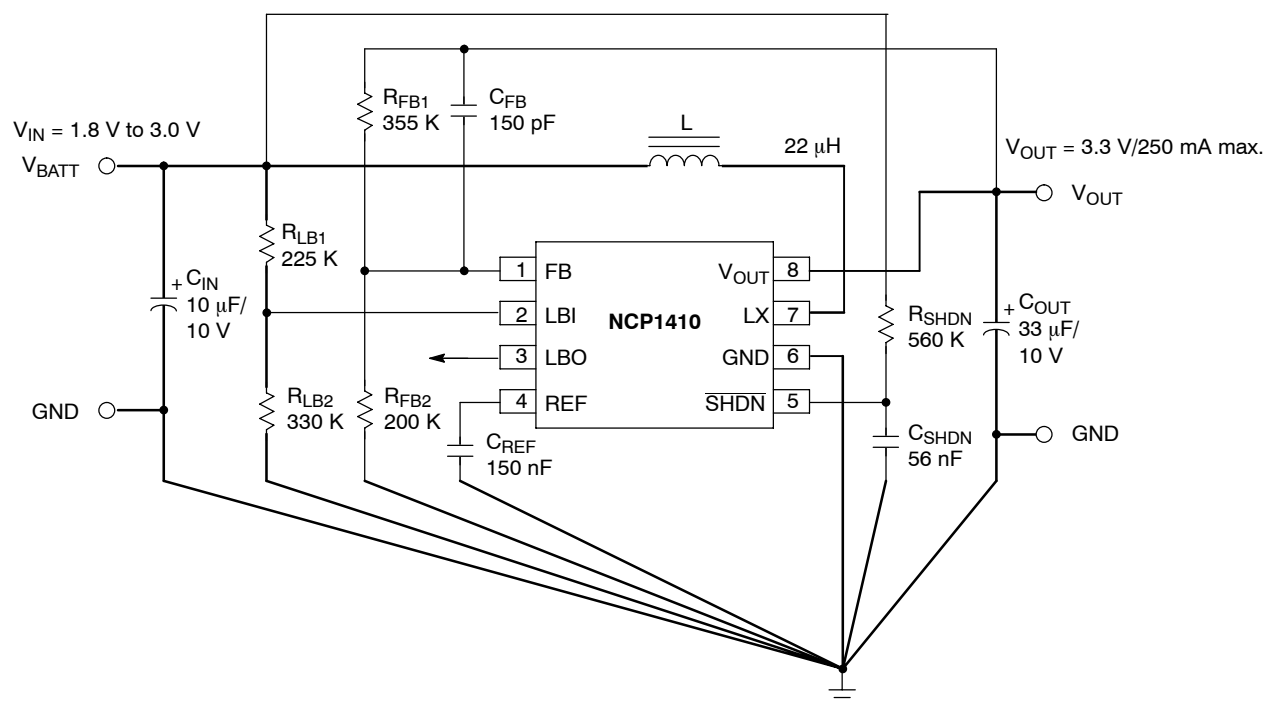


Figure 28. Typical Application Schematic for 2 Alkaline Cells Supply

GENERAL DESIGN PROCEDURES

Switching mode converter design is considered as black magic to most engineers, some complicate empirical formulae are available for reference usage. Those formulae are derived from the assumption that the key components, i.e. power inductor and capacitors are available with no tolerance. Practically, it's not true, the result is not a matter of how accurate the equations you are using to calculate the component values, the outcome is still somehow away from the optimum point. In below a simple method based on the most basic first order equations to estimate the inductor and capacitor values for NCP1410 operate in Continuous Conduction Mode is introduced. The component value set can be used as a starting point to fine tune the circuit operation. By all means, detail bench testing is needed to get the best performance out of the circuit.

Design Parameters:

$V_{IN} = 1.8 \text{ V to } 3.0 \text{ V}$, Typical 2.4 V
 $V_{OUT} = 3.3 \text{ V}$
 $I_{OUT} = 200 \text{ mA}$ (250 mA max)
 $V_{LB} = 2.0 \text{ V}$
 $V_{OUT-RIPPLE} = 40 \text{ mV}_{P-P}$ at $I_{OUT} = 250 \text{ mA}$

Calculate the feedback network:

Select $R_{FB2} = 200 \text{ K}$

$$R_{FB1} = R_{FB2} \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

$$R_{FB1} = 200 \text{ K} \left(\frac{3.3 \text{ V}}{1.19 \text{ V}} - 1 \right) = 355 \text{ K}$$

Calculate the Low Battery Detect divider:

$V_{LB} = 2.0 \text{ V}$

Select $R_{LB2} = 330 \text{ K}$

$$R_{LB1} = R_{LB2} \left(\frac{V_{LB}}{V_{REF}} - 1 \right)$$

$$R_{LB1} = 330 \text{ K} \left(\frac{2.0 \text{ V}}{1.19 \text{ V}} - 1 \right) = 225 \text{ K}$$

Determine the Steady State Duty Ratio, D for typical V_{IN} , operation will be optimized around this point:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D}$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}} = 1 - \frac{2.4 \text{ V}}{3.3 \text{ V}} = 0.273$$

Determine the average inductor current, I_{LAVG} at maximum I_{OUT} :

$$I_{LAVG} = \frac{I_{OUT}}{1 - D} = \frac{250 \text{ mA}}{1 - 0.273} = 344 \text{ mA}$$

Determine the peak inductor ripple current, $I_{RIPPLE-P}$ and calculate the inductor value:

Assume $I_{RIPPLE-P}$ is 20% of I_{LAVG} , the inductance of the power inductor can be calculated as in below:

$$I_{RIPPLE-P} = 0.20 \times 344 \text{ mA} = 68.8 \text{ mA}$$

$$L = \frac{V_{IN} \times t_{ON}}{2 I_{RIPPLE-P}} = \frac{2.4 \text{ V} \times 1.4 \mu\text{S}}{2(68.8 \text{ mA})} = 24.4 \mu\text{H}$$

Standard value of $22 \mu\text{H}$ is selected for initial trial.

Determine the output voltage ripple, $V_{OUT-RIPPLE}$ and calculate the output capacitor value:

$$V_{OUT-RIPPLE} = 40 \text{ mV}_{P-P} \text{ at } I_{OUT} = 250 \text{ mA}$$

$$C_{OUT} > \frac{I_{OUT} \times t_{ON}}{V_{OUT-RIPPLE} - I_{OUT} \times ESR_{COUT}}$$

where $t_{ON} = 1.4 \mu\text{S}$ and $ESR_{COUT} = 0.1 \Omega$,

$$C_{OUT} > \frac{250 \text{ mA} \times 1.4 \mu\text{S}}{40 \text{ mV} - 250 \text{ mA} \times 0.1 \Omega} = 23.33 \mu\text{F}$$

From above calculation, you need at least $23.33 \mu\text{F}$ in order to achieve the specified ripple level at conditions stated. Practically, a one level larger capacitor will be used to accommodate factors not take into account in the calculation, therefore a capacitor value of $33 \mu\text{F}$ is selected.

NCP1411

Sync-Rect PFM Step-Up DC-DC Converter with Low-Battery Detector and Ring-Killer

NCP1411 is a monolithic micropower high frequency Boost (step-up) voltage switching converter IC specially designed for battery operated hand-held electronic products up to 250 mA loading. It integrates Synchronous Rectifier for improving efficiency as well as eliminating the external Schottky Diode. High switching frequency (up to 600 kHz) allows low profile inductor and output capacitor being used. Low-Battery Detector, Logic-Controlled Shutdown and Cycle-by-Cycle Current Limit provide value-added features for various battery-operated applications. The innovative Ring-Killer circuitry guarantees quiet operation in discontinuous conduction mode. With all these functions ON, the device quiescent supply current is only 9.0 μ A typical. This device is available in the space saving compact Micro8™ package.

Features

- Pb-Free Package is Available
- High Efficiency, up to 92%
- Very Low Device Quiescent Supply Current of 9.0 μ A Typical
- Built-in Synchronous Rectifier (P-FET) Eliminates One External Schottky Diode
- High Switching Frequency (up to 600 kHz) Allows use of Small Size Inductor
- High Accuracy Reference Output, 1.19 V $\pm$ 0.6% @ 25°C, can supply more than 2.5 mA when $V_{OUT} \geq 3.3$ V
- Ring-Killer for Quiet Operation in Discontinuous Conduction Mode
- 1.0 V Startup at No Load Guaranteed
- Output Voltage from 1.5 V to 5.5 V Adjustable
- Output Current up to 250 mA @ $V_{IN} = 2.5$ V, $V_{OUT} = 3.3$ V
- Logic-Controlled Shutdown
- Open Drain Low-Battery Detector Output
- 1.0 A Cycle by Cycle Current Limit
- Low Profile and Minimum External Parts
- Compact Micro8 Package

Typical Applications

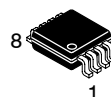
- Personal Digital Assistant (PDA)
- Handheld Digital Audio Product
- Camcorder and Digital Still Camera
- Handheld Instrument
- Conversion from One or Two NiMH or NiCd, or One Li-ion Cell to 3.3 V/5.0 V



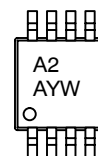
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MARKING DIAGRAM

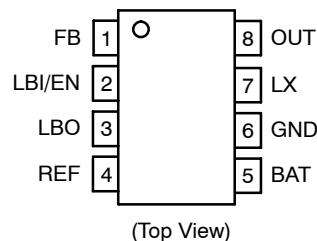


Micro8
DM SUFFIX
CASE 846A



A2 = Device Marking
A = Assembly Location
Y = Year
W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP1411DMR2	Micro8	4000 Tape & Reel
NCP1411DMR2G	Micro8 (Pb-Free)	4000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP1411

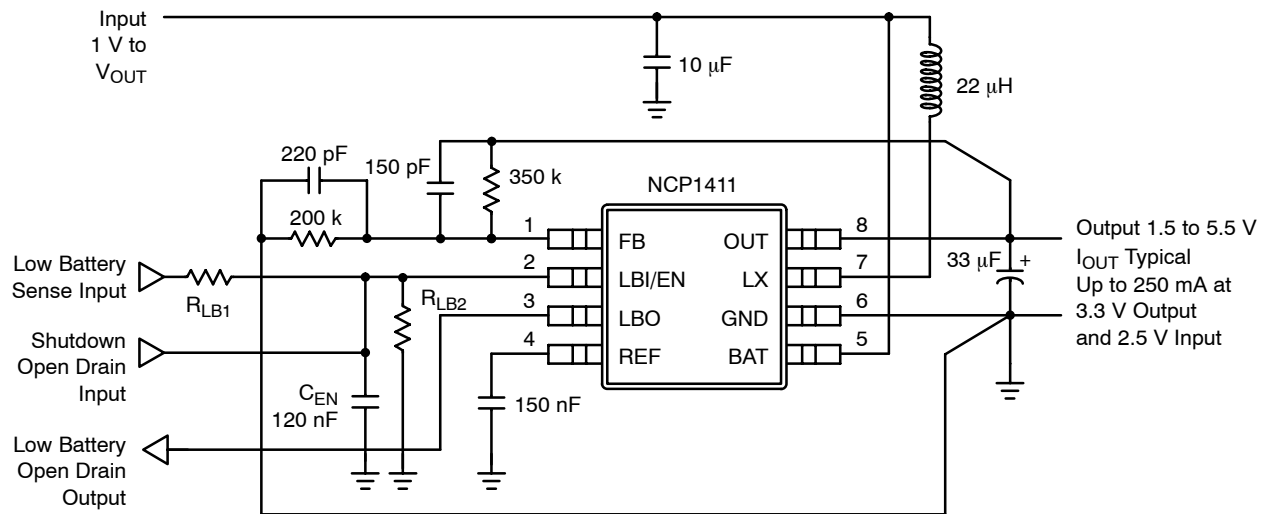


Figure 1. Typical Operating Circuit

PIN FUNCTION DESCRIPTION

Pin #	Symbol	Pin Description
1	FB	Output Voltage Feedback Input.
2	LBI/EN	Low-Battery Detector Input and IC Enable.
3	LBO	Open-Drain Low-Battery Detector Output. Output is LOW when $V_{LBI} < 1.178$ V. LBO is high impedance during shutdown.
4	REF	1.190 V Reference Voltage Output, bypassing with 150 nF capacitor if this pin is not loaded, bypassing with 1.0 μ F if this pin is loaded up to 2.5 mA @ $V_{OUT} = 3.3$ V.
5	BAT	Battery input connection for internal Ring-Killer.
6	GND	Ground.
7	LX	N-Channel and P-Channel Power MOSFET Drain Connection.
8	OUT	Power Output. OUT also provides bootstrapped power to the device.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Device Power Supply (Pin 8)	V_{OUT}	-0.3 to 6.0	V
Input/Output Pins (Pins 1-5, Pin 7)	V_{IO}	-0.3 to 6.0	V
Thermal Characteristics – Micro8 Plastic Package Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$ Thermal Resistance, Junction-to-Air	P_D $R_{\theta JA}$	520 240	mW $^\circ\text{C/W}$
Operating Junction Temperature Range	T_J	-40 to +150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- This device contains ESD protection and exceeds the following tests:
Human Body Model (HBM) ± 2.0 kV per JEDEC standard: JESD22-A114.
Machine Model (MM) ± 200 V per JEDEC standard: JESD22-A115.
- The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

- Latchup Current Maximum Rating: ± 150 mA per JEDEC standard: JESD78.
- Moisture Sensitivity Level: MSL 1 per IPC/JEDEC standard: J-STD-020A.

NCP1411

ELECTRICAL CHARACTERISTICS ($V_{OUT} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ for typical value, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for min/max values unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	V_{IN}	1.0	–	5.5	V
Output Voltage Range (Adjusted by external feedback)	V_{OUT}	V_{IN}	–	5.5	V
Reference Voltage ($C_{REF} = 150\text{ nF}$, under no loading, $T_A = 25^\circ\text{C}$)	V_{REF_NL}	1.183	1.190	1.197	V
Reference Voltage ($C_{REF} = 150\text{ nF}$, under no loading, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$)	$V_{REF\_NL\_A}$	1.178	–	1.202	V
Reference Voltage Temperature Coefficient	TC_{VREF}	–	0.03	–	mV/°C
Reference Voltage Load Current ($V_{OUT} = 3.3\text{ V}$, $V_{REF} = V_{REF\_NL} \pm 1.5\%$, $C_{REF} = 1.0\text{ }\mu\text{F}$) (Note 5)	I_{REF}	2.5	–	–	mA
Reference Voltage Load Regulation ($V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 0$ to $100\text{ }\mu\text{A}$, $C_{REF} = 1.0\text{ }\mu\text{F}$)	V_{REF_LOAD}	–	0.015	1.0	mV
Reference Voltage Line Regulation (V_{OUT} from 1.5 V to 5.5 V , $C_{REF} = 1.0\text{ }\mu\text{F}$)	V_{REF_LINE}	–	0.03	1.0	mV/V
FB, LBI Input Threshold ($I_{LOAD} = 0\text{ mA}$)	V_{FB} , V_{LBI}	1.174	1.190	1.200	V
N-FET ON Resistance	$R_{DS(ON)-N}$	–	0.6	–	Ω
P-FET ON Resistance	$R_{DS(ON)-P}$	–	0.9	–	Ω
LX Switch Current Limit (N-FET)	I_{LIM}	–	1.0	–	A
Operating Current into OUT ($V_{FB} = 1.4\text{ V}$, i.e. no switching, $V_{OUT} = 3.3\text{ V}$)	I_Q	–	9.0	14	μA
Shutdown Current into OUT (LBI/EN = GND)	I_{SD}	–	0.05	1.0	μA
LX Switch MAX. ON-Time ($V_{FB} = 1.0\text{ V}$, $V_{OUT} = 3.3\text{ V}$)	t_{ON}	1.2	1.4	1.8	μs
LX Switch MIN. OFF-Time ($V_{FB} = 1.0\text{ V}$, $V_{OUT} = 3.3\text{ V}$)	t_{OFF}	0.25	0.31	0.37	μs
FB Input Current	I_{FB}	–	1.5	9.0	nA
Shutdown Current into BAT (LBI/EN = 0 V, $V_{OUT} = V_{BAT} = 3.0\text{ V}$)	I_{LBT}	–	50	–	nA
BAT to LX resistance ($V_{FB} = 1.4\text{ V}$, $V_{OUT} = 3.3\text{ V}$)	R_{LBT_LX}	–	100	–	Ω
LBI/EN Input Current	$I_{LBI/EN}$	–	1.5	8.0	nA
LBO Low Output Voltage ($V_{LBI} = 0\text{ V}$, $I_{SINK} = 1.0\text{ mA}$)	V_{LBO_L}	–	–	0.05	V
ENABLE (Pin 2) Input threshold, Low	V_{EN}	–	–	0.3	V
ENABLE (Pin 2) Input threshold, High	V_{EN}	0.6	–	–	V

5. Loading capability increases with V_{OUT} .

NCP1411

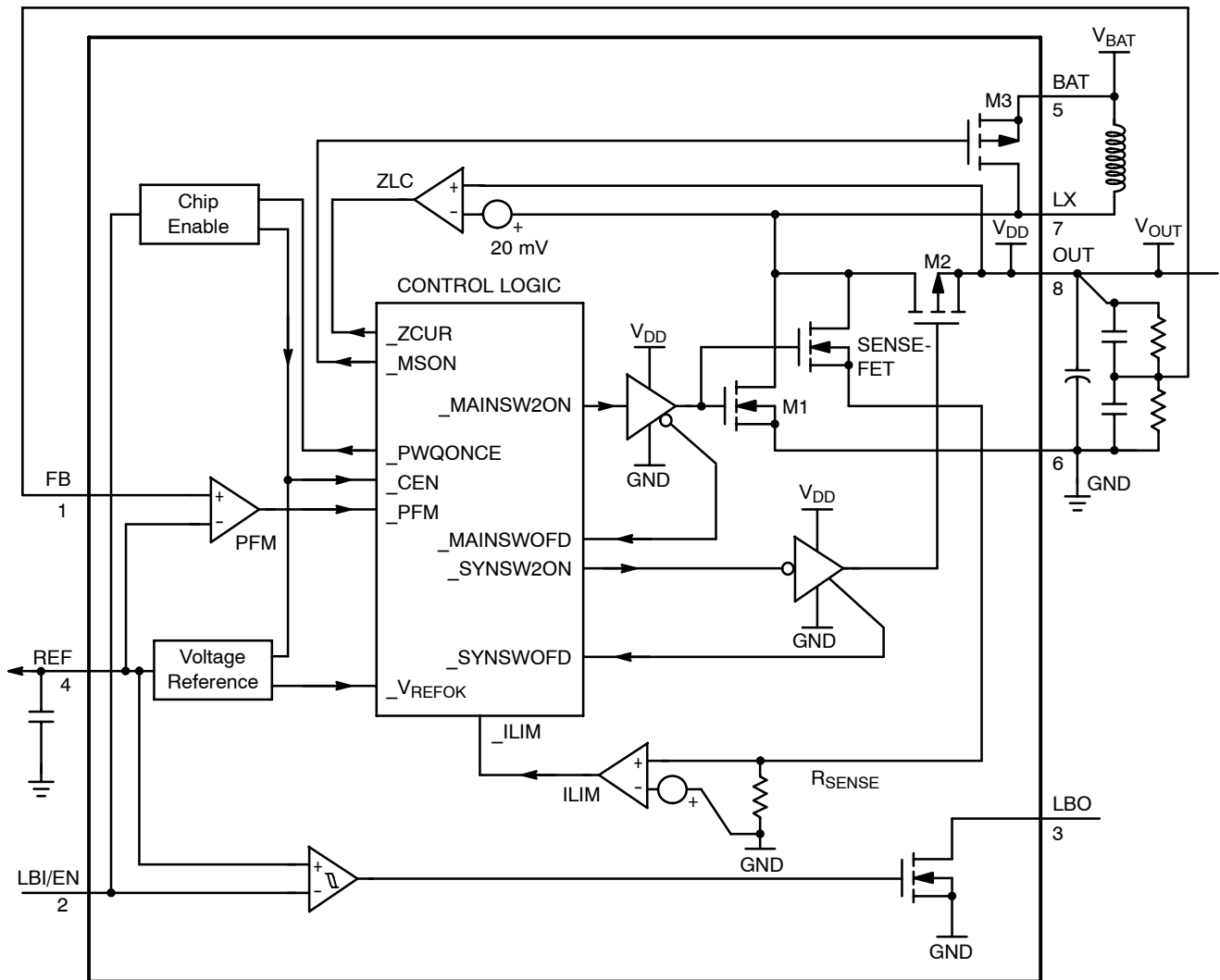


Figure 2. Simplified Functional Diagram

TYPICAL OPERATING CHARACTERISTICS

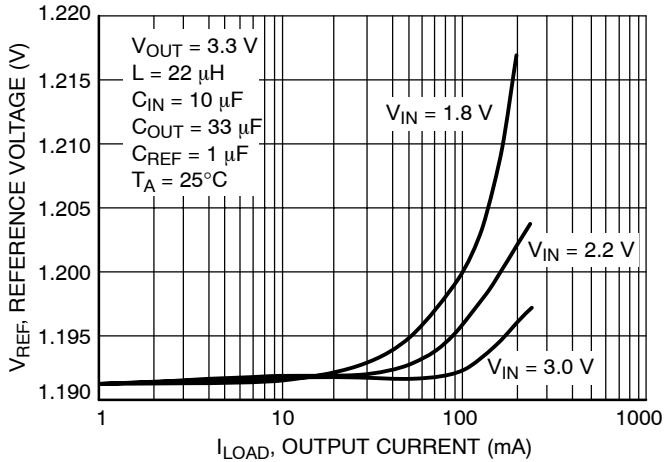


Figure 3. Reference Voltage versus Output Current

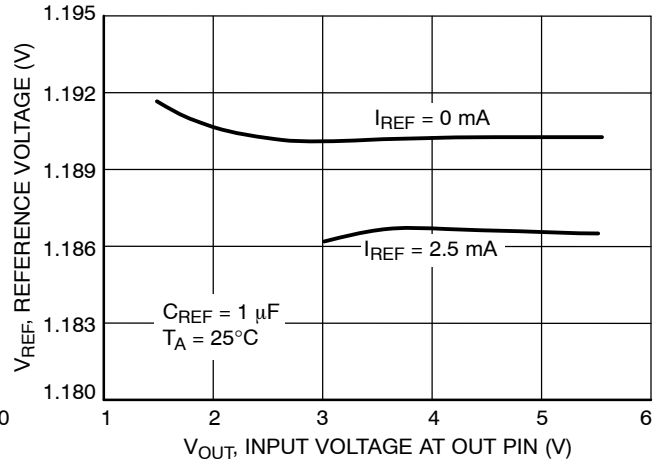


Figure 4. Reference Voltage versus Input Voltage at OUT Pin

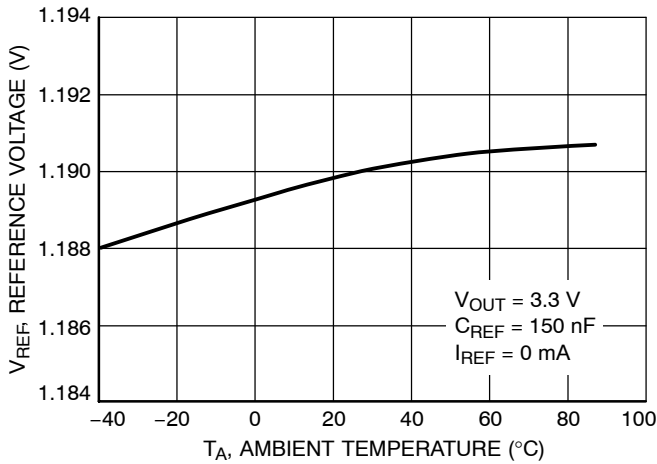


Figure 5. Reference Voltage versus Temperature

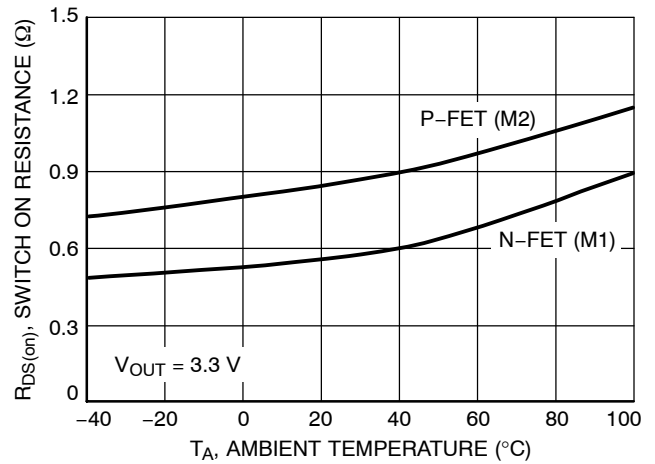


Figure 6. Switch ON Resistance versus Temperature

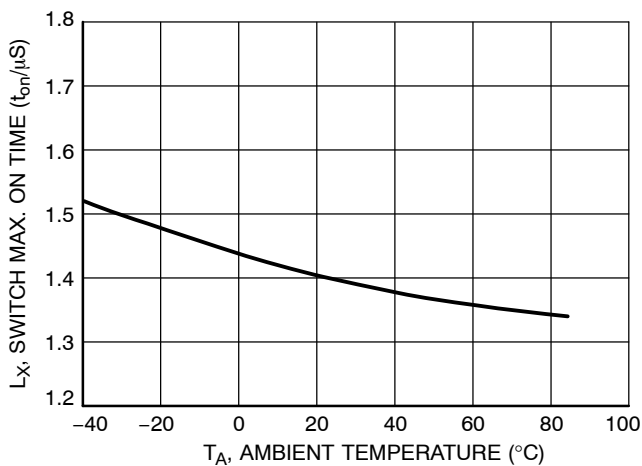


Figure 7. L_X Switch Max. ON Time versus Temperature

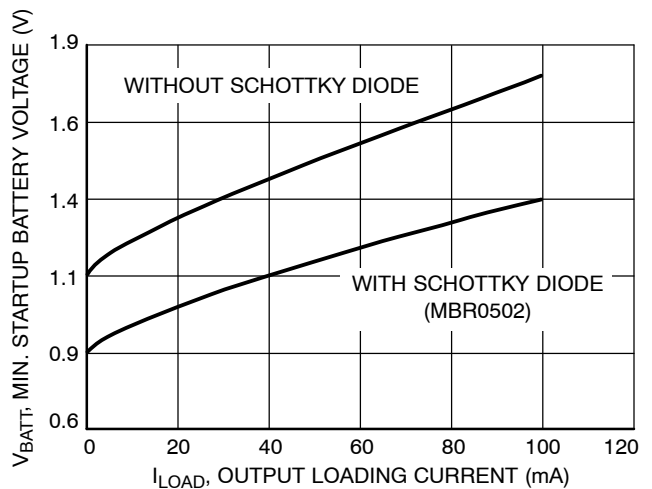


Figure 8. Min. Startup Battery Voltage versus Loading Current

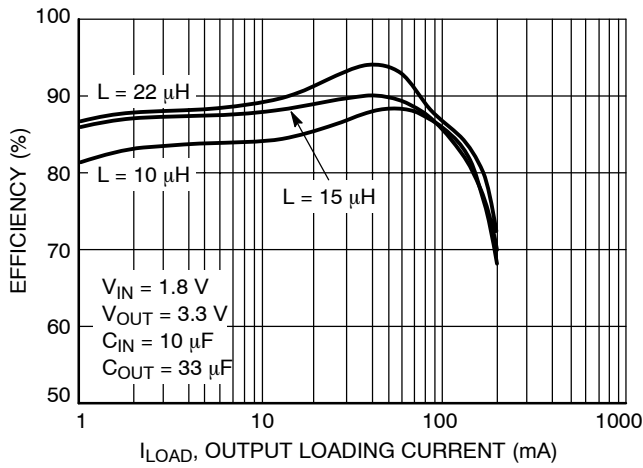


Figure 9. Efficiency versus Load Current

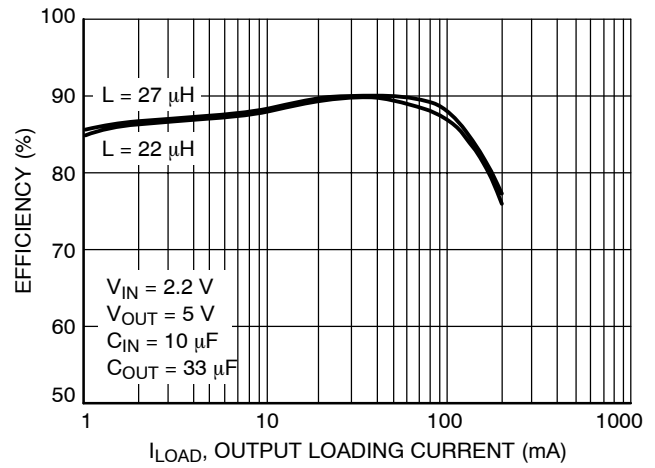


Figure 10. Efficiency versus Load Current

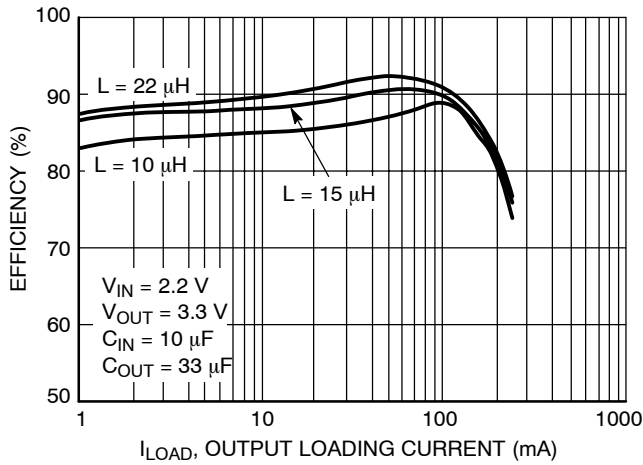


Figure 11. Efficiency versus Load Current

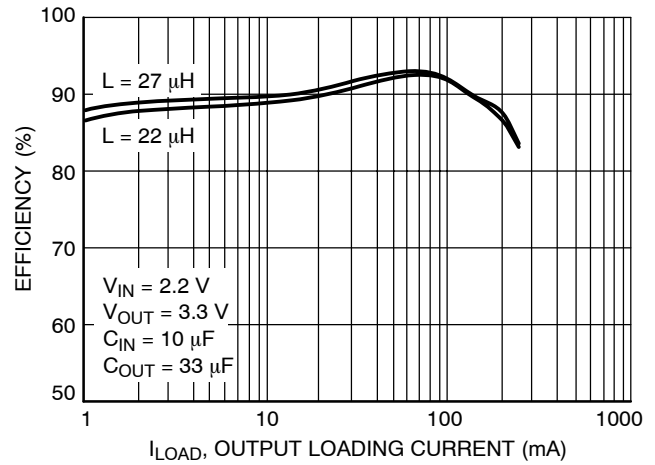


Figure 12. Efficiency versus Load Current

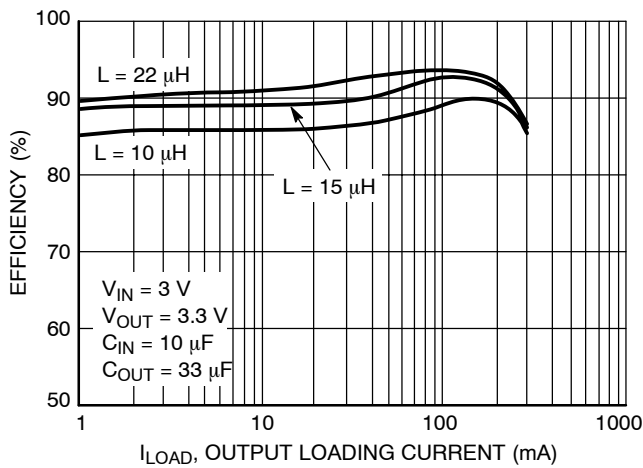


Figure 13. Efficiency versus Load Current

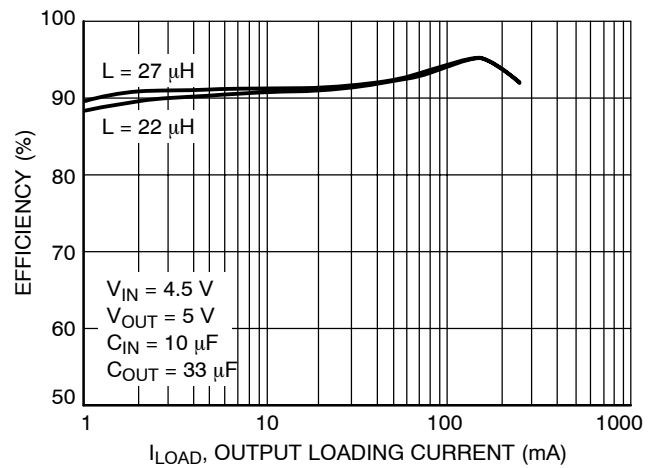


Figure 14. Efficiency versus Load Current

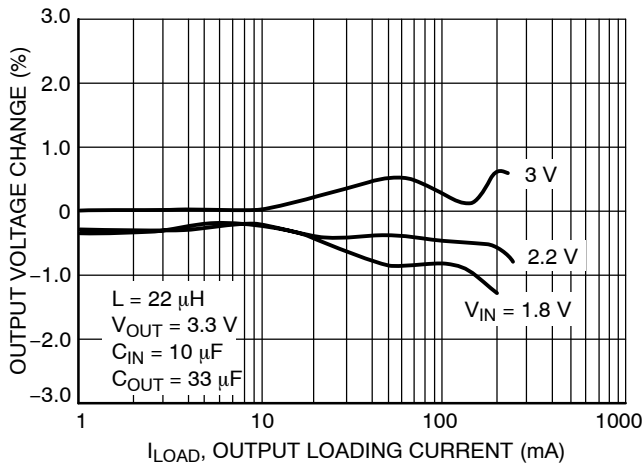


Figure 15. Output Voltage Change versus Load Current

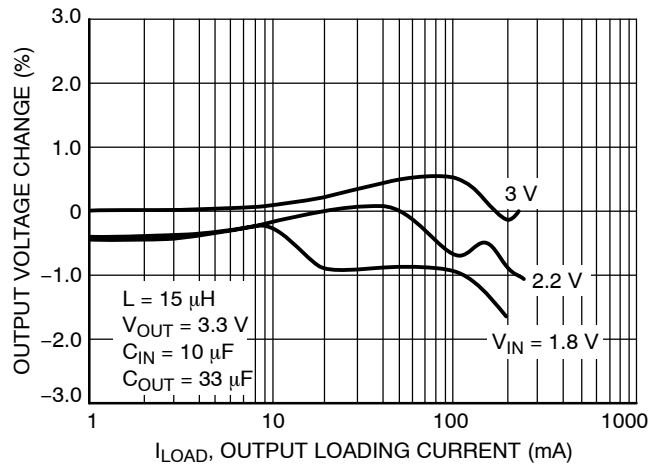


Figure 16. Output Voltage Change versus Load Current

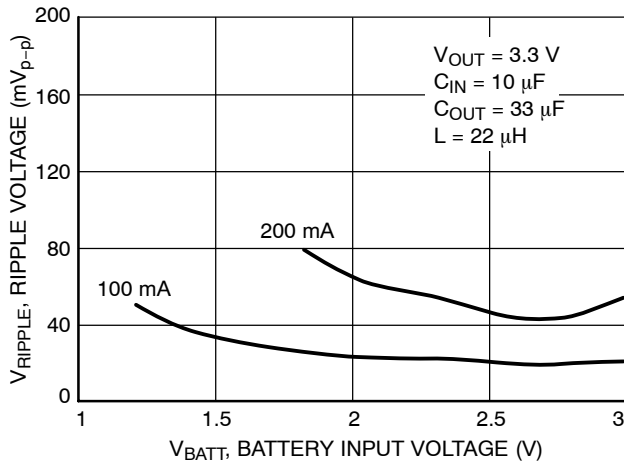


Figure 17. Battery Input Voltage versus Output Ripple Voltage

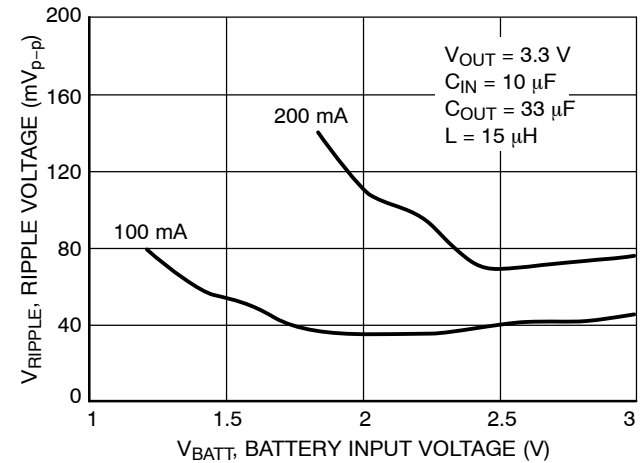


Figure 18. Battery Input Voltage versus Output Ripple Voltage

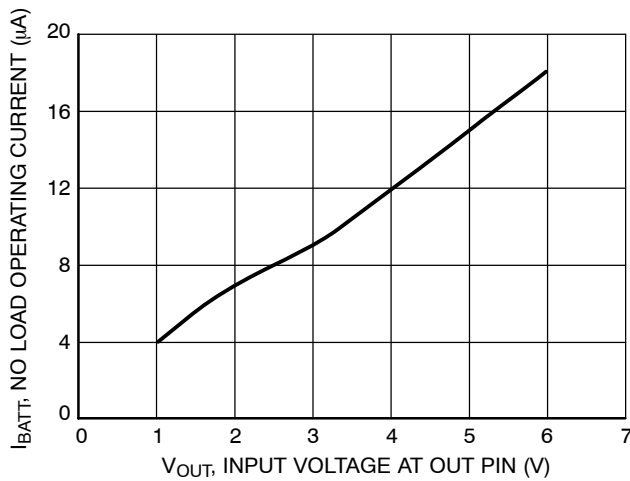
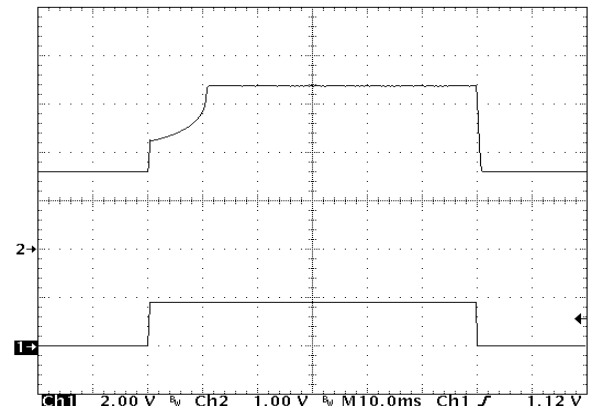


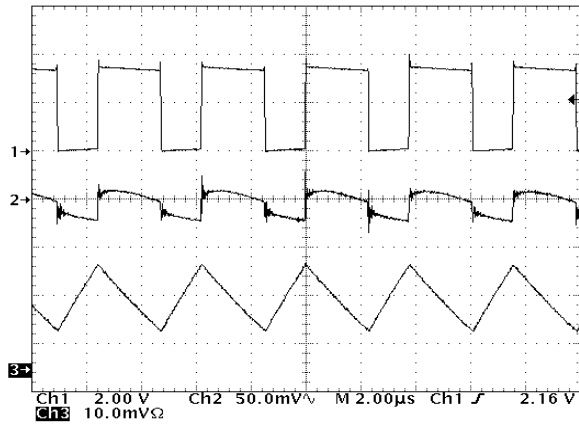
Figure 19. No Load Operating Current versus Input Voltage at OUT Pin



($V_{IN} = 2.2 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$, $I_{LOAD} = 100 \text{ mA}$; $L = 22 \mu\text{H}$, $C_{OUT} = 33 \mu\text{F}$)

Upper Trace: Output Voltage Waveform, 2.0 V/Division
Lower Trace: Shutdown Pin Waveform, 1.0 V/Division

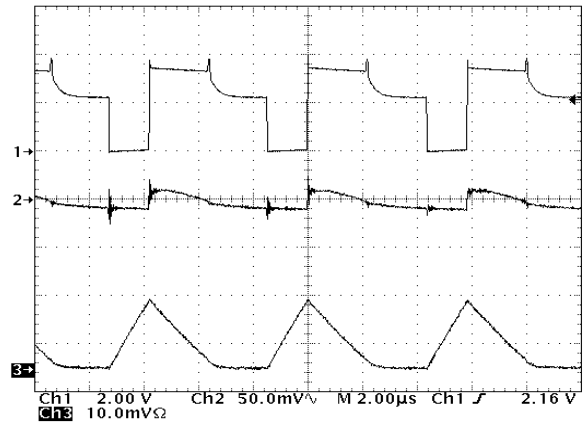
Figure 20. Startup Transient Response



($V_{IN} = 2.2\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 100\text{ mA}$; $L = 22\text{ }\mu\text{H}$, $C_{OUT} = 33\text{ }\mu\text{F}$)

Upper Trace: Voltage at L_X pin, 2.0 V/Division
Middle Trace: Output Voltage Ripple, 50 mV/Division
Lower Trace: Inductor Current, I_L , 100 mA/Division

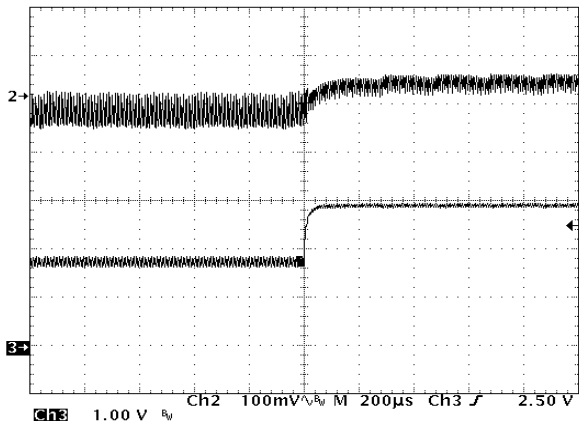
Figure 21. Continuous Conduction Mode Switching Waveform



($V_{IN} = 2.2\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 30\text{ mA}$; $L = 22\text{ }\mu\text{H}$, $C_{OUT} = 33\text{ }\mu\text{F}$)

Upper Trace: Voltage at L_X pin, 2.0 V/Division
Middle Trace: Output Voltage Ripple, 50 mV/Division
Lower Trace: Inductor Current, I_L , 100 mA/Division

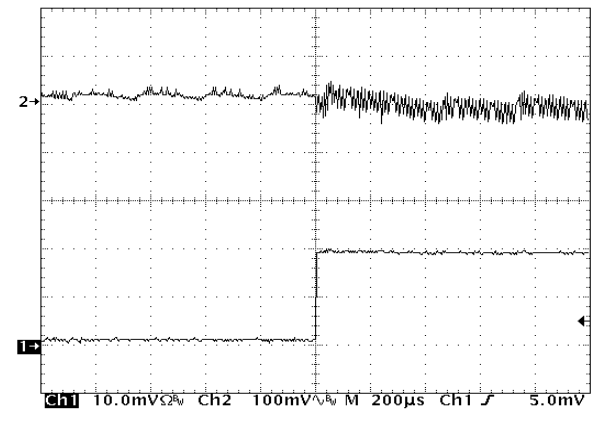
Figure 22. Discontinuous Conduction Mode Switching Waveform



($V_{IN} = 1.8\text{ V to } 3.0\text{ V}$, $L = 22\text{ }\mu\text{H}$, $C_{OUT} = 33\text{ }\mu\text{F}$)

Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Battery Voltage, V_{IN} , 1.0 V/Division

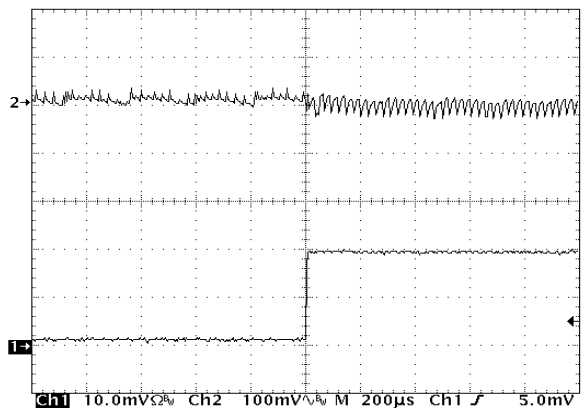
Figure 23. Line Transient Response for $V_{OUT} = 3.3\text{ V}$



($V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 10\text{ mA to } 100\text{ mA}$; $L = 22\text{ }\mu\text{H}$, $C_{OUT} = 33\text{ }\mu\text{F}$)

Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Load Current, I_{LOAD} , 50 mA/Division

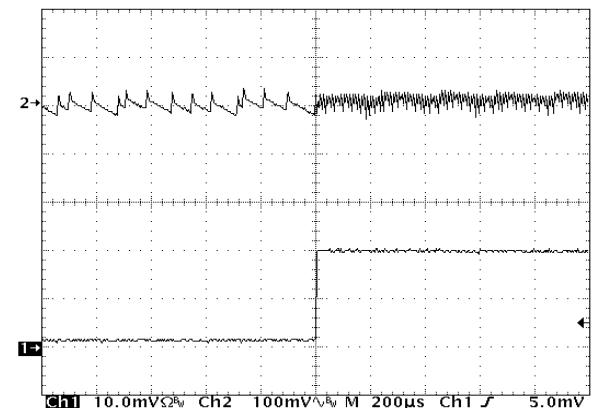
Figure 24. Load Transient Response for $V_{IN} = 1.8\text{ V}$



($V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 10\text{ mA to } 100\text{ mA}$; $L = 22\text{ }\mu\text{H}$, $C_{OUT} = 33\text{ }\mu\text{F}$)

Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Load Current, I_{LOAD} , 50 mA/Division

Figure 25. Load Transient Response for $V_{IN} = 2.4\text{ V}$



($V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 10\text{ mA to } 100\text{ mA}$; $L = 22\text{ }\mu\text{H}$, $C_{OUT} = 33\text{ }\mu\text{F}$)

Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Load Current, I_{LOAD} , 50 mA/Division

Figure 26. Load Transient Response for $V_{IN} = 3.3\text{ V}$

DETAILED OPERATION DESCRIPTIONS

NCP1411 is a monolithic micropower high frequency step-up voltage switching converter IC specially designed for battery operated hand-held electronic products up to 250 mA loading. It integrates Synchronous Rectifier for improving efficiency as well as eliminating the external Schottky Diode. High switching frequency (up to 600 kHz) allows low profile inductor and output capacitor being used. Low-Battery Detector, Logic-Controlled Shutdown and Cycle-by-Cycle Current Limit provide value-added features for various battery-operated application. With all these functions ON, the quiescent supply current is only 9.0 μ A typical. This device is available in a compact Micro8 package.

PFM Regulation Scheme

From the simplified Functional Diagram (Figure 2), the output voltage is divided down and fed back to pin 1 (FB). This voltage goes to the non-inverting input of the PFM comparator whereas the comparator's inverting input is connected to REF. A switching cycle is initiated by the falling edge of the comparator, at the moment, the main switch (M1) is turned ON. After the maximum ON-time (typical 1.4 μ S) elapses or the current limit is reached, M1 is turned OFF, and the synchronous switch (M2) is turned ON. The M1 OFF time is not less than the minimum OFF-time (typical 0.31 μ S), this is to ensure energy transfer from the inductor to the output capacitor. If the regulator is operating at Continuous Conduction Mode (CCM), M2 is turned OFF just before M1 is supposed to be ON again. If the regulator is operating at Discontinuous Conduction Mode (DCM), which means the coil current will decrease to zero before the next cycle, M1 is turned OFF as the coil current is almost reaching zero. The comparator (ZLC) with fixed offset is dedicated to sense the voltage drop across M2 as it is conducting, when the voltage drop is below the offset, the ZLC comparator output goes HIGH, and M2 is turned OFF. Negative feedback of closed loop operation regulates voltage at pin 1 (FB) equal to the internal voltage reference (1.190 V).

Synchronous Rectification

Synchronous Rectifier is used to replace Schottky Diode for eliminating the conduction loss contributed by forward voltage of the latter. Synchronous Rectifier is normally realized by powerFET with gate control circuitry which, however, involved relative complicated timing concerns.

As main switch M1 is being turned OFF, if the synchronous switch M2 is just turned ON with M1 not being completed turned OFF, current will be shunt from the output bulk capacitor through M2 and M1 to ground. This power loss lowers overall efficiency. So a certain amount of dead time is introduced to make sure M1 is completely OFF before M2 is being turned ON.

When the main regulator is operating in CCM, as M2 is being turned OFF, and M1 is just turned ON with M2 not being completely turned OFF, the above mentioned

situation will occur. So dead time is introduced to make sure M2 is completely turned OFF before M1 is being turned ON.

When the regulator is operating in DCM, as coil current is dropped to zero, M2 is supposed to be OFF. Fail to do so, reverse current will flow from the output bulk capacitor through M2 and then the inductor to the battery input. It causes damage to the battery. So the ZLC comparator comes with fixed offset voltage to switch M2 OFF before any reverse current builds up. However, if M2 is switch OFF too early, large residue coil current flows through the body diode of M2 and increases conduction loss. Therefore, determination on the offset voltage is essential for optimum performance.

With the implementation of synchronous rectification, efficiency can be as high as 92%. For single cell input voltage, use an external Schottky diode such as MBR0520 connected from pin 7 to pin 8 to ensure quick startup.

Ring-Killer

When the device entered Discontinuous Conduction Mode operation, a typical ringing at LX pin will start while the inductor current just ceased. This ringing is caused primarily by the capacitance and inductance at LX node and the result can produce unwanted EMI problem to the system. In order to eliminate this ringing, an internal damping switch (M3) is implemented to provide a low impedance path to dissipate the residue energy stored in the inductor once the operation entered the Discontinuous Conduction Mode. This feature can improve the EMI problem. The performance of the Ring-Killer switch is shown in Figure 22.

Cycle-by-Cycle Current Limit

From Figure 2, SENSEFET is applied to sample the coil current as M1 is ON. With that sample current flowing through a sense resistor, sense-voltage is developed. Threshold detector (ILIM) detects whether the sense-voltage is higher than preset level. If it happens, detector output signifies the CONTROL LOGIC to switch OFF M1, and M1 can only be switched ON as next cycle starts after the minimum OFF-time (typical 0.31 μ S). With properly sizing of SENSEFET and sense resistor, the peak coil current limit is set at 1.0 A typically.

Voltage Reference

The voltage at REF is set typically at +1.190 V. It can deliver up to 2.5 mA with load regulation $\pm 1.5\%$, at V_{OUT} equal to 3.3 V. If V_{OUT} is increased, the REF load capability can also be increased. A bypass capacitor of 0.15 μ F is required for proper operation when REF is not loaded. If REF is loaded, 1.0 μ F capacitor at REF is needed.

Shutdown

The IC will shutdown when the voltage at pin 2 (LBI/EN) is pulled lower than 0.3 V. During shutdown, M1 and M2 are both switched OFF, however, the body diode of M2 allows current flow from battery to the output, the IC internal circuit will consume less than 0.05 μ A current typically. If the

pin 1 voltage raised higher than 0.6 V, the IC will be enabled. The internal circuit will only consume 9.0 μ A current typically from the OUT pin. In order to ensure proper startup, a timing capacitor C_{EN} as shown in Figure 1 is required to provide the reset pulse during batteries are plugged in. The product of R_{LB1} and C_{EN} must be larger than 28 msec.

Low-Battery Detection

A comparator with 30 mV hysteresis is applied to perform the low-battery detection function. When pin 2 (LBI/EN) is at a voltage, which can be defined by a resistor divider from the battery voltage, lower than the internal reference voltage, 1.190 V, the comparator output will cause a 50 Ohm low side switch to be turned ON. It will pull down the voltage at pin 3 (LBO) which has a hundreds kilo-Ohm of pull-high resistance. If the pin 2 voltage is higher than 1.190 V +30 mV, the comparator output will cause the 50 Ohm low side switch to be turned OFF, pin 3 will become high impedance, and its voltage will be pulled high.

APPLICATIONS INFORMATION

Output Voltage Setting

The output voltage of the converter is determined by the external feedback network comprised of R_{FB1} and R_{FB2} and the relationship is given by:

$$V_{OUT} = 1.190 \text{ V} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where R_{FB1} and R_{FB2} are the upper and lower feedback resistors respectively.

Low Battery Detect Level Setting

The Low Battery Detect Voltage of the converter is determined by the external divider network comprised of R_{LB1} and R_{LB2} and the relationship is given by:

$$V_{LB} = 1.190 \text{ V} \times \left(1 + \frac{R_{LB1}}{R_{LB2}}\right)$$

where R_{LB1} and R_{LB2} are the upper and lower divider resistors respectively.

Inductor Selection

The NCP1411 is tested to produce optimum performance with a 22 μ H inductor at $V_{IN} = 3.0 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$ supplying output current up to 250 mA. For other input/output requirements, inductance in the range 10 μ H to 47 μ H can be used according to end application specifications. Selecting an inductor is a compromise between output current capability and tolerable output voltage ripple. Of course, the first thing we need to obey is to keep the peak inductor current below its saturation limit at maximum current and the I_{LIM} of the device. In NCP1411, I_{LIM} is set at 1.0 A. As a rule of thumb, low inductance values supply higher output current, but also increase the ripple at output and reducing efficiency, on the other hand, high inductance values can improve output ripple and efficiency, however it also limit the output current capability at the same

time. One other parameter of the inductor is its DC resistance, this resistance can introduce unwanted power loss and hence reduce overall efficiency, the basic rule is selecting an inductor with lowest DC resistance within the board space limitation of the end application.

Capacitors Selection

In all switching mode boost converter applications, both the input and output terminals sees impulsive voltage/current waveforms. The currents flowing into and out of the capacitors multiplying with the Equivalent Series Resistance (ESR) of the capacitor producing ripple voltage at the terminals. During the syn-rect switch off cycle, the charges stored in the output capacitor is used to sustain the output load current. Load current at this period and the ESR combined and reflected as ripple at the output terminal. For all cases, the lower the capacitor ESR, the lower the ripple voltage at output. As a general guide line, low ESR capacitors should be used. Ceramic capacitors have the lowest ESR, but low ESR tantalum capacitors can also be used as a cost effective substitute.

Optional Startup Schottky Diode for Low Battery Voltage

In general operation, no external schottky diode is required, however, in case you are intended to operate the device close to 1.0 V level, a schottky diode connected between the LX and OUT pins as shown in Figure 27 can help during startup of the converter. The effect of the additional schottky was shown in Figure 8.

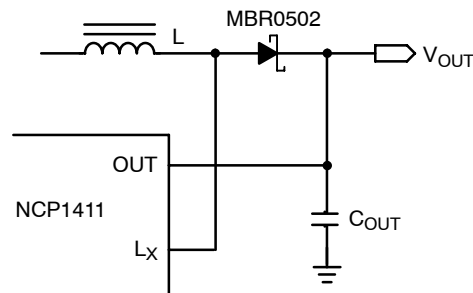


Figure 27. PCB Layout Recommendations

PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise and unwanted feedback that can affect the performance of the converter. Hints suggested in below can be used as a guide line in most situations.

Grounding

Star-ground connection should be used to connect the output power return ground, the input power return ground and the device power ground together at one point. All high current running paths must be thick enough for current flowing through and producing insignificant voltage drop

NCP1411

along the path. Feedback signal path must be separated with the main current path and sensing directly at the anode of the output capacitor.

Components Placement

Power components, i.e. input capacitor, inductor and output capacitor, must be placed as close together as possible. All connecting traces must be short, direct and thick. High current flowing and switching paths must be

kept away from the feedback (FB, pin 1) terminal to avoid unwanted injection of noise into the feedback path.

Feedback Network

Feedback of the output voltage must be a separate trace detached from the power path. External feedback network must be placed very close to the feedback (FB, pin 1) pin and sensing the output voltage directly at the anode of the output capacitor.

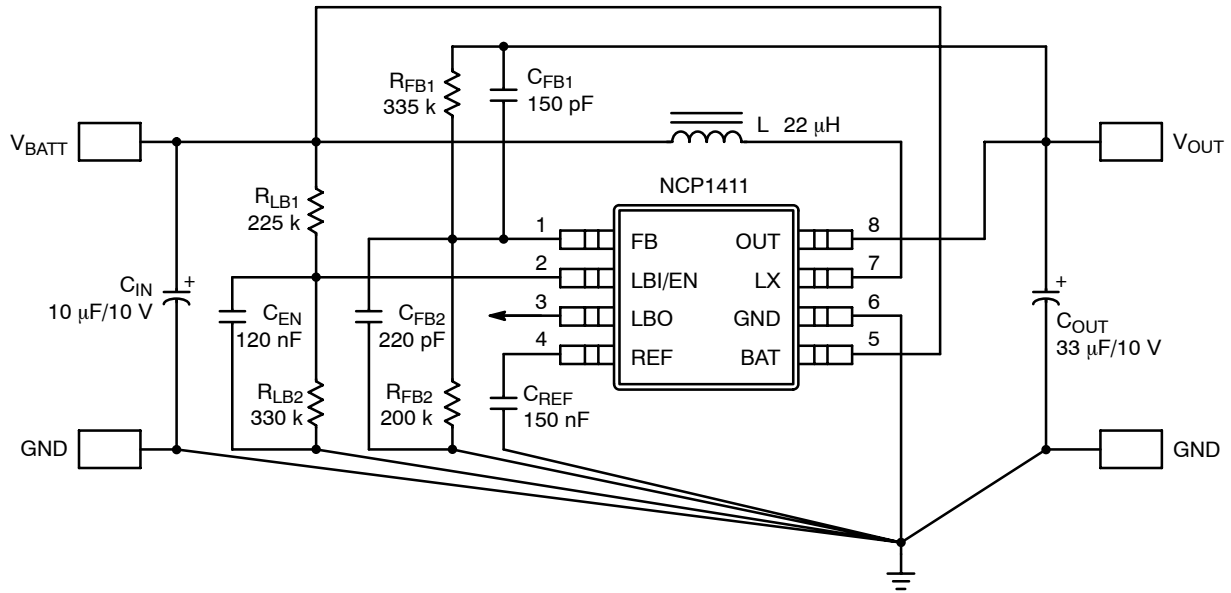


Figure 28. Typical Application Schematic for 2 Alkaline Cells Supply

GENERAL DESIGN PROCEDURES

Switching mode converter design is considered as black magic to most engineers, some complicate empirical formulae are available for reference usage. Those formulae are derived from the assumption that the key components, i.e. power inductor and capacitors are available with no tolerance. Practically, its not true, the result is not a matter of how accurate the equations you are using to calculate the component values, the outcome is still somehow away from the optimum point. In below a simple method base on the most basic first order equations to estimate the inductor and capacitor values for NCP1411 operate in Continuous Conduction Mode is introduced. The component value set can be used as a starting point to fine tune the circuit operation. By all means, detail bench testing is needed to get the best performance out of the circuit.

Design Parameters:

V_{IN} = 1.8 V to 3.0 V, Typical 2.4 V
 V_{OUT} = 3.3 V
 I_{OUT} = 200 mA (250 mA max)
 V_{LB} = 2.0 V
 $V_{OUT-RIPPLE}$ = 40 mV_{P-P} at $I_{OUT} = 250$ mA

Calculate the feedback network:

Select $R_{FB2} = 200$ K

$$R_{FB1} = R_{FB2} \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

$$R_{FB1} = 200 \text{ K} \left(\frac{3.3 \text{ V}}{1.19 \text{ V}} - 1 \right) = 355 \text{ K}$$

With the feedback resistor divider, additional small capacitor, C_{FB1} in parallel with R_{FB1} is required to ensure stability. The value can be in between 68 pF to 220 pF, the rule is to select the lowest capacitance to ensure stability. Also a small capacitor, C_{FB2} in parallel with R_{FB2} may also be needed to lower the feedback ripple hence improve output regulation. The use of C_{FB2} is a compromise between output ripple level and regulation, so careful selection of the value according to end application requirement is needed. In this example, values for C_{FB1} and C_{FB2} are 150 pF and 220 pF respectively.

Calculate the Low Battery Detect divider:

V_{LB} = 2.0 V
 Select $R_{LB2} = 330$ K

$$R_{LB1} = R_{LB2} \left(\frac{V_{LB}}{V_{REF}} - 1 \right)$$

$$R_{LB1} = 330 \text{ K} \left(\frac{2.0 \text{ V}}{1.19 \text{ V}} - 1 \right) = 225 \text{ K}$$

$$C_{EN} = \frac{28 \text{ msec}}{225 \text{ K}} = 120 \text{ nF}$$

Determine the Steady State Duty Ratio, D for typical V_{IN} , operation will be optimized around this point:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D}$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}} = 1 - \frac{2.4 \text{ V}}{3.3 \text{ V}} = 0.273$$

Determine the average inductor current, I_{LAVG} at maximum I_{OUT} :

$$I_{LAVG} = \frac{I_{OUT}}{1 - D} = \frac{250 \text{ mA}}{1 - 0.273} = 344 \text{ mA}$$

Determine the peak inductor ripple current, $I_{RIPPLE-P}$ and calculate the inductor value:

Assume $I_{RIPPLE-P}$ is 20% of I_{LAVG} , the inductance of the power inductor can be calculated as in below:

$$I_{RIPPLE-P} = 0.20 \times 344 \text{ mA} = 68.8 \text{ mA}$$

$$L = \frac{V_{IN} \times t_{ON}}{2I_{RIPPLE-P}} = \frac{2.4 \text{ V} \times 1.4 \mu\text{S}}{2(68.8 \text{ mA})} = 24.4 \mu\text{H}$$

Standard value of 22 μH is selected for initial trial.

Determine the output voltage ripple, $V_{OUT-RIPPLE}$ and calculate the output capacitor value:

$$V_{OUT-RIPPLE} = 40 \text{ mV}_{P-P} \text{ at } I_{OUT} = 250 \text{ mA}$$

$$C_{OUT} \geq \frac{I_{OUT} \times t_{ON}}{V_{OUT} - RIPPLE - I_{OUT} \times ESR_{COUT}}$$

where $t_{ON} = 1.4 \mu\text{S}$ and $ESR_{COUT} = 0.1 \Omega$,

$$C_{OUT} \geq \frac{250 \text{ mA} \times 1.4 \mu\text{S}}{40 \text{ mV} - 250 \text{ mA} \times 0.1 \Omega} = 23.33 \mu\text{F}$$

From above calculation, we need at least 23.33 μF in order to achieve the specified ripple level at conditions stated. Practically, a one level larger capacitor will be used to accommodate factors not take into account in the calculation. So a capacitor value of 33 μF is selected.

NCP1417

200 mA DC-DC Step-up Converter with Dual Low Battery Protection

NCP1417 is a monolithic micropower high frequency Boost (step-up) voltage switching converter IC specially designed for battery operated hand-held electronic products up to 200 mA loading. It integrates Synchronous Rectifier for improving efficiency as well as eliminating the external Schottky Diode. High switching frequency (up to 600 kHz) allows use of a low profile inductor and output capacitor. Dual Low-Battery Detectors and Cycle-by-Cycle Current Limit provide value-added features for various battery-operated applications. With all these functions ON, the quiescent supply current is only 9.0 μ A typical. This device is available in a space saving compact Micro8™ package.

Features

- High Efficiency, Up to 92%, Typical
- Very Low Device Quiescent Supply Current of 9.0 μ A Typical
- Built-in Synchronous Rectifier (P-FET) Eliminates One External Schottky Diode
- High Switching Frequency (Up to 600 kHz) Allows Small Size Inductor and Capacitor
- High Accuracy Reference Output, 1.19 V $\pm$ 0.6% @ 25°C, Can Supply More Than 2.5 mA when $V_{OUT} \geq 3.3$ V
- 1.0 V Startup at No Load Guaranteed
- Output Voltage from 1.5 V to 5.5 V Adjustable
- Output Current Up to 200 mA @ $V_{in} = 2.5$ V, $V_{out} = 3.3$ V
- Multi-Function LBI/Shutdown Control Pin
- Dual Open Drain Low-Battery Detector Outputs
- 1.0 A Cycle by Cycle Current Limit
- Low Profile and Minimum External Parts
- Compact Micro8 Package

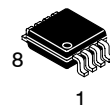
Applications

- Personal Digital Assistants (PDA)
- Handheld Digital Audio Product
- Camcorders and Digital Still Camera
- Handheld Instrument
- Conversion from One or Two NiMH or NiCd or One Lithium-ion Cells to 3.3 V/5.0 V



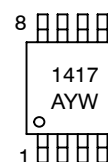
ON Semiconductor®

<http://onsemi.com>



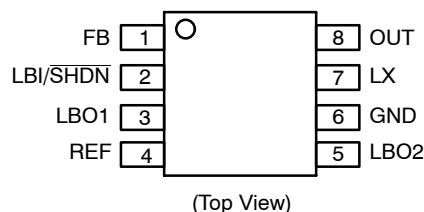
Micro8
DM SUFFIX
CASE 846A

MARKING DIAGRAM



1417 = Device Marking
A = Assembly Location
Y = Year
W = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCP1417DMR2	Micro8	4000 Tape & Reel

NCP1417

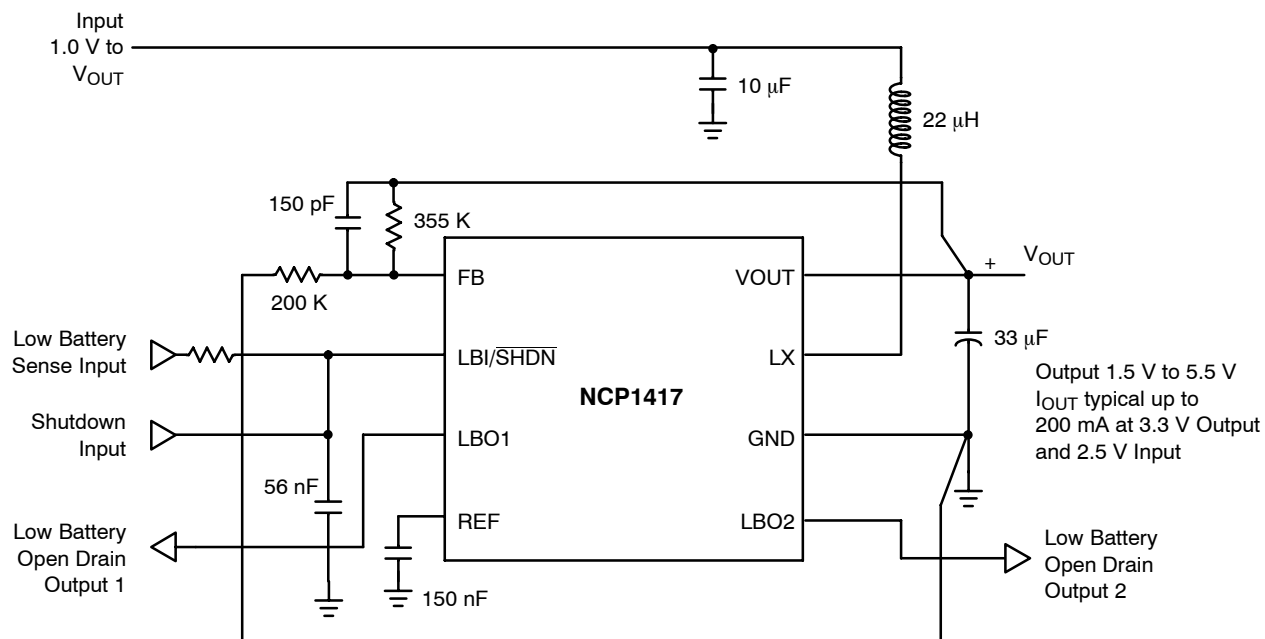


Figure 1. Typical Operating Circuit

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply (Pin 8)	V_{OUT}	-0.3 to 6.0	V
Input/Output Pins Pin 1-5, Pin 7	V_{IO}	-0.3 to 6.0	V
Thermal Characteristics Micro8 Plastic Package Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$ Thermal Resistance Junction to Air	P_D $R_{\theta JA}$	520 240	mW $^\circ\text{C/W}$
Operating Junction Temperature Range	T_J	-40 to +150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^\circ\text{C}$

- This device contains ESD protection and exceeds the following tests:
Human Body Model (HBM) ± 2.0 kV per JEDEC standard: JESD22-A114.
Machine Model (MM) ± 200 V per JEDEC standard: JESD22-A115.
- The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_J(\text{max}) - T_A}{R_{\theta JA}}$$

- Latch-up Current Maximum Rating: ± 150 mA per JEDEC standard: JESD78.
- Moisture Sensitivity Level: MSL 1 per IPC/JEDEC standard: J-STD-020A.

NCP1417

ELECTRICAL CHARACTERISTICS ($V_{OUT} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ for typical value, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for min/max values unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Voltage	V_{IN}	1.0	–	5.5	V
Output Voltage Range (Adjusted by External Feedback)	V_{OUT}	V_{IN}	–	5.5	V
Reference Voltage ($C_{REF} = 150\text{ nF}$, Under No Loading, $T_A = 25^\circ\text{C}$)	V_{REF_NL}	1.183	1.190	1.197	V
Reference Voltage ($C_{REF} = 150\text{ nF}$, Under No Loading, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$)	$V_{REF\_NL\_A}$	1.178	–	1.202	V
Reference Voltage Temperature Coefficient	TC_{VREF}	–	0.03	–	mV/ $^\circ\text{C}$
Reference Voltage Load Current ($V_{OUT} = 3.3\text{ V}$, $V_{REF} = V_{REF\_NL} \pm 1.5\%$, $C_{REF} = 1.0\text{ }\mu\text{F}$) (Note 5)	I_{REF}	2.5	–	–	mA
Reference Voltage Load Regulation ($V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 0\text{ to }100\text{ }\mu\text{A}$, $C_{REF} = 1.0\text{ }\mu\text{F}$)	V_{REF_LOAD}	–	0.015	1.0	mV
Reference Voltage Line Regulation	V_{REF_LINE}	–	0.03	1.0	mV/V
FB, LBI Input Threshold	V_{FB} , V_{LBI}	1.172	1.190	1.200	V
Internal NFET ON-Resistance ($I_{LX} = 100\text{ mA}$)	$R_{DS(ON)\_N}$	–	0.65	–	Ω
Internal PFET ON-Resistance ($I_{LX} = 100\text{ mA}$)	$R_{DS(ON)\_P}$	–	1.3	–	Ω
LX Switch Current Limit (NFET)	I_{LIM}	–	1.0	–	A
Operating Current into OUT ($V_{FB} = 1.4\text{ V}$, i.e. No Switching, $V_{OUT} = 3.3\text{ V}$)	I_Q	–	9.0	14	μA
Shutdown Current into OUT (SHDN = GND)	I_{SD}	–	0.05	1.0	μA
LX Switch MAX. ON-Time ($V_{FB} = 1.0\text{ V}$, $V_{OUT} = 3.3\text{ V}$)	t_{ON}	0.8	1.4	2.0	μs
LX Switch MIN. OFF-Time ($V_{FB} = 1.0\text{ V}$, $V_{OUT} = 3.3\text{ V}$)	t_{OFF}	0.22	0.25	0.46	μs
FB Input Current	I_{FB}	–	1.5	20	nA
LBI/SHDN Input Current	I_{LBI} , I_{SHDN}	–	1.5	8.0	nA
LBO1/LBO2 Low Output Voltage ($V_{LBI} = 0$, $I_{SINK} = 1.0\text{ mA}$)	V_{LBO_L1} V_{LBO_L2}	– –	– –	0.08 0.08	V
LBI/SHDN Input Threshold for LBO1	V_{LBI1}	1.172	1.190	1.200	V
LBI/SHDN Input Threshold for LBO2	V_{LBI2}	0.904	0.944	0.965	V
LBI/SHDN Input Threshold, Low	V_{SHDN_L}	–	–	0.3	V
LBI/SHDN Input Threshold, High	V_{SHDN_H}	0.6	–	–	V

5. Loading capability decreases with V_{OUT} .

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Pin Description
1	FB	Output Voltage Feedback Input.
2	LBI/SHDN	Low-Battery Detector Input and Shutdown Control input multi-function pin.
3	LBO1	Open-Drain Low-Battery Detector Output. Output is LOW when V_{LBI} is $< 1.172\text{ V}$. LBO1 is high impedance during shutdown.
4	REF	1.190 V Reference Voltage Output, bypassing with 150 nF capacitor if this pin is not loaded, bypassing with 1 μF if this pin is loaded up to 2.5 mA @ $V_{OUT} = 3.3\text{ V}$.
5	LBO2	Open-Drain Low-Battery Detector Output. Output is LOW when V_{LBI} is $< 0.904\text{ V}$. LBO2 is high impedance during shutdown.
6	GND	Ground
7	LX	N-Channel and P-Channel Power MOSFET Drain Connection.
8	OUT	Power Output. OUT provides bootstrap power to the IC.

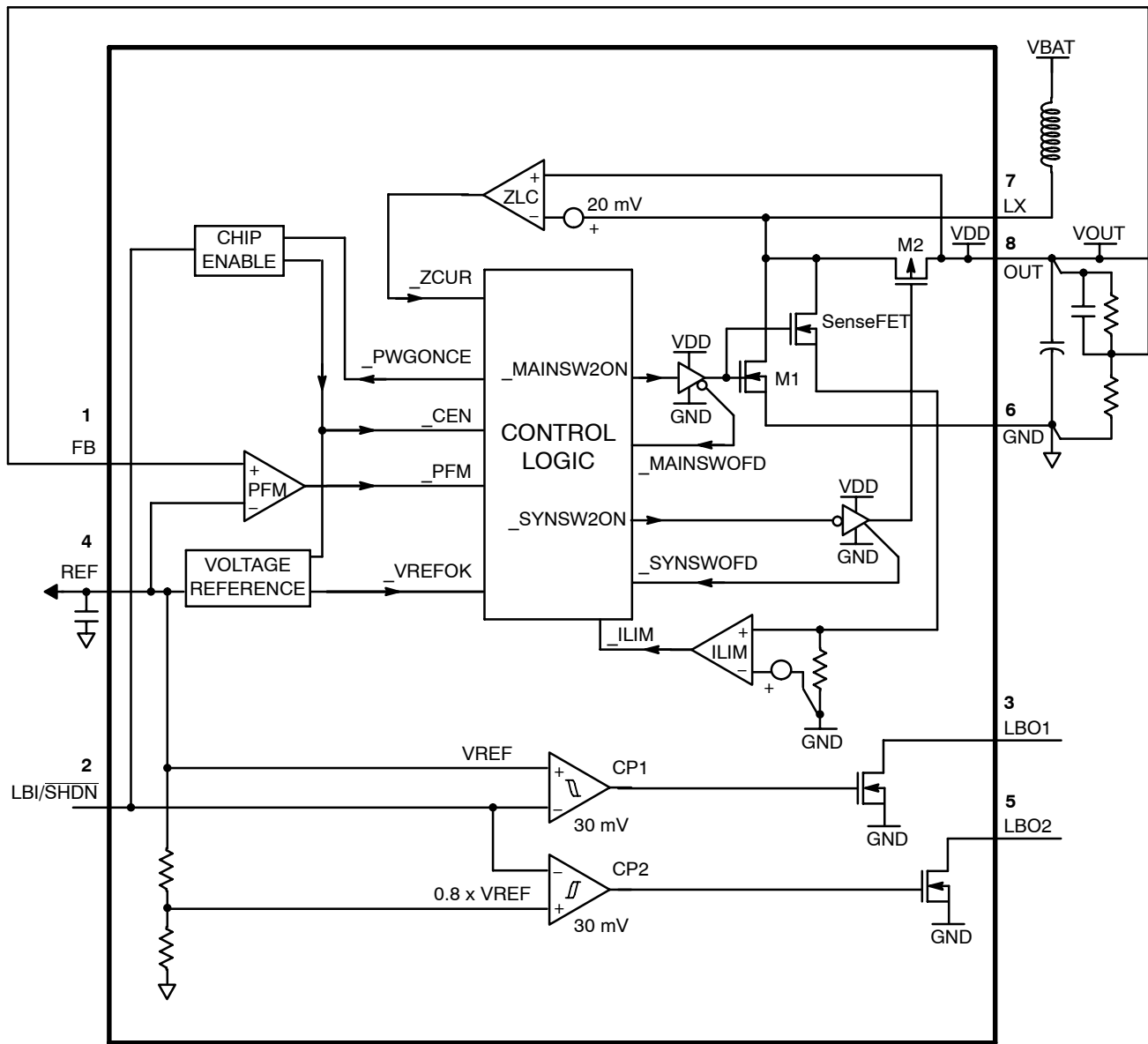


Figure 2. Simplified Functional Diagram

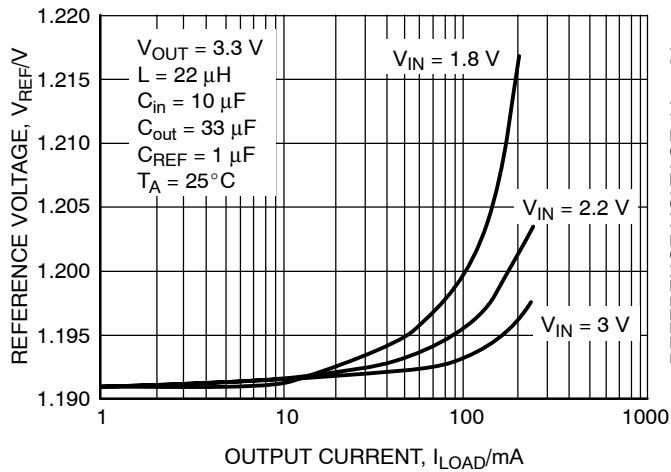


Figure 3. Reference Voltage versus Output Current

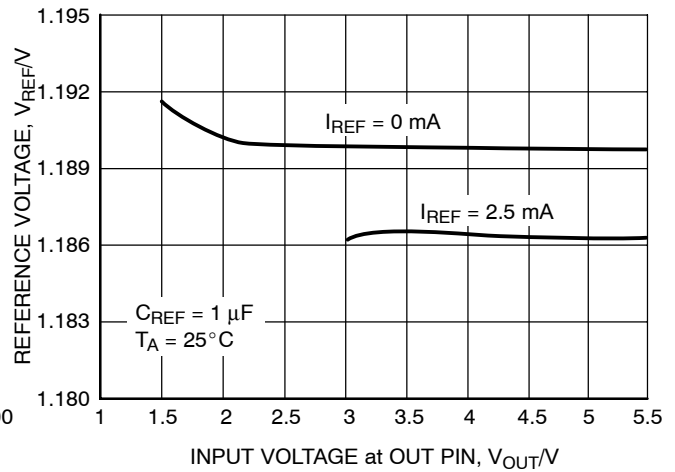


Figure 4. Reference Voltage versus Input Voltage at OUT Pin

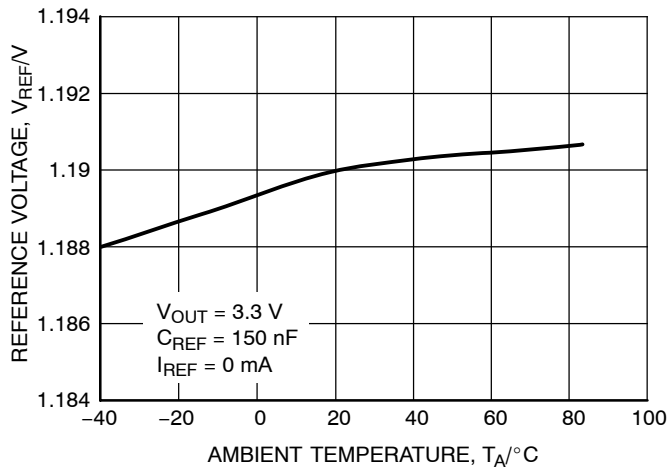


Figure 5. Reference Voltage versus Temperature

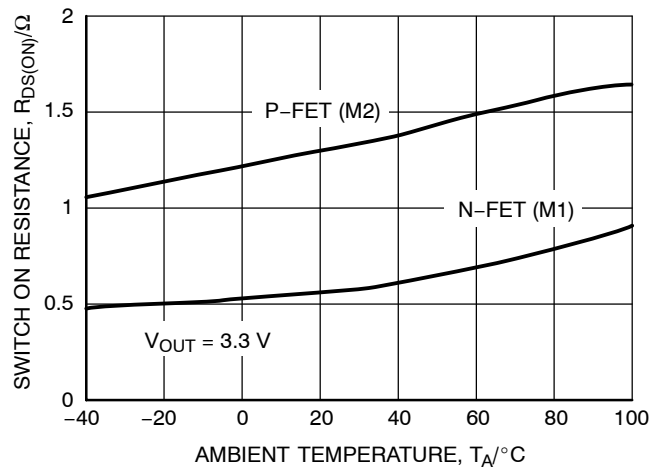


Figure 6. Switch ON Resistance versus Temperature

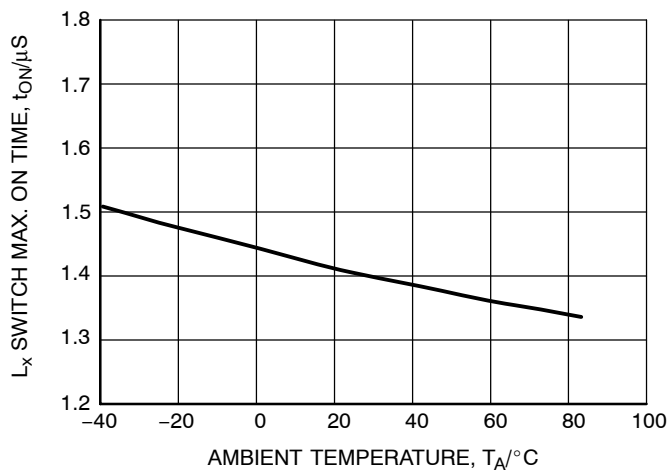


Figure 7. L_x Switch Max. ON Time versus Temperature

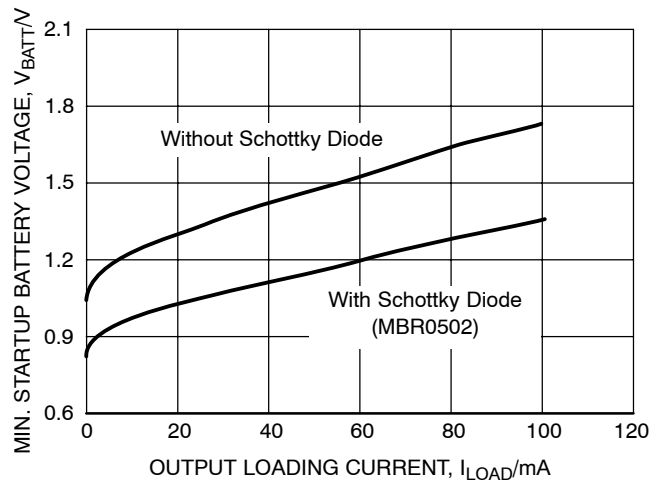


Figure 8. Min. Startup Battery Voltage versus Loading Current

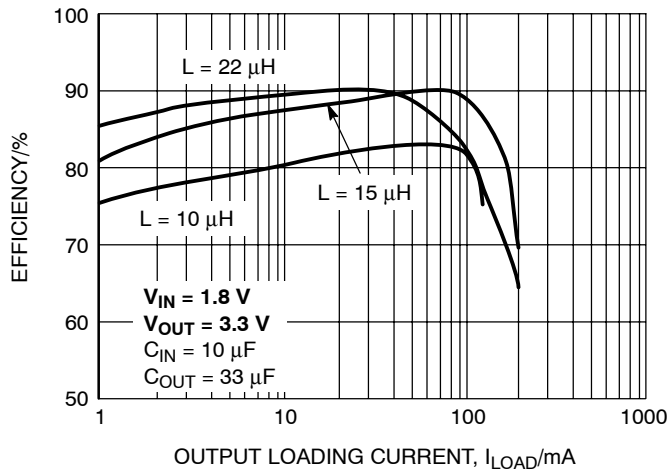


Figure 9. Efficiency versus Load Current

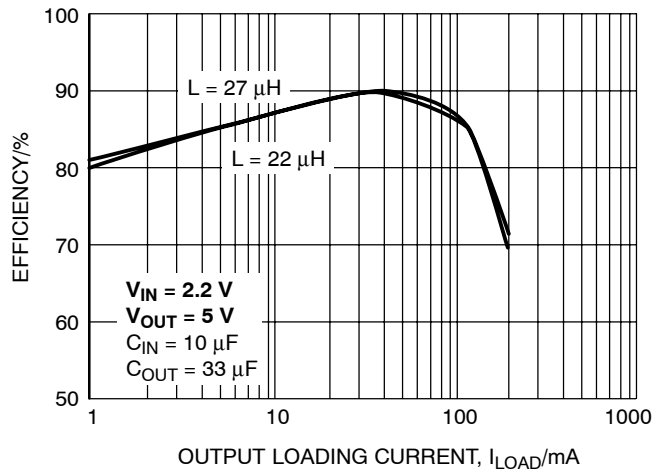


Figure 10. Efficiency versus Load Current

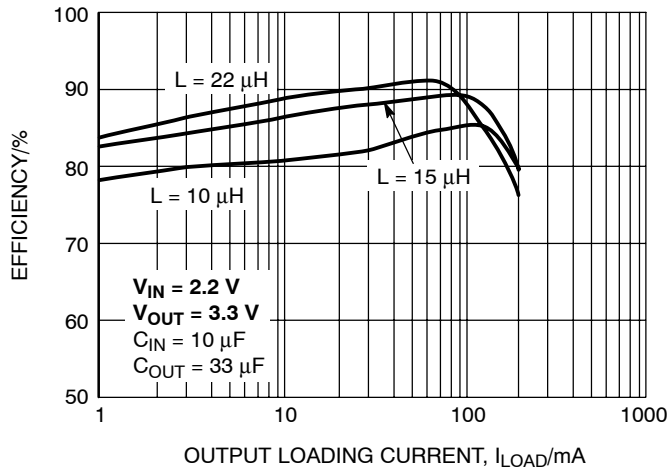


Figure 11. Efficiency versus Load Current

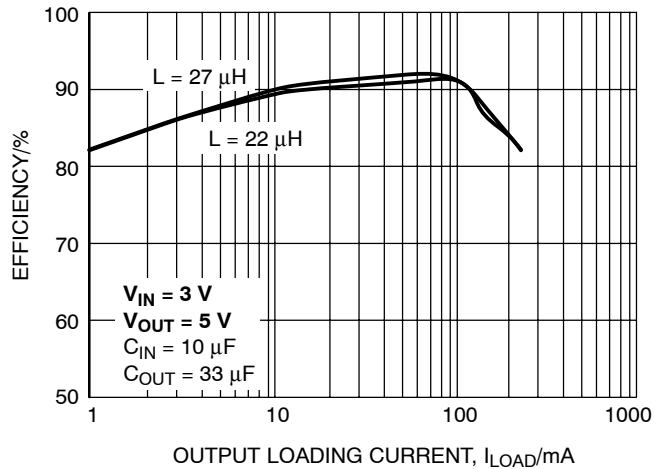


Figure 12. Efficiency versus Load Current

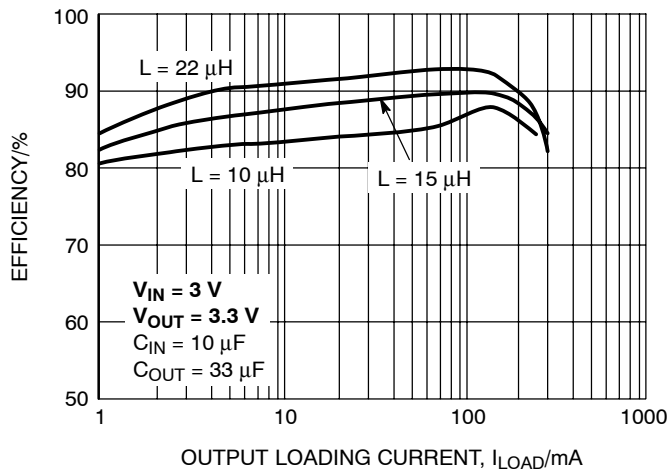


Figure 13. Efficiency versus Load Current

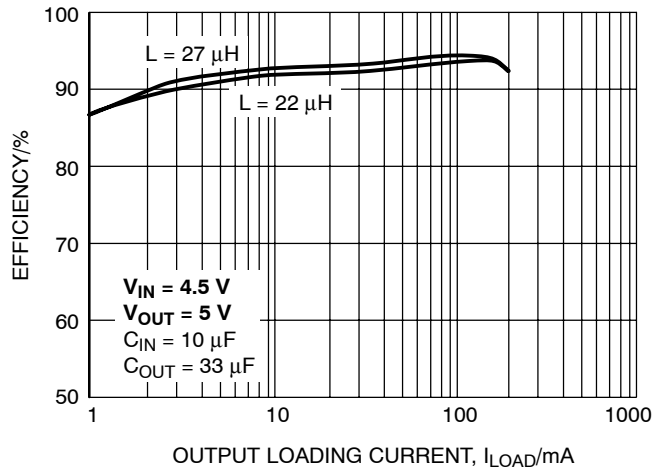


Figure 14. Efficiency versus Load Current

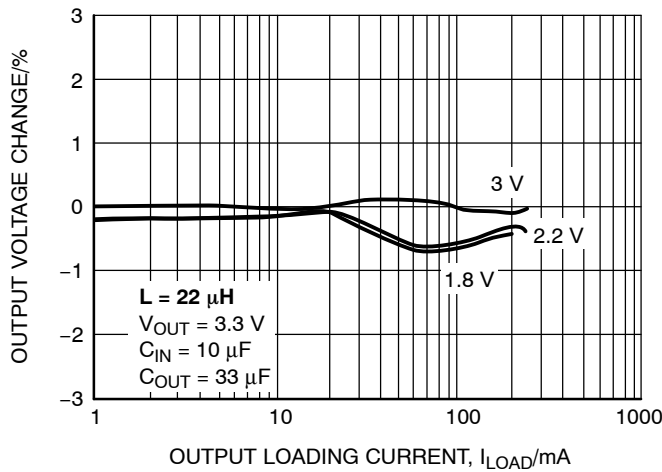


Figure 15. Output Voltage Change versus Load Current

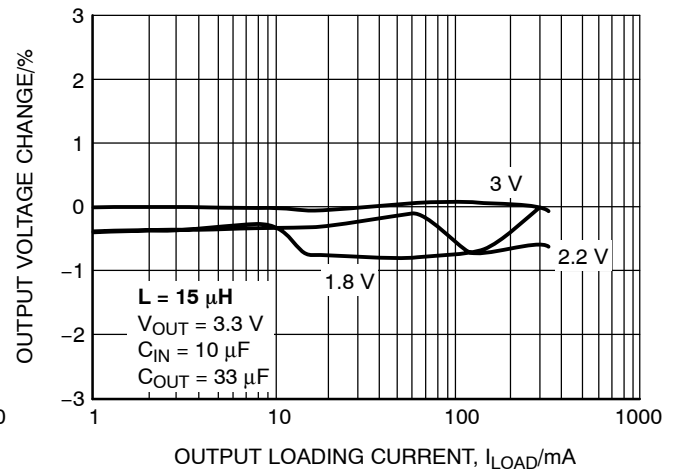


Figure 16. Output Voltage Change versus Load Current

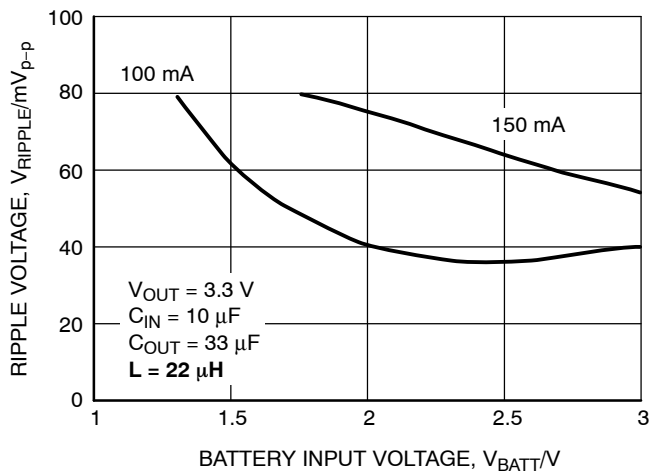


Figure 17. Battery Input Voltage versus Output Ripple Voltage

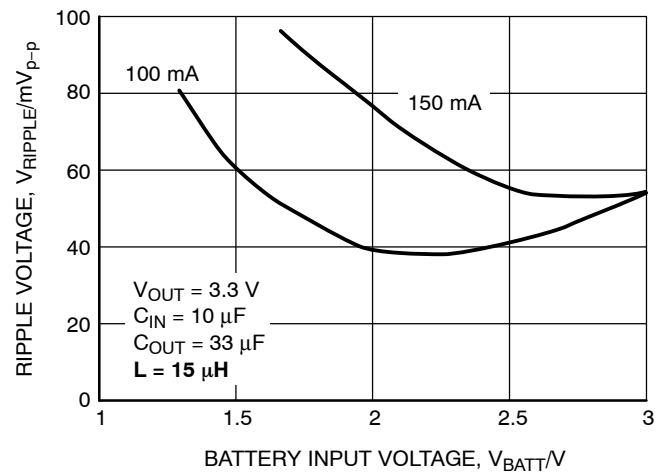


Figure 18. Battery Input Voltage versus Output Ripple Voltage

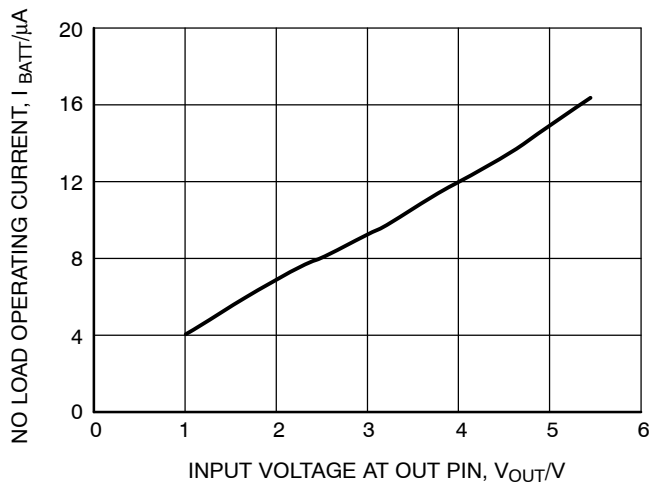


Figure 19. No Load Operating Current versus Input Voltage at OUT Pin

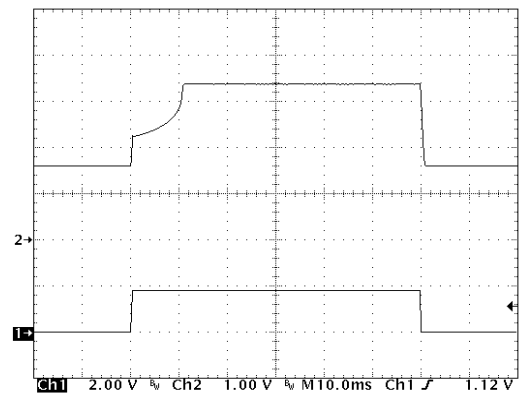
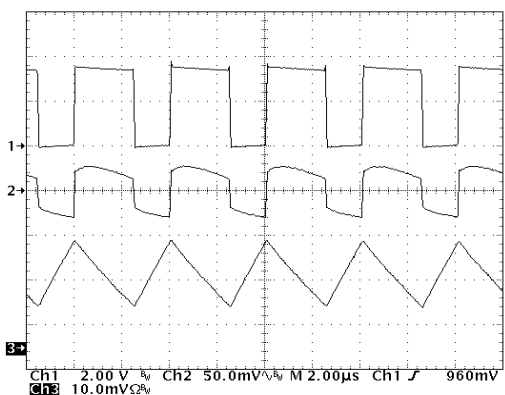


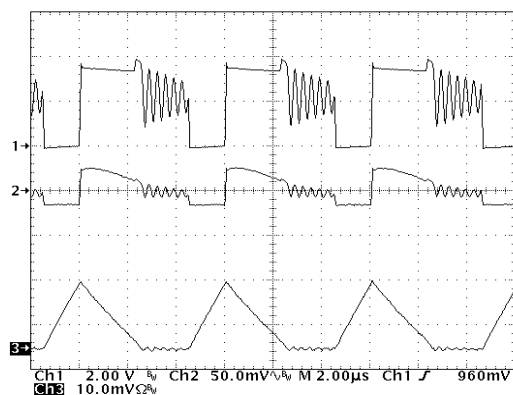
Figure 20. Startup Transient Response
($V_{IN} = 2.2 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$, $I_{LOAD} = 100 \text{ mA}$; $L = 22 \mu\text{H}$, $C_{OUT} = 33 \mu\text{F}$)
Upper Trace: Output Voltage Waveform, 1.0 V/Division
Lower Trace: Shutdown Pin Waveform, 1.0 V/Division



($V_{IN} = 2.2\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 100\text{ mA}$; $L = 22\text{ μH}$, $C_{OUT} = 33\text{ μF}$)

Upper Trace: Voltage at Lx pin, 2.0 V/Division
Middle Trace: Output Voltage Ripple, 50 mV/Division
Lower Trace: Inductor Current, I_L , 100 mA/Division

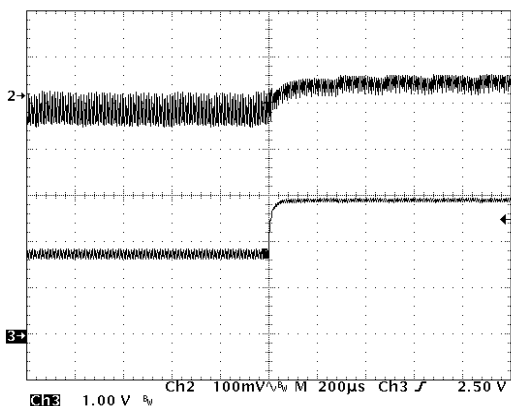
Figure 21. Continuous Conduction Mode Switching Waveform



($V_{IN} = 2.2\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 30\text{ mA}$; $L = 22\text{ μH}$, $C_{OUT} = 33\text{ μF}$)

Upper Trace: Voltage at Lx pin, 2.0 V/Division
Middle Trace: Output Voltage Ripple, 50 mV/Division
Lower Trace: Inductor Current, I_L , 100 mA/Division

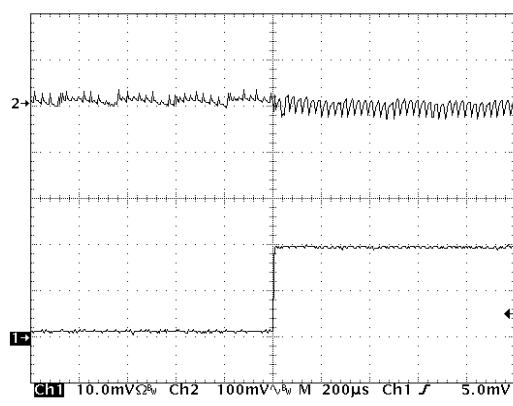
Figure 22. Discontinuous Conduction Mode Switching Waveform



($V_{IN} = 1.8\text{ V}$, $V_{OUT} = 3.0\text{ V}$, $L = 22\text{ μH}$, $C_{OUT} = 33\text{ μF}$)

Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Battery Voltage, V_{IN} , 1.0 V/Division

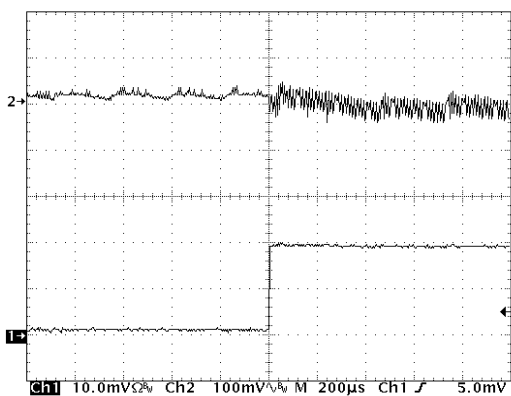
Figure 23. Line Transient Response for $V_{OUT} = 3.3\text{ V}$



($V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 10\text{ mA to } 100\text{ mA}$; $L = 22\text{ μH}$, $C_{OUT} = 33\text{ μF}$)

Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Load Current, I_{LOAD} , 50 mA/Division

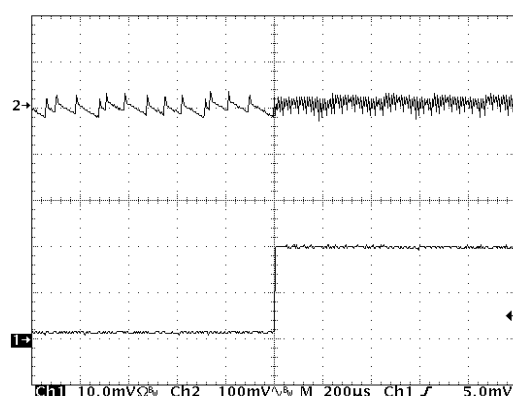
Figure 24. Load Transient Response for $V_{IN} = 1.8\text{ V}$



($V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 10\text{ mA to } 100\text{ mA}$; $L = 22\text{ μH}$, $C_{OUT} = 33\text{ μF}$)

Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Load Current, I_{LOAD} , 50 mA/Division

Figure 25. Load Transient Response for $V_{IN} = 2.4\text{ V}$



($V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 10\text{ mA to } 100\text{ mA}$; $L = 22\text{ μH}$, $C_{OUT} = 33\text{ μF}$)

Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Load Current, I_{LOAD} , 50 mA/Division

Figure 26. Load Transient Response for $V_{IN} = 3.3\text{ V}$

DETAILED OPERATION DESCRIPTIONS

NCP1417 is a monolithic micropower high frequency step-up voltage switching converter IC specially designed for battery operated hand-held electronic products up to 200 mA loading. It integrates Synchronous Rectifier for improving efficiency as well as eliminating the external Schottky Diode. High switching frequency (up to 600 kHz) allows low profile inductor and output capacitor being used. Dual Low-Battery Detectors, Logic-Controlled Shutdown and Cycle-by-Cycle Current Limit provide value-added features for various battery-operated application. With all these functions ON, the quiescent supply current is only 9 μ A typical. This device is available in compact Micro8 package.

PFM Regulation Scheme

From the simplified Functional Diagram (Figure 2), the output voltage is divided down and fed back to pin 1 (FB). This voltage goes to the non-inverting input of the PFM comparator whereas the comparator's inverting input is connected to REF. A switching cycle is initiated by the falling edge of the comparator, at the moment, the main switch (M1) is turned ON. After the maximum ON-time (typical 1.4 μ S) elapses or the current limit is reached, M1 is turned OFF, and the synchronous switch (M2) is turned ON. The M1 OFF time is not less than the minimum OFF-time (typical 0.25 μ S), this is to ensure energy transfer from the inductor to the output capacitor. If the regulator is operating at continuous conduction mode (CCM), M2 is turned OFF just before M1 is supposed to be ON again. If the regulator is operating at discontinuous conduction mode (DCM), which means the coil current will decrease to zero before the next cycle, M1 is turned OFF as the coil current is almost reaching zero. The comparator (ZLC) with fixed offset is dedicated to sense the voltage drop across M2 as it is conducting, when the voltage drop is below the offset, the ZLC comparator output goes HIGH, and M2 is turned OFF. Negative feedback of closed loop operation regulates voltage at pin 1 (FB) equal to the internal voltage reference (1.190 V).

Synchronous Rectification

Synchronous Rectifier is used to replace Schottky Diode to eliminate the conduction loss contributed by forward voltage drop of the latter. Synchronous Rectifier is normally realized by powerFET with gate control circuitry which, however, involved relative complicated timing concerns.

As main switch M1 is being turned OFF, if the synchronous switch M2 is just turned ON with M1 not being completed turned OFF, current will be shunt from the output bulk capacitor through M2 and M1 to ground. This power loss lowers overall efficiency. So a certain amount of dead time is introduced to make sure M1 is completely OFF before M2 is being turned ON.

When the main regulator is operating in CCM, as M2 is being turned OFF, and M1 is just turned ON with M2 not being completely turned OFF, the above mentioned

situation will occur. So dead time is introduced to make sure M2 is completely turned OFF before M1 is being turned ON.

When the regulator is operating in DCM, as coil current is dropped to zero, M2 is supposed to be OFF. Fail to do so, reverse current will flow from the output bulk capacitor through M2 and then the inductor to the battery input. It causes damage to the battery. So the ZLC comparator comes with fixed offset voltage to switch M2 OFF before any reverse current builds up. However, if M2 is switch OFF too early, large residue coil current flows through the body diode of M2 and increases conduction loss. Therefore, determination on the offset voltage is essential for optimum performance.

With the implementation of synchronous rectification, efficiency can be as high as 92%. For single cell input voltage, use an external schottky diode such as MBR0520 connected from pin 7 to pin 8 to ensure quick start-up.

Cycle-by-Cycle Current Limit

From Figure 2, SenseFET is applied to sample the coil current as M1 is ON. With that sample current flowing through a sense resistor, sense-voltage is developed. Threshold detector (ILIM) detects whether the sense-voltage is higher than preset level. If it happens, detector output signifies the CONTROL LOGIC to switch OFF M1, and M1 can only be switched ON as next cycle starts after the minimum OFF-time (typical 0.25 μ S). With properly sizing of SenseFET and sense resistor, the peak coil current limit is set at 1.0 A typically.

Voltage Reference

The voltage at REF is set typically at +1.190 V. It can deliver up to 2.5 mA with load regulation $\pm 1.5\%$, at VOUT equal to 3.3 V. If VOUT is increased, the REF load capability can also be increased. A bypass capacitor of 0.15 μ F is required for proper operation when REF is not loaded. If REF is loaded, 1.0 μ F capacitor at REF is needed.

Shutdown

The IC is shutdown when the voltage at pin 2 (LBI/SHDN) is pulled lower than 0.3 V via an open drain transistor. During shutdown, M1 and M2 are both switched OFF, however, the body diode of M2 allows current flow from battery to the output, the IC internal circuit will consume less than 0.05 μ A current typically. If the pin 2 pull low is released, the IC will be enabled. The internal circuit will only consume 9.0 μ A current typically from the OUT pin.

Dual Low-Battery Detection

Two comparators with 30 mV hysteresis are applied to perform the dual low-battery detection function. When pin 2 (LBI) is at a voltage, which can be defined by a resistor divider from the battery voltage, lower than the internal reference voltage, 1.190 V, the first comparator, CP1 output will cause a 50 Ω low side switch to be turned ON. It will pull down the voltage at pin 3 (LBO1) which has a hundreds kilo-Ohm of pull-high resistance. If the pin 2 voltage is

higher than 1.190 V + 30 mV, the comparator output will cause the 50 Ω low side switch to be turned OFF, pin 3 will become high impedance, and its voltage will be pulled high. The second low-battery detector functions in the same manner, the second comparator, CP2 with a lower triggering reference point derived from the internal reference is used instead, typical 0.944 V. This configuration provides two levels of low battery warning to the target system.

APPLICATIONS INFORMATION

Output Voltage Setting

The output voltage of the converter is determined by the external feedback network comprised of R_{FB1} and R_{FB2} and the relationship is given by:

$$V_{OUT} = 1.190 \text{ V} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where R_{FB1} and R_{FB2} are the upper and lower feedback resistors respectively.

Low Battery Detect Level Setting

The Low Battery Detect Voltages of the converter are determined by the external divider network comprised of R_{LB1} and R_{LB2} and the relationship is given by:

$$V_{LB1} = 1.190 \text{ V} \times \left(1 + \frac{R_{LB1}}{R_{LB2}}\right)$$

where R_{LB1} and R_{LB2} are the upper and lower divider resistors respectively. By setting the V_{LB1} , the second low battery detection point, V_{LB2} will be fixed automatically.

Inductor Selection

The NCP1417 is tested to produce optimum performance with a 22 μH inductor at $V_{IN} = 3.0 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$ supplying output current up to 200 mA. For other input/output requirements, inductance in the range 10 μH to 47 μH can be used according to end application specifications. Selecting an inductor is a compromise between output current capability and tolerable output voltage ripple. Of course, the first thing we need to obey is to keep the peak inductor current below its saturation limit at maximum current and the I_{LIM} of the device. In NCP1417, I_{LIM} is set at 1.0 A. As a rule of thumb, low inductance values supply higher output current, but also increase the ripple at output and reducing efficiency, on the other hand, high inductance values can improve output ripple and efficiency, however it also limit the output current capability at the same time. One other parameter of the inductor is its DC resistance, this resistance can introduce unwanted power loss and hence reduce overall efficiency, the basic rule is selecting an inductor with lowest DC resistance within the board space limitation of the end application.

Capacitors Selection

In all switching mode boost converter applications, both the input and output terminals sees impulsive voltage/current waveforms. The currents flowing into and

out of the capacitors multiplying with the Equivalent Series Resistance (ESR) of the capacitor producing ripple voltage at the terminals. During the syn-rect switch off cycle, the charges stored in the output capacitor is used to sustain the output load current. Load current at this period and the ESR combined and reflected as ripple at the output terminal. For all cases, the lower the capacitor ESR, the lower the ripple voltage at output. As a general guide line, low ESR capacitors should be used. Ceramic capacitors have the lowest ESR, but low ESR tantalum capacitors can also be used as a cost effective substitute.

Optional Startup Schottky Diode for Low Battery Voltage

In general operation, no external schottky diode is required, however, in case you are intended to operate the device close to 1.0 V level, a schottky diode connected between the LX and OUT pins as shown in Figure 27 can help during startup of the converter. The effect of the additional schottky is shown in Figure 8.

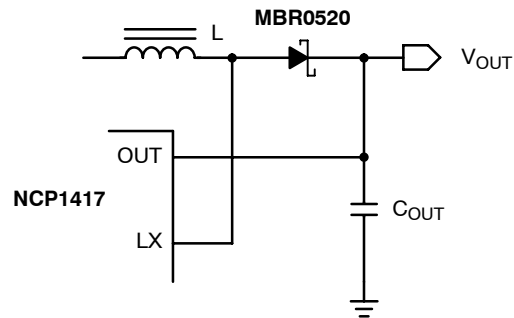


Figure 27.

PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise and unwanted feedback that can affect the performance of the converter. Hints suggested in below can be used as a guide line in most situations.

Grounding

Star-ground connection should be used to connect the output power return ground, the input power return ground and the device power ground together at one point. All high current running paths must be thick enough for current flowing through and producing insignificant voltage drop along the path. Feedback signal path must be separated with the main current path and sensing directly at the anode of the output capacitor.

Components Placement

Power components, i.e. input capacitor, inductor and output capacitor, must be placed as close together as possible. All connecting traces must be short, direct and thick. High current flowing and switching paths must be

NCP1417

kept away from the feedback (FB, pin 1) terminal to avoid unwanted injection of noise into the feedback path.

Feedback Network

Feedback of the output voltage must be a separate trace detached from the power path. External feedback network

must be placed very close to the feedback (FB, pin 1) pin and sensing the output voltage directly at the anode of the output capacitor.

TYPICAL APPLICATION CIRCUIT

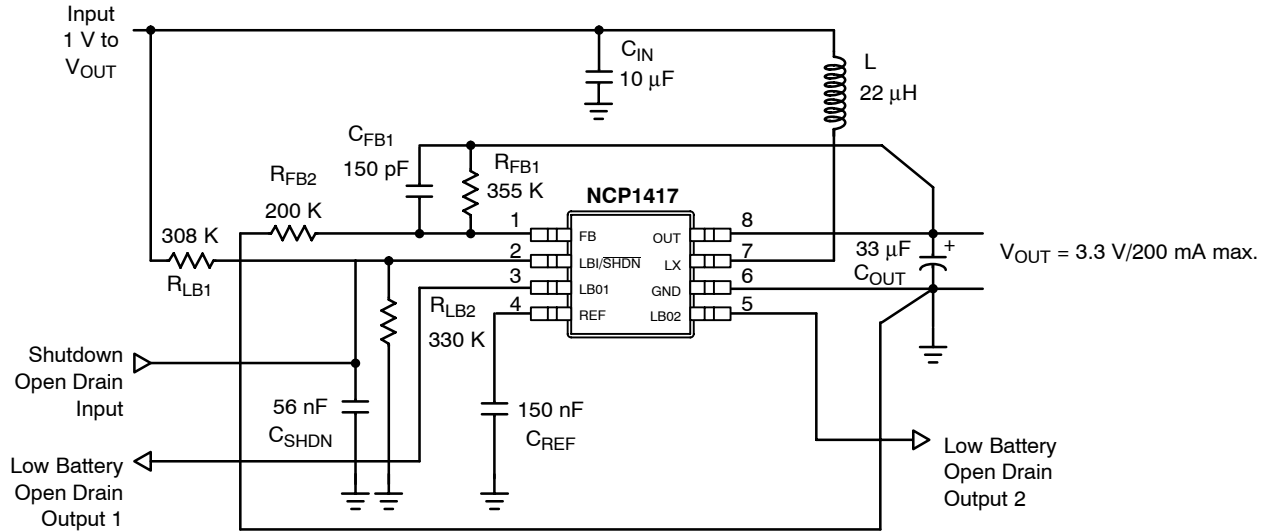


Figure 28. Typical Application Schematic for 2 Alkaline Cells Supply

GENERAL DESIGN PROCEDURES

Switch mode converter design is considered as black magic to most engineers, some complicate empirical formulae are available for reference usage. Those formulae are derived from the assumption that the key components, i.e. power inductor and capacitors are available with no tolerance. Practically, its not true, the result is not a matter of how accurate the equations you are using to calculate the component values, the outcome is still somehow away from the optimum point. Following, is a simple method based on the most basic first order equations to estimate the inductor and capacitor values for NCP1417 operating in Continuous Conduction Mode. The component value set can be used as a starting point to fine tune the circuit operation. By all means, detail bench testing is needed to get the best performance out of the circuit.

Design Parameters:

$V_{IN} = 1.8 \text{ V to } 3.0 \text{ V, Typical } 2.4 \text{ V}$

$V_{OUT} = 3.3 \text{ V}$

$I_{OUT} = 150 \text{ mA (200 mA max)}$

$V_{LB1} = 2.3 \text{ V; } V_{LB2} \approx 0.8 V_{LB1} = 1.84 \text{ V}$

$V_{OUT-RIPPLE} = 40 \text{ mV}_{P-P} \text{ at } I_{OUT} = 200 \text{ mA}$

Calculate the feedback network:

Select $R_{FB2} = 200 \text{ K}$

$$R_{FB1} = R_{FB2} \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

$$R_{FB1} = 200 \text{ K} \left(\frac{3.3 \text{ V}}{1.19 \text{ V}} - 1 \right) = 355 \text{ K}$$

With the feedback resistor divider, additional small capacitor, C_{FB1} in parallel with R_{FB1} is required to ensure stability. The value can be in between 68 pF to 220 pF, the rule is to select the lowest capacitance to ensure stability. Also a small capacitor, C_{FB2} in parallel with R_{FB2} may also be needed to lower the feedback ripple hence improve output ripple and regulation. In this example, only C_{FB1} is used and the value is 150 pF.

Calculate the Low Battery Detect divider:

$$V_{LB1} = 2.3 \text{ V}$$

$$\text{Select } R_{LB2} = 330 \text{ K}$$

$$R_{LB1} = R_{LB2} \left(\frac{V_{LB1}}{V_{REF}} - 1 \right)$$

$$R_{LB1} = 330 \text{ K} \left(\frac{2.3 \text{ V}}{1.19 \text{ V}} - 1 \right) = 308 \text{ K}$$

Once the V_{LB1} is set, the next low battery detection point, V_{LB2} will be fixed automatically.

Determine the Steady State Duty Ratio, D for typical V_{IN} , operation will be optimized around this point:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D}$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}} = 1 - \frac{2.4 \text{ V}}{3.3 \text{ V}} = 0.273$$

Determine the average inductor current, I_{LAVG} at maximum I_{OUT} :

$$I_{LAVG} = \frac{I_{OUT}}{1 - D} = \frac{200 \text{ mA}}{1 - 0.273} = 275 \text{ mA}$$

Determine the peak inductor ripple current, $I_{RIPPLE-P}$ and calculate the inductor value:

Assume $I_{RIPPLE-P}$ is 25% of I_{LAVG} , the inductance of the power inductor can be calculated as follows:

$$I_{RIPPLE-P} = 0.25 \times 275 \text{ mA} = 68.8 \text{ mA}$$

$$L = \frac{V_{IN} \times t_{ON}}{2I_{RIPPLE-P}} = \frac{2.4 \text{ V} \times 1.4 \mu\text{S}}{2(68.8 \text{ mA})} = 24.4 \mu\text{H}$$

Standard value of 22 μH is selected for initial trial.

Determine the output voltage ripple, $V_{OUT-RIPPLE}$ and calculate the output capacitor value:

$$V_{OUT-RIPPLE} = 40 \text{ mV}_{P-P} \text{ at } I_{OUT} = 200 \text{ mA}$$

$$C_{OUT} > \frac{I_{OUT} \times t_{ON}}{V_{OUT-RIPPLE} - I_{OUT} \times ESR_{COUT}}$$

where $t_{ON} = 1.4 \mu\text{S}$ and $ESR_{COUT} = 0.15 \Omega$,

$$C_{OUT} > \frac{200 \text{ mA} \times 1.4 \mu\text{S}}{40 \text{ mV} - 200 \text{ mA} \times 0.15 \Omega} = 28 \mu\text{F}$$

From above calculation, you need at least 28 μF in order to achieve the specified ripple level at conditions stated. Practically, a one level larger capacitor will be used to accommodate factors not take into account in the calculation. So a capacitor value of 33 μF is selected as initial trial.

NCP1421

600 mA Sync-Rect PFM Step-Up DC-DC Converter with True-Cutoff and Ring-Killer

NCP1421 is a monolithic micropower high-frequency step-up switching converter IC specially designed for battery-operated hand-held electronic products up to 600 mA loading. It integrates Sync-Rect to improve efficiency and to eliminate the external Schottky Diode. High switching frequency (up to 1.2 MHz) allows for a low profile, small-sized inductor and output capacitor to be used. When the device is disabled, the internal conduction path from LX or BAT to OUT is fully blocked and the OUT pin is isolated from the battery. This True-Cutoff function reduces the shutdown current to typically only 50 nA. Ring-Killer is also integrated to eliminate the high-frequency ringing in discontinuous conduction mode. In addition to the above, Low-Battery Detector, Logic-Controlled Shutdown, Cycle-by-Cycle Current Limit and Thermal Shutdown provide value-added features for various battery-operated applications. With all these functions on, the quiescent supply current is typically only 8.5 μ A. This device is available in the compact and low profile Micro8™ package.

Features

- Pb-Free Package is Available
- High Efficiency: 94% for 3.3 V Output at 200 mA from 2.5 V Input
88% for 3.3 V Output at 500 mA from 2.5 V Input
- High Switching Frequency, up to 1.2 MHz (not hitting current limit)
- Output Current up to 600 mA at $V_{IN} = 2.5$ V and $V_{OUT} = 3.3$ V
- True-Cutoff Function Reduces Device Shutdown Current to typically 50 nA
- Anti-Ringing Ring-Killer for Discontinuous Conduction Mode
- High Accuracy Reference Output, 1.20 V $\pm$ 1.5%, can Supply 2.5 mA Loading Current when $V_{OUT} > 3.3$ V
- Low Quiescent Current of 8.5 μ A
- Integrated Low-Battery Detector
- Open Drain Low-Battery Detector Output
- 1.0 V Startup at No Load Guaranteed
- Output Voltage from 1.5 V to 5.0 V Adjustable
- 1.5 A Cycle-by-Cycle Current Limit
- Multi-function Logic-Controlled Shutdown Pin
- On Chip Thermal Shutdown with Hysteresis

Typical Applications

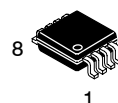
- Personal Digital Assistants (PDA)
- Handheld Digital Audio Products
- Camcorders and Digital Still Cameras
- Hand-held Instruments
- Conversion from one to two Alkaline, NiMH, NiCd Battery Cells to 3.0–5.0 V or one Lithium-ion cells to 5.0 V
- White LED Flash for Digital Cameras



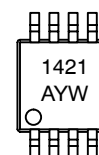
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM

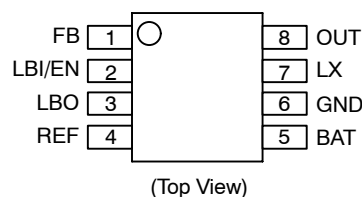


Micro8
DM SUFFIX
CASE 846A



1421 = Device Code
A = Assembly Location
Y = Year
W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP1421DMR2	Micro8	4000 Tape & Reel
NCP1421DMR2G	Micro8 (Pb-Free)	4000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP1421

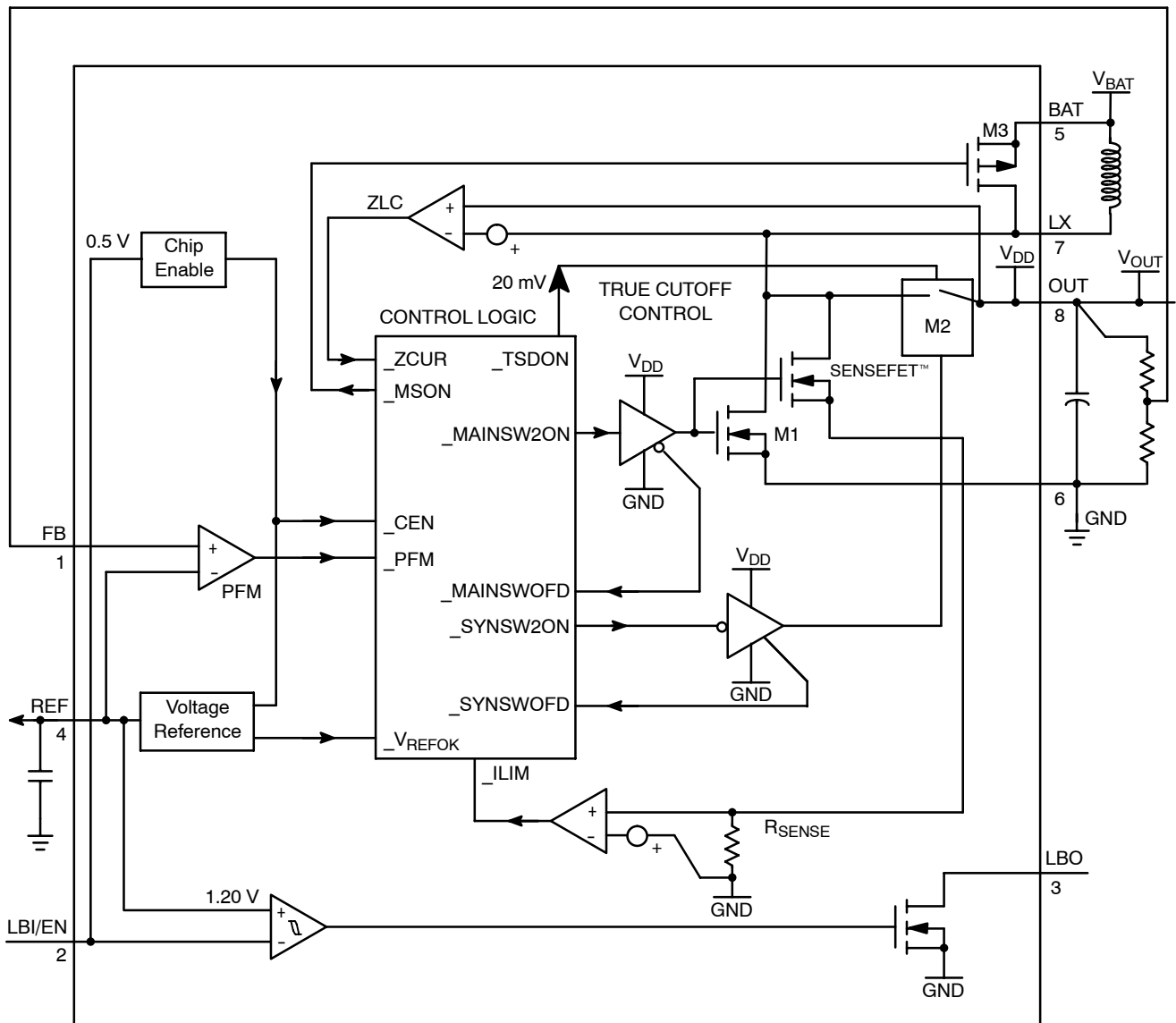


Figure 1. Detailed Block Diagram

PIN FUNCTION DESCRIPTIONS

Pin	Symbol	Description
1	FB	Output Voltage Feedback Input.
2	LBI/EN	Low-Battery Detector Input and IC Enable. With this pin pulled down below 0.5 V, the device is disabled and enters the shutdown mode.
3	LBO	Open-Drain Low-Battery Detector Output. Output is LOW when $V_{LBI} < 1.20$ V. LBO is high impedance in shutdown mode.
4	REF	1.20 V Reference Voltage Output, bypass with 1.0 μ F capacitor. If this pin is not loaded, bypass with 300 nF capacitor; this pin can be loaded up to 2.5 mA @ $V_{OUT} = 3.3$ V.
5	BAT	Battery input connection for internal ring-killer.
6	GND	Ground.
7	LX	N-Channel and P-Channel Power MOSFET drain connection.
8	OUT	Power Output. OUT also provides bootstrap power to the device.

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply (Pin 8)	V_{OUT}	-0.3, 5.5	V
Input/Output Pins (Pin 1–5, Pin 7)	V_{IO}	-0.3, 5.5	V
Thermal Characteristics Micro8 Plastic Package Thermal Resistance Junction-to-Air	P_D $R_{\theta JA}$	520 240	mW $^\circ\text{C/W}$
Operating Junction Temperature Range	T_J	-40 to +150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- This device contains ESD protection and exceeds the following tests:
Human Body Model (HBM) ± 2.0 kV per JEDEC standard: JESD22-A114. *Except OUT pin, which is 1k V.
Machine Model (MM) ± 200 V per JEDEC standard: JESD22-A115. *Except OUT pin, which is 100 V.
- The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(\max)} - T_A}{R_{\theta JA}}$$

- Latchup Current Maximum Rating: ± 150 mA per JEDEC standard: JESD78.
- Moisture Sensitivity Level: MSL 1 per IPC/JEDEC standard: J-STD-020A.

NCP1421

ELECTRICAL CHARACTERISTICS ($V_{OUT} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ for typical value, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for min/max values unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage	V_{IN}	1.0	–	5.0	V
Output Voltage Range	V_{OUT}	1.5	–	5.0	V
Reference Voltage ($V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 0\text{ }\mu\text{A}$, $C_{REF} = 200\text{ nF}$, $T_A = 25^\circ\text{C}$)	V_{REF_NL}	1.183	1.200	1.217	V
Reference Voltage ($V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 0\text{ }\mu\text{A}$, $C_{REF} = 200\text{ nF}$, $T_A = -40^\circ\text{C}$ to 85°C)	V_{REF_NL}	1.174	–	1.220	V
Reference Voltage Temperature Coefficient	TC_{VREF}	–	0.03	–	mV/ $^\circ\text{C}$
Reference Voltage Load Current ($V_{OUT} = 3.3\text{ V}$, $V_{REF} = V_{REF\_NL} \pm 1.5\%$, $C_{REF} = 1.0\text{ }\mu\text{F}$) (Note 5)	I_{REF}	–	2.5	–	mA
Reference Voltage Load Regulation ($V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 0$ to $100\text{ }\mu\text{A}$, $C_{REF} = 1.0\text{ }\mu\text{F}$)	V_{REF_LOAD}	–	0.05	1.0	mV
Reference Voltage Line Regulation (V_{OUT} from 1.5 V to 5.0 V , $C_{REF} = 1.0\text{ }\mu\text{F}$)	V_{REF_LINE}	–	0.05	1.0	mV/V
FB Input Threshold ($I_{LOAD} = 0\text{ mA}$, $T_A = 25^\circ\text{C}$)	V_{FB}	1.192	1.200	1.208	V
FB Input Threshold ($I_{LOAD} = 0\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C)	V_{FB}	1.184	–	1.210	V
LBI Input Threshold ($I_{LOAD} = 0\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C)	V_{LBI}	1.162	–	1.230	V
LBI Input Threshold ($T_A = 25^\circ\text{C}$)	V_{LBI}	1.182	1.200	1.218	V
Internal NFET ON-Resistance	$R_{DS(ON)\_N}$	–	0.3	–	Ω
Internal PFET ON-Resistance	$R_{DS(ON)\_P}$	–	0.3	–	Ω
LX Switch Current Limit (N-FET) (Note 7)	I_{LIM}	–	1.5	–	A
Operating Current into BAT ($V_{BAT} = 1.8\text{ V}$, $V_{FB} = 1.8\text{ V}$, $V_{LX} = 1.8\text{ V}$, $V_{OUT} = 3.3\text{ V}$)	I_{QBAT}	–	1.3	3	μA
Operating Current into OUT ($V_{FB} = 1.4\text{ V}$, $V_{OUT} = 3.3\text{ V}$)	I_Q	–	8.5	14	μA
LX Switch MAX. ON-Time ($V_{FB} = 1.0\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$)	t_{ON}	0.46	0.72	1.15	μs
LX Switch MIN. OFF-Time ($V_{FB} = 1.0\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$)	t_{OFF}	–	0.12	0.22	μs
FB Input Current	I_{FB}	–	1.0	50	nA
True-Cutoff Current into BAT ($LBI/EN = GND$, $V_{OUT} = 0$, $V_{IN} = 3.3\text{ V}$, $LX = 3.3\text{ V}$)	I_{BAT}	–	50	–	nA
BAT-to-LX Resistance ($V_{FB} = 1.4\text{ V}$, $V_{OUT} = 3.3\text{ V}$) (Note 7)	R_{BAT_LX}	–	100	–	Ω
LBI/EN Input Current	I_{LBI}	–	1.5	50	nA
LBO Low Output Voltage ($V_{LBI} = 0$, $I_{SINK} = 1.0\text{ mA}$)	V_{LBO_L}	–	–	0.2	V
Soft-Start Time ($V_{IN} = 2.5\text{ V}$, $V_{OUT} = 5.0\text{ V}$, $C_{REF} = 200\text{ nF}$) (Note 6)	T_{SS}	–	1.5	20	ms
EN Pin Shutdown Threshold ($T_A = 25^\circ\text{C}$)	V_{SHDN}	0.35	0.5	0.67	V
Thermal Shutdown Temperature (Note 7)	T_{SHDN}	–	–	145	$^\circ\text{C}$
Thermal Shutdown Hysteresis (Note 7)	T_{SDHYS}	–	30	–	$^\circ\text{C}$

5. Loading capability increases with V_{OUT} .

6. Design guarantee, value depends on voltage at V_{OUT} .

7. Values are design guaranteed.

TYPICAL OPERATING CHARACTERISTICS

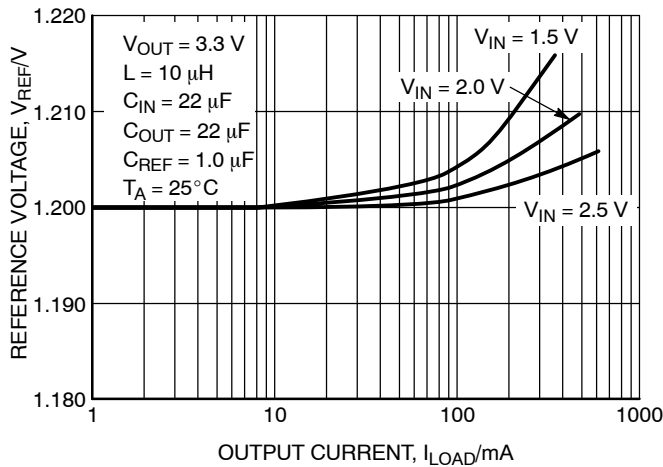


Figure 2. Reference Voltage vs. Output Current

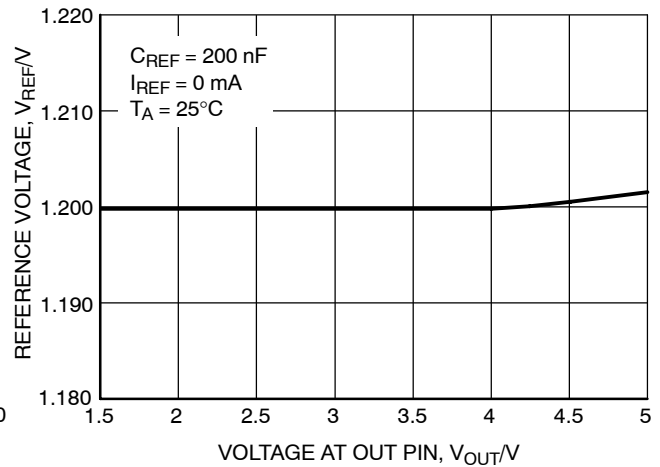


Figure 3. Reference Voltage vs. Voltage at OUT Pin

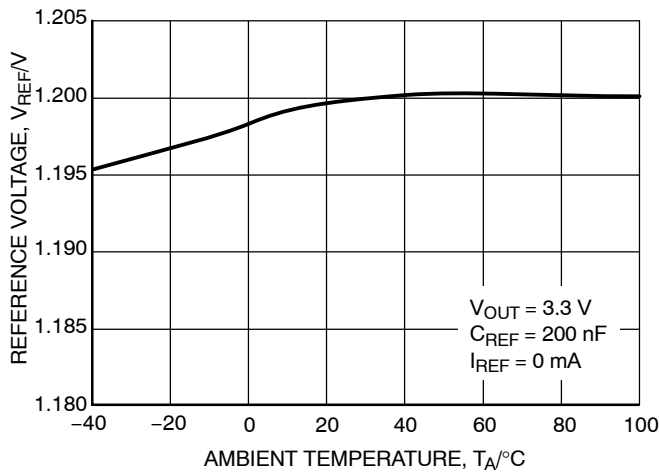


Figure 4. Reference Voltage vs. Temperature

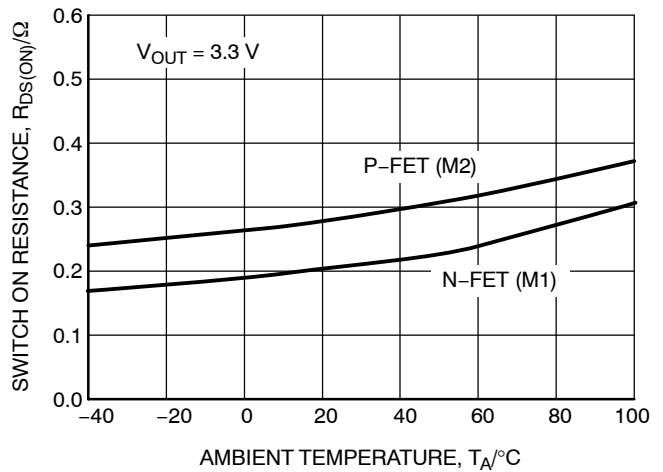


Figure 5. Switch ON Resistance vs. Temperature

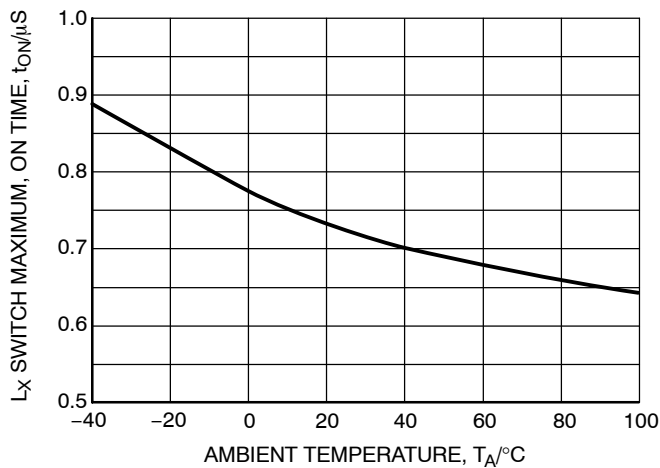
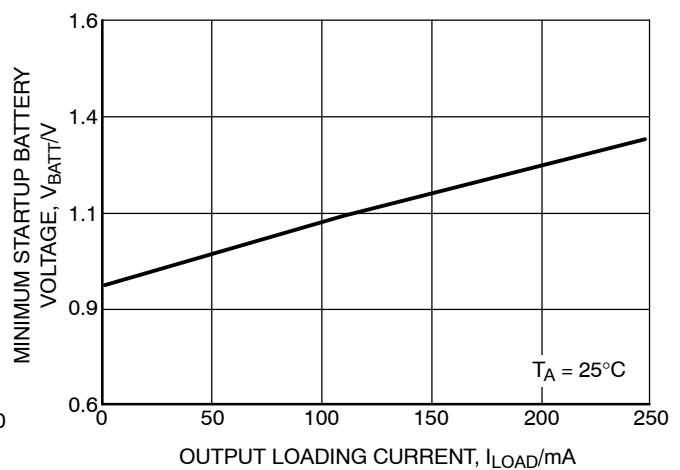
Figure 6. L_X Switch Max. ON Time vs. Temperature

Figure 7. Minimum Startup Battery Voltage vs. Loading Current

TYPICAL OPERATING CHARACTERISTICS

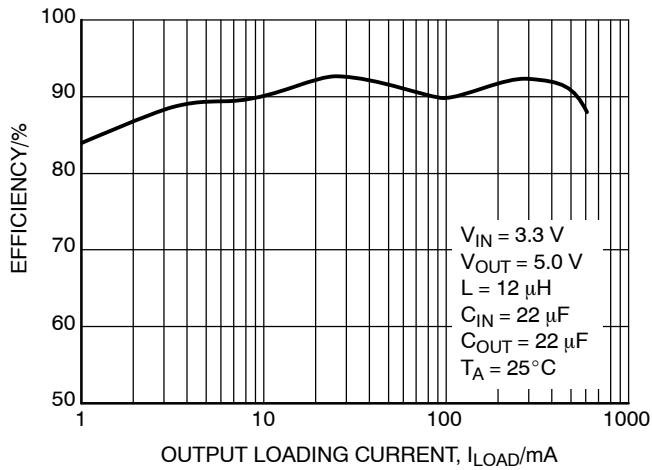


Figure 8. Efficiency vs. Load Current

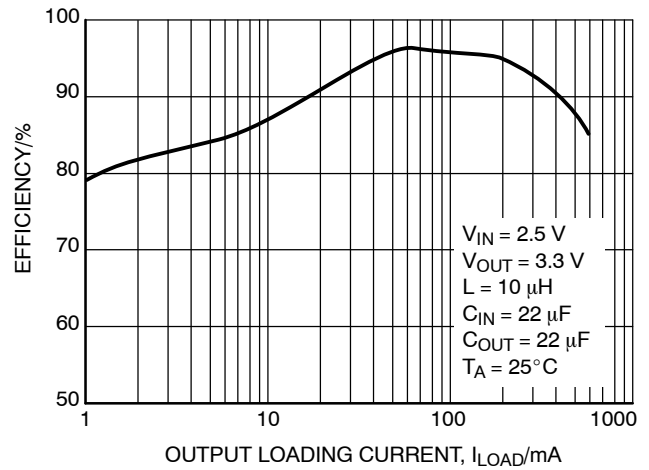


Figure 9. Efficiency vs. Load Current

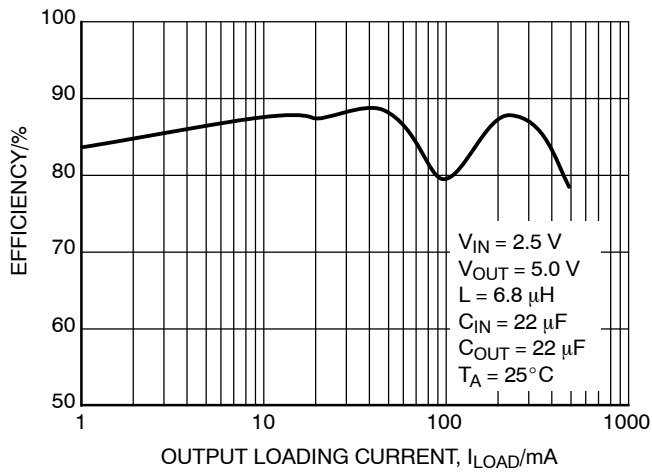


Figure 10. Efficiency vs. Load Current

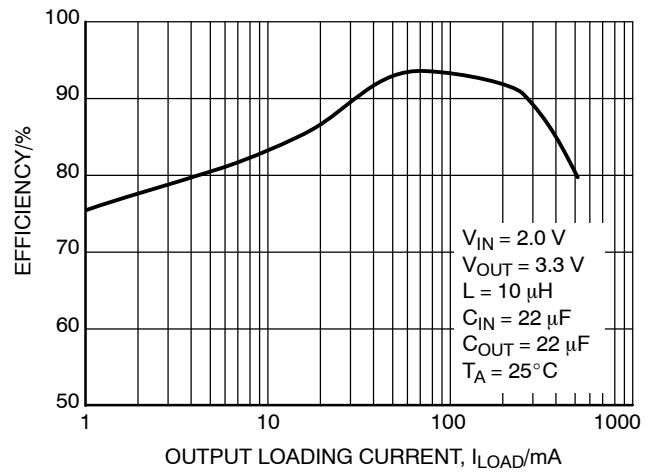


Figure 11. Efficiency vs. Load Current

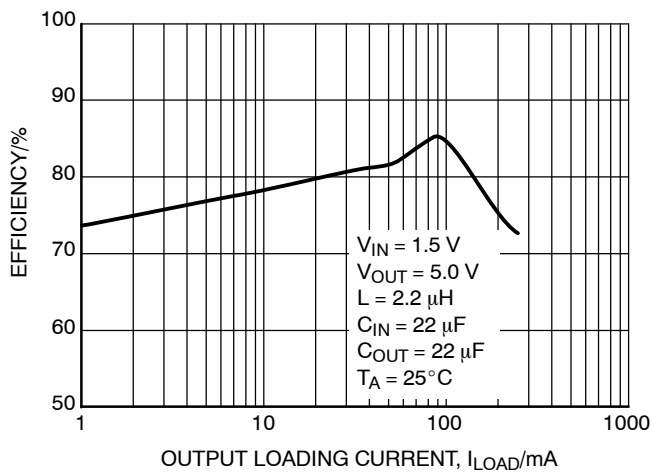


Figure 12. Efficiency vs. Load Current

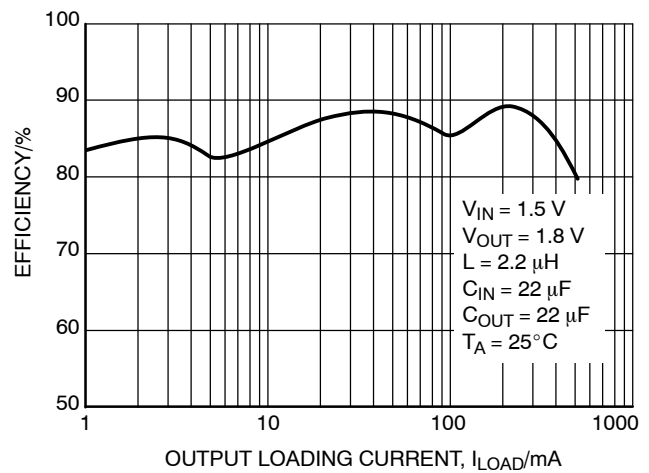


Figure 13. Efficiency vs. Load Current

TYPICAL OPERATING CHARACTERISTICS

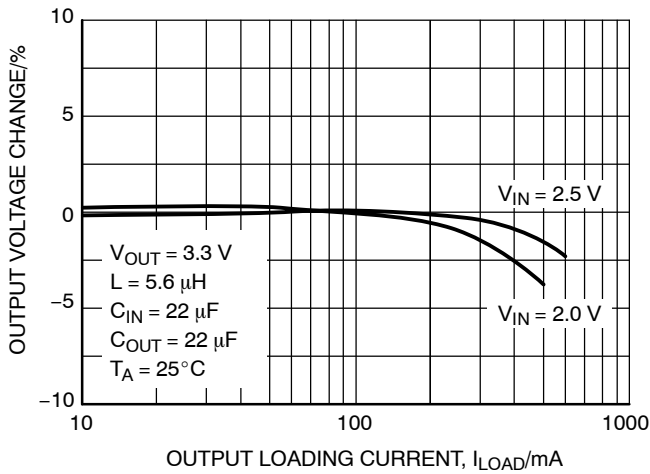


Figure 14. Output Voltage Change vs. Load Current

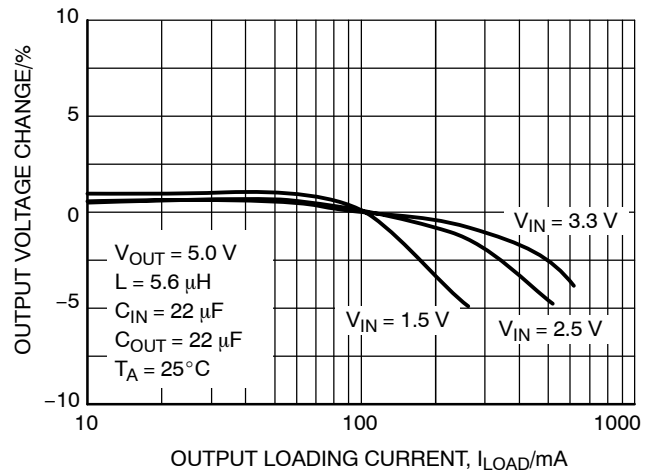


Figure 15. Output Voltage Change vs. Load Current

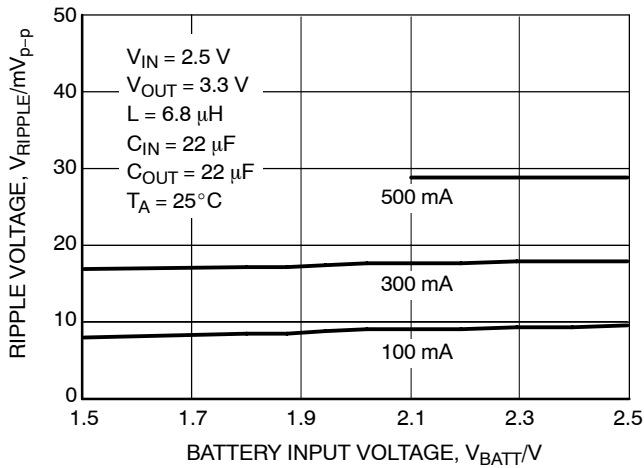
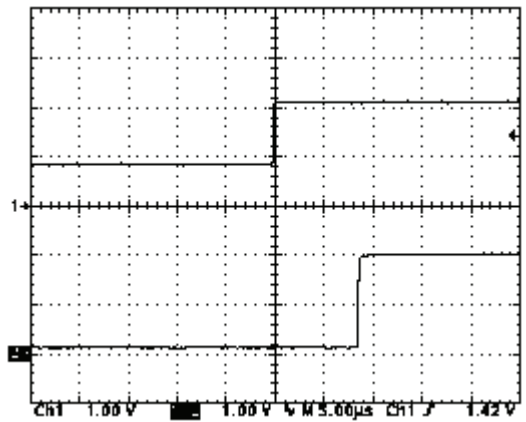


Figure 16. Battery Input Voltage vs. Output Ripple Voltage



Upper Trace: Voltage at LBI Pin, 1.0 V/Division
Lower Trace: Voltage at LBO Pin, 1.0 V/Division

Figure 17. Low Battery Detect

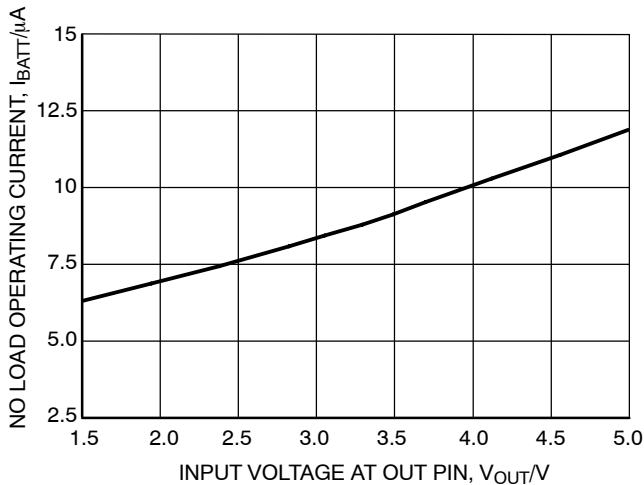
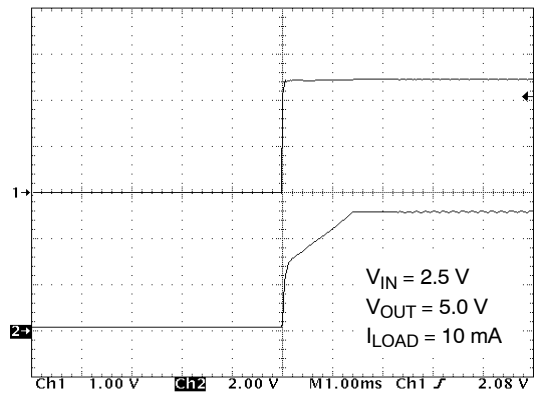


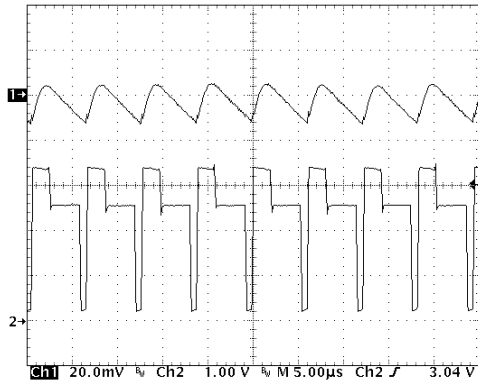
Figure 18. No Load Operating Current vs. Input Voltage at OUT Pin



Upper Trace: Input Voltage Waveform, 1.0 V/Division
Lower Trace: Output Voltage Waveform, 2.0 V/Division

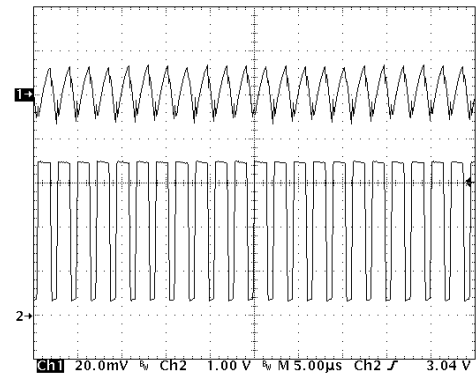
Figure 19. Startup Transient Response

TYPICAL OPERATING CHARACTERISTICS



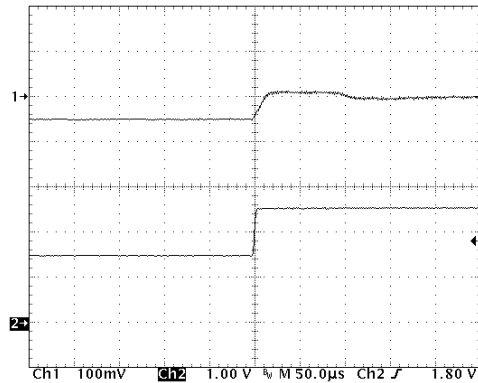
($V_{IN} = 2.5\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 50\text{ mA}$; $L = 5.6\text{ }\mu\text{H}$, $C_{OUT} = 22\text{ }\mu\text{F}$)
 Upper Trace: Output Voltage Ripple, 20 mV/Division
 Lower Trace: Voltage at Lx pin, 1.0 V/Division

Figure 20. Discontinuous Conduction Mode Switching Waveform



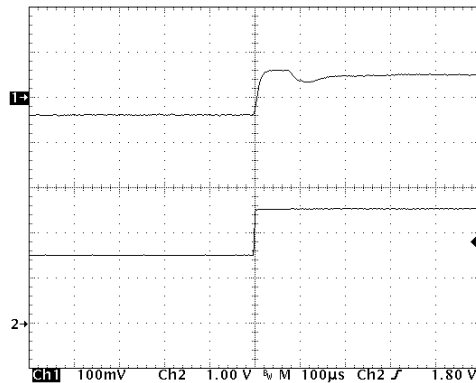
($V_{IN} = 2.5\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 500\text{ mA}$; $L = 5.6\text{ }\mu\text{H}$, $C_{OUT} = 22\text{ }\mu\text{F}$)
 Upper Trace: Output Voltage Ripple, 20 mV/Division
 Lower Trace: Voltage at LX pin, 1.0 V/Division

Figure 21. Continuous Conduction Mode Switching Waveform



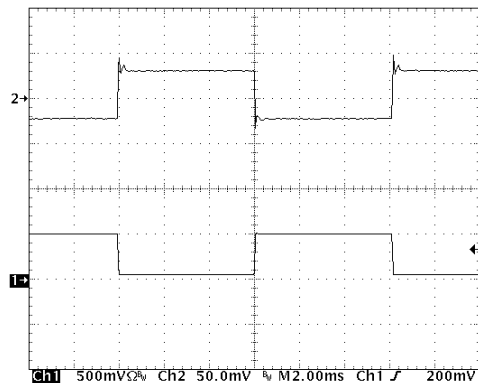
($V_{IN} = 1.5\text{ V to }2.5\text{ V}$; $L = 5.6\text{ }\mu\text{H}$, $C_{OUT} = 22\text{ }\mu\text{F}$, $I_{LOAD} = 100\text{ mA}$)
 Upper Trace: Output Voltage Ripple, 100 mV/Division
 Lower Trace: Battery Voltage, V_{IN} , 1.0 V/Division

Figure 22. Line Transient Response for $V_{OUT} = 3.3\text{ V}$



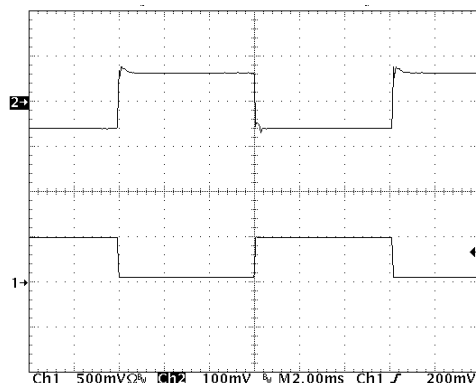
($V_{IN} = 1.5\text{ V to }2.5\text{ V}$; $L = 5.6\text{ }\mu\text{H}$, $C_{OUT} = 22\text{ }\mu\text{F}$, $I_{LOAD} = 100\text{ mA}$)
 Upper Trace: Output Voltage Ripple, 100 mV/Division
 Lower Trace: Battery Voltage, V_{IN} , 1.0 V/Division

Figure 23. Line Transient Response For $V_{OUT} = 5.0\text{ V}$



($V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 50\text{ mA to }500\text{ mA}$; $L = 5.6\text{ }\mu\text{H}$, $C_{OUT} = 22\text{ }\mu\text{F}$)
 Upper Trace: Output Voltage Ripple, 50 mV/Division
 Lower Trace: Load Current, I_{LOAD} , 500 mA/Division

Figure 24. Load Transient Response For $V_{IN} = 2.5\text{ V}$



($V_{OUT} = 5.0\text{ V}$, $I_{LOAD} = 50\text{ mA to }500\text{ mA}$; $L = 5.6\text{ }\mu\text{H}$, $C_{OUT} = 22\text{ }\mu\text{F}$)
 Upper Trace: Output Voltage Ripple, 100 mV/Division
 Lower Trace: Load Current, I_{LOAD} , 500 mA/Division

Figure 25. Load Transient Response For $V_{IN} = 3.0\text{ V}$

DETAILED OPERATION DESCRIPTION

NCP1421 is a monolithic micropower high-frequency step-up voltage switching converter IC specially designed for battery operated hand-held electronic products up to 600 mA loading. It integrates a Synchronous Rectifier to improve efficiency as well as to eliminate the external Schottky diode. High switching frequency (up to 1.2 MHz) allows for a low profile inductor and output capacitor to be used. Low-Battery Detector, Logic-Controlled Shutdown, and Cycle-by-Cycle Current Limit provide value-added features for various battery-operated applications. With all these functions ON, the quiescent supply current is typically only 8.5 μ A. This device is available in a compact Micro8 package.

PFM Regulation Scheme

From the simplified functional diagram (Figure 1), the output voltage is divided down and fed back to pin 1 (FB). This voltage goes to the non-inverting input of the PFM comparator whereas the comparator's inverting input is connected to the internal voltage reference, REF. A switching cycle is initiated by the falling edge of the comparator, at the moment the main switch (M1) is turned ON. After the maximum ON-time (typically 0.72 μ S) elapses or the current limit is reached, M1 is turned OFF and the synchronous switch (M2) is turned ON. The M1 OFF time is not less than the minimum OFF-time (typically 0.12 μ S), which ensures complete energy transfer from the inductor to the output capacitor. If the regulator is operating in Continuous Conduction Mode (CCM), M2 is turned OFF just before M1 is supposed to be ON again. If the regulator is operating in Discontinuous Conduction Mode (DCM), which means the coil current will decrease to zero before the new cycle starts, M1 is turned OFF as the coil current is almost reaching zero. The comparator (ZLC) with fixed offset is dedicated to sense the voltage drop across M2 as it is conducting; when the voltage drop is below the offset, the ZLC comparator output goes HIGH and M2 is turned OFF. Negative feedback of closed-loop operation regulates voltage at pin 1 (FB) equal to the internal reference voltage (1.20 V).

Synchronous Rectification

The Synchronous Rectifier is used to replace the Schottky Diode to reduce the conduction loss contributed by the forward voltage of the Schottky Diode. The Synchronous Rectifier is normally realized by powerFET with gate control circuitry that incorporates relatively complicated timing concerns.

As the main switch (M1) is being turned OFF and the synchronous switch M2 is just turned ON with M1 not being completely turned OFF, current is shunt from the output bulk capacitor through M2 and M1 to ground. This power loss lowers overall efficiency and possibly damages the switching FETs. As a general practice, a certain amount

of dead time is introduced to make sure M1 is completely turned OFF before M2 is being turned ON.

The previously mentioned situation occurs when the regulator is operating in CCM, M2 is being turned OFF, M1 is just turned ON, and M2 is not being completely turned OFF. A dead time is also needed to make sure M2 is completely turned OFF before M1 is being turned ON.

As coil current is dropped to zero when the regulator is operating in DCM, M2 should be OFF. If this does not occur, the reverse current flows from the output bulk capacitor through M2 and the inductor to the battery input, causing damage to the battery. The ZLC comparator comes with fixed offset voltage to switch M2 OFF before any reverse current builds up. However, if M2 is switched OFF too early, large residue coil current flows through the body diode of M2 and increases conduction loss. Therefore, determination of the offset voltage is essential for optimum performance. With the implementation of the synchronous rectification scheme, efficiency can be as high as 94% with this device.

Cycle-by-Cycle Current Limit

In Figure 1, a SENSEFET is used to sample the coil current as M1 is ON. With that sample current flowing through a sense resistor, a sense-voltage is developed. The threshold detector (I_{LIM}) detects whether the sense-voltage is higher than the preset level. If the sense voltage is higher than the present level, the detector output notifies the Control Logic to switch OFF M1, and M1 can only be switched ON when the next cycle starts after the minimum OFF-time (typically 0.12 μ S). With proper sizing of the SENSEFET and sense resistor, the peak coil current limit is typically set at 1.5 A.

Voltage Reference

The voltage at REF is typically set at 1.20 V and can output up to 2.5 mA with load regulation $\pm 2\%$ at V_{OUT} equal to 3.3 V. If V_{OUT} is increased, the REF load capability can also be increased. A bypass capacitor of 200 nF is required for proper operation when REF is not loaded. If REF is loaded, a 1.0 μ F capacitor at the REF pin is needed.

True-Cutoff

The NCP1421 has a True-Cutoff function controlled by the multi-function pin LBI/EN (pin 2). Internal circuitry can isolate the current through the body diode of switch M2 to load. Thus, it can eliminate leakage current from the battery to load in shutdown mode and significantly reduce battery current consumption during shutdown. The shutdown function is controlled by the voltage at pin 2 (LBI/EN). When pin 2 is pulled to lower than 0.3 V, the controller enters shutdown mode. In shutdown mode, when switches M1 and M2 are both switched OFF, the internal

reference voltage of the controller is disabled and the controller typically consumes only 50 nA of current. If the pin 2 voltage is raised to higher than 0.5 V (for example, by a resistor connected to V_{IN}), the IC is enabled again, and the internal circuit typically consumes 8.5 μ A of current from the OUT pin during normal operation.

Low-Battery Detection

A comparator with 30 mV hysteresis is applied to perform the low-battery detection function. When pin 2

(LBI/EN) is at a voltage (defined by a resistor divider from the battery voltage) lower than the internal reference voltage of 1.20 V, the comparator output turns on a 50 Ω low side switch. It pulls down the voltage at pin 3 (LBO) which has hundreds of k Ω of pull-high resistance. If the pin 2 voltage is higher than 1.20 V + 30 mV, the comparator output turns off the 50 Ω low side switch. When this occurs, pin 3 becomes high impedance and its voltage is pulled high again.

APPLICATIONS INFORMATION

Output Voltage Setting

A typical application circuit is shown in Figure 26. The output voltage of the converter is determined by the external feedback network comprised of R1 and R2. The relationship is given by:

$$V_{OUT} = 1.20 \text{ V} \times \left(1 + \frac{R1}{R2}\right)$$

where R1 and R2 are the upper and lower feedback resistors, respectively.

Low Battery Detect Level Setting

The Low Battery Detect Voltage of the converter is determined by the external divider network that is comprised of R3 and R4. The relationship is given by:

$$V_{LB} = 1.20 \text{ V} \times \left(1 + \frac{R3}{R4}\right)$$

where R3 and R4 are the upper and lower divider resistors respectively.

Inductor Selection

The NCP1421 is tested to produce optimum performance with a 5.6 μ H inductor at $V_{IN} = 2.5 \text{ V}$ and $V_{OUT} = 3.3 \text{ V}$, supplying an output current up to 600 mA. For other input/output requirements, inductance in the range 3 μ H to 10 μ H can be used according to end application specifications. Selecting an inductor is a compromise between output current capability, inductor saturation limit, and tolerable output voltage ripple. Low inductance values can supply higher output current but also increase the ripple at output and reduce efficiency. On the other hand, high inductance values can improve output ripple and efficiency; however, it is also limited to the output current capability at the same time.

Another parameter of the inductor is its DC resistance. This resistance can introduce unwanted power loss and reduce overall efficiency. The basic rule is to select an inductor with the lowest DC resistance within the board space limitation of the end application. In order to help with the inductor selection, reference charts are shown in Figure 27 and 28.

Capacitors Selection

In all switching mode boost converter applications, both the input and output terminals see impulsive

voltage/current waveforms. The currents flowing into and out of the capacitors multiply with the Equivalent Series Resistance (ESR) of the capacitor to produce ripple voltage at the terminals. During the Syn-Rect switch-off cycle, the charges stored in the output capacitor are used to sustain the output load current. Load current at this period and the ESR combine and reflect as ripple at the output terminals. For all cases, the lower the capacitor ESR, the lower the ripple voltage at output. As a general guideline, low ESR capacitors should be used. Ceramic capacitors have the lowest ESR, but low ESR tantalum capacitors can also be used as an alternative.

PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise, and unwanted feedback that can affect the performance of the converter. Hints suggested below can be used as a guideline in most situations.

Grounding

A star-ground connection should be used to connect the output power return ground, the input power return ground, and the device power ground together at one point. All high-current paths must be as short as possible and thick enough to allow current to flow through and produce insignificant voltage drop along the path. The feedback signal path must be separated from the main current path and sense directly at the anode of the output capacitor.

Components Placement

Power components (i.e., input capacitor, inductor and output capacitor) must be placed as close together as possible. All connecting traces must be short, direct, and thick. High current flowing and switching paths must be kept away from the feedback (FB, pin 1) terminal to avoid unwanted injection of noise into the feedback path.

Feedback Network

Feedback of the output voltage must be a separate trace detached from the power path. The external feedback network must be placed very close to the feedback (FB, pin 1) pin and sense the output voltage directly at the anode of the output capacitor.

NCP1421

TYPICAL APPLICATION CIRCUIT

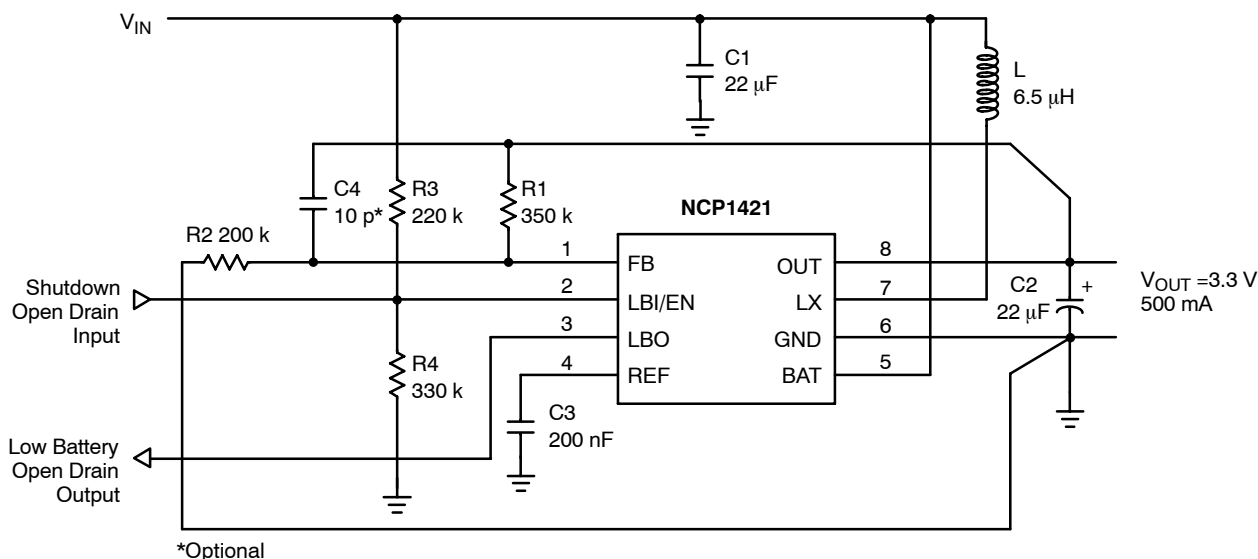


Figure 26. Typical Application Schematic for 2 Alkaline Cells Supply

GENERAL DESIGN PROCEDURES

Switching mode converter design is considered a complicated process. Selecting the right inductor and capacitor values can allow the converter to provide optimum performance. The following is a simple method based on the basic first-order equations to estimate the inductor and capacitor values for NCP1421 to operate in Continuous Conduction Mode (CCM). The set component values can be used as a starting point to fine tune the application circuit performance. Detailed bench testing is still necessary to get the best performance out of the circuit.

Design Parameters:

$V_{IN} = 1.8 \text{ V to } 3.0 \text{ V}$, Typical 2.4 V

$V_{OUT} = 3.3 \text{ V}$

$I_{OUT} = 500 \text{ mA}$ (600 mA max)

$V_{LB} = 2.0 \text{ V}$

$V_{OUT-ripple} = 45 \text{ mV}_{p-p}$ at $I_{OUT} = 500 \text{ mA}$

Calculate the feedback network:

Select $R2 = 200 \text{ k}$

$$R1 = R2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

$$R1 = 200 \text{ k} \left(\frac{3.3 \text{ V}}{1.20 \text{ V}} - 1 \right) = 350 \text{ k}$$

Calculate the Low Battery Detect divider:

$V_{LB} = 2.0 \text{ V}$

Select $R4 = 330 \text{ k}$

$$R3 = R4 \left(\frac{V_{LB}}{V_{REF}} - 1 \right)$$

$$R3 = 330 \text{ k} \left(\frac{2.0 \text{ V}}{1.20 \text{ V}} - 1 \right) = 220 \text{ k}$$

Determine the Steady State Duty Ratio, D , for typical V_{IN} . The operation is optimized around this point:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D}$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}} = 1 - \frac{2.4 \text{ V}}{3.3 \text{ V}} = 0.273$$

Determine the average inductor current, I_{LAVG} , at maximum I_{OUT} :

$$I_{LAVG} = \frac{I_{OUT}}{1 - D} = \frac{500 \text{ mA}}{1 - 0.273} = 688 \text{ mA}$$

Determine the peak inductor ripple current, $I_{RIPPLE-P}$, and calculate the inductor value:

Assume $I_{RIPPLE-P}$ is 20% of I_{LAVG} . The inductance of the power inductor can be calculated as follows:

$$L = \frac{V_{IN} \times t_{ON}}{2 I_{RIPPLE-P}} = \frac{2.4 \text{ V} \times 0.75 \mu\text{s}}{2 (137.6 \text{ mA})} = 6.5 \mu\text{H}$$

A standard value of $6.5 \mu\text{H}$ is selected for initial trial.

Determine the output voltage ripple, $V_{OUT-ripple}$, and calculate the output capacitor value:

$V_{OUT-ripple} = 40 \text{ mV}_{p-p}$ at $I_{OUT} = 500 \text{ mA}$

$$C_{OUT} > \frac{I_{OUT} \times t_{ON}}{V_{OUT-ripple} - I_{OUT} \times ESR_{COUT}}$$

where $t_{ON} = 0.75 \mu\text{s}$ and $ESR_{COUT} = 0.05 \Omega$,

$$C_{OUT} > \frac{500 \text{ mA} \times 0.75 \mu\text{s}}{45 \text{ mV} - 500 \text{ mA} \times 0.05 \Omega} = 18.75 \mu\text{F}$$

NCP1421

From the previous calculations, you need at least 18.75 μF in order to achieve the specified ripple level at the conditions stated. Practically, a capacitor that is one level larger is used to accommodate factors not taken into account in the calculations. Therefore, a capacitor value of 22 μF is selected. The NCP1421 is internally compensated for most applications, but in case additional compensation

is required, the capacitor C4 can be used as external compensation adjustment to improve system dynamics.

In order to provide an easy way for customers to select external parts for NCP1421 in different input voltage and output current conditions, values of inductance and capacitance are suggested in Figure 27, 28 and 29.

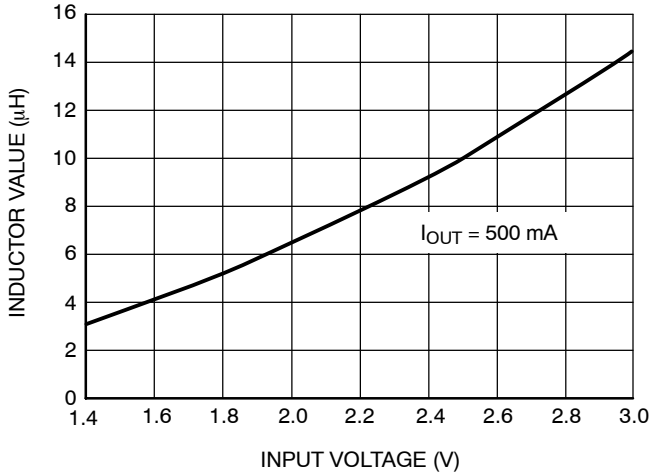


Figure 27. Suggested Inductance of $V_{OUT} = 3.3\text{ V}$

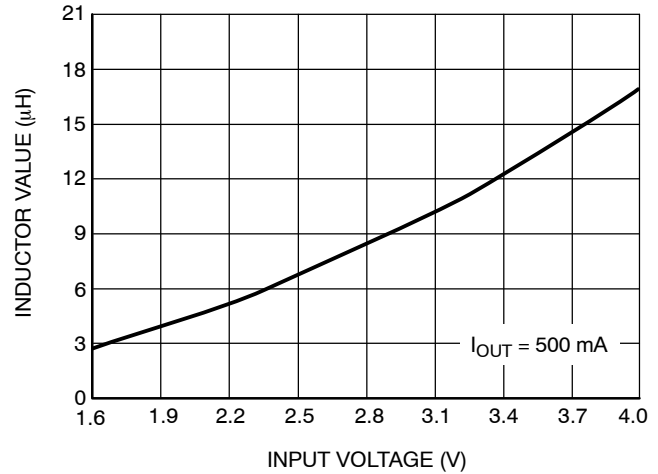


Figure 28. Suggested Inductance of $V_{OUT} = 5.0\text{ V}$

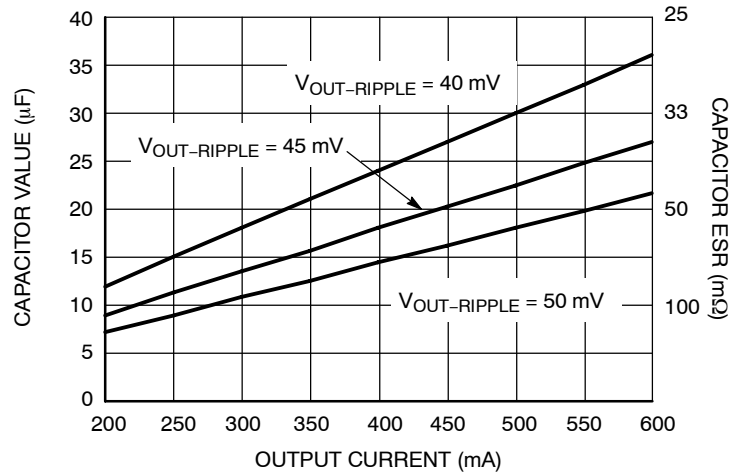


Figure 29. Suggested Capacitance for Output Capacitor

Table 2. Suggestions for Passive Components

Output Current	Inductors	Capacitors
500 mA	Sumida CR43, CR54, CDRH6D28 series	Panasonic ECJ series Kemet TL494 series
250 mA	Sumida CR32 series	Panasonic ECJ series Kemet TL494 series

NCP1500

Dual Mode PWM/Linear BUCK Converter

The NCP1500 is a dual mode converter that operates as either a pulse width modulated (PWM) buck converter or as a linear regulator. The converter automatically transitions between the two modes. The converter operates as a PWM when a synchronization signal is present at the sync input. The converter operates as a linear regulator in the absence of a synchronization signal. The PWM mode offers excellent performance at normal to heavy loads at the sacrifice of output ripple voltage. The linear mode offers excellent noise rejection at the sacrifice of system efficiency. The user is able to select which mode will give the best performance for a given operating condition. Internal protection features include thermal shutdown with hysteresis and cycle-by-cycle current limit in the PWM mode. Additionally, the converter transitions into PFM mode at very light loads if a synchronization signal is present and an output overvoltage condition is detected.

PWM Features

- Current Mode Control with Cycle-by-Cycle Current Limit
- Nominal Synchronization Frequency of 270 to 630 kHz
- Built-in Slope Compensation

Linear Regulator Features

- Low Output Noise

Overall Features

- Thermal Shutdown with Hysteresis
- Digitally Programmable Output Voltage Between 4 Voltages: 1.0, 1.3, 1.5, and 1.8
- Fast Transient Response
- Input Voltage Range From 2.7 V to 5.4 V
- Space Saving Micro8 Package
- Low Shutdown Current of 0.18 μ A Typical
- Pb-Free Package is Available

Typical Applications

- Baseband Supplies for Portable Handsets
- PDAs
- Supplies for DSP Circuitry

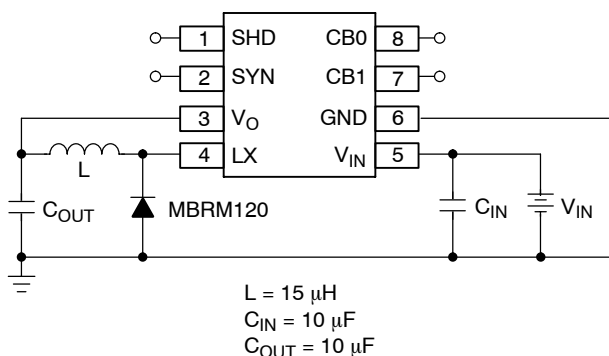


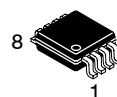
Figure 1. Typical Operating Circuit



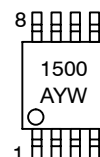
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MARKING DIAGRAM

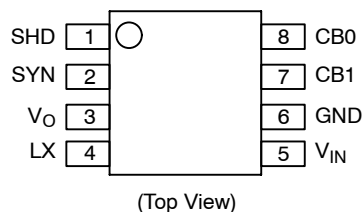


**Micro8™
(MSOP-8)
DM SUFFIX
CASE 846A**



A = Assembly Location
Y = Year
W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP1500DMR2	Micro8	4000 Tape/Reel
NCP1500DMR2G	Micro8 (Pb-Free)	4000 Tape/Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PIN FUNCTION DESCRIPTIONS

Pin #	Symbol	Pin Description
1	SHD	Device is placed in shutdown when SHD is driven low. In shutdown mode, the internal MOSFET and output are turned off. Driven to high for normal operation. This pin is floating internally and needs to be tied to a fixed source externally.
2	SYN	External Synchronization Clock Signal Input. If a clock signal is present at this pin, the device will go into PWM mode. If SYN is driven low, the device operates in linear mode.
3	V _O	Connected to internal voltage divider for feedback.
4	LX	Pin for the connection between the drain of the internal P-MOSFET and the external inductor.
5	V _{IN}	Voltage Supply Input. Bypass with 10 μ F capacitor.
6	GND	Ground.
7	CB1	Control Bit 1 Input for output voltage level selection. Internally pulled low.
8	CB0	Control Bit 0 Input for output voltage level selection. Internally pulled low.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply (Pin 5)	V _{IN}	–0.3 to 6.0	V
Input/Output Pins Pin 1–4 & Pin 7–8	V _{IO}	–0.3 to 6.0	V
Thermal Characteristics Micro8 Plastic Package Thermal Resistance Junction to Air	R _{θJA}	240	°C/W
Operating Junction Temperature Range	T _J	–40 to +140	°C
Operating Ambient Temperature Range	T _A	– 40 to +85	°C
Storage Temperature Range	T _{stg}	– 55 to +150	°C

- This device series contains ESD protection and exceeds the following tests:
Human Body Model (HBM) ± 2.0 kV per JEDEC standard: JESD22–A114.
Machine Model (MM) ± 200 V per JEDEC standard: JESD22–A115.
- Latch-up Current Maximum Rating: ± 150 mA per JEDEC standard: JESD78.

NCP1500

ELECTRICAL CHARACTERISTICS ($V_{IN} = 3.6\text{ V}$, $V_O = 1.5\text{ V}$, $T_A = 25^\circ\text{C}$, $F_{syn} = 600\text{ kHz}$ 50% Duty Cycle sinewave with $V_H = 2.0\text{ V}$ and $V_L = 0\text{ V}$ for PWM mode; $T_A = -40$ to 85°C for Min/Max values, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}	2.7	–	5.4	V
Main FET Leakage Current (Pins 5 to 4) $T_A = 25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to 85°C	I_{LEAK}	– –	0.06 –	0.3 10	μA

Mode Selection Pin

SYN “H” Input Voltage	V_{SYNH}	1.3	–	–	V
SYN “L” Input Voltage	V_{SYNL}	–	–	1.1	V
SYN “H” Input Current	I_{SYNH}	–	0	0.5	μA
SYN “L” Input Current	I_{SYNL}	–0.5	0	–	μA
External Synchronization Frequency	F_{SYNC}	270	–	630	kHz

Output Level Selection Pins

CB “H” Input Voltage Threshold	V_{CBH}	0.90	–	–	V
CB “L” Input Voltage Threshold	V_{CBL}	–	–	0.63	V
CB “H” Input Current	I_{CBH}	–	0.1	–	μA
CB “L” Input Current	I_{CBL}	–	0	–	μA

Shutdown Pin

SHD “H” Input Voltage Threshold	V_{SHDH}	0.59	–	–	V
SHD “L” Input Voltage Threshold	V_{SHDL}	–	–	0.26	V
SHD “H” Input Current	I_{SHDH}	–	0.1	–	μA
SHD “L” Input Current	I_{SHDL}	–	0	–	μA

PWM Mode

Output Voltage ($I_{OUT} = 35\text{ mA}$, $T_A = 25^\circ\text{C}$) CB0, CB1 = (H, H) CB0, CB1 = (H, L) CB0, CB1 = (L, L) CB0, CB1 = (L, H)	V_{OUT0}	0.941 1.235 1.425 1.710	0.99 1.30 1.50 1.80	1.050 1.365 1.575 1.890	V
Line Regulation, $I_{out} = 100\text{ mA}$ 3.0 to 3.6 V 3.0 to 4.2 V	ΔV_{out0}	– –	1.0 2.0	– –	mV
Load Regulation 50 to 120 mA 20 to 200 mA	ΔV_{out0}	– –	1.0 13	– –	mV
Minimum On-Time	T_{ONMIN}	–	210	–	nsec
Internal PFET ON-Resistance ($I_{LX} = 400\text{ mA}$, $V_{IN} = 2.0\text{ V}$)	$R_{DS(ON)_P}$	–	0.65	1.2	Ω
Main Output Switch Current Limit	I_{LIM}	–	800	–	mA

Linear Regulator Mode (Lx shorted to Vo)

Output Voltage ($I_{out} = 0\text{ mA}$, $T_A = 25^\circ\text{C}$) CB0, CB1 = (H, H) CB0, CB1 = (H, L) CB0, CB1 = (L, L) CB0, CB1 = (L, H)	V_{out0}	0.941 1.235 1.425 1.710	0.99 1.30 1.50 1.80	1.050 1.365 1.575 1.890	V
Startup Current Load in Linear Mode	$I_{STARTLIN}$	80	–	–	mA

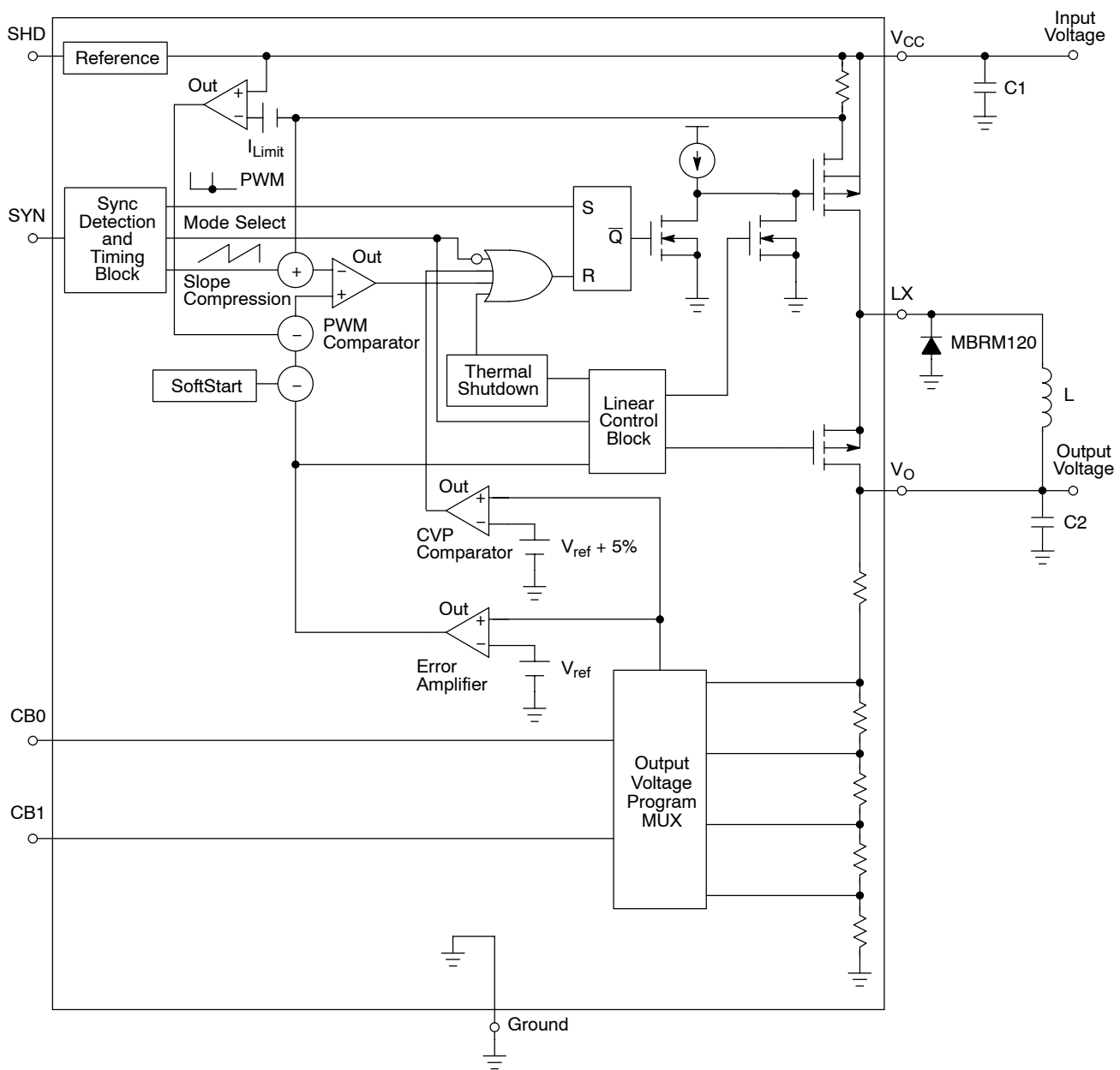
Overvoltage Protection

Output Overvoltage Threshold in PWM Mode	VO_{PFM}	–	+5.0	+10	%

Total Device

Power Supply Current Standby (SHD tied low, $V_{IN} = 3.6\text{ V}$, SYN tied low) $T_A = 25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to 85°C PWM Mode (SHD tied high, $V_{IN} = 3.6\text{ V}$, $V_{out} = 1.6\text{ V}$, $V_{CB0} = V_{CB1} = 0\text{ V}$, SYN @ 600 kHz/50% duty cycle, $I_{out} = 0\text{ mA}$) Linear Mode (SHD tied high, $V_{IN} = 3.6\text{ V}$, $V_{out} = 1.5\text{ V}$, SYN tied low, $I_{out} = 0\text{ mA}$)	I_{CC}	– – – –	0.18 – 96 30	0.5 10 150 70	μA

NCP1500



Component	Value	Manufacturer
C1, C2	10 μ F, 6.3 V	TDK, C3216X5R0J106M
L	15 μ H	TDK, RLF5018T-150MR76 ($I_{out} = 300$ mA) Coilcraft, D01606T-153 ($I_{out} = 300$ mA) TDK, NLC252018T-150 ($I_{out} = 100$ mA)

Figure 2. Typical Circuit with the Internal Schematic

DETAILED OPERATING DESCRIPTION

Introduction

The NCP1500 is a dual mode regulator intended for use in baseband supplies for portable equipment. Its unique features provide power to the baseband circuitry while, at the same time save valuable battery energy. When the handset is idle, the user can activate the linear regulator function. In this mode, the regulator provides a regulated low current, low noise output voltage keeping the baseband circuit biased. When the handset is in its normal operating mode, the regulator synchronizes to the baseband clock and turns into a switching regulator. This allows the regulator to provide efficient power to the baseband circuit.

Operating Description

Synchronization Protocol and Mode Selection

The NCP1500 has a SYNC input. The device operates at a fixed switch frequency determined by the frequency of the synchronization signal applied. The part automatically operates in PWM mode after synchronization pulses are present for several cycles. The NCP1500 will output 2 pulses when a sync signal is present. The first is a PWM pulse. This pulse 'sets' a latch that initiates output switch conduction. The width of this pulse controls the minimum on time in PWM mode. The second signal is a slope compensation ramp. A ramp signal is generated. This signal is summed with the current information before being fed into the PWM comparator. The purpose of this circuit is to provide stable operation at output switch duty cycles in excess of 50%. The device automatically switches to linear mode when the SYNC signal is removed for approximately 6.0 μs . **It is recommended that the sync signal be externally pulled low to enable the linear mode.** Pulling the pin high or open may cause portions of the circuit to remain active, increasing the total current consumption of the IC. The threshold level of the SYNC signal is typically 1.3 V. The duty cycle of the sync signal must be within 20 to 80%.

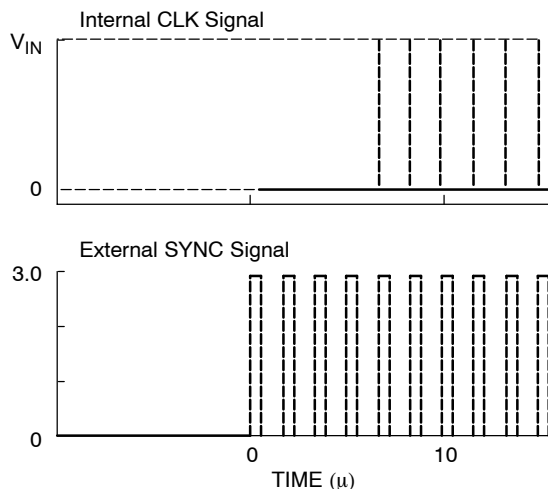


Figure 3. Timing Diagram of the SYNC Signal

Figure 3 shows the waveform when the SYNC signal is applied. After several cycles, the MODE select changes and PWM operation is activated with the internal clock signal.

Reference/Shutdown

The NCP1500 uses an internal reference, typically at 0.8 V. An external shutdown pin is provided. When this pin is pulled low, the reference and other circuitry are disabled, placing the part into a low quiescent current standby mode. In this mode, the pass device is off and the output voltage will be zero. The typical standby current is 0.18 μA .

Error Amplifier/Output Voltage Program

A fully compensated error amplifier is provided inside the NCP1500. No external circuitry is required to stabilize the operation of the NCP1500. The error amplifier provides an error signal to both the PWM circuit and the linear regulator circuit. The output of the error amplifier is directly connected to the linear regulator control circuit. However, the output of the error amplifier is connected first to a subtraction circuit before going to the input of the PWM comparator. The subtraction circuit is activated only during an over current condition. During this condition, a signal proportional to the amount of over current is subtracted from the error amplifier signal. This subtraction results in a lower signal applied to the PWM comparator, thus lowering the output duty cycle.

The output voltage is digitally programmable up to four voltages. Two program pins are provided to accomplish this task. The program pins control a mux, which switch a bank of resistors. The appropriate resistor bank is switched to the error amplifier input, depending on the program input. The following truth table can be used to program the output voltage:

CB0	CB1	Output Voltage
0	0	1.5
0	1	1.8
1	0	1.3
1	1	1.0

Both program pins are internally pulled low. Thus, if the input pins are left open, the output voltage will be 1.5 V.

PWM Section

The PWM section consists of a PWM comparator, set dominant latch, slope compensation circuit, current sense circuit, and current limit circuit.

The NCP1500 operates as a current mode regulator in PWM mode. In this mode, a PWM pulse from the synchronization section initiates the output switch conduction. Output switch conduction is terminated when the peak inductor current reaches a threshold level established by the error amplifier. The output switch conduction duty cycle is allowed to go to 100% to increase transient load response when going from light load to heavy load.

A reset dominant latch is provided in the NCP1500. A 3 input OR gate controls the reset pin. Any one of the 3 inputs will terminate output switch conduction. Once terminated, output switch conduction cannot begin again until the next PWM pulse. The only state the NCP1500 does not switch every cycle is if the 5% overvoltage comparator trips. When the comparator trips, the switching regulator will remain off until the voltage drops below the nominal voltage. This state

is similar to a PFM mode of operation. Output switch conduction can begin at the next PWM cycle after the OVP input is reset.

Current mode controllers can exhibit an instability at duty cycles over 50%. A slope compensation circuit is provided inside the NCP1500 to overcome the potential instability. Slope compensation consists of a ramp signal generated by the synchronization block and adding this to the current signal. The summed signal is then applied to the PWM comparator.

A current limit feature is provided in the PWM mode only. The current limit is set to allow peak switch current in excess of 800 mA. It is implemented as a cycle-by-cycle current limit. Each on-cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch transistor current buildup during conduction. An error signal is generated upon sensing an over-current condition. This signal is subtracted from the error amplifier output. This in turn reduces the PWM comparison threshold voltage, thus limiting the output duty cycle.

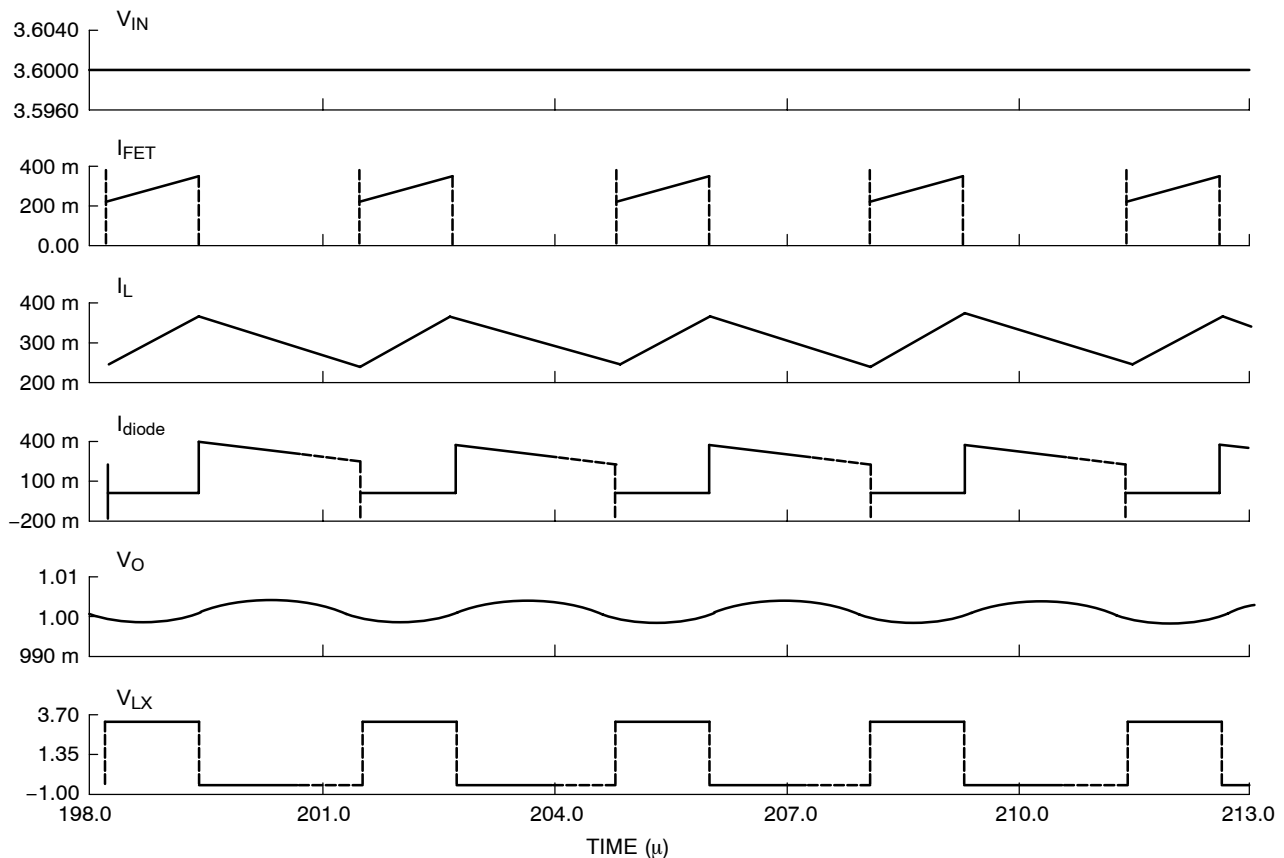


Figure 4. PWM Waveforms During Normal Operation

NCP1500

Linear Mode Operation

The NCP1500 operates as a linear regulator if the synchronization signal is absent. The part is designed to provide up to 50 mA nominally in this mode. Transients of up to 100 mA can be accommodated if the thermal impact is low. The main output is in series with an external inductor. This can cause a lag in the transient response of the device

when going from light load to heavy load. A bypass transistor is incorporated to release the energy stored in the inductor in order to avoid oscillation within the operation range. (Patent Pending).

The following figure shows the transient step load response of the NCP1500 in this mode of operation.

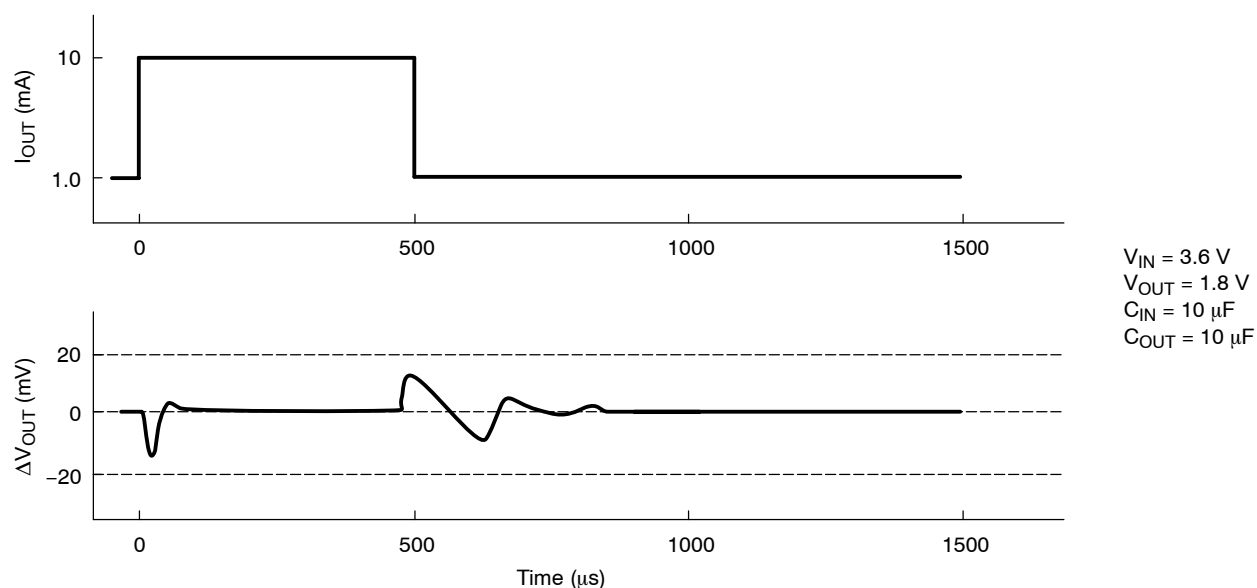


Figure 5. Load Transient Response in Linear Mode

Over Voltage Protection

NCP1500 has an overvoltage protection circuit that protects the output during the PWM mode. Normally, in PWM mode, the output switch will conduct at the onset of every synchronization pulse. The minimum output duty cycle is 3%. The output voltage will rise at minimum duty cycle and a light load or no load condition is present at the output. If the output rises more than 5% of the programmed

voltage, an overvoltage comparator will trip. This signal will reset the PWM latch and hold it in a reset condition until the output voltage decays below its threshold. The output will then be allowed to switch at the next synchronization pulse. This type of operation is usually referred to as PFM or skip mode operation.

The following figure is a simulation of the regulator during this condition:

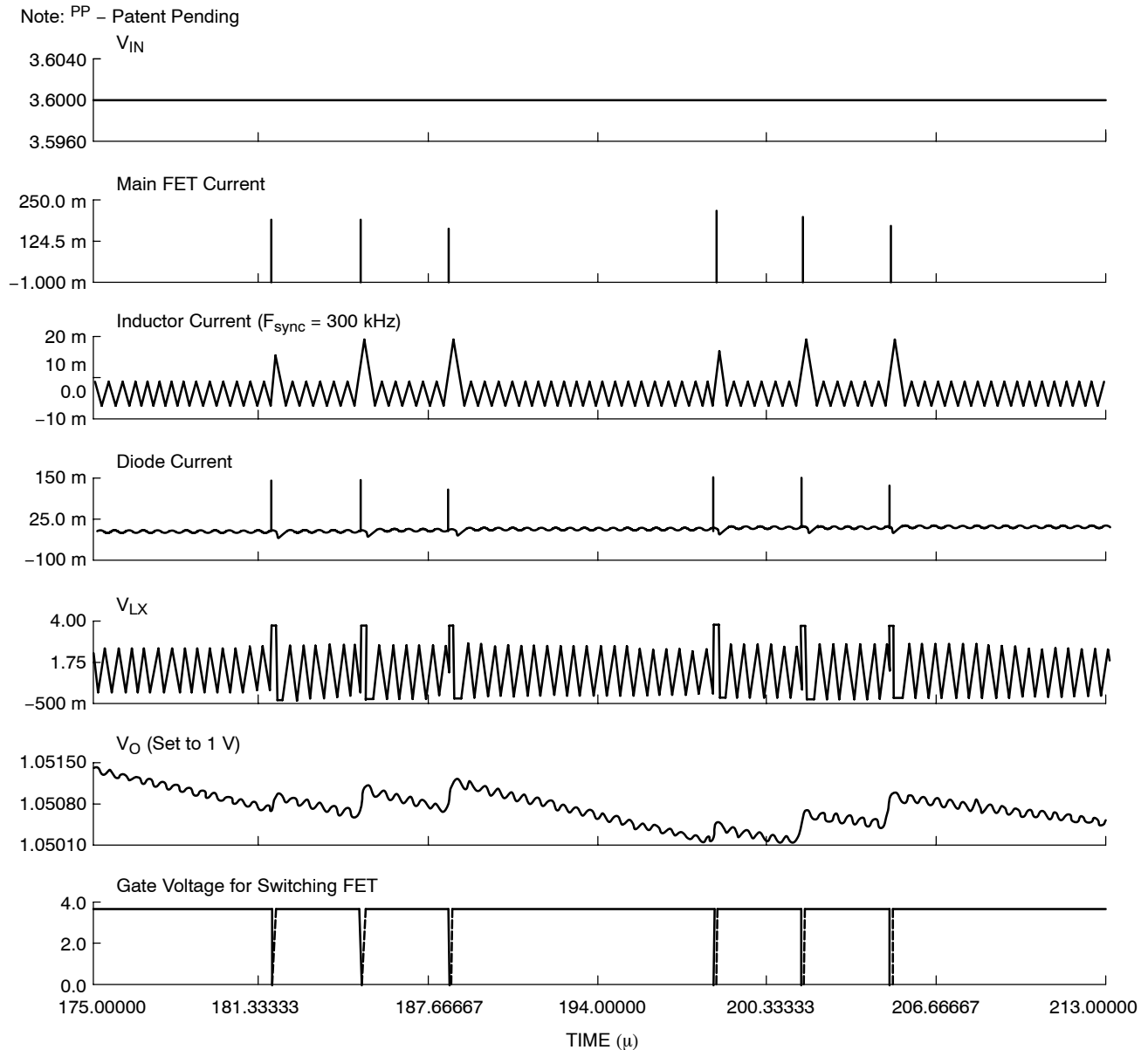


Figure 6. Waveforms of PFM Mode Operation During Over Voltage

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event at the maximum junction temperature is exceeded. When activated, typically at 150°C, the PWM latch is reset and the linear regulator control circuitry is disabled. The thermal shutdown circuit is designed with 25°C of hysteresis. This means that the

PWM latch and the regulator control circuitry cannot be re-enabled until the die temperature drops by this amount. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended as a substitute for proper heatsinking.** The NCP1500 is contained in the Micro8 package.

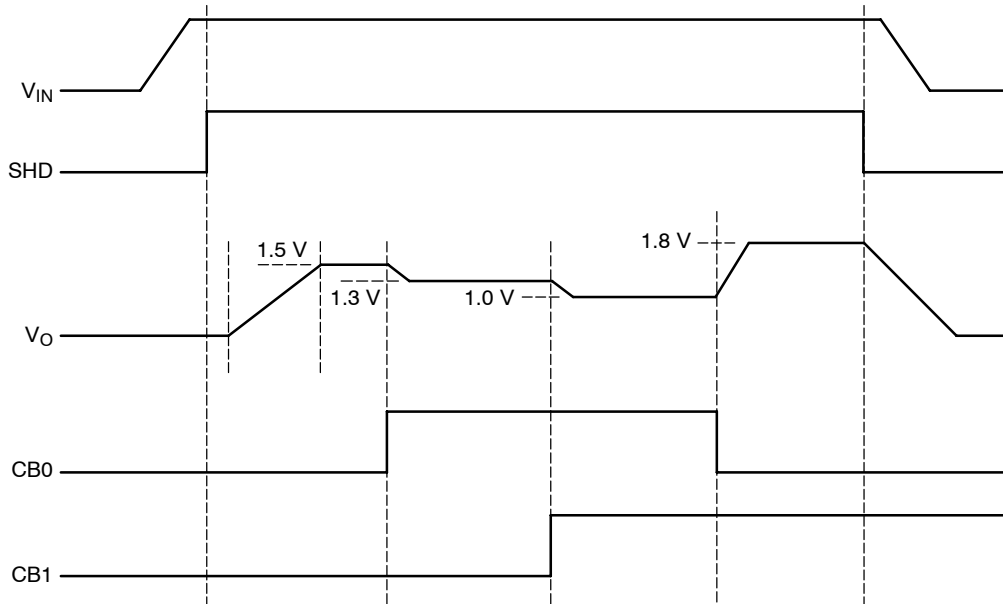


Figure 7. Power-Up and Power-Down Sequence

APPLICATIONS INFORMATION

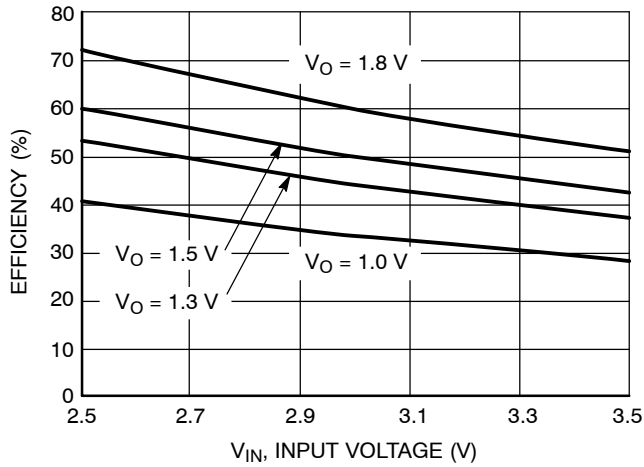


Figure 8. Efficiency in Linear Mode Operation vs. Input Voltage ($I_{OUT} = 10 \text{ mA}$)

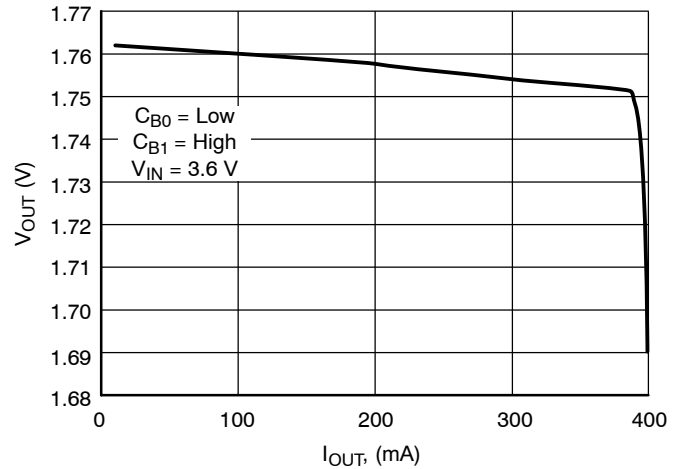


Figure 9. Output Voltage vs. Output Current in LDO Mode

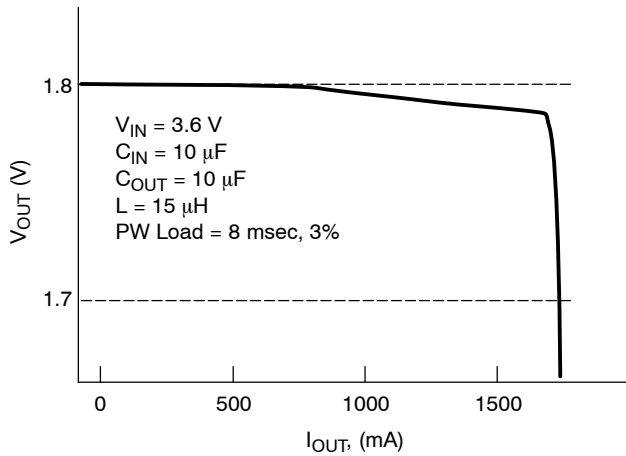


Figure 10. Output Voltage vs. Output Current in PWM Mode

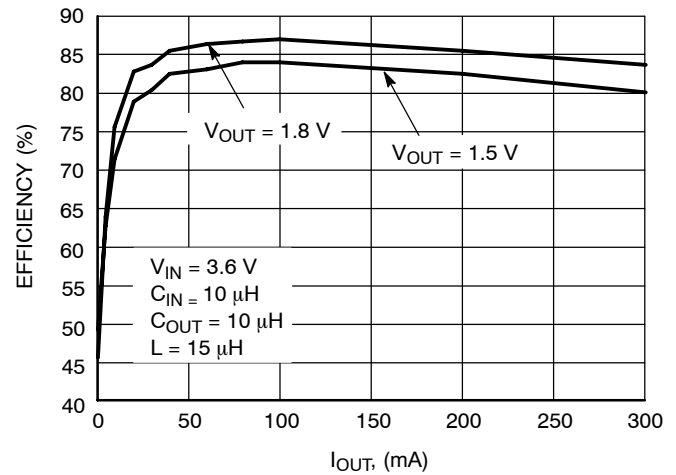


Figure 11. PWM Efficiency

Table 3. Efficiency Measurement in PWM Mode

V_{OUT} (V)	V_{IN} (V)	I_{OUT} (mA)										
		1	5	10	20	30	40	60	80	100	200	300
1.5	2.5	44%	75%	82%	86%	87%	88%	88%	88%	90%	84%	80%
	3.0	44%	68%	76%	82%	84%	85%	86%	86%	86%	83%	80%
	3.6	49%	62%	71%	79%	80%	83%	83%	84%	84%	82%	80%
	4.2	51%	64%	66%	75%	77%	80%	81%	82%	82%	82%	79%
1.8	2.5	48%	79%	86%	90%	90%	91%	91%	91%	91%	87%	84%
	3.0	41%	73%	80%	85%	88%	88%	89%	89%	89%	86%	84%
	3.6	45%	64%	76%	83%	84%	86%	86%	87%	87%	85%	84%
	4.2	52%	63%	71%	78%	81%	83%	84%	85%	85%	85%	83%

NOTE: See figure 1 for circuit configuration.
 $C_{in} = C_{out} = \text{C3216X5R106M}$
 $L = \text{D01606T-153}$

NCP1501

Dual Mode PWM/Linear Buck Converter

The NCP1501 is a dual mode regulator that operates either as a PWM Buck Converter or as a Low Drop Out Linear Regulator. If a synchronization signal is present, the NCP1501 operates as a current mode PWM converter with synchronous rectification. The synchronization signal allows the user to control the location of the spurious frequency noise generated by a PWM converter. Linear mode is active when a synchronization signal is not present. The NCP1501 configuration allows an efficient high power operation and low noise during system sleep modes.

Features

- Synchronous Rectification for Higher Efficiency in PWM Mode
- Linear Mode Operation for Low Noise Output at Low Loads
- Integrated MOSFETs and Feedback Circuits
- Cycle-by-Cycle Peak Current Limit of 800 mA (typ)
- Automatic Switching Between PWM and Linear Mode
- Operating Frequency Range of 500 to 1000 kHz
- Optimized for Ceramic Capacitors and Low Profile Inductors
- Thermal Limit Protection
- Built-in Slope Compensation for Current Mode PWM Converter
- Fixed Output Voltages of 1.05 V, 1.35 V, 1.57 V, 1.8 V
- Shutdown Current Consumption of 0.2 μ A
- Internal Soft Start
- Transistor Count: 3500
- Pb-Free Package is Available

Typical Applications

- Cellular Phones
- PDAs
- Pagers
- Supplies for DSP Cores
- Portable Applications

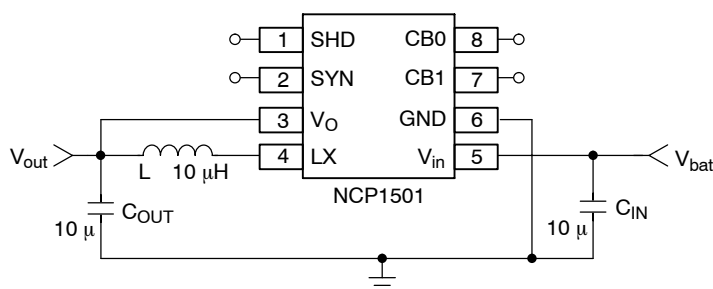


Figure 1. Typical Applications Circuit



ON Semiconductor®

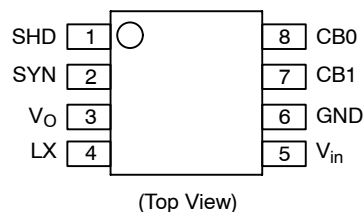
<http://onsemi.com>

MARKING DIAGRAM



1501 = Device Code
A = Assembly Location
Y = Year
W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP1501DMR2	Micro8	4000/Tape & Reel
NCP1501DMR2G	Micro8 (Pb-Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP1501

PIN FUNCTION DESCRIPTIONS

Pin #	Symbol	Pin Description
1	SHD	Enable Pin for the NCP1501. This pin is active high. Internal pull down resistor forces the part off if the pin is not connected on the board.
2	SYN	External Synchronization Signal Pin. The device will operate in PWM mode if a clock signal is present. The pin must be pulled low to enter LDO mode. Internal pull down resistor on pin.
3	V _O	Feedback for the NCP1501. An internal MOSFET is connected across V _O and LX for LDO mode.
4	LX	Connection for the pass devices to the inductor.
5	V _{in}	Input voltage to the NCP1501.
6	GND	Ground Connection for the device.
7	CB1	Voltage Selection Bit. Internal pull up resistor on pin.
8	CB0	Voltage Selection Bit. Internal pull down resistor on pin.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Maximum Voltage All Pins	V _{max}	5.5	V
Maximum operating Voltage All Pins	V _{max}	5.2	V
Thermal Resistance, Junction-to-Air	R _{θJA}	240	°C/W
Operating Ambient Temperature Range	T _A	–30 to +85	°C
ESD Withstand Voltage	V _{ESD}	> 2500 > 100	V
Moisture Sensitivity	MSL	Level 1	
Storage Temperature Range	T _{stg}	–55 to +150	°C
Junction Operating Temperature Range	T _J	–30 to +125	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22–A114–A
2. Tested to EIA/JESD22–A115–A

ELECTRICAL CHARACTERISTICS (V_{in} = 3.6 V, V_O = 1.57 V, T_A = 25°C, F_{syn} = 600 kHz 50% Duty Cycle square wave for PWM mode; T_A = –30 to 85°C for Min/Max values, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit

V_{CC} Pin

Quiescent Current of Switching Mode, I _{out} = 0 mA	I _q PWM	–	124	500	μA
Quiescent Current of LDO Mode, I _{out} = 0 mA	I _q LDO	–	32	65	μA
Quiescent Current, SHD Low	I _q Off	–	0.2	1.0	μA
Input Voltage Range	V _{in}	2.7	–	5.2	V

Sync Pin

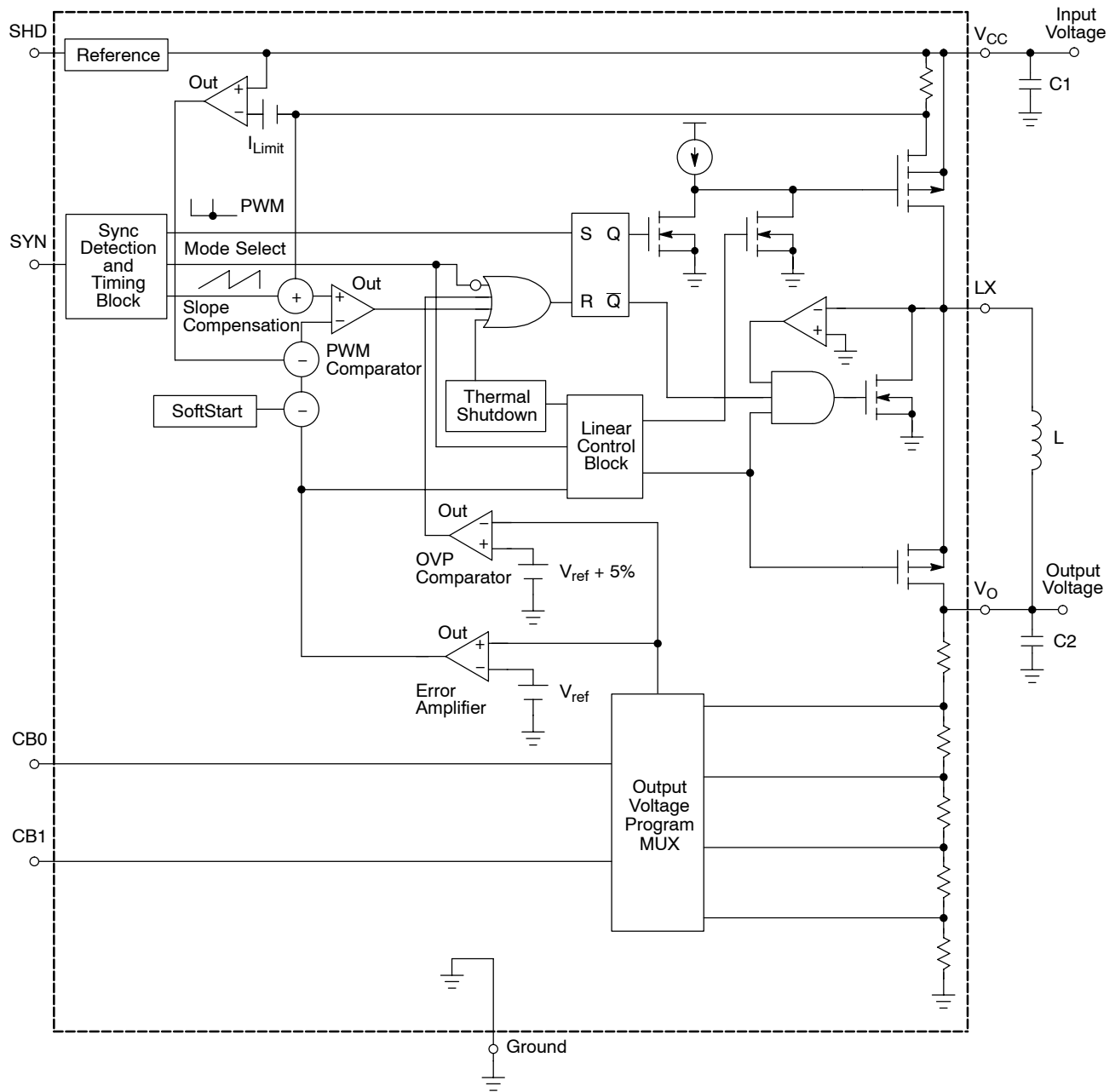
Input Voltage	V _{sync}	–0.3	–	V _{CC} +0.3	V
Frequency Operational Range	F _{sync}	500	–	1000	kHz
Minimum Synchronization Pulse Width	D _c _{sync(min)}	–	30	–	%
Maximum Synchronization Pulse Width	D _c _{sync(max)}	–	70	–	%
SYNC “H” Voltage Threshold	V _{sync(H)}	–	920	1200	mV
SYNC “L” Voltage Threshold	V _{sync(L)}	400	830	–	mV
SYNC “H” Input Current, V _{sync} = 3.6 V	I _{sync(H)}	–	1.8	–	μA
SYNC “L” Input Current, V _{sync} = 0 V	I _{sync(L)}	–0.5	0.005	–	μA

NCP1501

ELECTRICAL CHARACTERISTICS (continued) ($V_{in} = 3.6\text{ V}$, $V_O = 1.57\text{ V}$, $T_A = 25^\circ\text{C}$, $F_{syn} = 600\text{ kHz}$ 50% Duty Cycle square wave for PWM mode; $T_A = -30$ to 85°C for Min/Max values, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Level Selection Pins					
Input Voltage	V_{CB}	-0.3	-	$V_{CC}+0.3$	V
CB0,1 "H" Voltage Threshold	$V_{CB(H)}$	-	910	1200	mV
CB0,1 "L" Voltage Threshold	$V_{CB(L)}$	400	850	-	mV
CB0,1 "H" Input Current, $CBx = 3.6\text{ V}$	$I_{CB(H)}$	-	1.8	-	μA
CB0,1 "L" Input Current, $CBx = 0\text{ V}$	$I_{CB(L)}$	-0.5	0	-	μA
Shutdown Pin					
Input Voltage	V_{SHD}	-0.3	-	$V_{CC}+0.3$	V
SHD "H" Voltage Threshold	$V_{SHD(H)}$	-	920	1200	mV
SHD "L" Voltage Threshold	$V_{SHD(L)}$	400	850	-	mV
SHD "H" Input Current, $SHD = 3.6\text{ V}$	$I_{SHD(H)}$	-	1.8	-	μA
SHD "L" Input Current, $SHD = 0\text{ V}$	$I_{SHD(L)}$	-0.5	0	-	μA
Feedback Pin					
Input Voltage	V_{fb}	-0.3	-	$V_{CC}+0.3$	V
Input Current, $V_{fb} = 1.8\text{ V}$	I_{fb}	-	8.5	-	μA
PWM Mode Characteristics					
Switching P-FET Current Limit	I_{lim}	-	800	-	mA
Duty Cycle	DC	-	-	100	%
Minimum On Time	$T_{on(min)}$	-	100	-	nsec
$R_{DS(on)}$ Switching N-FET P-FET	$R_{DS(on)}$	- -	0.7 0.6	- -	Ohms
Switching P-FET and N-FET Leakage Current	I_{leak}	-	0.01	10	μA
Output Over Voltage Threshold	V_O	-	3.0	-	%
Output Voltage Accuracy, $V_{out(set)} = 1.05\text{ V}$ $CB0 = L$, $CB1 = L$ $V_{out(set)} = 1.35\text{ V}$ $CB0 = L$, $CB1 = H$ $V_{out(set)} = 1.57\text{ V}$ $CB0 = H$, $CB1 = H$ $V_{out(set)} = 1.80\text{ V}$ $CB0 = H$ $CB1 = L$	V_{out}	1.018 1.309 1.523 1.740	1.050 1.350 1.570 1.800	1.082 1.391 1.617 1.860	V
Load Transient Response, 10 to 100 mA Load Step	V_{out}	-	40	-	mV
Line Transient Response, $I_{out} = 100\text{ mA}$, 3.0 to 3.6 V_{in} Line Step	V_{out}	-	± 5	-	mV _{pp}
LDO Mode Characteristics					
$R_{DS(on)}$ LDO FET (Inductor Switch), LX to V_{out}	$R_{DS(on)}$	-	7.0	-	Ohms
Dropout Voltage (Limited by $V_{in(min)} = 2.5\text{ V}$ and $V_{out(max)} = 1.8\text{ V}$)	$V_{in} - V_{out}$	-	0.7	-	V
Output Voltage Accuracy, $V_{out(set)} = 1.05\text{ V}$ $CB0 = L$, $CB1 = L$ $V_{out(set)} = 1.35\text{ V}$ $CB0 = L$, $CB1 = H$ $V_{out(set)} = 1.57\text{ V}$ $CB0 = H$, $CB1 = H$ $V_{out(set)} = 1.80\text{ V}$ $CB0 = H$ $CB1 = L$	V_{out}	1.018 1.309 1.523 1.740	1.050 1.350 1.570 1.800	1.082 1.391 1.617 1.860	V
Thermal Shutdown					
Thermal Shutdown	TSD	-	160	-	$^\circ\text{C}$
Hysteresis	TSD _{hys}	-	25	-	$^\circ\text{C}$

NCP1501



Component	Value	Manufacturer
C1, C2	10 μ F, 6.3 V	TDK, C2012X5R0J106M (0805 size)
L	10 μ H	TDK, LLF4017-100 ($I_{out} = 300$ mA) Coilcraft, LPO4812-103MX ($I_{out} = 300$ mA) Coilcraft, 0805PS-103M ($I_{out} = 150$ mA) TDK, NLC252018T-100 ($I_{out} = 100$ mA)

Figure 2. Typical Circuit with the Internal Schematic

DETAILED OPERATING DESCRIPTION

The Buck regulator is a synchronous rectifier PWM regulator with integrated MOSFETs. This regulator has an LDO function for low power modes to conserve power and lower ripple voltage associated with PFM mode. The NCP1501 does not contain an internal oscillator for the switching mode. The Dual PWM/LDO mode is an exclusive Patent Pending circuit.

The PWM clock is generated via an external clock signal on the Synchronization pin. The operating frequency range for the PWM is 500 kHz to 1000 kHz. The output current of the PWM is typically 100 mA with a guarantee of over 300 mA for the 2.7 to 5.2 input voltage range.

If a synchronization pulse is not present, the NCP1501 changes into the LDO mode. The LDO function assures the user of an extremely low output ripple voltage and greatly reduced quiescent current when the users system is in a sleep mode. Internally to the NCP1501, the Synchronization pin

has a pull down resistor to force the part into LDO mode when a clock signal is not present. To place the NCP1501 in LDO mode, the user must set the Synchronization pin low. The LDO mode guarantees an output in excess of 50 mA.

Pins CB0 and CB1 control the output voltage selection. The four voltages are 1.05 V, 1.35 V, 1.57 V, 1.8 V. CB0 contains a pull down resistor and CB1 contains a pull up resistor internal to the NCP1501. The resistors force the output of the converter to 1.35 V if the pins are floating connections to the external circuit.

The Shutdown Pin enables the operation of the device. The Shutdown Pin has an internal pull down resistor to force the NCP1501 into the off mode if this pin is floating due to the external circuit. During Startup, the NCP1501 has a soft start function to limit fast dV/dt and eliminate overshoot on the output.

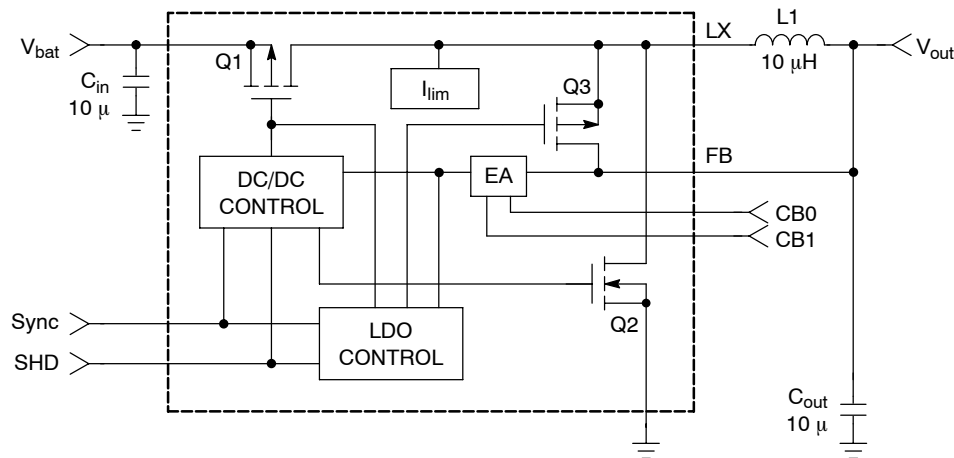


Figure 3. Block Diagram and Circuit Schematic of the NCP1501

The external components required are an input and an output 10 0 μF ceramic capacitor and a 10 μH inductor.

PWM Mode

During normal operation, a synchronization pulse acts as the clock for the DC/DC controller. The rising edge of the clock pulls the gate of Q1 low allowing the inductor to charge. When the current through Q1 reaches either the current limit or feedback voltage reaches its limit, Q1 will turn off and Q2 will turn on. Q2 replaces the free wheeling diode typically associated with Buck Converters. Q2 will turn off when either a rising edge sync pulse is present or all the stored energy is depleted from the inductor. Q3 remains off during this mode.

The output voltage accuracy in the PWM mode is well within 3% of the nominal set value. An over voltage protection circuit is present in the PWM mode to limit the positive voltage spike due to fast load transient conditions. The PWM also has the ability to go to 100% duty cycle for transient conditions and low input to output voltage differentials.

In PWM mode, each switching cycle has a guaranteed on–time of 100 ns. The NCP1501 has two protection circuits that can eliminate the cycle. When tripped, the over voltage protection or the thermal shutdown overrides the gate drive of the high side MOSFET.

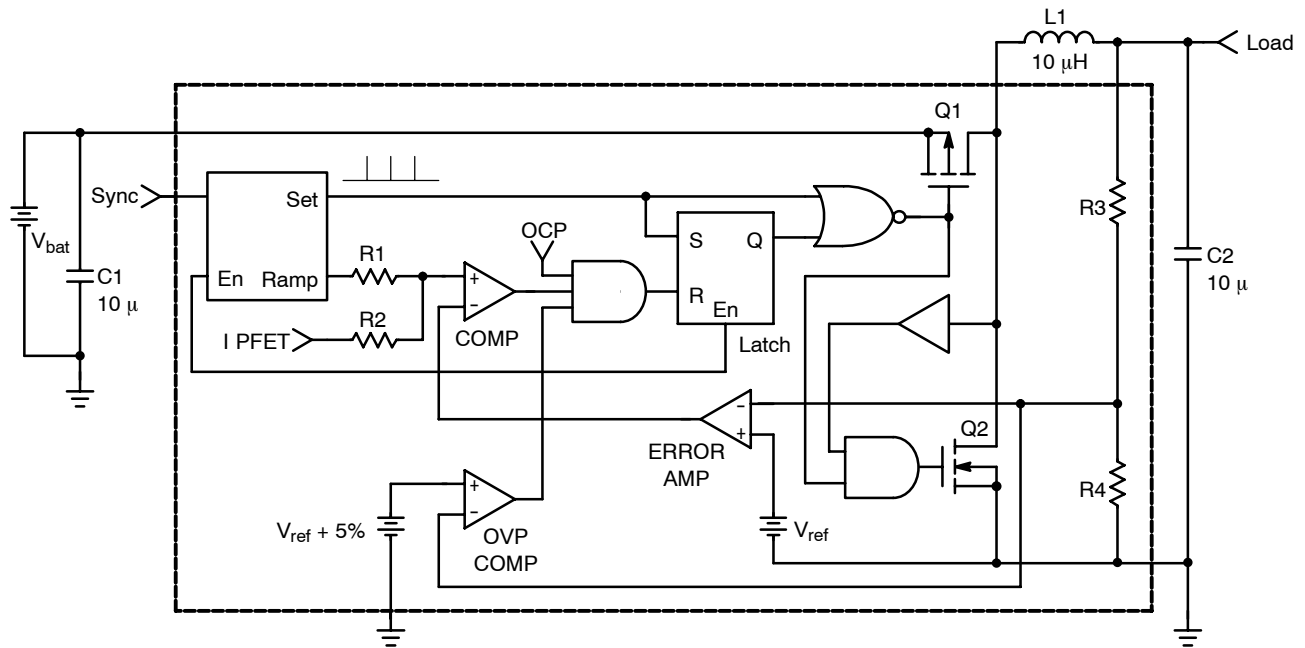


Figure 4. PWM Circuit Schematic

LDO Mode

When the synchronization pulse is not present, the NCP1501 operates as an LDO. The DC/DC Control Circuitry will relinquish control of Q1 and turn off Q2. The

LDO Control Circuitry will turn on Q3 as a bypass circuit to the inductor. Q1 is the controlling pass device of the LDO that regulates the input to output voltage dropout. The LDO can source an output current in excess of 50 mA.

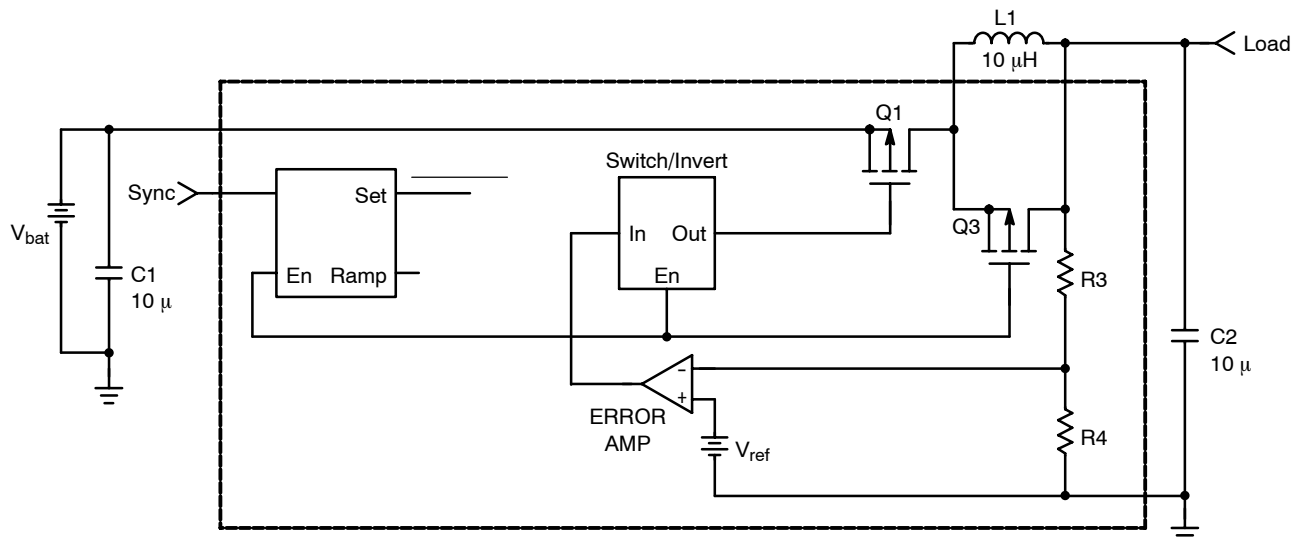


Figure 5. LDO Circuit Schematic

NCP1501

Voltage Output Selection

The output voltage selection is accomplished via two external pins: CB0 and CB1. If CB0 and CB1 pins are left floating by the external circuit, the output voltage will default to 1.35 V. The corresponding voltages are as follows.

CB0	CB1	NCP1501
		V _{out} (V)
0	0	1.05
0	1	1.35
1	1	1.57
1	0	1.80

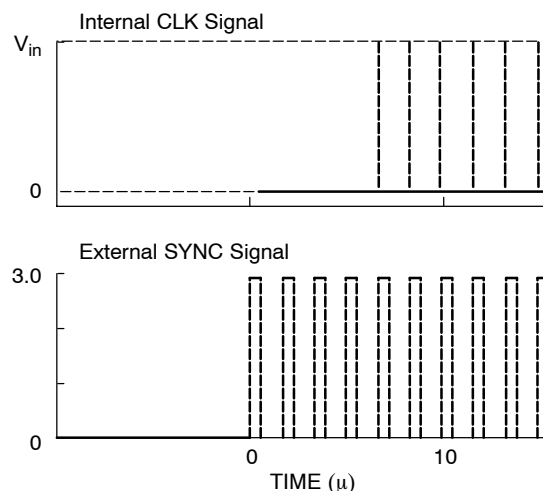


Figure 6. Transition Waveforms from LDO to PWM Mode

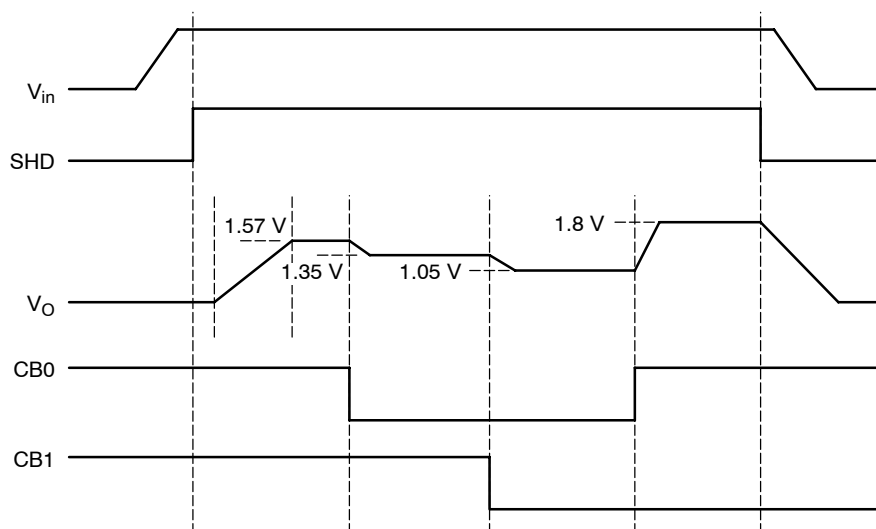


Figure 7. Power Up and Power Down Sequence

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 160°C, the PWM latch is reset and the linear regulator control circuitry is disabled. The thermal shutdown circuit is designed with 25°C of hysteresis. This means that the

PWM latch and the regulator control circuitry cannot be re-enabled until the die temperature drops by this amount. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended as a substitute for proper heatsinking. The NCP1501 is contained in the Micro-8 package.

NCP1501

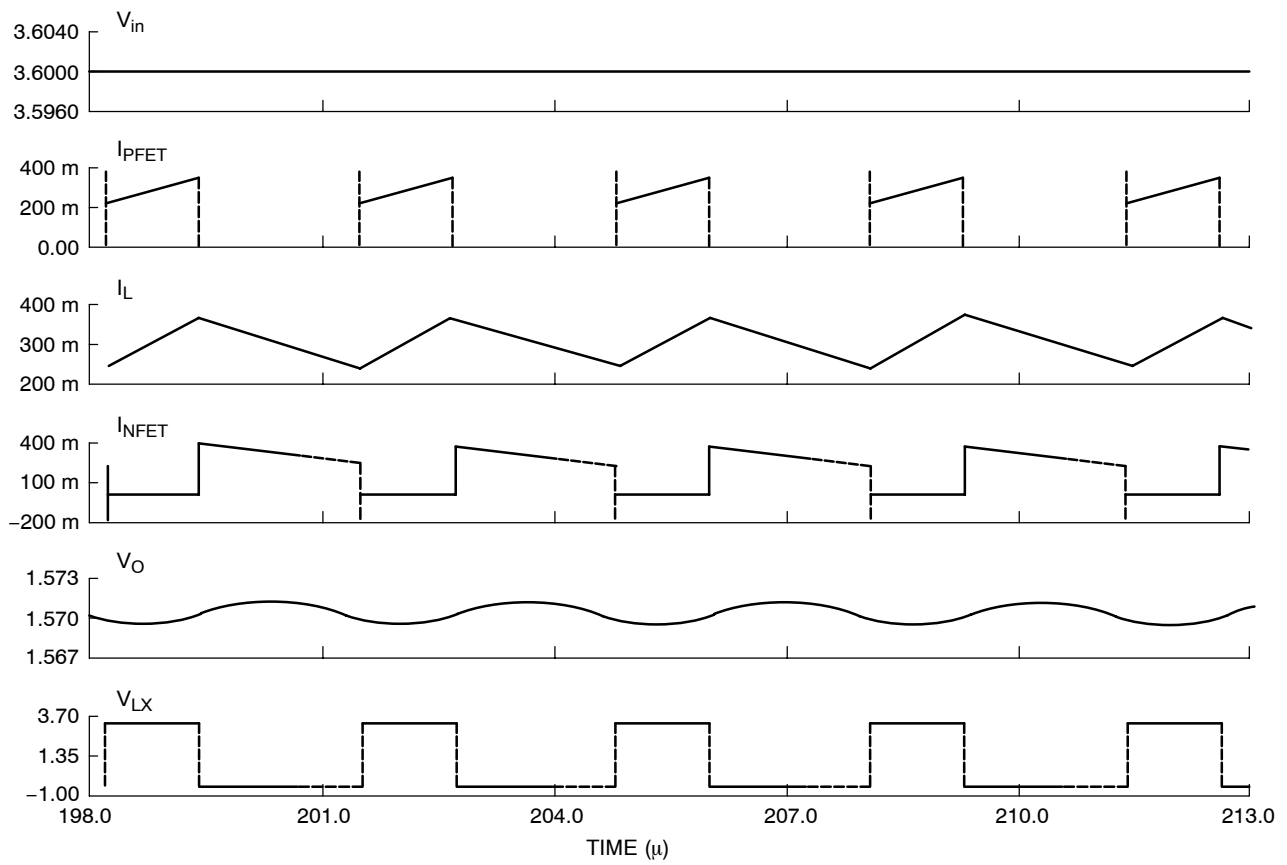


Figure 8. Waveforms During Normal Operation

APPLICATIONS INFORMATION

NCP1501 is a dual mode PWM or LDO step down converter. This dual mode takes advantage of the best of each mode. There are three required external components: an input and output capacitor and an inductor.

The PWM mode allows high efficiency for larger loads. A typical efficiency for an input of 3.6 V and an output of 1.8 V and 100 mA is over 90%. Low $R_{DS(on)}$ and synchronous rectification contained within the device contributes to the very high efficiency. As with other synchronous rectification devices, the NCP1501 does not require an external diode to supplement the NFET during switching on or off. A synchronization pin allows the user to define the frequency noise spikes of the PWM. The duty cycle of the synchronization signal must be within the range

of 30% to 70%. The rising edge of the signal from the synchronization pin acts as the oscillator signal to set the latch and reset the ramp compensation signal. An Over Voltage Protection circuit ensures the output will respond properly to fast transients from large to small loads. The NCP1501 allows the PWM mode to enter a 100% duty cycle for fast load transient conditions and low input to output voltage differentials.

The LDO mode is effective during low load conditions by lowering the quiescent current and reducing the output ripple voltage associated with PWM converters entering PFM mode. NCP1501 enters the LDO mode when a synchronization signal is not present. It is recommended to pull the synchronization signal low for LDO mode.

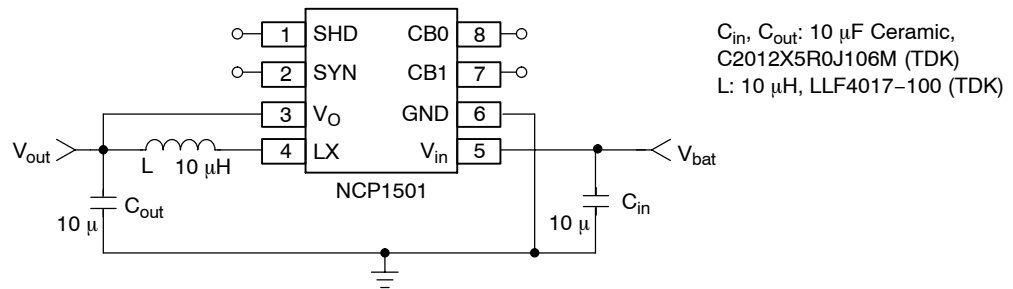


Figure 9. Typical Operating Schematic

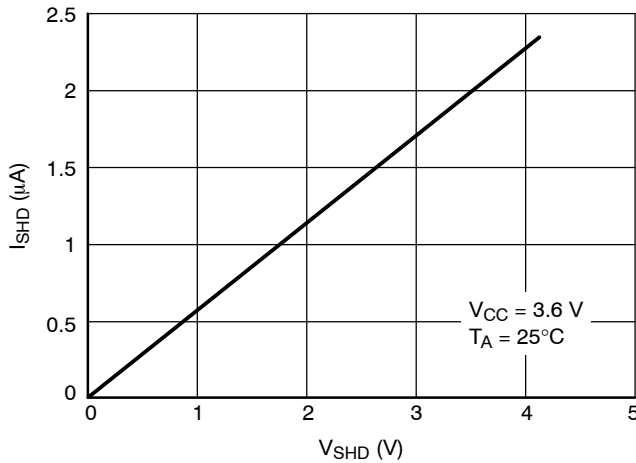


Figure 10. Input Current versus Voltage for the Shutdown Pin

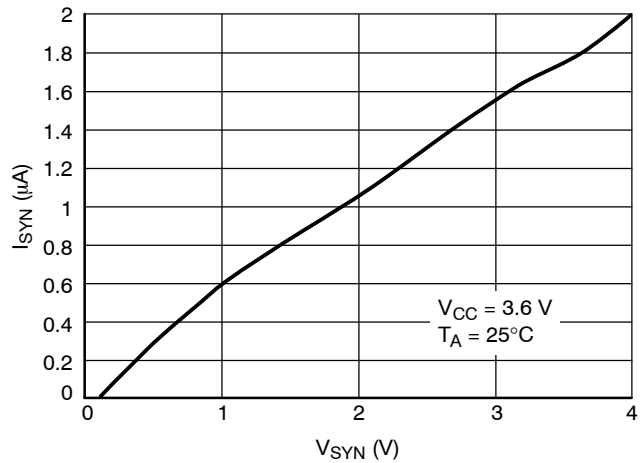


Figure 11. Input Current versus Voltage for the Synchronization Pin

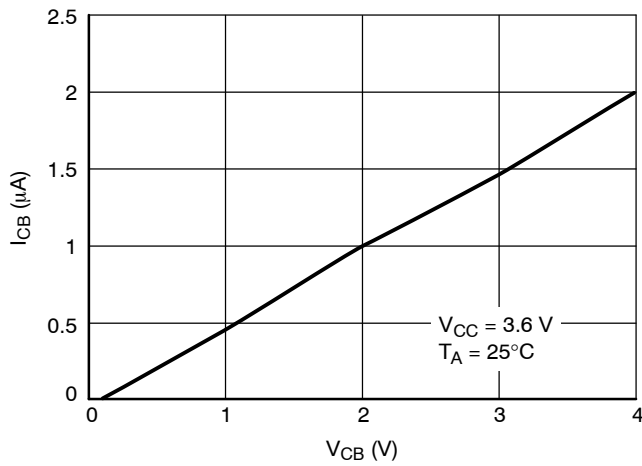


Figure 12. Input Current versus Voltage for the CB Pins

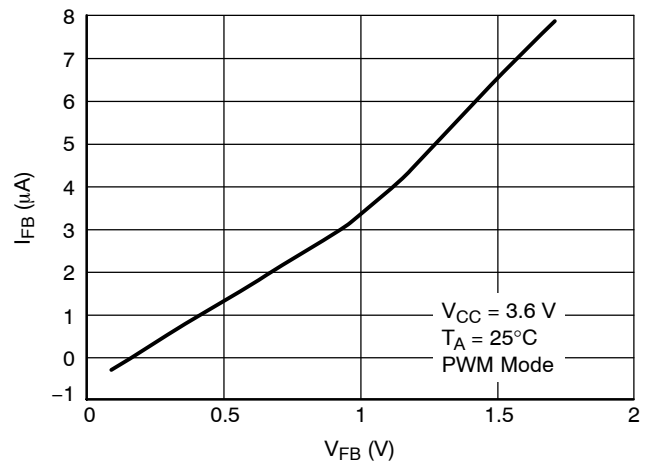


Figure 13. Input Current versus Voltage for the Feedback Pin

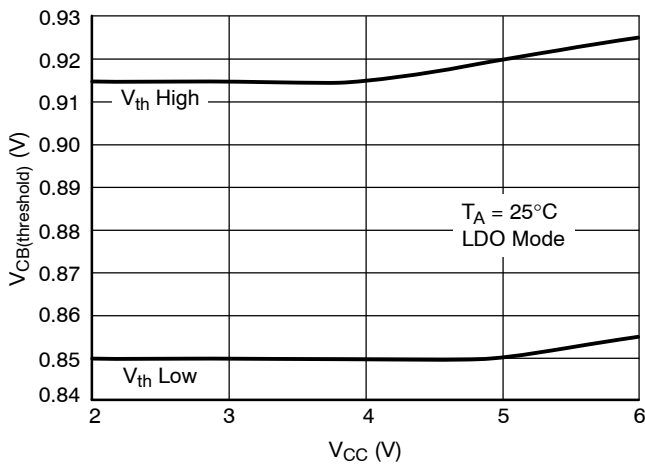


Figure 14. V_{CC} Input Voltage versus CB Threshold

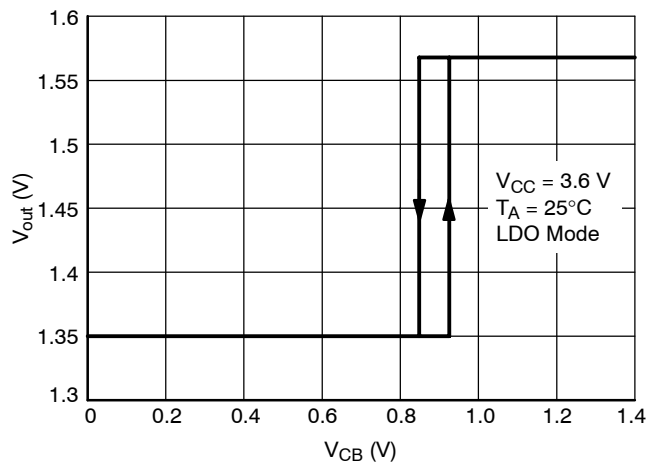


Figure 15. Transition Level of CB Pins

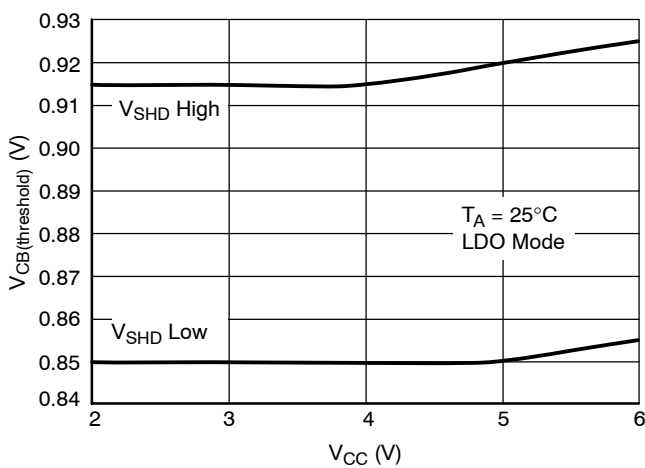


Figure 16. Input Voltage versus Shutdown Voltage

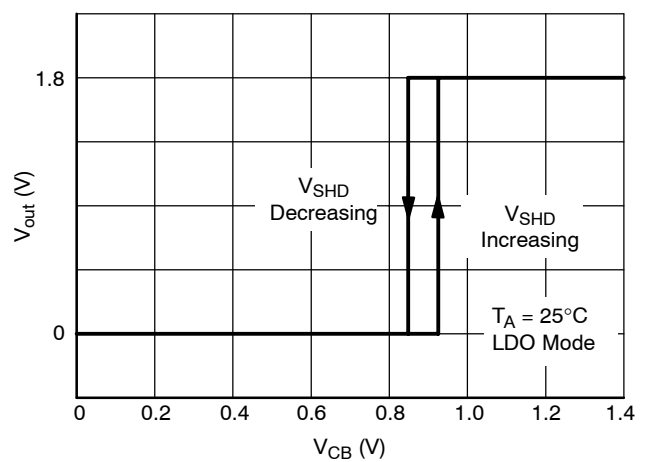


Figure 17. Output Voltage versus Shutdown Pin Voltage

NCP1501

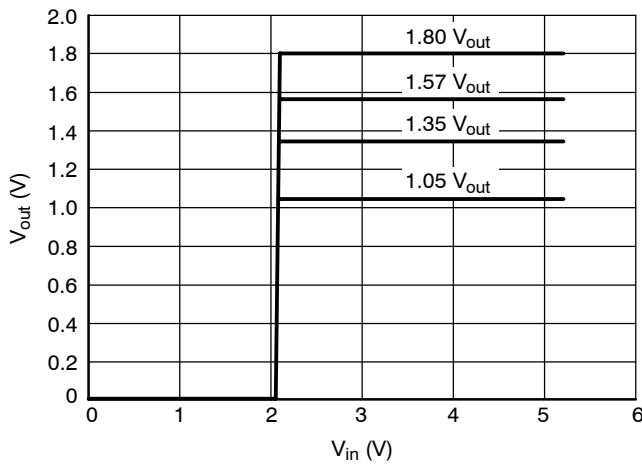


Figure 18. Output Voltage versus PWM Input Voltage

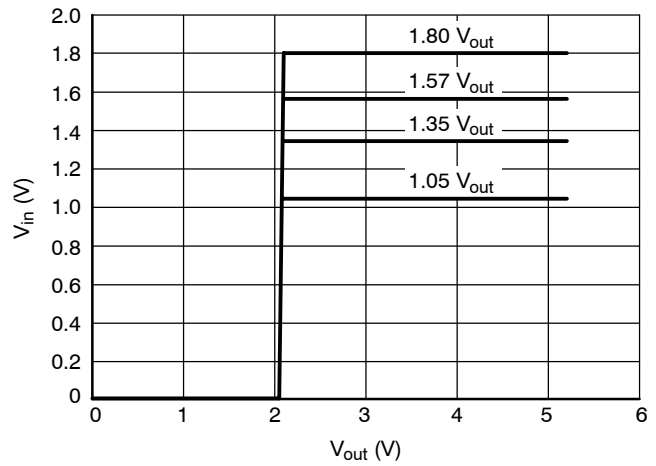


Figure 19. Input Voltage versus Output Voltage

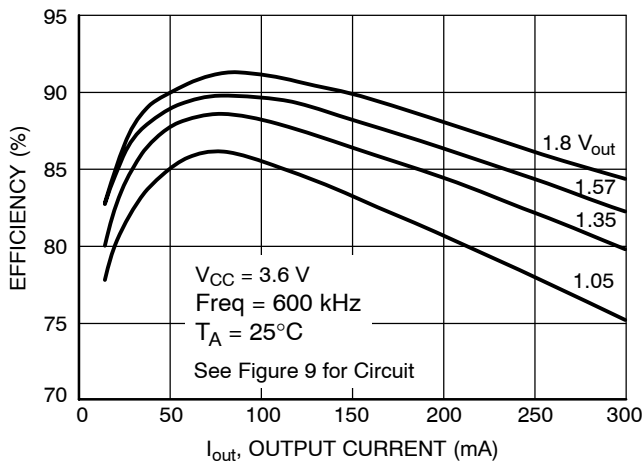


Figure 20. Efficiency versus Output Current

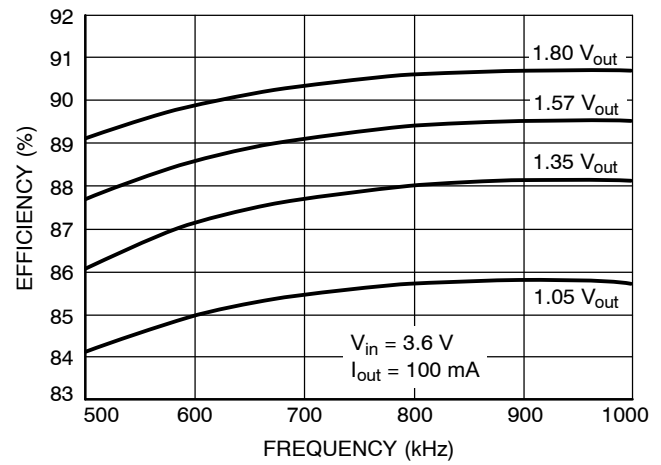


Figure 21. Efficiency versus Frequency

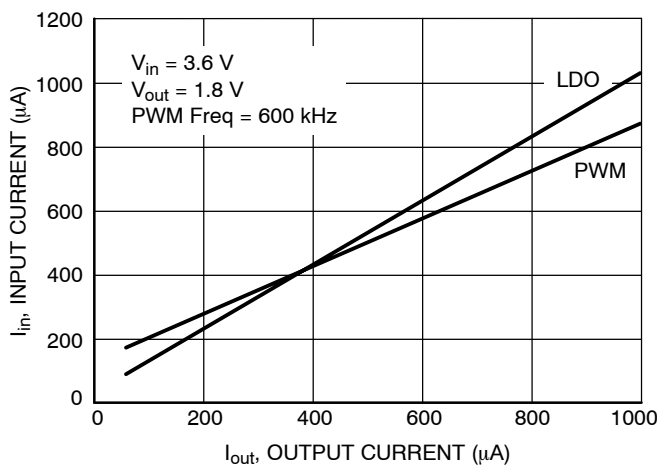


Figure 22. Input Current versus Output Current Comparison for PWM and LDO Mode

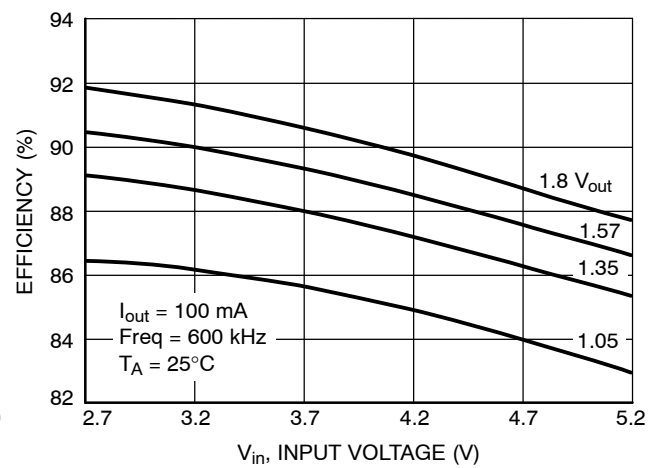


Figure 23. Efficiency versus Input Voltage

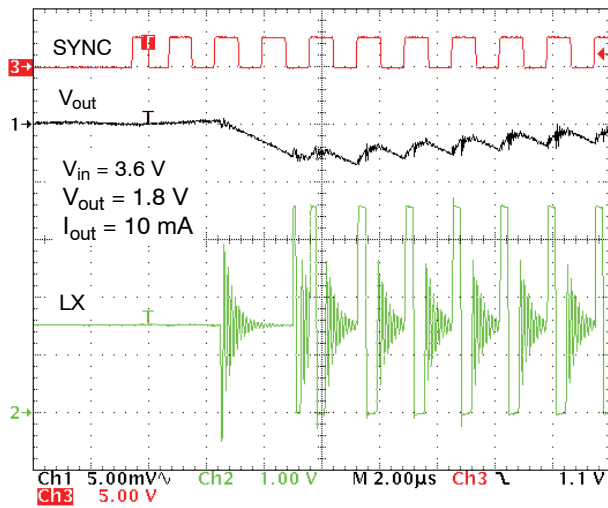


Figure 24. Transition from LDO to PWM Mode

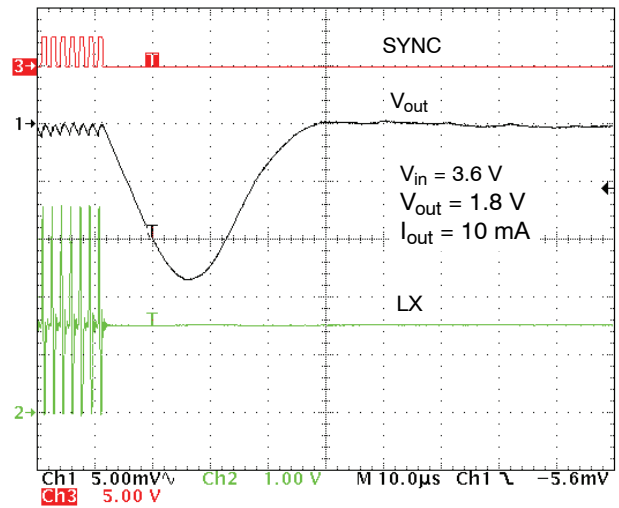


Figure 25. Transition from PWM to LDO Mode

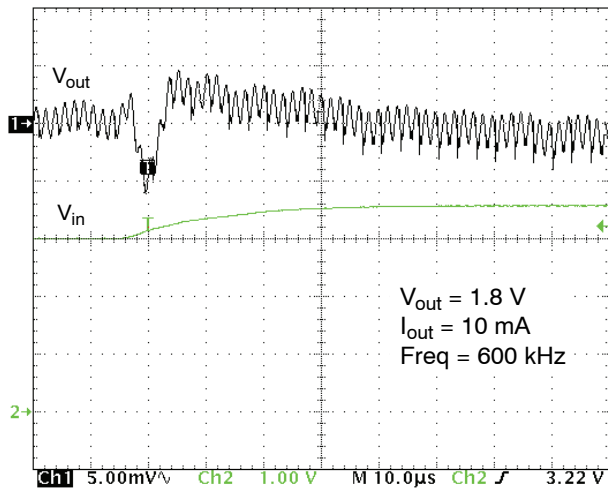


Figure 26. Line Transient from 3.0 to 3.6 V

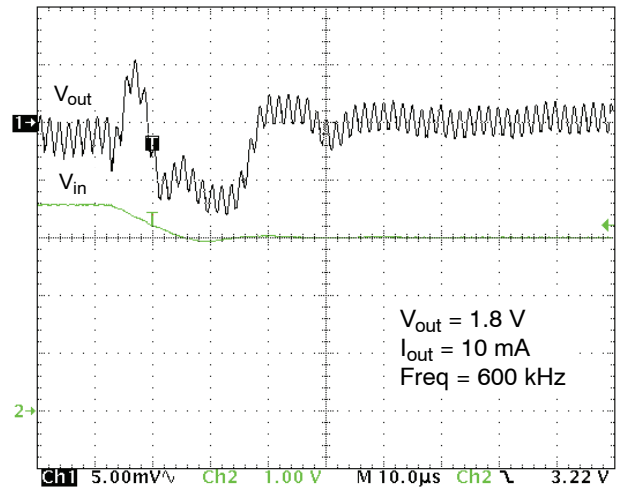


Figure 27. Line Transient from 3.6 to 3.0 V

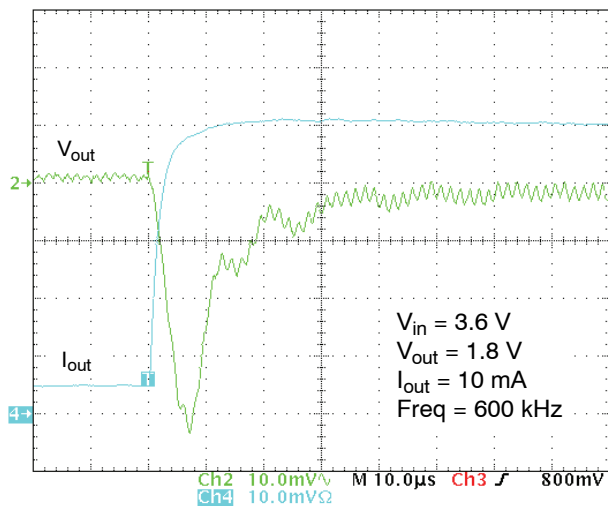


Figure 28. Load Transient from 10 to 100 mA

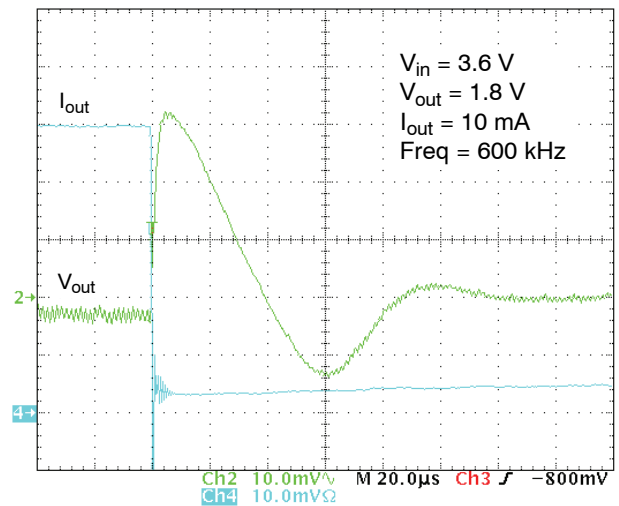


Figure 29. Load Transient from 100 to 10 mA

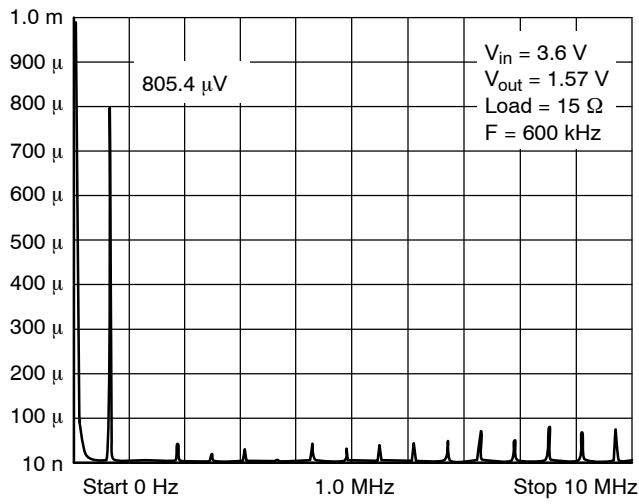


Figure 30. V_{rms} versus Frequency

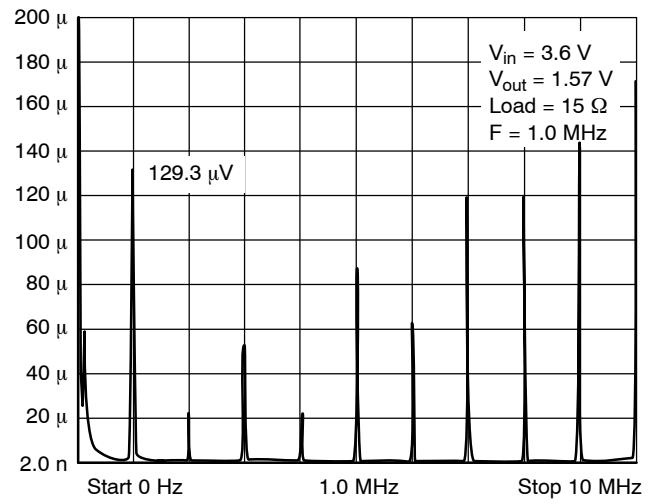


Figure 31. V_{rms} versus Frequency

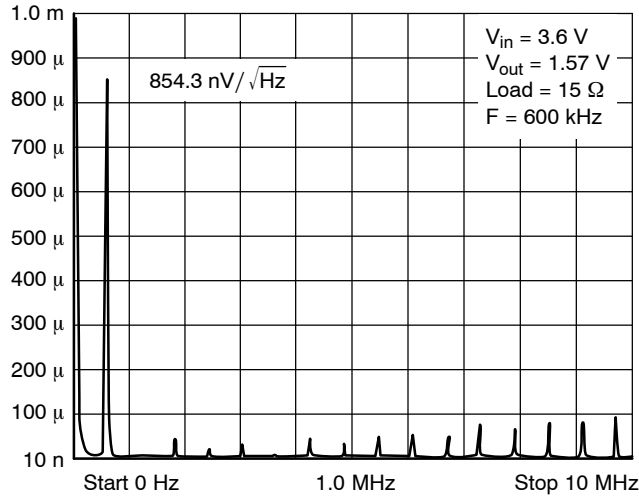


Figure 32. Noise versus Frequency

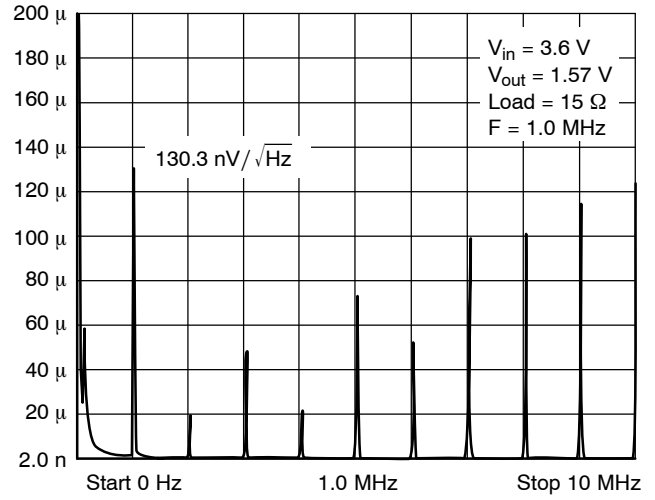


Figure 33. V_{RMS} versus Frequency

NCP1508

Up to 500 mA, 1 MHz, High Efficiency Synchronous Step-Down DC-DC Converter in DFN Package

The NCP1508 step-down PWM DC-DC converter is optimized for portable applications powered from 1-cell Li-ion or 3 cell Alkaline/NiCd/NiMH batteries. This DC-DC converter utilizes a current-mode control architecture for easy compensation and better line regulation. It also uses synchronous rectification to increase efficiency and reduce external part count. The NCP1508 optimizes efficiency in light load conditions when switched from a normal PWM mode to a "pulsed switching" mode. The device also has a built-in 1 MHz (nominal) oscillator for the PWM circuitry, or it can be synchronized to an external 500 kHz to 1000 kHz clock signal. Finally, it includes an integrated soft-start, cycle-by-cycle current limiting, and thermal shutdown protection. The NCP1508 is available in a space saving, low profile 3x3 mm 10 pin DFN package.

Features

- High Efficiency:
 - 93% for 1.89 V Output at 3.6 V Input and 125 mA Load Current
 - 91% for 1.89 V Output at 3.6 V Input and 300 mA Load Current
- Digital Programmable Output Voltages: 1.0, 1.3, 1.5 or 1.89 V
- Output Current up to 500 mA at $V_{in} = 3.6$ V
- Low Quiescent Current of 14 μ A in Pulsed Switching Mode
- Low 0.2 μ A Shutdown Current
- -30°C to 85°C Operation Temperature
- Low Profile DFN Package
- Pb-Free Package is Available

Application

- Cellular Phones, Smart Phones and PDAs
- Digital Still Cameras
- MP3 Players and Portable Audio Systems
- Wireless and DSL Modems
- Portable Equipment

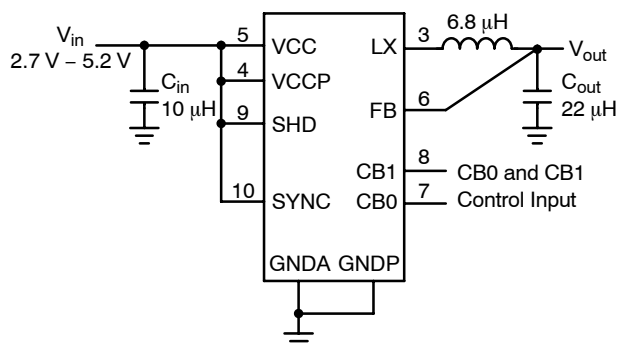


Figure 1. Typical Application Circuit



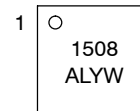
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM



10 PIN DFN
MN SUFFIX
CASE 485C



1508 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NCP1508MNR2	10 Pin DFN	3000 Tape & Reel
NCP1508MNR2G	10 Pin DFN (Pb-Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

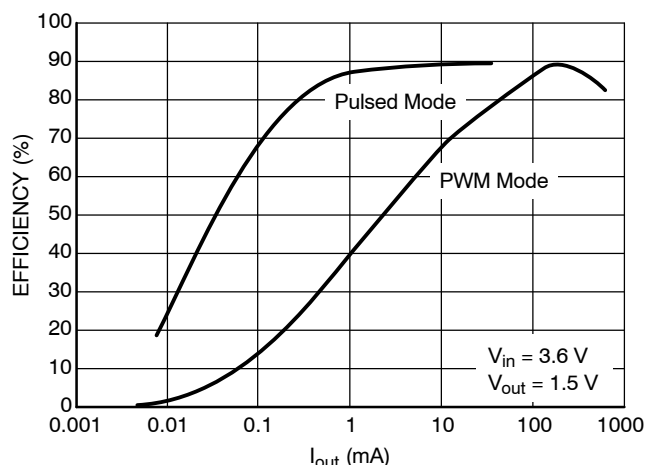


Figure 2. Efficiency vs. Output Current

NCP1508

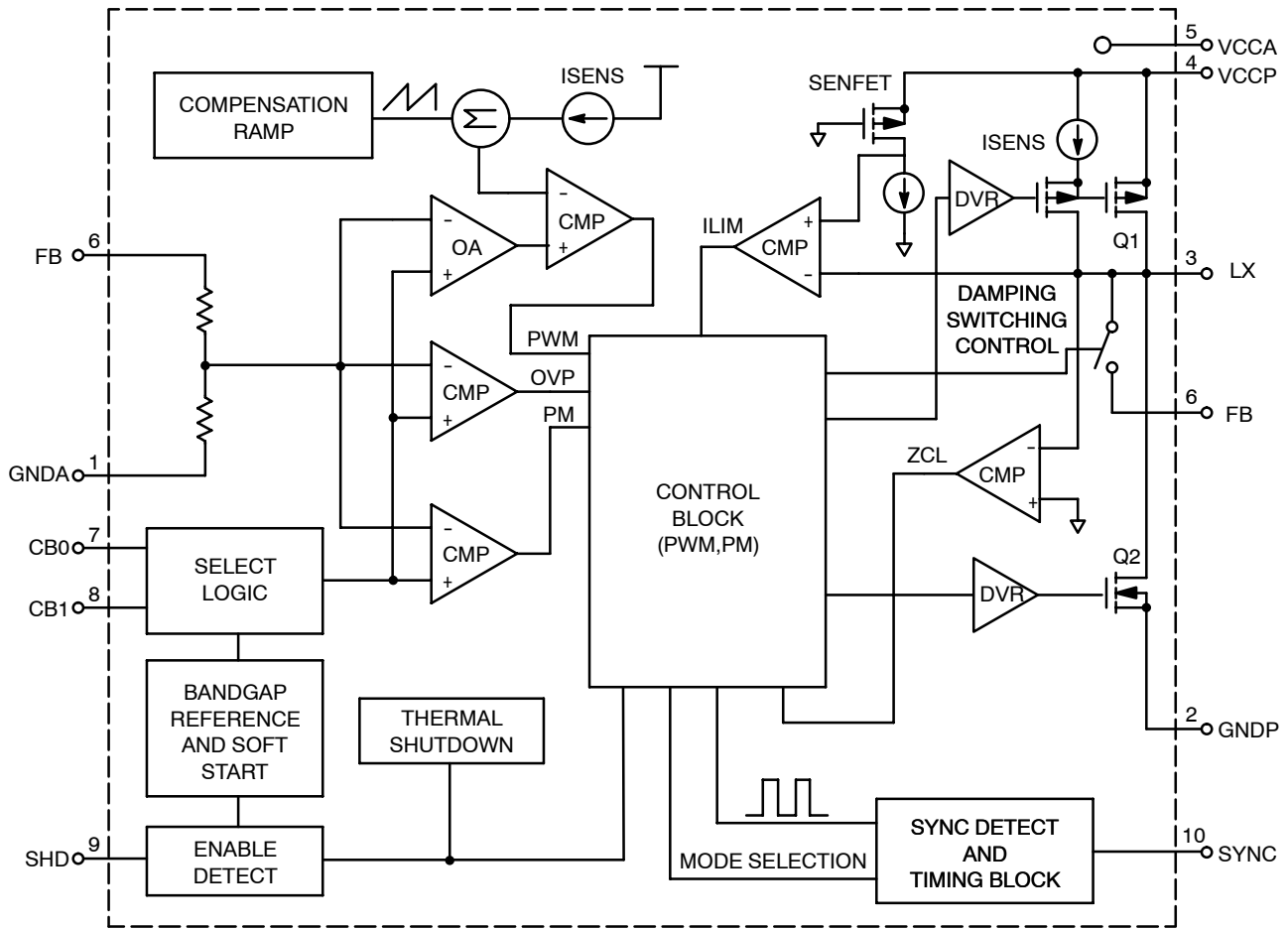


Figure 3. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Type	Description
1	GNDA	Analog Ground	Ground connection for the Analog Section of the IC. This is the GND for the FB, REF, SYNC, CB, and SHD pins.
2	GNDP	Power Ground	Ground Connection for the N-FET Power Stage.
3	LX	Analog Output	Connection from Power Pass Elements to the Inductor.
4	VCCP	Analog Input	Power Supply Input for the Switching P-FET.
5	VCC	Analog Input	Power Supply Input for Power and Analog V_{CC} .
6	FB	Analog Input	Feedback Voltage from the Output of the Power Supply.
7	CB0	Analog Input	Selects V_{out} . This pin contains an internal pulldown resistor.
8	CB1	Analog Input	Selects V_{out} . This pin contains an internal pullup resistor.
9	SHD	Analog Input	Enable for Switching Regulator. This pin is Active High to enable the NCP1508. The SHD Pin has an internal pulldown resistor to force the converter off if this pin is not connected to the external circuit.
10	SYNC	Analog Input	Synchronization input for the PWM converter. If a clock signal is present, the converter uses the rising edge for the turn on. If this pin is low, the converter is in the Pulsed mode. If this pin is high, the converter uses the internal oscillator for the PWM mode. This pin contains an internal pulldown resistor.

NCP1508

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Maximum Voltage All Pins	$V_{\max}$	5.5	V
Maximum Operating Voltage All Pins	$V_{\max}$	5.2	V
Thermal Resistance, Junction-to-Air	R_{JA}	68.5	°C/W
Operating Ambient Temperature Range	T_A	–30 to 85	°C
ESD Withstand Voltage	V_{ESD}	Human Body Model (Note 1) > 2500	V
		Machine Model (Note 1) > 150	
Moisture Sensitivity	MSL	Level 1	
Storage Temperature Range	T_{stg}	–55 to 150	°C
Junction Operating Temperature	T_J	–30 to 125	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- This device series contains ESD protection and exceeds the following tests:
 Human Body Model, 100 pF discharge through a 1.5 k Ω following specification JESD22/A114.
 Machine Model, 200 pF discharged through all pins following specification JESD22/A115.
 Latchup as per JESD78 Class II: > 100 mA.

NCP1508

ELECTRICAL CHARACTERISTICS ($V_{in} = 3.6\text{ V}$, $V_o = 1.5\text{ V}$, $T_A = 25^\circ\text{C}$, $F_{syn} = 600\text{ kHz}$ 50% Duty Cycle square wave for PWM mode; $T_A = -30\text{ to }85^\circ\text{C}$ for Min/Max values, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit

V_{CC} Pin

Quiescent Current of SYNC Mode, $I_{out} = 0\text{ mA}$	I _q PWM	–	175	–	μA
Quiescent Current of PWM Mode, $I_{out} = 0\text{ mA}$	I _q PWM	–	185	–	μA
Quiescent Current of Pulsed Mode, $I_{out} = 0\text{ mA}$	I _q Pulsed	–	14	–	μA
Quiescent Current, SHD Low	I _q Off	–	0.1	1.0	μA
Input Voltage Range	V _{in}	2.5	–	5.2	V

SYNC Pin

Input Voltage	V _{sync}	–0.3	–	V _{CC} + 0.3	V
Frequency Operational Range	F _{sync}	500	600	1000	kHz
Minimum Synchronization Pulse Width	D _{csync} Min	–	30	–	%
Maximum Synchronization Pulse Width	D _{csync} Max	–	70	–	%
SYNC “H” Voltage Threshold	V _{synch}	–	920	1200	mV
SYNC “L” Voltage Threshold	V _{syncl}	400	830	–	mV
SYNC “H” Input Current, V _{sync} = 3.6 V	I _{synch}	–	2.2	–	μA
SYNC “L” Input Current, V _{sync} = 0 V	I _{syncl}	–0.5	–	–	μA

Output Level Selection Pins

Input Voltage	V _{cb}	–0.3	–	V _{CC} + 0.3	V
CB0, CB1 “H” Voltage Threshold	V _{cb} h	–	920	1200	mV
CB0, CB1 “L” Voltage Threshold	V _{cb} l	400	830	–	mV
CB0 “H” Input Current, CB = 3.6 V	I _{cb0} h	–	2.2	–	μA
CB0 “L” Input Current, CB = 0 V	I _{cb0} l	–0.5	–	–	μA
CB1 “H” Input Current, CB = 3.6 V	I _{cb1} h	–	0.3	1.0	μA
CB1 “L” Input Current, CB = 0 V	I _{cb1} l	–	–2.2	–	μA

Shutdown Pin

Input Voltage	V _{shd}	–0.3	–	V _{CC} + 0.3	V
SHD “H” Voltage Threshold	V _{shd} h	–	920	1200	mV
SHD “L” Voltage Threshold	V _{shd} l	400	830	–	mV
SHD “H” Input Current, SHD = 3.6 V	I _{shd} h	–	2.2	–	μA
SHD “L” Input Current, SHD = 0 V	I _{shd} l	–0.5	–	–	μA

Feedback Pin

Input Voltage	V _{fb}	–0.3	–	V _{CC} + 0.3	V
Input Current, V _{fb} = 1.5 V	I _{fb}	–	5.0	7.5	μA

SYNC PWM Mode Characteristics

Switching P–FET Current Limit	I _{lim}	–	800	–	mA
Duty Cycle (Note 2)	DC	–	–	100	%
Minimum On Time	T _{on(min)}	–	75	–	nsec
R _{DS(on)} Switching P–FET and N–FET	R _{DS(on)}	–	0.23	–	Ω
Switching P–FET and N–FET Leakage Current	I _{leak}	–	0	10	μA
Output Overvoltage Threshold	V _o	–	5.0	–	%

NCP1508

ELECTRICAL CHARACTERISTICS (continued) ($V_{in} = 3.6\text{ V}$, $V_o = 1.5\text{ V}$, $T_A = 25^\circ\text{C}$, $F_{syn} = 600\text{ kHz}$ 50% Duty Cycle square wave for PWM mode; $T_A = -30$ to 85°C for Min/Max values, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit

SYNC PWM Mode Characteristics (continued)

Feedback Voltage Accuracy, V_{out} Set = 1.0 V, $CB0 = L$, $CB1 = L$, $I_{out} = 300\text{ mA}$	V_{out}	0.950	1.000	1.050	V
Feedback Voltage Accuracy, V_{out} Set = 1.3 V, $CB0 = L$, $CB1 = H$, $I_{out} = 300\text{ mA}$	V_{out}	1.261	1.300	1.339	V
Feedback Voltage Accuracy, V_{out} Set = 1.5 V, $CB0 = H$, $CB1 = H$, $I_{out} = 300\text{ mA}$	V_{out}	1.450	1.500	1.550	V
Feedback Voltage Accuracy, V_{out} Set = 1.89 V, $CB0 = H$, $CB1 = L$, $I_{out} = 300\text{ mA}$	V_{out}	1.833	1.890	1.947	V
Line Regulation, $V_{in} = 2.7\text{ V}$ – 3.6 V , $I_{out} = 100\text{ mA}$	–	–15	–	+15	mV
Line Regulation, $V_{in} = 3.6\text{ V}$ – 5.2 V , $I_{out} = 100\text{ mA}$	–	–15	–	+15	mV
Load Regulation, $I_{out} = 100\text{ mA}$ – 300 mA	–	–15	–	+15	mV
Load Transient Response, 10 to 100 mA Load Step	V_{out}	–	50	–	mV
Line Transient Response, $I_{out} = 100\text{ mA}$, 3.0 to 3.6 V_{in} Line Step	V_{out}	–	± 5.0	–	mVpp

PWM Mode with Internal Oscillator Characteristics

Switching P–FET Current Limit	I_{lim}	–	800	–	mA
Duty Cycle (Note 2)	DC	–	–	100	%
Minimum On Time	$T_{on(min)}$	–	75	–	nsec
Internal Oscillator Frequency $-T_A = 25^\circ\text{C}$ $-30^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	F_{osc}	760 700	980 980	1240 1240	kHz
$R_{DS(on)}$ Switching P–FET and N_FET	$R_{DS(on)}$	–	0.23	–	Ω
Switching P–FET and N–FET Leakage Current	I_{leak}	–	0	10	μA
Output Overvoltage Threshold	V_o	–	5.0	–	%
Feedback Voltage Accuracy, V_{out} Set = 1.0 V, $CB0 = L$, $CB1 = L$, $I_{out} = 300\text{ mA}$	V_{out}	0.950	1.000	1.050	V
Feedback Voltage Accuracy, V_{out} Set = 1.3 V, $CB0 = L$, $CB1 = H$, $I_{out} = 300\text{ mA}$	V_{out}	1.261	1.300	1.339	V
Feedback Voltage Accuracy, V_{out} Set = 1.5 V, $CB0 = H$, $CB1 = H$, $I_{out} = 300\text{ mA}$	V_{out}	1.450	1.500	1.550	V
Feedback Voltage Accuracy, V_{out} Set = 1.89 V, $CB0 = H$, $CB1 = L$, $I_{out} = 300\text{ mA}$	V_{out}	1.833	1.890	1.947	V
Line Regulation, $V_{in} = 2.7\text{ V}$ – 3.6 V , $I_{out} = 100\text{ mA}$	–	–15	–	+15	mV
Line Regulation, $V_{in} = 3.6\text{ V}$ – 5.2 V , $I_{out} = 100\text{ mA}$	–	–15	–	+15	mV
Load Regulation, $I_{out} = 100\text{ mA}$ – 300 mA	–	–15	–	+15	mV
Load Transient Response, 10 to 100 mA Load Step	V_{out}	–	50	–	mV
Line Transient Response, $I_{out} = 100\text{ mA}$, 3.0 to 3.6 V_{in} Line Step	V_{out}	–	± 5.0	–	mVpp

Pulsed Mode Characteristics

Peak Current Limit	I_{lim}	–	200	–	mA
Output Current	I_{out}	0.05	–	30	mA
Output Ripple Voltage, $I_{out} = 100\text{ }\mu\text{A}$	V_{out}	–	22	100	mV
Feedback Voltage Accuracy, V_{out} Set = 1.0 V, $CB0 = L$, $CB1 = L$	V_{out}	0.950	1.000	1.050	V
Feedback Voltage Accuracy, V_{out} Set = 1.3 V, $CB0 = L$, $CB1 = H$	V_{out}	1.261	1.300	1.339	V
Feedback Voltage Accuracy, V_{out} Set = 1.5 V, $CB0 = H$, $CB1 = H$	V_{out}	1.450	1.500	1.550	V
Feedback Voltage Accuracy, V_{out} Set = 1.89 V, $CB0 = H$, $CB1 = L$	V_{out}	1.833	1.890	1.947	V

2. Maximum value is guaranteed by design.

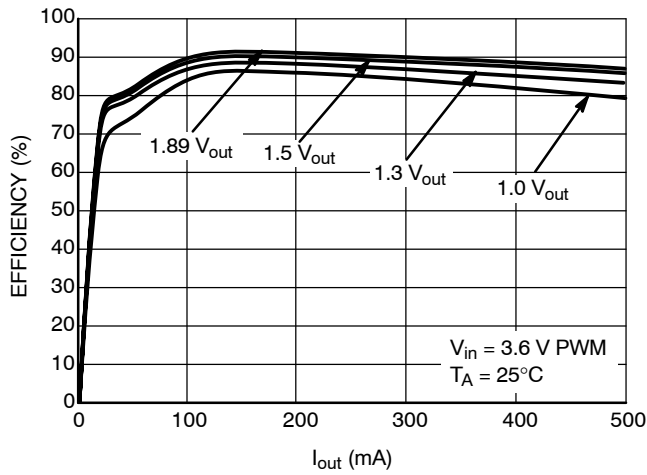


Figure 4. Efficiency vs. Output Current in PWM Mode

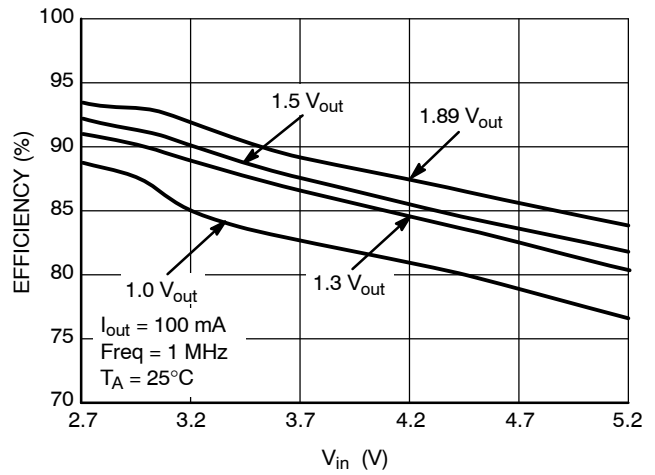


Figure 5. Efficiency vs. Input Voltage in PWM Mode

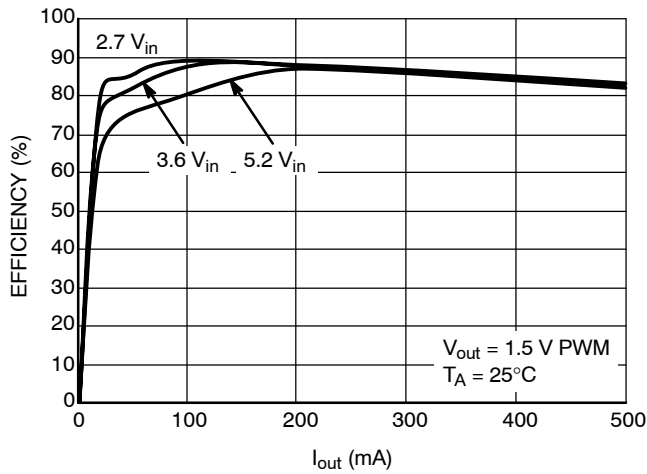


Figure 6. Efficiency vs. Output Current at Different Input Voltage

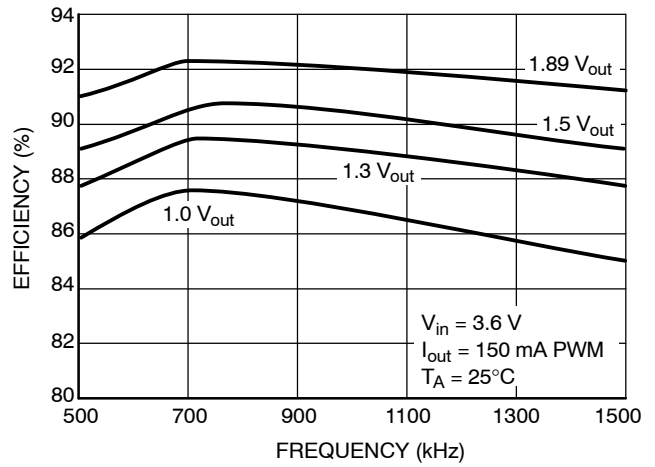


Figure 7. Efficiency vs. Frequency

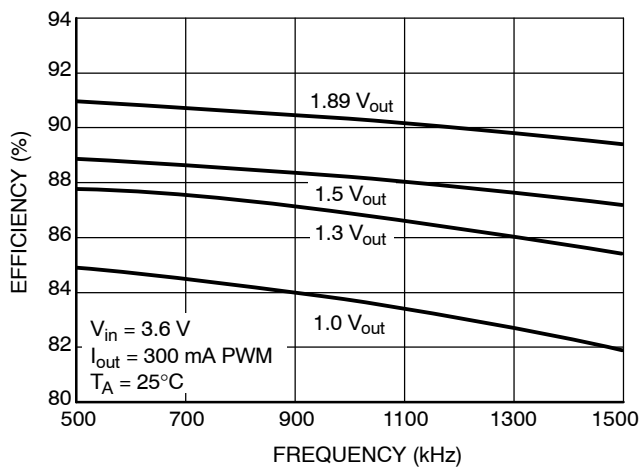


Figure 8. Efficiency vs. Frequency

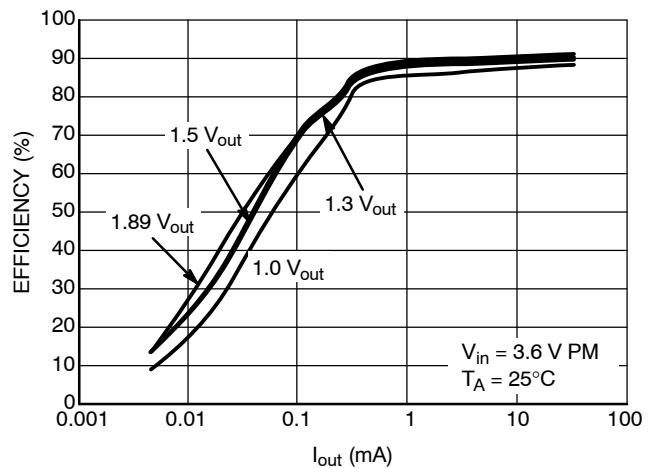


Figure 9. Efficiency vs. Output Current in Pulsed Mode

NCP1508

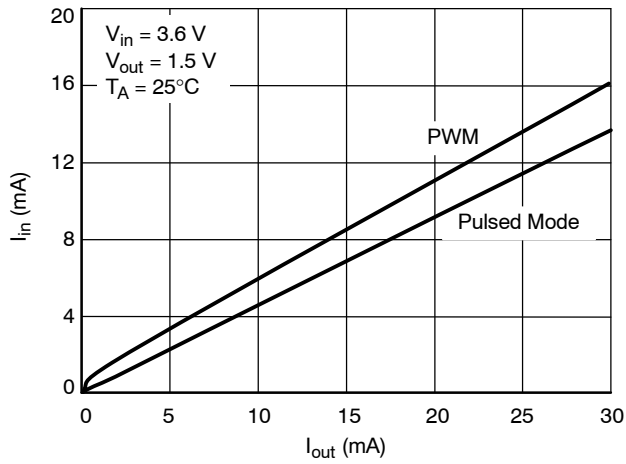


Figure 10. Input Current Comparison

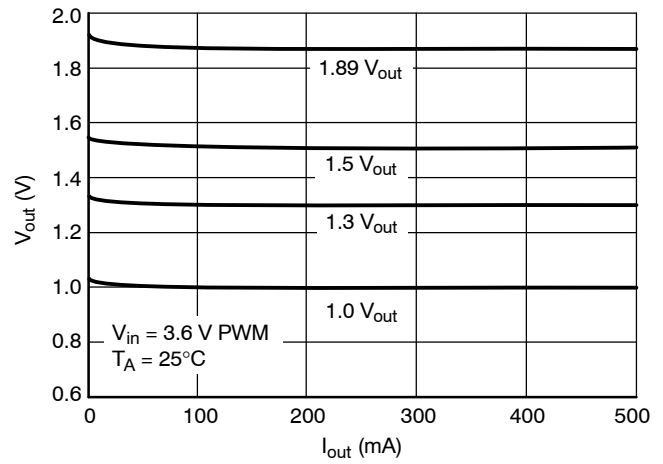


Figure 11. Output Voltage vs. Output Current

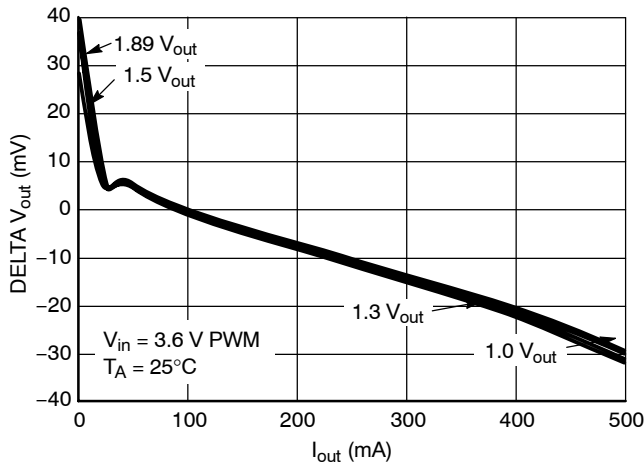


Figure 12. Load Regulation in PWM Mode

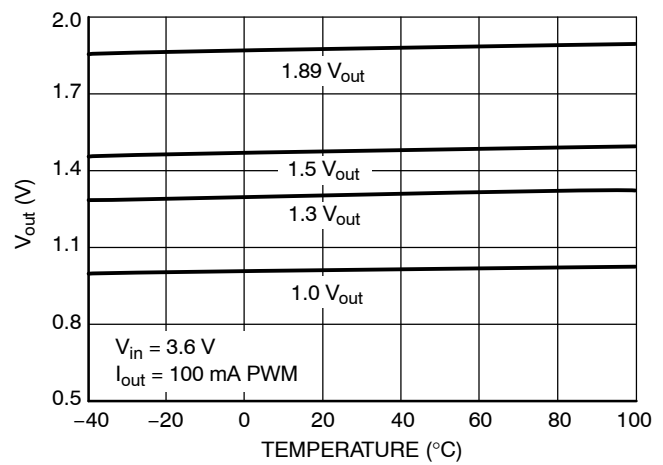


Figure 13. Output Voltage vs. Temperature

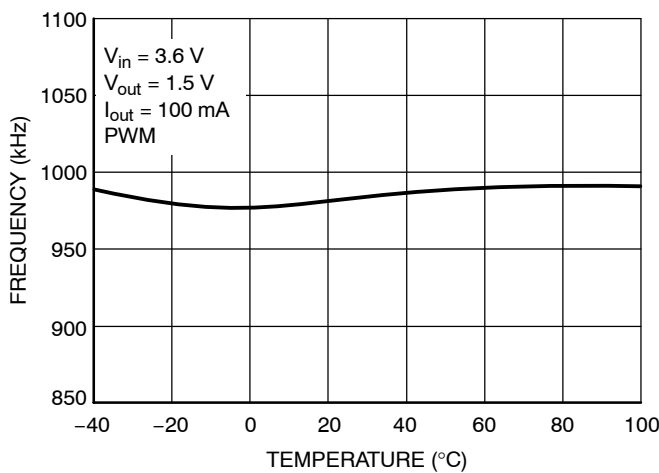


Figure 14. Oscillator Frequency vs. Temperature

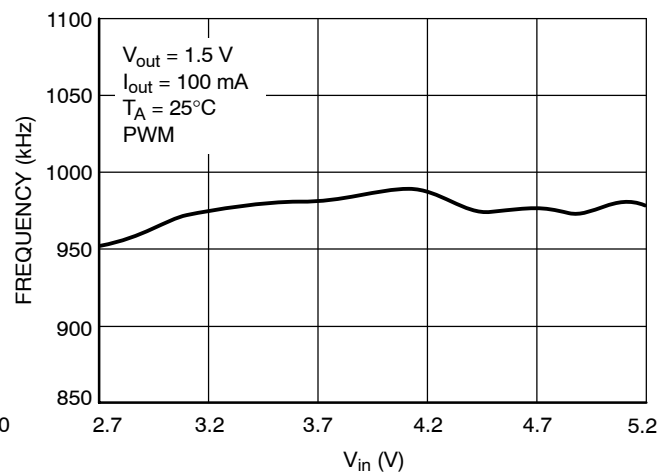


Figure 15. Oscillator Frequency vs. Input Voltage

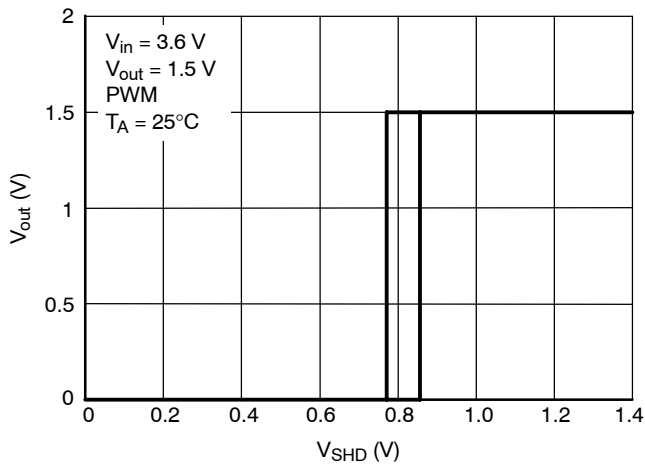


Figure 16. Output Voltage vs. Shutdown Pin Voltage

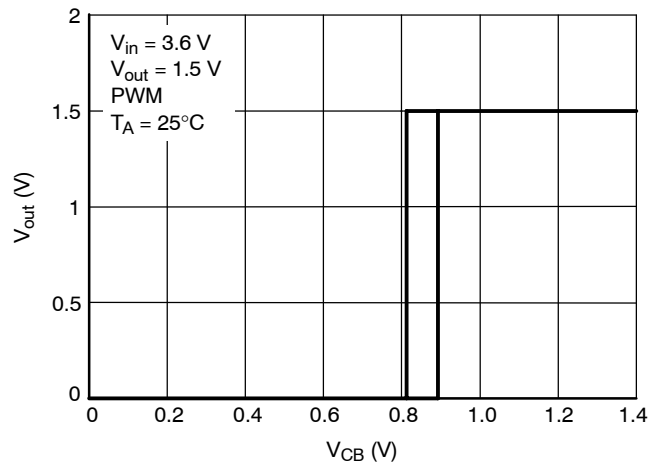


Figure 17. Transition Level of CB Pins

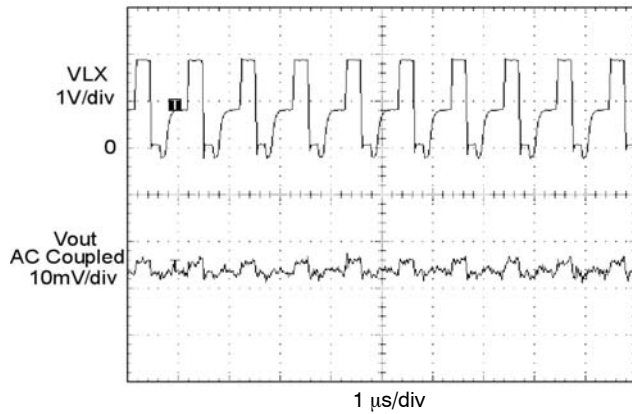


Figure 18. Light-Load PWM Switching Waveform ($V_{in} = 3.6$ V, $V_{out} = 1.5$ V, $I_{out} = 30$ mA)

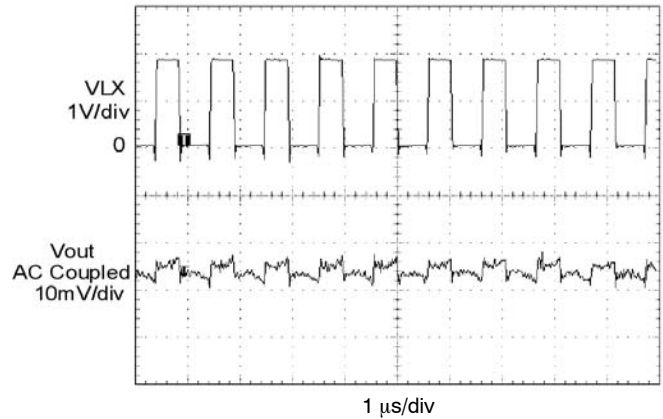


Figure 19. Heavy-Load PWM Switching Waveform ($V_{in} = 3.6$ V, $V_{out} = 1.5$ V, $I_{out} = 300$ mA)

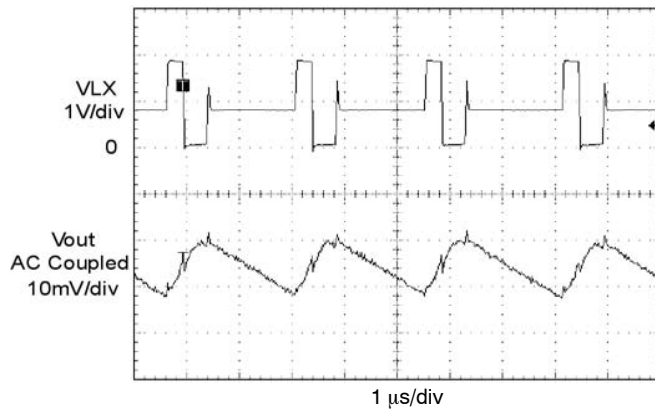


Figure 20. Pulsed Mode Switching Waveform ($V_{in} = 3.6$ V, $V_{out} = 1.5$ V, $I_{out} = 30$ mA)

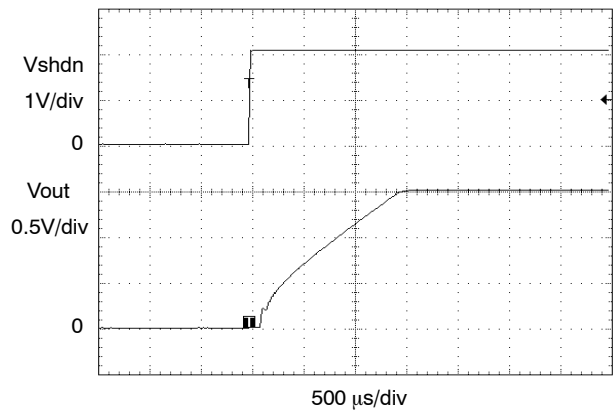


Figure 21. Soft-Start ($V_{in} = 3.6$ V, $V_{out} = 1.5$ V, $I_{out} = 150$ mA)

NCP1508

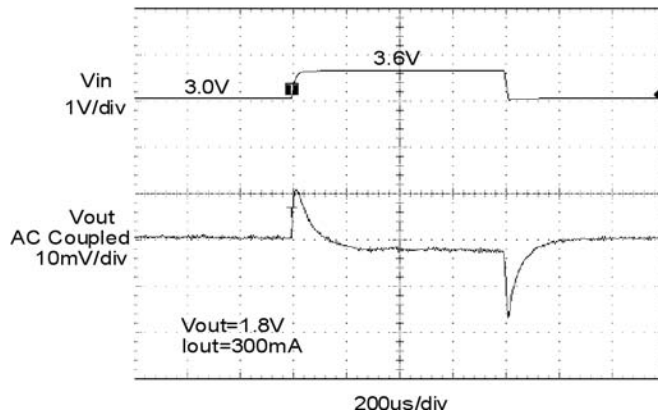


Figure 22. Line Transient Response

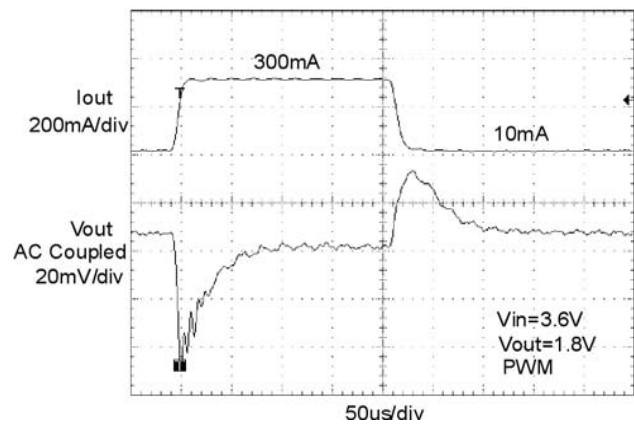


Figure 23. Load Transient Response

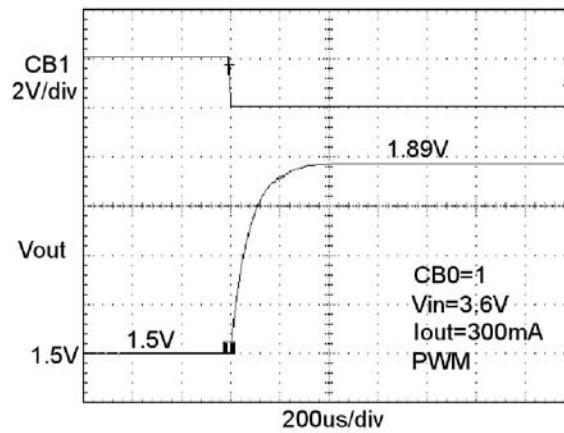


Figure 24. Output Voltage Transition from 1.57 V to 1.8 V

DETAILED OPERATING DESCRIPTION

Overview

The NCP1508 is a monolithic micro-power high frequency PWM step-down DC-DC converter specifically optimized for applications requiring high efficiency and a small PCB footprint such as portable battery powered products. It integrates synchronous rectification to improve efficiency as well as eliminate the external Schottky diode. High switching frequency allows for a low profile inductor and capacitors to be used. Four digital selectable output voltages (1.0, 1.3, 1.5 and 1.89 V) can be generated from the input supply that can range from 2.7–5.2 V. All loop compensation is integrated as well further reducing the external component count as well.

The DC-DC converter has two operating modes (normal PWM, pulsed switching), which are intended to allow for optimum efficiency under either light (up to 30 mA) or heavy loads. The user determines the operating mode by controlling the SYNC input. In addition the SYNC input can be used to synchronize the PWM to an external system clock signal in the range of 500–1000 kHz.

PWM Operating Mode

The NCP1508 can be set to current mode PWM operation by connecting SYNC pin to V_{CC} . In this mode, the output voltage is regulated by modulating on-time pulse width of the main switch Q1 at a fixed frequency of 1 MHz. The switching of the PMOS Q1 is controlled by a flip-flop driven by the internal oscillator and a comparator that compares the error signal from an error amplifier with the sum of the sensed current signal and compensation ramp. At the beginning of each cycle, the main switch Q1 is turned ON by the rising edge of the internal oscillation clock. The inductor current ramps up until the sum of the current sense signal and compensation ramp becomes higher than the error voltage amplifier. Once this has occurred, the PWM comparator resets the flip-flop, Q1 is turned OFF and the synchronous switch Q2 is turned ON. Q2 replaces the external Schottky diode to reduce the conduction loss and improve the efficiency. To avoid overall power loss, a certain amount of dead time is introduced to ensure Q1 is completely turned OFF before Q2 is being turned ON.

In continuous conduction mode (CCM), Q1 is turned ON after Q2 is completely turned OFF to start a new clock cycle. In discontinuous conduction mode (DCM), the zero crossing comparator (ZLC) will turn off Q2 when the inductor current drops to zero.

Overvoltage Protection

The overvoltage protection circuit is present in PWM mode to prevent the output voltage from going too high under light load or fast load transient conditions. The output overvoltage threshold is 5% above nominal set

value. If the output voltage rises above 5% of the nominal value, the OVP comparator is activated and switch Q1 is turned OFF. Switching will continue when the output voltage falls below the threshold of OVP comparator.

Pulsed Mode (PM)

Under light load conditions (< 30 mA), NCP1508 can be configured to enter a low current pulsed mode operation to reduce power consumption. This is accomplished by SYNC pin held LOW. The output regulation is implemented by pulse frequency modulation. If the output voltage drops below the threshold of PM comparator (typically $V_{nom}-2\%$), a new cycle will be initiated by the PM comparator to turn on the switch Q1. Q1 remains ON until 200 mA inductor peak current is reached. Then ILIM comparator goes high to switch off Q1. After a short dead time delay, switch rectifier Q2 is turn ON. The zero crossing comparator will detect when the inductor current drops to zero and send the signal to turn off Q2. The output voltage continues to decrease through discharging the output capacitor. When the output voltage falls below the threshold of PM comparator again, a new cycle starts immediately.

Cycle-by-Cycle Current Limit

From the block diagram (Figure 3), an ILIM comparator is used to realize cycle-by-cycle current limit protection. The comparator compares the LX pin voltages with the reference voltage from the SENFET, which is biased by constant current. If the inductor current reaches the limit, ILIM comparator detects the LX voltage falling below the reference voltage from SENFET and releases the signal to turn off the switch Q1. The cycle-by-cycle current limit is set at 800 mA in PWM and 200 mA in PM.

Frequency Synchronization and Operating Mode Selection

The SYNC pin can also be used for frequency synchronization by connecting it with an external clock signal. It operates in PWM mode when synchronized to an external clock. The switching cycle initiates by the rising edge of the clock. The synchronization clock signals between 0.4 V and 1.2 V from 500 kHz to 1000 kHz.

Gating on and off the clock, the SYNC pin can also be used to select between PM and PWM modes. It allows efficient dynamical power management by adjusting the converter operation to the specific system requirement. Set SYNC pin low to select PM mode at light load conditions (up to 30 mA) and set SYNC pin high or connect with external clock to select PWM mode at heavy load condition to achieve optimum efficiency. Table 1 shows the mode selection with three different SYNC pin states.

Table 1. Operating Mode Selection

SYNC Pin State	Operating Mode
LOW	Pulsed Mode (PM)
HIGH	PWM, 1 MHz Switch Frequency
CLOCK	PWM, Frequency Synchronization

Output Voltage Selection

The output voltage is digitally programmed to one of four voltage levels depending on the logic state of CB0 and CB1. Therefore if the NCP1508's load, such as a digital cellular phone's baseband processor, supports dynamic power management, the device can lower or raise its core voltage under software control. When combined with the pulsed current mode function in low load situations, this active voltage management further stretches the useful operating life of the handset between charges. Figure 24 shows a typical transition between 1.5 to 1.89 volts.

The output voltage levels are listed in Table 2. The CB0 has a pull down resistor and the CB1 has a pullup resistor. The default output voltage is 1.3 V when CB0 and CB1 are floating.

Table 2. Truth Table for CB0 and CB1 with the corresponding output voltage

CB0	CB1	Vout(V)
0	0	1.0
0	1	1.3
1	1	1.5
1	0	1.89

Soft-Start

The NCP1508 uses soft-start to limit the inrush current when the device is initially powered up or enabled. Soft-start is implemented by gradually increasing the reference voltage until it reaches the full reference voltage. During startup, a pulsed current source charges the internal soft-start capacitor to provide gradually increasing reference voltage for the PWM loop. When the voltage across the capacitor ramps up to the nominal reference voltage, the pulsed current source will be switched off and the reference voltage will switch to the regular reference voltage. From Figure 21, it shows the soft-start time is about 1.5 ms.

Shutdown Mode

When the SHD pin has a voltage applied of less than 0.4 V, the NCP1508 will be disabled. In shutdown mode, the internal reference, oscillator and most of the control circuitries are turned off. Therefore, the typical current consumption will be 0.1 μ A (typical value).

Applying a voltage above 1.2 V to SHD pin will enable the device for normal operation. The device will go through soft-start to normal operation.

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. If the junction temperature exceeds 160°C, the device shuts down. In this mode switch Q1 and Q2 and the control circuits are all turned off. The device restarts in soft-start after the temperature drops below 135°C. This feature is provided to prevent catastrophic failures from accidental device overheating and it is not intended as a substitute for proper heatsinking.

APPLICATIONS INFORMATION

Component Selection

Input Capacitor Selection

In PWM operating mode, the input current is pulsating with large switching noise. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly. The capacitance needed for the input bypass capacitor depends on the source impedance of the input supply. The RMS capacitor current is calculated as:

$$I_{RMS} \approx I_O \sqrt{D \cdot D'} \quad (\text{eq. 1})$$

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is $I_{O,max}/2$.

For NCP1508, a low profile ceramic capacitor of 10 μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to the V_{CC} Pin.

Inductor Value Selection

Selecting the proper inductor value is based on the desired ripple current. The relationship between the inductance and the inductor ripple current is given by the equation in below.

$$\Delta i_L = \frac{V_{out}}{L f_s} \left(1 - \frac{V_{out}}{V_{in}} \right) \quad (\text{eq. 2})$$

Large value inductors will have small ripple current and low value inductor will have high ripple current. For NCP1508, the compensation is internally fixed and a fixed 6.8 μH inductor is needed for most of the applications.

Output Capacitor Selection

Selecting the proper output capacitor is based on the desired output ripple voltage. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output ripple voltage is given by:

$$\Delta V_C = \Delta i_L \cdot \left(\text{ESR} + \frac{1}{4 f_s C_{out}} \right) \quad (\text{eq. 3})$$

The RMS output capacitor current is given by:

$$I_{RMS}(C_{out}) = \frac{V_O \cdot (1 - D)}{2 \sqrt{3} \cdot L \cdot f_s} \quad (\text{eq. 4})$$

Where f_s is the switching frequency and ESR is the effective series resistance of the output capacitor. A low ESR, 22 μF ceramic capacitor is recommended for NCP1508 in most of applications. For example, with TDK C2012X5R0J226 output capacitor, the output ripple is less than 10 mV at 300 mA.

Design Example

As a design example, assume that the NCP1508 is used in a single lithium-ion battery application. The input voltage, V_{in} , is 3.0 V to 4.2 V. Output condition is V_{out} at 1.5 V with a typical load current of 120 mA and a maximum of 300 mA. For NCP1508, the inductor has a predetermined

value, 6.8 μH . The inductor ESR will factor into the overall efficiency of the converter. The inductor needs to be selected by the required peak current.

Equation 5 is the basic equation for an inductor and describes the voltage across the inductor. The inductance value determines the slope of the current of the inductor.

$$\frac{V_L}{L} = \frac{di_L}{dt} \quad (\text{eq. 5})$$

Equation 5 is rearranged to solve for the change in current for the on-time of the converter in Continuous Conduction Mode.

$$\begin{aligned} i_{L,pk-pk} &= \frac{(V_{in} - V_{out})}{L} \cdot DT_s \\ &= \frac{(V_{in} - V_{out})}{L} \cdot \frac{V_{in}}{V_{out}} \cdot \frac{1}{f_s} \end{aligned} \quad (\text{eq. 6})$$

$$i_{L,max} = I_{O,max} + \frac{\Delta i_{L,pk-pk}}{2}$$

Utilizing Equations 6, the peak-to-peak inductor current is calculated using the following worst-case conditions.

$$V_{in,max} = 4.2 \text{ V}, V_{out} = 1.5 \text{ V}, f_s = 1 \text{ MHz} - 20\%,$$

$$L = 6.8 \mu\text{H} - 10\%, i_{L,pk-pk} = 197 \text{ mA}, i_{L,max} = 399 \text{ mA}$$

Therefore, the inductor must have a maximum current exceeding 405 mA.

Since the compensation is fixed internally in the IC, the input and output capacitors as well as the inductor have a predetermined value too: $C_{in} = 10 \mu\text{F}$ and $C_{out} = 22 \mu\text{F}$. Low ESR capacitors are needed for best performance. Therefore, ceramic capacitors are recommended. Please see Table 3 for recommended inductors and capacitors.

PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise and unwanted feedbacks that can affect the performance of the converter. Hints suggested below can be used as a guideline in most situations.

1. Use star-ground connection to connect the IC ground nodes and capacitor GND nodes together at one point. Keep them as close as possible. And then connect this to the ground plane (if it is used) through several vias. This will reduce noise in ground plane by preventing the switching currents from flowing through the ground plane.

2. Place the power components (i.e., input capacitor, inductor and output capacitor) as close together as possible for best performance. All connecting traces must be short, direct, and thick to reduce voltage errors caused by resistive losses across these traces.

3. Separate the feedback path of the output voltage from the power path. Keep this path close to the NCP1508 circuit. And also route it away from noisy components.

NCP1508

This will prevent noise from coupling into voltage feedback trace.

4. Place the DC-DC converter away from noise sensitive circuitry, such as RF circuits. Interference with noise

sensitive circuitry in the DC-DC converter can be reduced by distance between them.

The following shows NCP1508 demo board layout and suggested bill of materials.

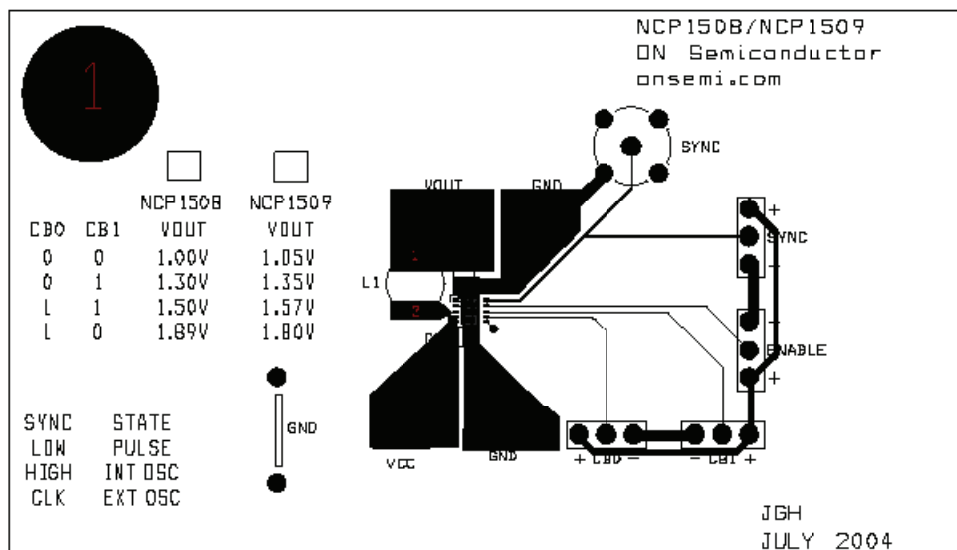


Figure 25. Top and Silkscreen Layer

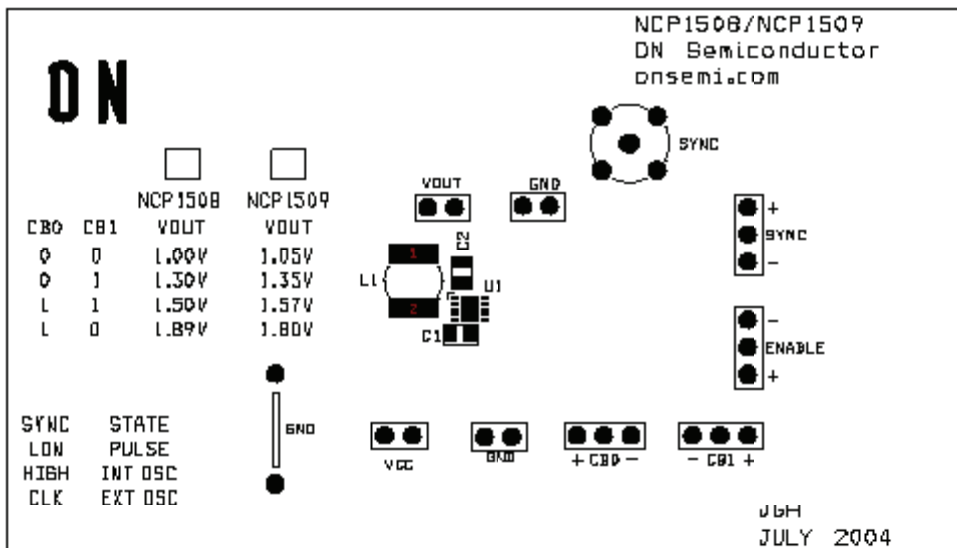


Figure 26. Soldermask Top and Silkscreen Layer

NCP1508

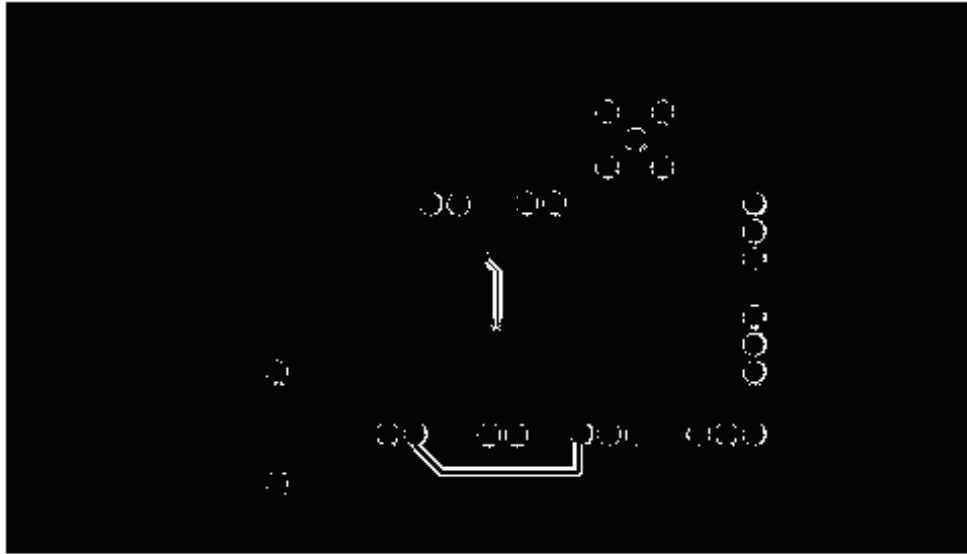


Figure 27. Bottom Layer

Table 3. Bill of Materials

Component	Value	Manufacturer	Part Number	Size (mm)	I _{out} (mA)	ESR (mΩ)
C _{in}	10 μF, X5R, 6.3 V	TDK Murata	C2012X5R0J106 GRM21BR60J106	2.0 x 1.25 x 1.25	–	–
C _{out}	22 μF, X5R, 6.3 V	TDK Murata	C2012X5R0J226 GRM21BR60J226	2.0 x 1.25 x 1.25	–	–
L	6.8 μH	TDK	VLCF4020–6R8	4.0 x 4.0 x 2.0	500**	146
		Coilcraft	0805PS–682	3.4 x 3.0 x 1.8	210*	1260
		Coilcraft	LPO4812	4.8 x 4.8 x 1.2	340*	225
		Sumida	CLS4D11	4.9 x 4.9 x 1.2	500**	220

*Output current calculated from V_{CC} = 4.2 V_{max}, 1.5 V_{out} and Freq = 700 kHz (1.0 MHz – 20 %).

**Calculated output current from V_{CC} = 4.2 V_{max} and Freq = 700 kHz exceeds 640 mA (I_{lim} – 20%). Therefore maximum output for these conditions shown as 500 mA.

NCP1509

Up to 500 mA, 1 MHz, High Efficiency Synchronous Step-Down DC-DC Converter in DFN Package

The NCP1509 step-down PWM DC-DC converter is optimized for portable applications powered from 1-cell Li-ion or 3 cell Alkaline/NiCd/NiMH batteries. This DC-DC converter utilizes a current-mode control architecture for easy compensation and better line regulation. It also uses synchronous rectification to increase efficiency and reduce external part count. The NCP1509 optimizes efficiency in light load conditions when switched from a normal PWM mode to a "pulsed switching" mode. The device also has a built-in 1 MHz (nominal) oscillator for the PWM circuitry, or it can be synchronized to an external 500 kHz to 1000 kHz clock signal. Finally, it includes an integrated soft-start, cycle-by-cycle current limiting, and thermal shutdown protection. The NCP1509 is available in a space saving, low profile 3x3 mm 10 pin DFN package.

Features

- High Efficiency:
 - 92.5% for 1.8 V Output at 3.6 V Input and 125 mA Load Current
 - 91% for 1.8 V Output at 3.6 V Input and 300 mA Load Current
- Digital Programmable Output Voltages: 1.05, 1.35, 1.57 or 1.8 V
- Output Current up to 500 mA at $V_{in} = 3.6$ V
- Low Quiescent Current of 14 μ A in Pulsed Switching Mode
- Low 0.2 μ A Shutdown Current
- -30°C to 85°C Operation Temperature
- Low Profile DFN Package
- Pb-Free Package is Available

Application

- Cellular Phones, Smart Phones and PDAs
- Digital Still Cameras
- MP3 Players and Portable Audio Systems
- Wireless and DSL Modems
- Portable Equipment

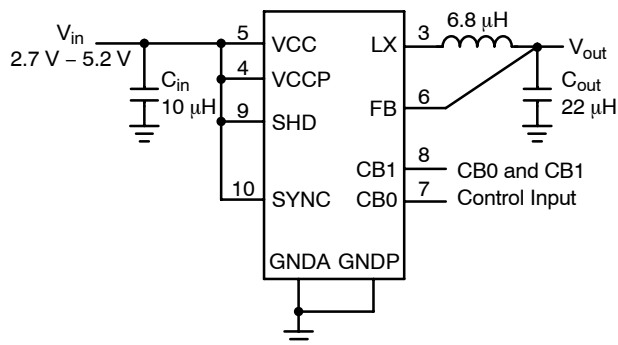


Figure 1. Typical Application Circuit



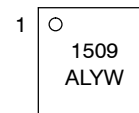
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM



10 PIN DFN
MN SUFFIX
CASE 485C



1509 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NCP1509MNR2	10 Pin DFN	3000 Tape & Reel
NCP1509MNR2G	10 Pin DFN (Pb-Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

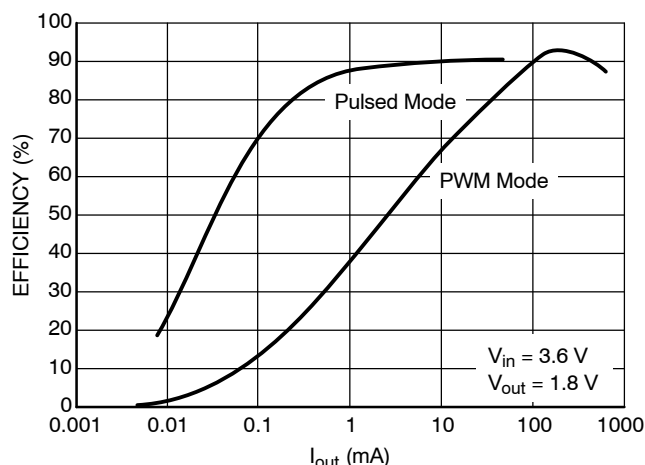


Figure 2. Efficiency vs. Output Current

NCP1509

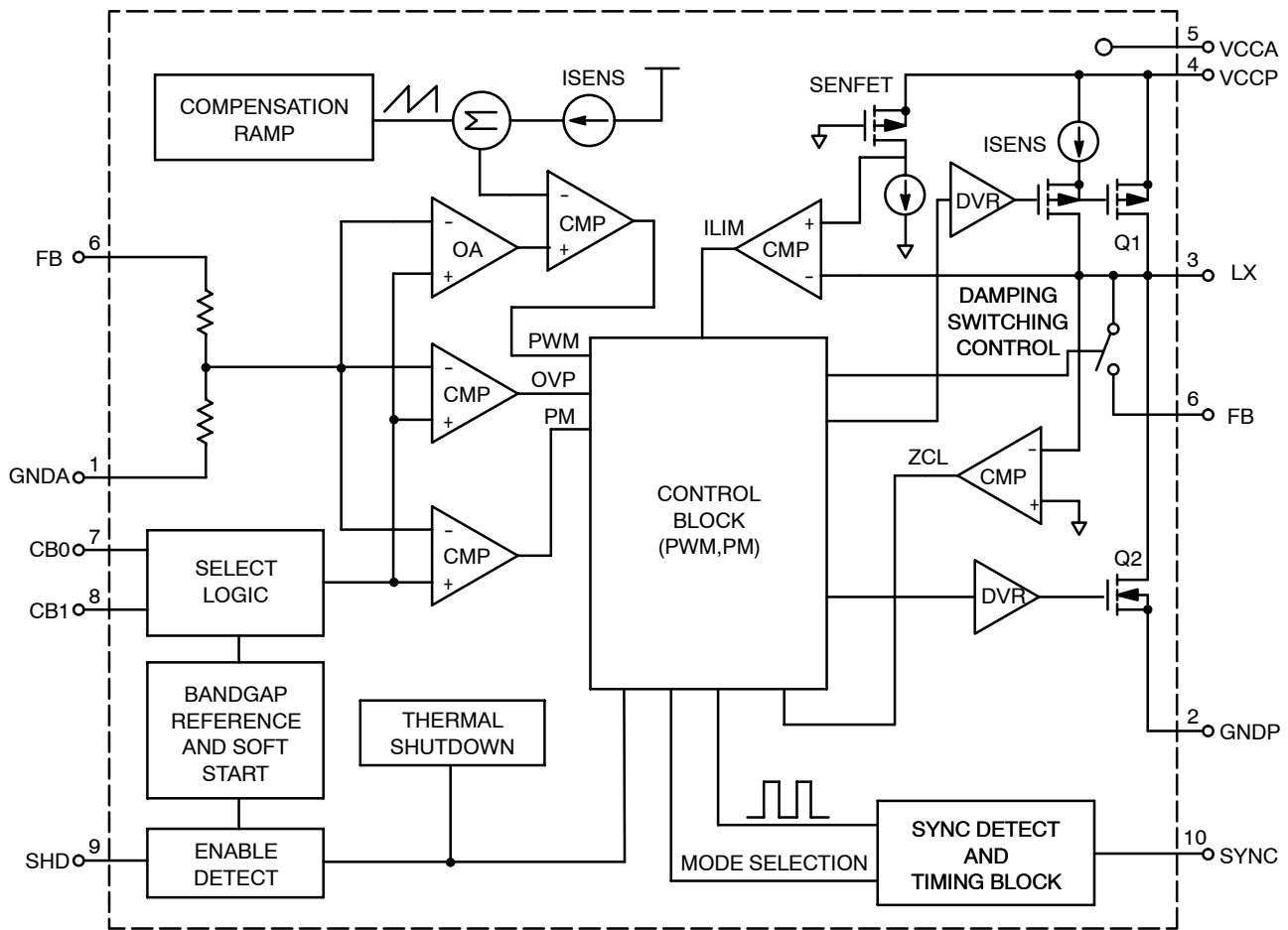


Figure 3. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin Number	Name	Type	Description
1	GNDA	Analog GND	Ground connection for the Analog Section of the IC. This is the GND for the FB, SYNC, CB0, CB1, PG and ENABLE pins.
2	GNDP	Power GND	Ground connection for the N-FET Power Stage.
3	LX	Power Output	Connection from Power MOSFETs to the Inductor.
4	VCCP	Power Input	Power Supply Input for the Switching P-FET.
5	VCCA	Power Input	Power Supply Input for the Analog Section of the IC.
6	FB	Analog Input	Feedback voltage from the output of the power supply.
7	CB0	Analog Input	V_{out} Selection Pin. This pin contains a pulldown resistor.
8	CB1	Analog Input	V_{out} Selection Pin. This pin contains a pullup resistor.
9	SHD	Analog Input	Enable for Switching Regulator. This pin is active high to turn on the NCP1509. This pin contains an internal pulldown resistor.
10	SYNC	Analog Input	Synchronization input for the PWM converter. If a clock signal is present, the converter uses the rising edge for the turn on of the PFET. If this pin is low, the converter is in Low Iq Pulse mode. If this pin is high, the converter uses the internal oscillator for the PWM mode. This pin has an internal pulldown resistor to force the operation into the Pulse mode.

NCP1509

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Maximum Voltage All Pins	$V_{\max}$	5.5	V
Maximum Operating Voltage All Pins	$V_{\max}$	5.2	V
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	68.5	°C/W
Operating Ambient Temperature Range	T_A	–30 to 85	°C
ESD Withstand Voltage	V_{ESD}	Human Body Model (Note 1) > 2500	V
		Machine Model (Note 1) > 150	
Moisture Sensitivity	MSL	Level 1	
Storage Temperature Range	T_{stg}	–55 to 150	°C
Junction Operating Temperature	T_J	–30 to 125	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- This device series contains ESD protection and exceeds the following tests:
 Human Body Model, 100 pF discharge through a 1.5 k Ω following specification JESD22/A114.
 Machine Model, 200 pF discharged through all pins following specification JESD22/A115.
 Latchup as per JESD78 Class II: > 100 mA.

NCP1509

ELECTRICAL CHARACTERISTICS ($V_{in} = 3.6\text{ V}$, $V_o = 1.57\text{ V}$, $T_A = 25^\circ\text{C}$, $F_{syn} = 600\text{ kHz}$ 50% Duty Cycle square wave for PWM mode; $T_A = -30$ to 85°C for Min/Max values, unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} Pin					
Quiescent Current of SYNC Mode, $I_{out} = 0\text{ mA}$	$I_q\text{ PWM}$	–	175	–	μA
Quiescent Current of PWM Mode, $I_{out} = 0\text{ mA}$	$I_q\text{ PWM}$	–	185	–	μA
Quiescent Current of Pulsed Mode, $I_{out} = 0\text{ mA}$	$I_q\text{ Pulsed}$	–	14	–	μA
Quiescent Current, SHD Low	$I_q\text{ Off}$	–	0.1	1.0	μA
Input Voltage Range	V_{in}	2.5	–	5.2	V

SYNC Pin

Input Voltage	V_{sync}	–0.3	–	$V_{cc} + 0.3$	V
Frequency Operational Range	F_{sync}	500	600	1000	kHz
Minimum Synchronization Pulse Width	$D_{csync}\text{ Min}$	–	5.0	–	%
Maximum Synchronization Pulse Width	$D_{csync}\text{ Max}$	–	95	–	%
SYNC “H” Voltage Threshold	V_{synch}	–	920	1200	mV
SYNC “L” Voltage Threshold	V_{syncl}	400	830	–	mV
SYNC “H” Input Current, $V_{sync} = 3.6\text{ V}$	I_{synch}	–	2.2	–	μA
SYNC “L” Input Current, $V_{sync} = 0\text{ V}$	I_{syncl}	–0.5	–	–	μA

Output Level Selection Pins

Input Voltage	V_{cb}	–0.3	–	$V_{cc} + 0.3$	V
CB0, CB1 “H” Voltage Threshold	$V_{cb}\text{ h}$	–	920	1200	mV
CB0, CB1 “L” Voltage Threshold	$V_{cb}\text{ l}$	400	830	–	mV
CB0 “H” Input Current, $CB = 3.6\text{ V}$	$I_{cb0}\text{ h}$	–	2.2	–	μA
CB0 “L” Input Current, $CB = 0\text{ V}$	$I_{cb0}\text{ l}$	–0.5	–	–	μA
CB1 “H” Input Current, $CB = 3.6\text{ V}$	$I_{cb1}\text{ h}$	–	0.3	1.0	μA
CB1 “L” Input Current, $CB = 0\text{ V}$	$I_{cb1}\text{ l}$	–	–2.2	–	μA

Shutdown Pin

Input Voltage	V_{shd}	–0.3	–	$V_{cc} + 0.3$	V
SHD “H” Voltage Threshold	$V_{shd}\text{ h}$	–	920	1200	mV
SHD “L” Voltage Threshold	$V_{shd}\text{ l}$	400	830	–	mV
SHD “H” Input Current, $SHD = 3.6\text{ V}$	$I_{shd}\text{ h}$	–	2.2	–	μA
SHD “L” Input Current, $SHD = 0\text{ V}$	$I_{shd}\text{ l}$	–0.5	–	–	μA

Feedback Pin

Input Voltage	V_{fb}	–0.3	–	$V_{cc} + 0.3$	V
Input Current, $V_{fb} = 1.5\text{ V}$	I_{fb}	–	5.0	7.5	μA

SYNC PWM Mode Characteristics

Switching P–FET Current Limit	I_{lim}	–	800	–	mA
Duty Cycle (Note 2)	DC	–	–	100	%
Minimum On Time	$T_{on(min)}$	–	75	–	nsec
$R_{DS(on)}$ Switching P–FET and N–FET	$R_{DS(on)}$	–	0.23	–	Ω
Switching P–FET and N–FET Leakage Current	I_{leak}	–	0	10	μA
Output Overvoltage Threshold	V_o	–	3.0	–	%
Feedback Voltage Accuracy, $V_{out}\text{ Set} = 1.05\text{ V}$ $C_{B0} = L$, $C_{B1} = L$, $I_{out} = 300\text{ mA}$	V_{out}	1.018	1.050	1.082	V

NCP1509

ELECTRICAL CHARACTERISTICS ($V_{in} = 3.6\text{ V}$, $V_o = 1.57\text{ V}$, $T_A = 25^\circ\text{C}$, $F_{syn} = 600\text{ kHz}$ 50% Duty Cycle square wave for PWM mode; $T_A = -30$ to 85°C for Min/Max values, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit

SYNC PWM Mode Characteristics (continued)

Feedback Voltage Accuracy, V_{out} Set = 1.35 V, $C_{B0} = L$, $C_{B1} = H$, $I_{out} = 300\text{ mA}$	V_{out}	1.309	1.350	1.391	V
Feedback Voltage Accuracy, V_{out} Set = 1.57 V, $C_{B0} = H$, $C_{B1} = H$, $I_{out} = 300\text{ mA}$	V_{out}	1.523	1.570	1.617	V
Feedback Voltage Accuracy, V_{out} Set = 1.8 V, $C_{B0} = H$, $C_{B1} = L$, $I_{out} = 300\text{ mA}$	V_{out}	1.746	1.800	1.854	V
Line Regulation, $V_{in} = 2.7\text{ V}$ – 3.6 V , $I_{out} = 100\text{ mA}$	–	–15	–	+15	mV
Line Regulation, $V_{in} = 3.6\text{ V}$ – 5.2 V , $I_{out} = 100\text{ mA}$	–	–15	–	+15	mV
Load Regulation, $I_{out} = 100\text{ mA}$ – 300 mA	–	–15	–	+15	mV
Load Transient Response, 10 to 100 mA Load Step	V_{out}	–	50	–	mV
Line Transient Response, $I_{out} = 100\text{ mA}$, 3.0 to 3.6 V_{in} Line Step	V_{out}	–	± 5.0	–	mVpp

PWM Mode with Internal Oscillator Characteristics

Switching P–FET Current Limit	I_{lim}	–	800	–	mA
Duty Cycle (Note 2)	DC	–	–	100	%
Minimum On Time	$T_{on(min)}$	–	75	–	nsec
Internal Oscillator Frequency $-T_A = 25^\circ\text{C}$ $-30^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	F_{osc}	760 700	980 980	1240 1240	kHz
$R_{DS(on)}$ Switching P–FET and N_FET	$R_{DS(on)}$	–	0.23	–	Ω
Switching P–FET and N–FET Leakage Current	I_{leak}	–	0	10	μA
Output Overvoltage Threshold	V_o	–	3.0	–	%
Feedback Voltage Accuracy, V_{out} Set = 1.05 V, $C_{B0} = L$, $C_{B1} = L$, $I_{out} = 300\text{ mA}$	V_{out}	1.018	1.050	1.082	V
Feedback Voltage Accuracy, V_{out} Set = 1.35 V, $C_{B0} = L$, $C_{B1} = H$, $I_{out} = 300\text{ mA}$	V_{out}	1.309	1.350	1.391	V
Feedback Voltage Accuracy, V_{out} Set = 1.57 V, $C_{B0} = H$, $C_{B1} = H$, $I_{out} = 300\text{ mA}$	V_{out}	1.523	1.570	1.617	V
Feedback Voltage Accuracy, V_{out} Set = 1.8 V, $C_{B0} = H$, $C_{B1} = L$, $I_{out} = 300\text{ mA}$	V_{out}	1.746	1.800	1.854	V
Line Regulation, $V_{in} = 2.7\text{ V}$ – 3.6 V , $I_{out} = 100\text{ mA}$	–	–15	–	+15	mV
Line Regulation, $V_{in} = 3.6\text{ V}$ – 5.2 V , $I_{out} = 100\text{ mA}$	–	–15	–	+15	mV
Load Regulation, $I_{out} = 100\text{ mA}$ – 300 mA	–	–15	–	+15	mV
Load Transient Response, 10 to 100 mA Load Step	V_{out}	–	50	–	mV
Line Transient Response, $I_{out} = 100\text{ mA}$, 3.0 to 3.6 V_{in} Line Step	V_{out}	–	± 5.0	–	mVpp

Pulsed Mode Characteristics

Peak Current Limit	I_{lim}	–	200	–	mA
Output Current	I_{out}	0.05	–	30	mA
Output Ripple Voltage, $I_{out} = 100\text{ }\mu\text{A}$	V_{out}	–	22	100	mV
Feedback Voltage Accuracy, V_{out} Set = 1.05 V, $C_{B0} = L$, $C_{B1} = L$	V_{out}	1.018	1.050	1.082	V
Feedback Voltage Accuracy, V_{out} Set = 1.35 V, $C_{B0} = L$, $C_{B1} = H$	V_{out}	1.309	1.350	1.391	V
Feedback Voltage Accuracy, V_{out} Set = 1.57 V, $C_{B0} = H$, $C_{B1} = H$	V_{out}	1.523	1.570	1.617	V
Feedback Voltage Accuracy, V_{out} Set = 1.8 V, $C_{B0} = H$, $C_{B1} = L$	V_{out}	1.746	1.800	1.854	V

2. Maximum value is guaranteed by design.

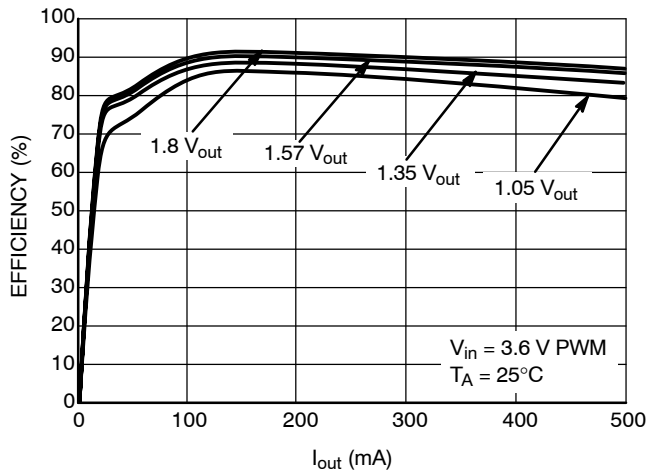


Figure 4. Efficiency vs. Output Current in PWM Mode

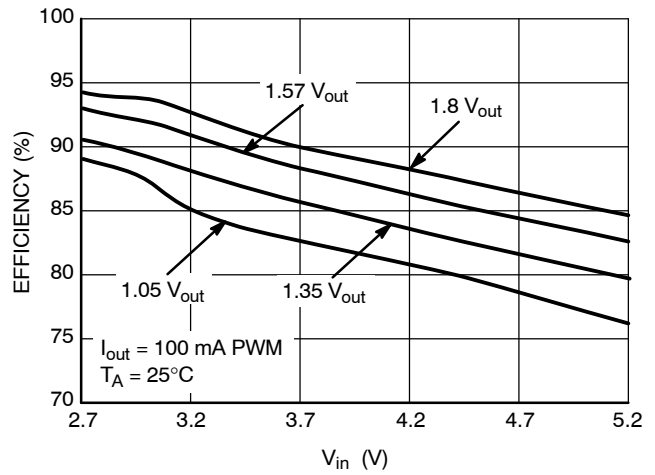


Figure 5. Efficiency vs. Input Voltage in PWM Mode

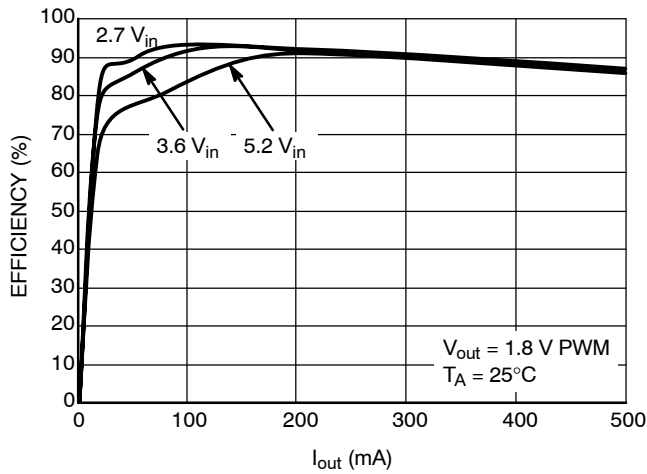


Figure 6. Efficiency vs. Output Current at Different Input Voltage

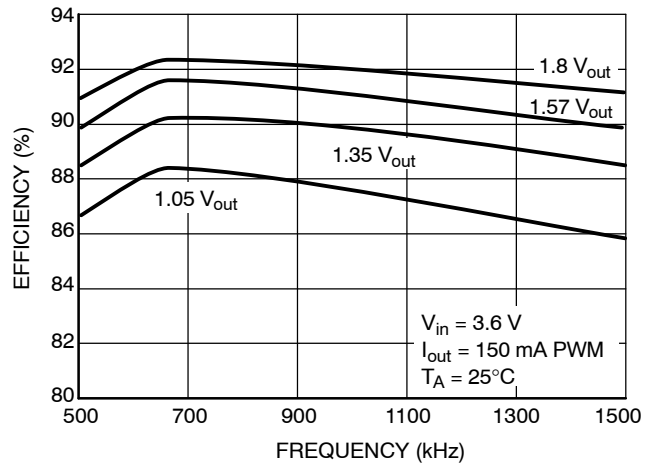


Figure 7. Efficiency vs. Frequency

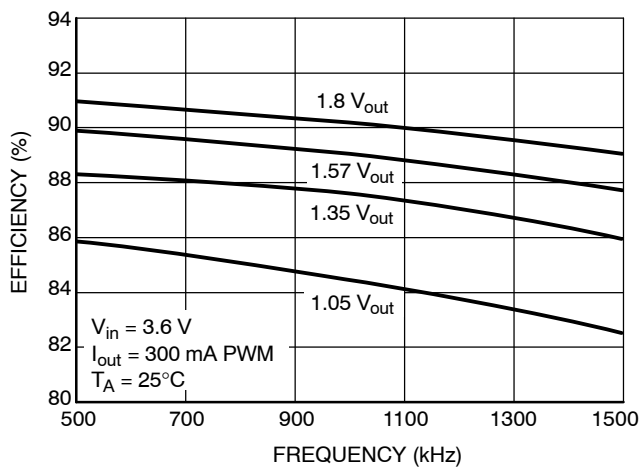


Figure 8. Efficiency vs. Frequency

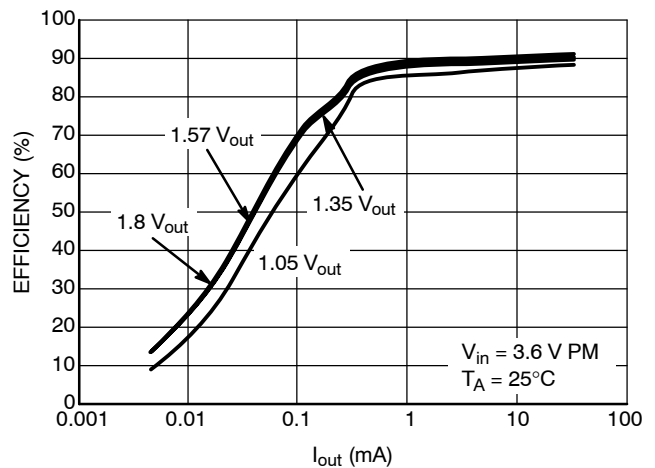


Figure 9. Efficiency vs. Output Current in Pulsed Mode

NCP1509

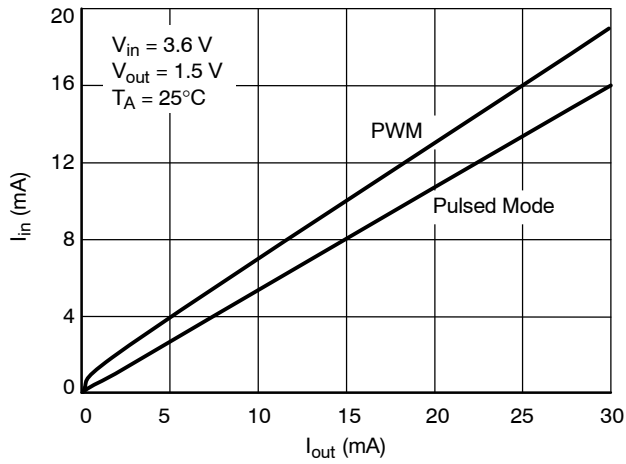


Figure 10. Input Current Comparison

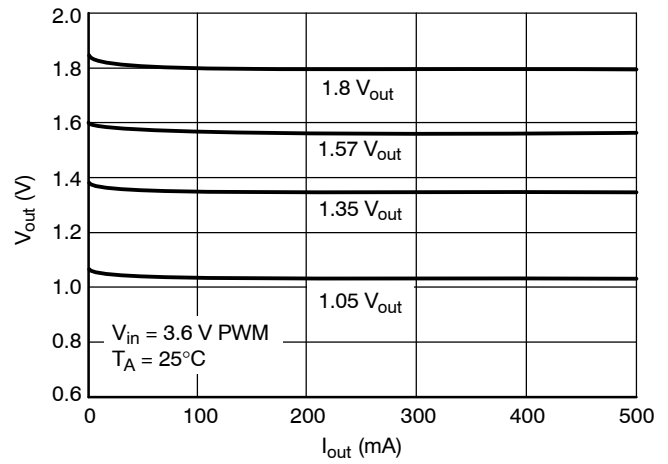


Figure 11. Output Voltage vs. Output Current

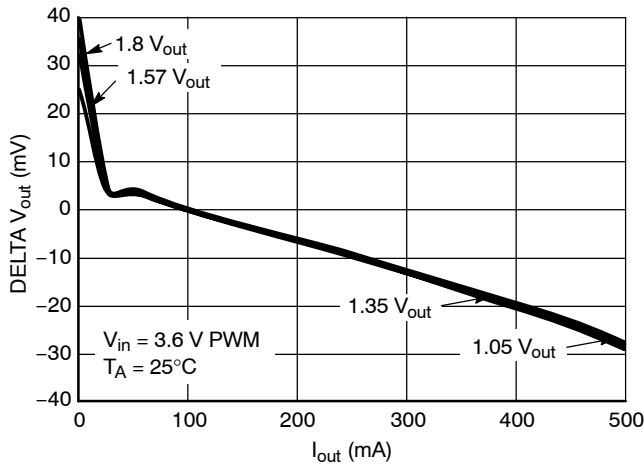


Figure 12. Load Regulation in PWM Mode

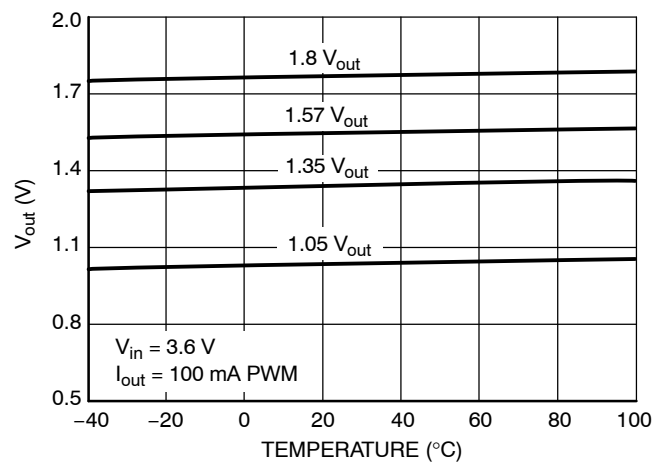


Figure 13. Output Voltage vs. Temperature

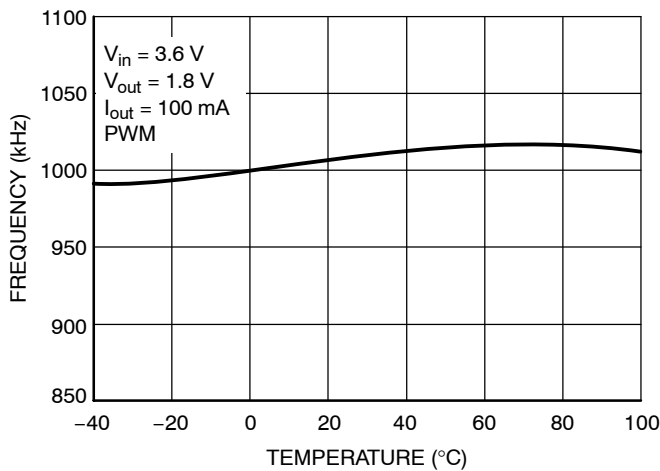


Figure 14. Oscillator Frequency vs. Temperature

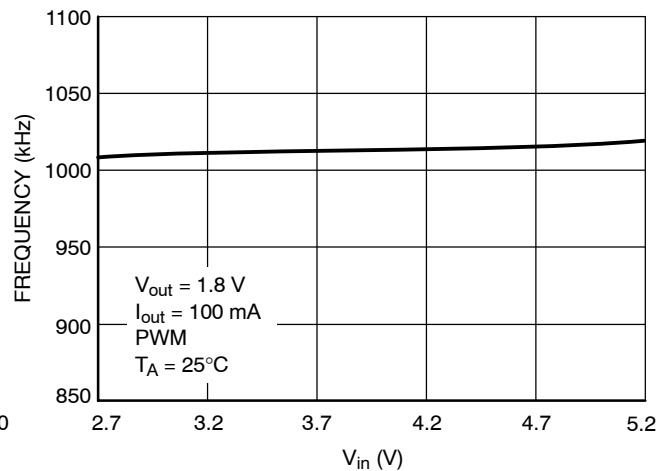


Figure 15. Oscillator Frequency vs. Input Voltage

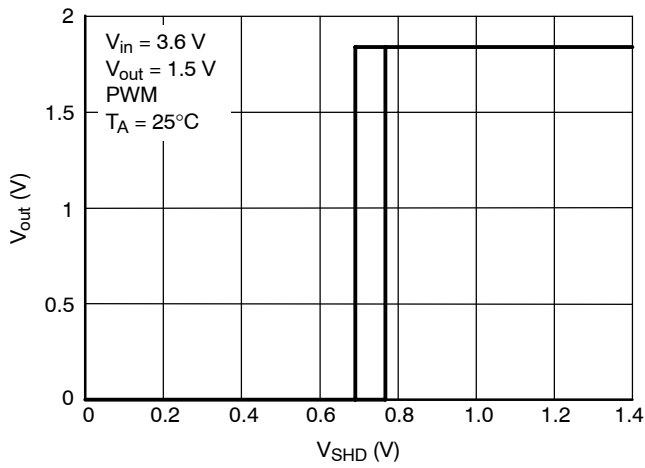


Figure 16. Output Voltage vs. Shutdown Pin Voltage

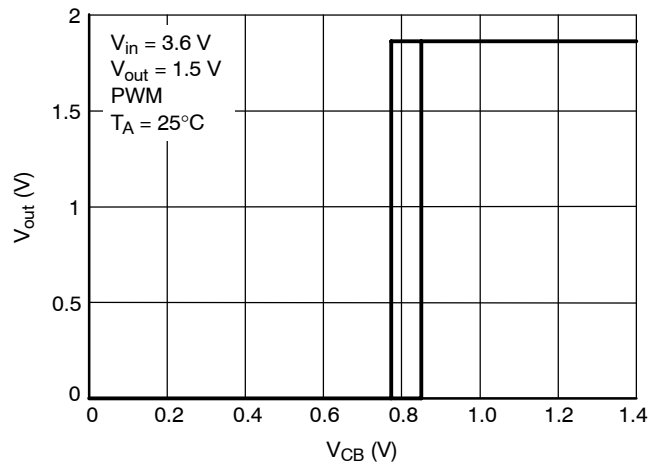


Figure 17. Transition Level of CB Pins

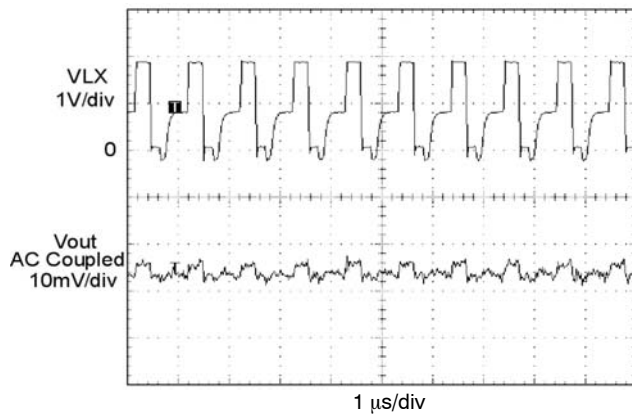


Figure 18. Light-Load PWM Switching Waveform ($V_{in} = 3.6$ V, $V_{out} = 1.8$ V, $I_{out} = 30$ mA)

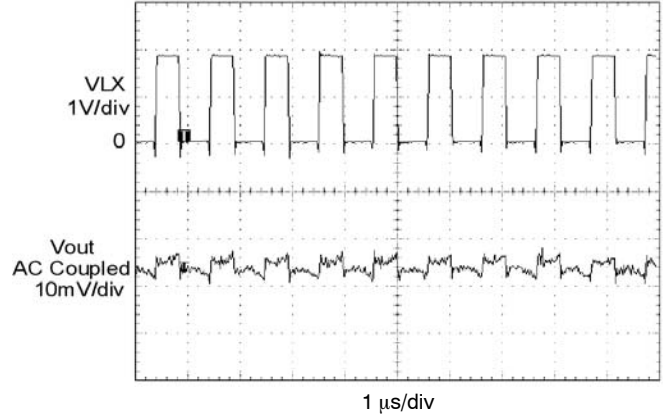


Figure 19. Heavy-Load PWM Switching Waveform ($V_{in} = 3.6$ V, $V_{out} = 1.8$ V, $I_{out} = 300$ mA)

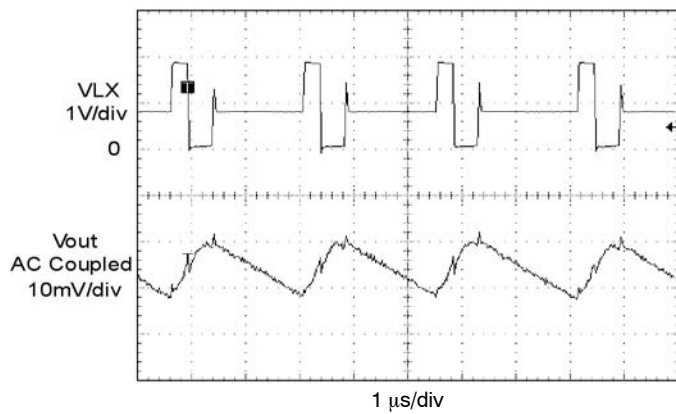


Figure 20. Pulsed Mode Switching Waveform ($V_{in} = 3.6$ V, $V_{out} = 1.8$ V, $I_{out} = 30$ mA)

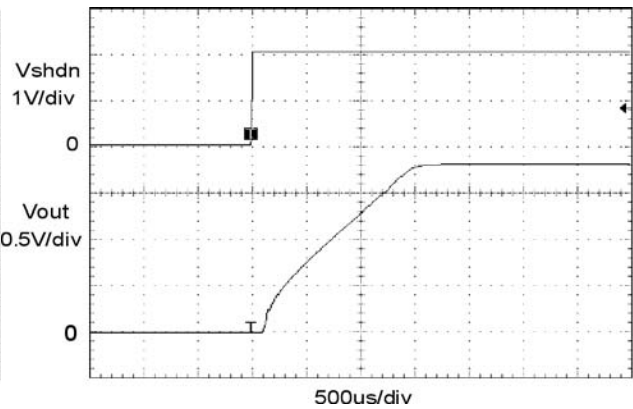


Figure 21. Soft-Start ($V_{in} = 3.6$ V, $V_{out} = 1.8$ V, $I_{out} = 150$ mA)

NCP1509

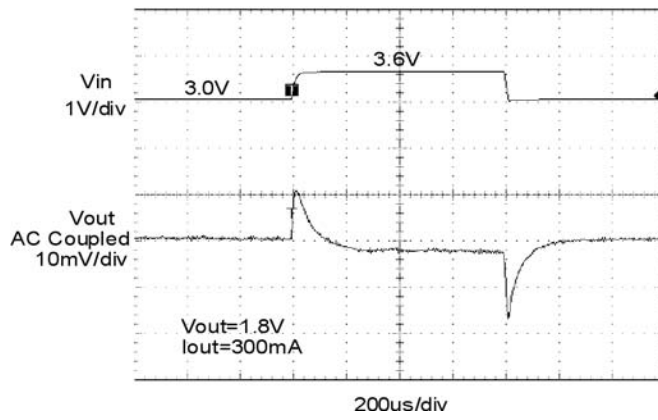


Figure 22. Line Transient Response

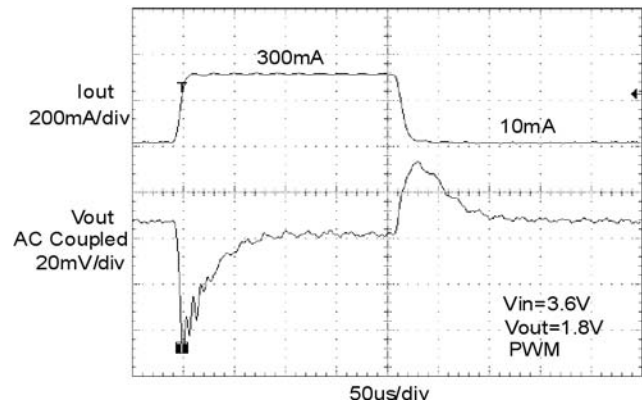


Figure 23. Load Transient Response

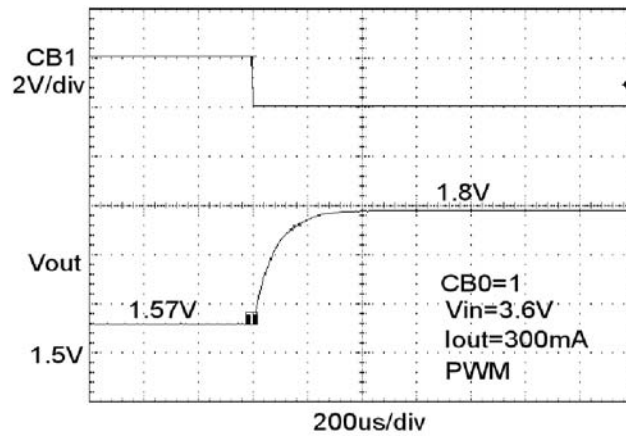


Figure 24. Output Voltage Transition
from 1.57 V to 1.8 V

DETAILED OPERATING DESCRIPTION

Overview

The NCP1509 is a monolithic micro-power high frequency PWM step-down DC-DC converter specifically optimized for applications requiring high efficiency and a small PCB footprint such as portable battery powered products. It integrates synchronous rectification to improve efficiency as well as eliminate the external Schottky diode. High switching frequency allows for a low profile inductor and capacitors to be used. Four digital selectable output voltages (1.05, 1.35, 1.57 and 1.8 V) can be generated from the input supply that can range from 2.7–5.2 V. All loop compensation is integrated as well further reducing the external component count as well.

The DC-DC converter has two operating modes (normal PWM, pulsed switching), which are intended to allow for optimum efficiency under either light (up to 30 mA) or heavy loads. The user determines the operating mode by controlling the SYNC input. In addition the SYNC input can be used to synchronize the PWM to an external system clock signal in the range of 500–1000 kHz.

PWM Operating Mode

The NCP1509 can be set to current mode PWM operation by connecting SYNC pin to V_{CC} . In this mode, the output voltage is regulated by modulating on-time pulse width of the main switch Q1 at a fixed frequency of 1 MHz. The switching of the PMOS Q1 is controlled by a flip-flop driven by the internal oscillator and a comparator that compares the error signal from an error amplifier with the sum of the sensed current signal and compensation ramp. At the beginning of each cycle, the main switch Q1 is turned ON by the rising edge of the internal oscillation clock. The inductor current ramps up until the sum of the current sense signal and compensation ramp becomes higher than the error voltage amplifier. Once this has occurred, the PWM comparator resets the flip-flop, Q1 is turned OFF and the synchronous switch Q2 is turned ON. Q2 replaces the external Schottky diode to reduce the conduction loss and improve the efficiency. To avoid overall power loss, a certain amount of dead time is introduced to ensure Q1 is completely turned OFF before Q2 is being turned ON.

In continuous conduction mode (CCM), Q1 is turned ON after Q2 is completely turned OFF to start a new clock cycle. In discontinuous conduction mode (DCM), the zero crossing comparator (ZLC) will turn off Q2 when the inductor current drops to zero.

Overvoltage Protection

The overvoltage protection circuit is present in PWM mode to prevent the output voltage from going too high under light load or fast load transient conditions. The output overvoltage threshold is 5% above nominal set

value. If the output voltage rises above 5% of the nominal value, the OVP comparator is activated and switch Q1 is turned OFF. Switching will continue when the output voltage falls below the threshold of OVP comparator.

Pulsed Mode (PM)

Under light load conditions (< 30 mA), NCP1509 can be configured to enter a low current pulsed mode operation to reduce power consumption. This is accomplished by SYNC pin held LOW. The output regulation is implemented by pulse frequency modulation. If the output voltage drops below the threshold of PM comparator (typically $V_{nom}-2\%$), a new cycle will be initiated by the PM comparator to turn on the switch Q1. Q1 remains ON until 200 mA inductor peak current is reached. Then ILIM comparator goes high to switch off Q1. After a short dead time delay, switch rectifier Q2 is turn ON. The zero crossing comparator will detect when the inductor current drops to zero and send the signal to turn off Q2. The output voltage continues to decrease through discharging the output capacitor. When the output voltage falls below the threshold of PM comparator again, a new cycle starts immediately.

Cycle-by-Cycle Current Limit

From the block diagram (Figure 3), an ILIM comparator is used to realize cycle-by-cycle current limit protection. The comparator compares the LX pin voltages with the reference voltage from the SENFET, which is biased by constant current. If the inductor current reaches the limit, ILIM comparator detects the LX voltage falling below the reference voltage from SENFET and releases the signal to turn off the switch Q1. The cycle-by-cycle current limit is set at 800 mA in PWM and 200 mA in PM.

Frequency Synchronization and Operating Mode Selection

The SYNC pin can also be used for frequency synchronization by connecting it with an external clock signal. It operates in PWM mode when synchronized to an external clock. The switching cycle initiates by the rising edge of the clock. The synchronization clock signals between 0.4 V and 1.2 V from 500 kHz to 1000 kHz.

Gating on and off the clock, the SYNC pin can also be used to select between PM and PWM modes. It allows efficient dynamical power management by adjusting the converter operation to the specific system requirement. Set SYNC pin low to select PM mode at light load conditions (up to 30 mA) and set SYNC pin high or connect with external clock to select PWM mode at heavy load condition to achieve optimum efficiency. Table 1 shows the mode selection with three different SYNC pin states.

Table 1. Operating Mode Selection

SYNC Pin State	Operating Mode
LOW	Pulsed Mode (PM)
HIGH	PWM, 1 MHz Switch Frequency
CLOCK	PWM, Frequency Synchronization

Output Voltage Selection

The output voltage is digitally programmed to one of four voltage levels depending on the logic state of CB0 and CB1. Therefore if the NCP1509's load, such as a digital cellular phone's baseband processor, supports dynamic power management, the device can lower or raise its core voltage under software control. When combined with the pulsed current mode function in low load situations, this active voltage management further stretches the useful operating life of the handset between charges. Figure 24 shows a typical transition between 1.57 to 1.8 volts.

The output voltage levels are listed in Table 2. The CB0 has a pull down resistor and the CB1 has a pullup resistor. The default output voltage is 1.35 V when CB0 and CB1 are floating.

Table 2. Truth Table for CB0 and CB1 with the corresponding output voltage

CB0	CB1	Vout(V)
0	0	1.05
0	1	1.35
1	1	1.57
1	0	1.8

Soft-Start

The NCP1509 uses soft-start to limit the inrush current when the device is initially powered up or enabled. Soft-start is implemented by gradually increasing the reference voltage until it reaches the full reference voltage. During startup, a pulsed current source charges the internal soft-start capacitor to provide gradually increasing reference voltage for the PWM loop. When the voltage across the capacitor ramps up to the nominal reference voltage, the pulsed current source will be switched off and the reference voltage will switch to the regular reference voltage. From Figure 21, it shows the soft-start time is about 1.5 ms.

Shutdown Mode

When the SHD pin has a voltage applied of less than 0.4 V, the NCP1509 will be disabled. In shutdown mode, the internal reference, oscillator and most of the control circuitries are turned off. Therefore, the typical current consumption will be 0.1 μ A (typical value).

Applying a voltage above 1.2 V to SHD pin will enable the device for normal operation. The device will go through soft-start to normal operation.

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. If the junction temperature exceeds 160°C, the device shuts down. In this mode switch Q1 and Q2 and the control circuits are all turned off. The device restarts in soft-start after the temperature drops below 135°C. This feature is provided to prevent catastrophic failures from accidental device overheating and it is not intended as a substitute for proper heatsinking.

APPLICATIONS INFORMATION

Component Selection

Input Capacitor Selection

In PWM operating mode, the input current is pulsating with large switching noise. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly. The capacitance needed for the input bypass capacitor depends on the source impedance of the input supply. The RMS capacitor current is calculated as:

$$I_{RMS} \approx I_O \sqrt{D \cdot D'} \quad (\text{eq. 1})$$

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is $I_{O,max}/2$.

For NCP1509, a low profile ceramic capacitor of 10 μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to the V_{CC} Pin.

Inductor Value Selection

Selecting the proper inductor value is based on the desired ripple current. The relationship between the inductance and the inductor ripple current is given by the equation in below.

$$\Delta i_L = \frac{V_{out}}{L f_s} \left(1 - \frac{V_{out}}{V_{in}} \right) \quad (\text{eq. 2})$$

Large value inductors will have small ripple current and low value inductor will have high ripple current. For NCP1509, the compensation is internally fixed and a fixed 6.8 μH inductor is needed for most of the applications.

Output Capacitor Selection

Selecting the proper output capacitor is based on the desired output ripple voltage. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output ripple voltage is given by:

$$\Delta V_C = \Delta i_L \cdot \left(\text{ESR} + \frac{1}{4 f_s C_{out}} \right) \quad (\text{eq. 3})$$

The RMS output capacitor current is given by:

$$I_{RMS}(C_{out}) = \frac{V_O \cdot (1 - D)}{2 \sqrt{3} \cdot L \cdot f_s} \quad (\text{eq. 4})$$

Where f_s is the switching frequency and ESR is the effective series resistance of the output capacitor. A low ESR, 22 μF ceramic capacitor is recommended for NCP1509 in most of applications. For example, with TDK C2012X5R0J226 output capacitor, the output ripple is less than 10 mV at 300 mA.

Design Example

As a design example, assume that the NCP1509 is used in a single lithium-ion battery application. The input voltage, V_{in} , is 3.0 V to 4.2 V. Output condition is V_{out} at 1.8 V with a typical load current of 120 mA and a maximum of 300 mA. For NCP1509, the inductor has a predetermined

value, 6.8 μH . The inductor ESR will factor into the overall efficiency of the converter. The inductor needs to be selected by the required peak current.

Equation 5 is the basic equation for an inductor and describes the voltage across the inductor. The inductance value determines the slope of the current of the inductor.

$$\frac{V_L}{L} = \frac{di_L}{dt} \quad (\text{eq. 5})$$

Equation 5 is rearranged to solve for the change in current for the on-time of the converter in Continuous Conduction Mode.

$$\begin{aligned} i_{L,pk-pk} &= \frac{(V_{in} - V_{out})}{L} \cdot DT_s \\ &= \frac{(V_{in} - V_{out})}{L} \cdot \frac{V_{in}}{V_{out}} \cdot \frac{1}{f_s} \end{aligned} \quad (\text{eq. 6})$$

$$i_{L,max} = I_{O,max} + \frac{\Delta i_{L,pk-pk}}{2}$$

Utilizing Equations 6, the peak-to-peak inductor current is calculated using the following worst-case conditions.

$$V_{in,max} = 4.2 \text{ V}, V_{out} = 1.8 \text{ V}, f_s = 1 \text{ MHz} - 20\%,$$

$$L = 6.8 \mu\text{H} - 10\%, i_{L,pk-pk} = 211 \text{ mA}, i_{L,max} = 405 \text{ mA}$$

Therefore, the inductor must have a maximum current exceeding 405 mA.

Since the compensation is fixed internally in the IC, the input and output capacitors as well as the inductor have a predetermined value too: $C_{in} = 10 \mu\text{F}$ and $C_{out} = 22 \mu\text{F}$. Low ESR capacitors are needed for best performance. Therefore, ceramic capacitors are recommended. Please see Table 3 for recommended inductors and capacitors.

PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise and unwanted feedbacks that can affect the performance of the converter. Hints suggested below can be used as a guideline in most situations.

1. Use star-ground connection to connect the IC ground nodes and capacitor GND nodes together at one point. Keep them as close as possible. And then connect this to the ground plane (if it is used) through several vias. This will reduce noise in ground plane by preventing the switching currents from flowing through the ground plane.

2. Place the power components (i.e., input capacitor, inductor and output capacitor) as close together as possible for best performance. All connecting traces must be short, direct, and thick to reduce voltage errors caused by resistive losses across these traces.

3. Separate the feedback path of the output voltage from the power path. Keep this path close to the NCP1509 circuit. And also route it away from noisy components.

NCP1509

This will prevent noise from coupling into voltage feedback trace.

4. Place the DC-DC converter away from noise sensitive circuitry, such as RF circuits. Interference with noise

sensitive circuitry in the DC-DC converter can be reduced by distance between them.

The following shows NCP1509 demo board layout and suggested bill of materials.

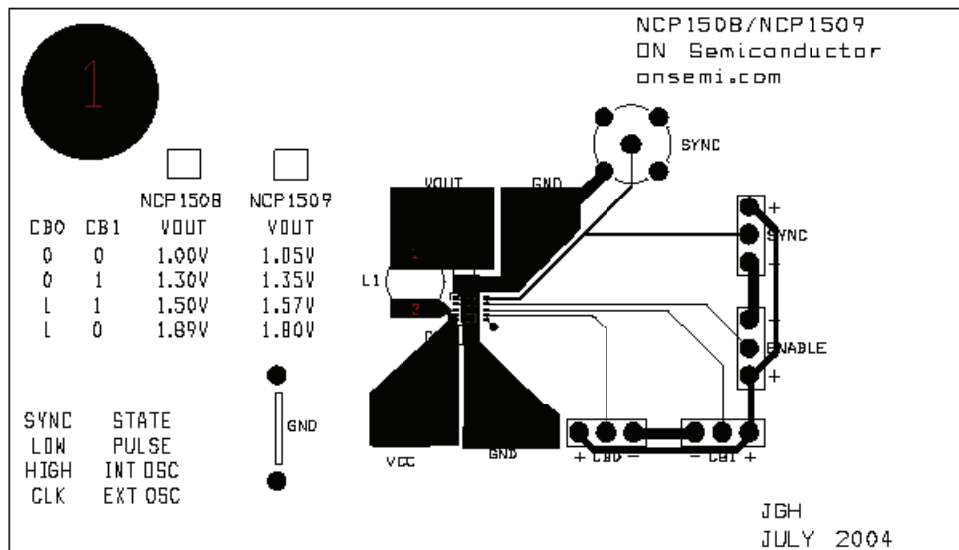


Figure 25. Top and Silkscreen Layer

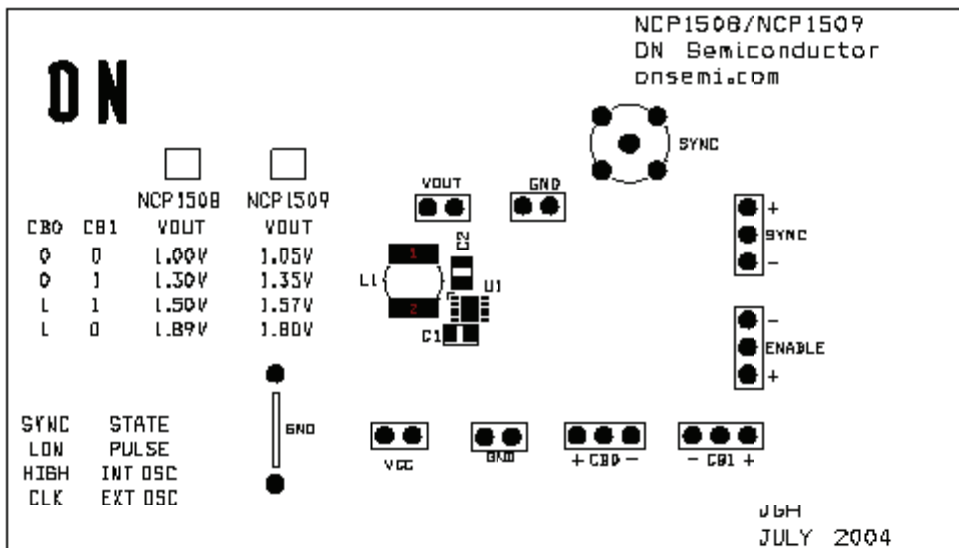


Figure 26. Soldermask Top and Silkscreen Layer

NCP1509

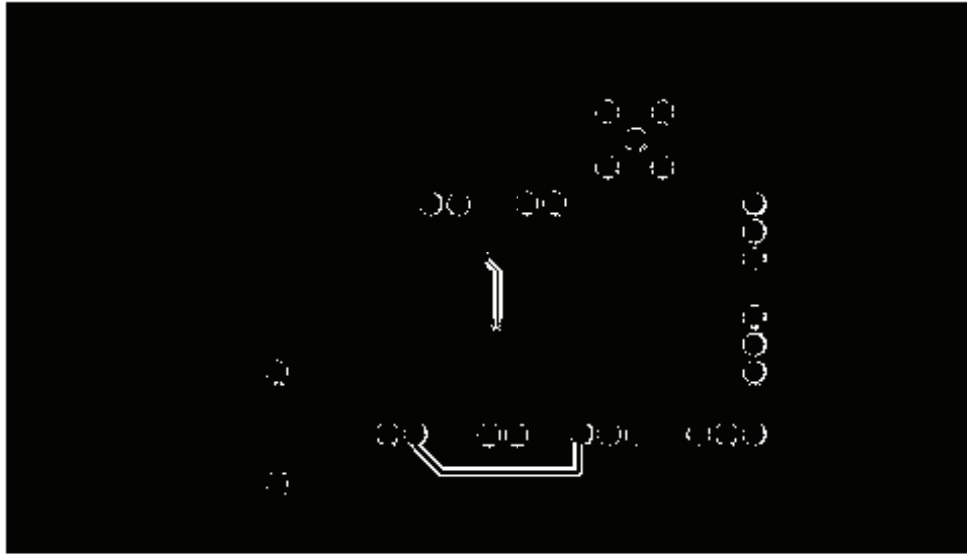


Figure 27. Bottom Layer

Table 3. Bill of Materials

Component	Value	Manufacturer	Part Number	Size (mm)	I _{out} (mA)	ESR (mΩ)
C _{in}	10 μF, X5R, 6.3 V	TDK Murata	C2012X5R0J106 GRM21BR60J106	2.0 x 1.25 x 1.25	–	–
C _{out}	22 μF, X5R, 6.3 V	TDK Murata	C2012X5R0J226 GRM21BR60J226	2.0 x 1.25 x 1.25	–	–
L	6.8 μH	TDK	VLCF4020–6R8	4.0 x 4.0 x 2.0	500**	146
		Coilcraft	0805PS–682	3.4 x 3.0 x 1.8	210*	1260
		Coilcraft	LPO4812	4.8 x 4.8 x 1.2	340*	225
		Sumida	CLS4D11	4.9 x 4.9 x 1.2	500**	220

*Output current calculated from $V_{CC} = 4.2 V_{max}$, $1.5 V_{out}$ and Freq = 700 kHz (1.0 MHz – 20 %).

**Calculated output current from $V_{CC} = 4.2 V_{max}$ and Freq = 700 kHz exceeds 640 mA ($I_{lim} - 20\%$). Therefore maximum output for these conditions shown as 500 mA.

NCP1510A

Up to 500 mA, High Efficiency Synchronous Step-Down DC-DC Converter in Chip Scale Package

The NCP1510A step-down PWM DC-DC converter is optimized for portable applications powered from 1-cell Li-ion or 3-cell Alkaline/NiCd/NiMH batteries. This DC-DC converter utilizes a current-mode control architecture for easy compensation and better line regulation. It also uses synchronous rectification to increase efficiency and reduce external part count. The NCP1510A optimizes efficiency in light load conditions when switched from a normal PWM mode to a "pulsed switching" mode. The device also has a built-in oscillator for the PWM circuitry, or it can be synchronized to an external 500 kHz to 1000 kHz clock signal. Finally, it includes an integrated soft-start, cycle-by-cycle current limiting, and thermal shutdown protection. The NCP1510A is available in a space saving, 9 pin chip scale package.

Features

- High Efficiency:
 - 92.5% for 1.8 V Output at 3.6 V Input and 125 mA Load Current
 - 91.5% for 1.8 V Output at 3.6 V Input and 300 mA Load Current
- Digital Programmable Output Voltages: 1.05, 1.35, 1.57 or 1.8 V
- Output Current up to 500 mA at $V_{in} = 3.6$ V
- Low Quiescent Current of 14 μ A in Pulsed Switching Mode
- Low 0.1 μ A Shutdown Current
- -30°C to 85°C Operation Temperature
- Ceramic Input/Output Capacitor
- 9 Pin Chip Scale Package
- Pb-Free Package is Available

Applications

- Cellular Phones, Smart Phones and PDAs
- Digital Still Cameras
- MP3 Players and Portable Audio Systems
- Wireless and DSL Modems
- Portable Equipment

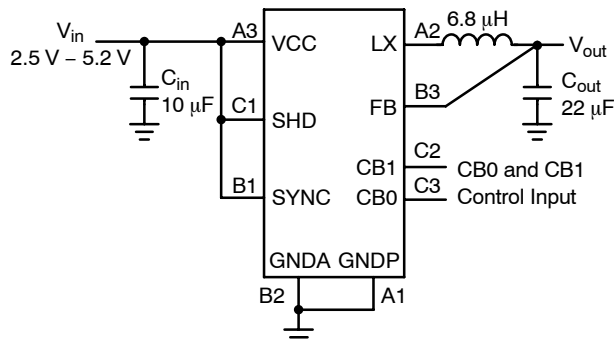


Figure 1. Typical Application Circuit



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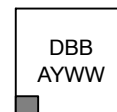
<http://onsemi.com>



A1

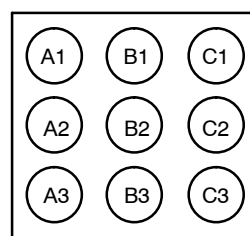
DBB = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

MARKING DIAGRAM



A1

PIN CONNECTIONS



(Bottom View)

Pin: A1 – GNDP
A2 – LX
A3 – VCC
B1 – SYNC
B2 – GNDA
B3 – FB
C1 – SHD
C2 – CB1
C3 – CB0

ORDERING INFORMATION

Device	Package	Shipping†
NCP1510AFCT1	Micro Bump	3000 Tape & Reel
NCP1510AFCT1G	Micro Bump (Pb-Free)	3000 Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

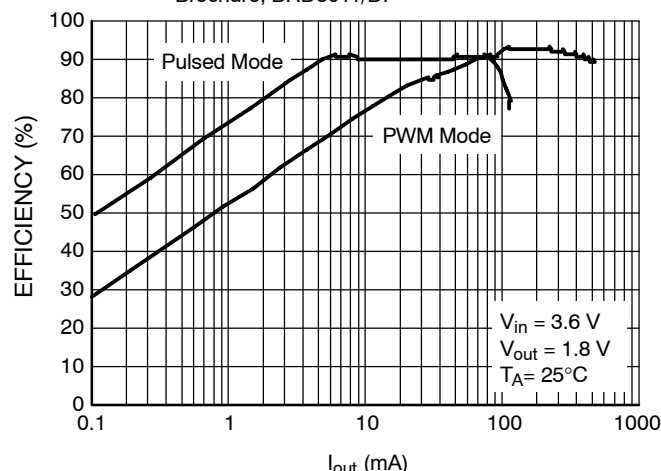


Figure 2. PWM versus Pulse Efficiency Comparison

NCP1510A

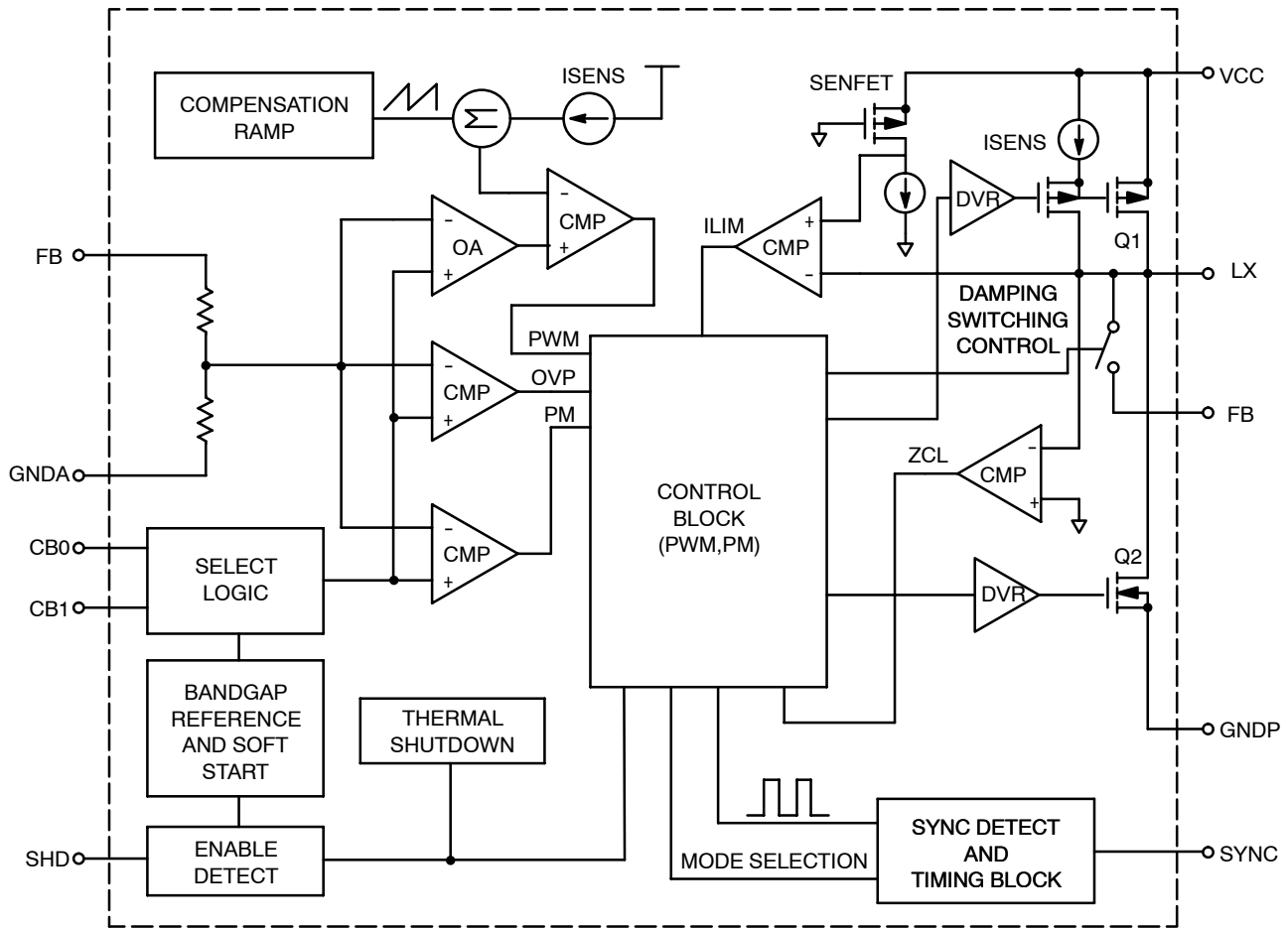


Figure 3. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Type	Description
A1	GNDP	Power Ground	Ground Connection for the NFET Power Stage.
A2	LX	Analog Output	Connection from Power Pass Elements to the Inductor.
A3	V _{CC}	Analog Input	Power Supply Input for Power and Analog V _{CC} .
B1	SYNC	Analog Input	Synchronization input for the PWM converter. If a clock signal is present, the converter uses the rising edge for the turn on. If this pin is low, the converter is in the Pulsed mode. If this pin is high, the converter uses the internal oscillator for the PWM mode. This pin contains an internal pull down resistor.
B2	GND A	Analog Ground	Ground connection for the Analog Section of the IC. This is the GND for the FB, Ref, Sync, CB, and SHD pins.
B3	FB	Analog Input	Feedback Voltage from the Output of the Power Supply.
C1	SHD	Analog Input	Enable for Switching Regulator. This Pin is Active High to enable the NCP1510A. The SHD Pin has an internal pull down resistor to force the converter off if this pin is not connected to the external circuit.
C2	CB1	Analog Input	Selects V _{out} . This pin contains an internal pull up resistor.
C3	CB0	Analog Input	Selects V _{out} . This pin contains an internal pull down resistor.

NCP1510A

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Maximum Voltage All Pins	$V_{\max}$	5.5	V
Maximum Operating Voltage All Pins	$V_{\max}$	5.2	V
Thermal Resistance, Junction-to-Air (Note 1)	$R_{\theta JA}$	159	°C/W
Operating Ambient Temperature Range	T_A	–30 to 85	°C
ESD Withstand Voltage	V_{ESD}	Human Body Model (Note 2) Machine Model (Note 2)	V
		> 2500 > 150	
Moisture Sensitivity	MSL	Level 1	
Storage Temperature Range	T_{stg}	–55 to 150	°C
Junction Operating Temperature	T_J	–30 to 125	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- For the 9-Pin Micro Bump package, the $R_{\theta JA}$ is highly dependent of the PCB heatsink area. $R_{\theta JA} = 159^{\circ}\text{C/W}$ with 50 mm² PCB heatsink area.
- This device series contains ESD protection and exceeds the following tests:
Human Body Model, 100 pF discharge through a 1.5 k Ω following specification JESD22/A114.
Machine Model, 200 pF discharged through all pins following specification JESD22/A115.
Latchup as per JESD78 Class II: > 100 mA.

NCP1510A

ELECTRICAL CHARACTERISTICS ($V_{in} = 3.6\text{ V}$, $V_o = 1.57\text{ V}$, $T_A = 25^\circ\text{C}$, $F_{syn} = 600\text{ kHz}$ 50% Duty Cycle square wave for PWM mode; $T_A = -30$ to 85°C for Min/Max values, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit

V_{CC} Pin

Quiescent Current of Sync Mode, $I_{out} = 0\text{ mA}$	Iq PWM	–	175	–	μA
Quiescent Current of PWM Mode, $I_{out} = 0\text{ mA}$	Iq PWM	–	185	–	μA
Quiescent Current of Pulsed Mode, $I_{out} = 0\text{ mA}$	Iq Pulsed	–	14	–	μA
Quiescent Current, SHD Low	Iq Off	–	0.1	0.5	μA
Input Voltage Range (Note 3)	V_{in}	2.5	–	5.2	V

Sync Pin

Input Voltage	Vsync	–0.3	–	$V_{cc} + 0.3$	V
Frequency Operational Range	Fsync	500	600	1000	kHz
Minimum Synchronization Pulse Width	Dcsync Min	–	30	–	%
Maximum Synchronization Pulse Width	Dcsync Max	–	70	–	%
SYNC “H” Voltage Threshold	Vsynch	–	920	1200	mV
SYNC “L” Voltage Threshold	Vsyncl	400	830	–	mV
SYNC “H” Input Current, Vsync = 3.6 V	Isynch	–	2.2	–	μA
SYNC “L” Input Current, Vsync = 0 V	Isyncl	–0.5	–	–	μA

Output Level Selection Pins

Input Voltage	Vcb	–0.3	–	$V_{cc} + 0.3$	V
CB0, CB1 “H” Voltage Threshold	Vcb h	–	920	1200	mV
CB0, CB1 “L” Voltage Threshold	Vcb l	400	830	–	mV
CB0 “H” Input Current, CB = 3.6 V	Icb0 h	–	2.2	–	μA
CB0 “L” Input Current, CB = 0 V	Icb0 l	–0.5	–	–	μA
CB1 “H” Input Current, CB = 3.6 V	Icb1 h	–	0.3	1.0	μA
CB1 “L” Input Current, CB = 0 V	Icb1 l	–	–2.2	–	μA

Shutdown Pin

Input Voltage	Vshd	–0.3	–	$V_{cc} + 0.3$	V
SHD “H” Voltage Threshold	Vshd h	–	920	1200	mV
SHD “L” Voltage Threshold	Vshd l	400	830	–	mV
SHD “H” Input Current, SHD = 3.6 V	Ishd h	–	2.2	–	μA
SHD “L” Input Current, SHD = 0 V	Ishd l	–0.5	–	–	μA

Feedback Pin

Input Voltage	Vfb	–0.3	–	$V_{cc} + 0.3$	V
Input Current, Vfb = 1.57 V	Ifb	–	5.0	7.5	μA

3. Recommended maximum input voltage is 5 V when the device frequency is synchronized with an external clock signal.

NCP1510A

ELECTRICAL CHARACTERISTICS ($V_{in} = 3.6\text{ V}$, $V_o = 1.57\text{ V}$, $T_A = 25^\circ\text{C}$, $F_{syn} = 600\text{ kHz}$ 50% Duty Cycle square wave for PWM mode; $T_A = -30\text{ to }85^\circ\text{C}$ for Min/Max values, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Sync PWM Mode Characteristics					
Switching P-FET Current Limit	I_{lim}	–	800	–	mA
Minimum On Time	$T_{on\ min}$	–	75	–	nsec
R_{dson} Switching P-FET and N_FET	R_{dson}	–	0.23	–	Ω
Switching P-FET and N-FET Leakage Current	I_{leak}	–	0	1.0	μA
Output Overvoltage Threshold	V_o	–	3.0	–	%
Feedback Voltage Accuracy, V_{out} Set = 1.05 V $C_{B0} = L$, $C_{B1} = L$	V_{out}	1.018	1.050	1.082	V
Feedback Voltage Accuracy, V_{out} Set = 1.35 V, $C_{B0} = L$, $C_{B1} = H$	V_{out}	1.309	1.350	1.391	V
Feedback Voltage Accuracy, V_{out} Set = 1.57 V, $C_{B0} = H$, $C_{B1} = H$	V_{out}	1.523	1.570	1.617	V
Feedback Voltage Accuracy, V_{out} Set = 1.8 V, $C_{B0} = H$, $C_{B1} = L$	V_{out}	1.746	1.800	1.854	V
Load Transient Response 10 to 100 mA Load Step	V_{out}	–	35	–	mV
Line Transient Response, $I_{out} = 100\text{ mA}$ 3.0 to 3.6 V_{in} Line Step	V_{out}	–	± 10	–	mVpp

PWM Mode with Internal Oscillator Characteristics

Switching P-FET Current Limit	I_{lim}	–	800	–	mA
Minimum On Time	$T_{on\ min}$	–	75	–	nsec
Internal Oscillator Frequency	F_{osc}	700	900	1200	kHz
R_{dson} Switching P-FET and N_FET	R_{dson}	–	0.23	–	Ω
Switching P-FET and N-FET Leakage Current	I_{leak}	–	0	1.0	μA
Output Overvoltage Threshold	V_o	–	5.0	–	%
Feedback Voltage Accuracy, V_{out} Set = 1.05 V, $C_{B0} = L$, $C_{B1} = L$	V_{out}	1.018	1.050	1.082	V
Feedback Voltage Accuracy, V_{out} Set = 1.35 V, $C_{B0} = L$, $C_{B1} = H$	V_{out}	1.309	1.350	1.391	V
Feedback Voltage Accuracy, V_{out} Set = 1.57 V, $C_{B0} = H$, $C_{B1} = H$	V_{out}	1.523	1.570	1.617	V
Feedback Voltage Accuracy, V_{out} Set = 1.8 V, $C_{B0} = H$, $C_{B1} = L$	V_{out}	1.746	1.800	1.854	V
Load Transient Response 10 to 100 mA Load Step	V_{out}	–	35	–	mV
Line Transient Response, $I_{out} = 100\text{ mA}$ 3.0 to 3.6 V_{in} Line Step	V_{out}	–	± 10	–	mVpp

Pulsed Mode Characteristics

On Time	T_{on}	–	660	–	nsec
Output Ripple Voltage, $I_{out} = 100\ \mu\text{A}$	V_{out}	–	22	–	mV
Feedback Voltage Accuracy, V_{out} Set = 1.05 V, $C_{B0} = L$, $C_{B1} = L$	V_{out}	0.998	1.050	1.102	V
Feedback Voltage Accuracy, V_{out} Set = 1.35 V, $C_{B0} = L$, $C_{B1} = H$	V_{out}	1.289	1.350	1.411	V
Feedback Voltage Accuracy, V_{out} Set = 1.57 V, $C_{B0} = H$, $C_{B1} = H$	V_{out}	1.503	1.570	1.637	V
Feedback Voltage Accuracy, V_{out} Set = 1.8 V, $C_{B0} = H$, $C_{B1} = L$	V_{out}	1.726	1.800	1.874	V

NCP1510A

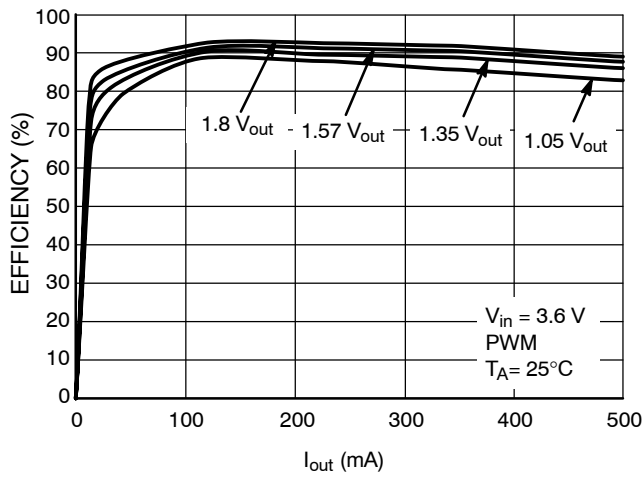


Figure 4. Efficiency vs. Output Current in PWM Mode

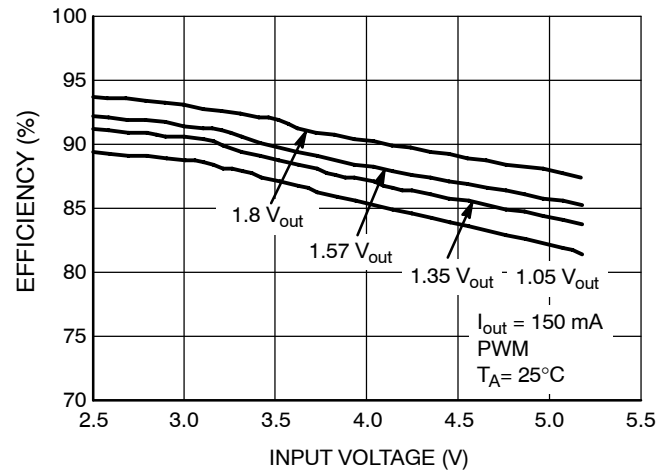


Figure 5. Efficiency vs. Input Voltage in PWM Mode

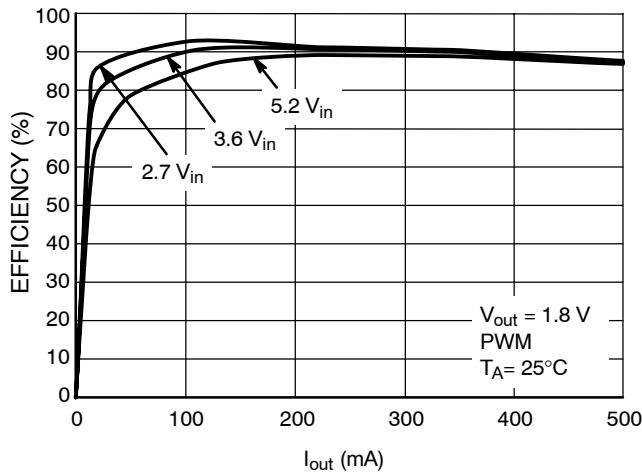


Figure 6. Efficiency vs. Output Current at Different Input Voltage

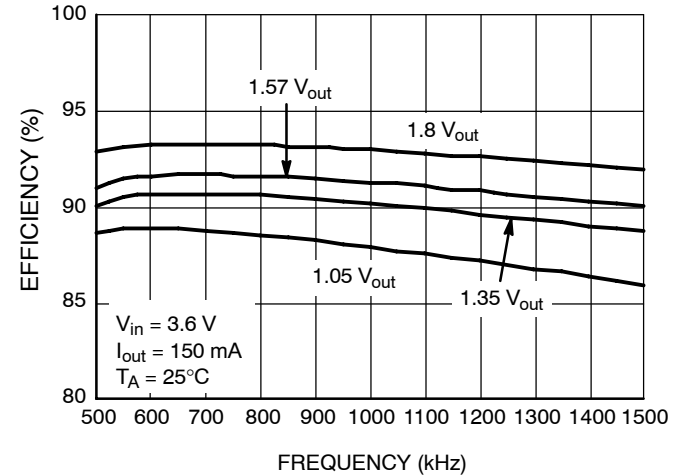


Figure 7. Efficiency vs. Frequency at $I_{out} = 150$ mA

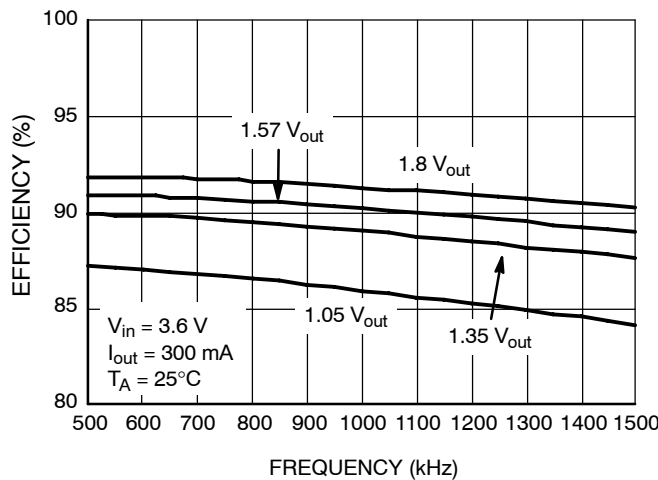


Figure 8. Efficiency vs. Frequency at $I_{out} = 300$ mA

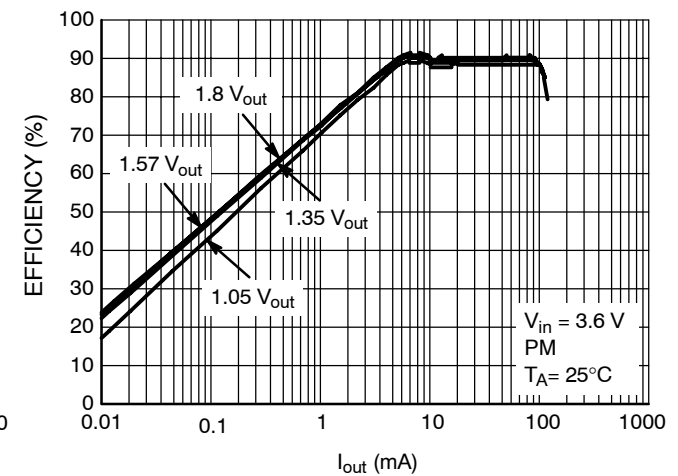


Figure 9. Efficiency vs. Output Current in Pulsed Mode

NCP1510A

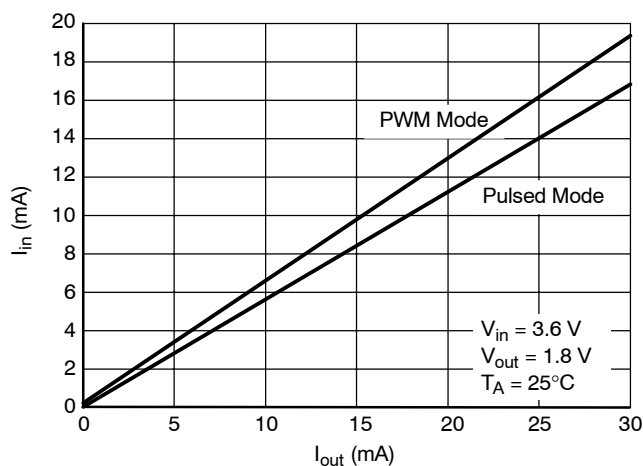


Figure 10. Input Current Comparison

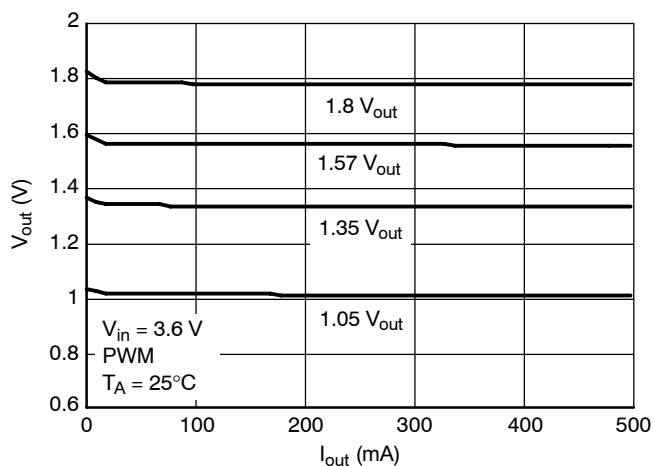


Figure 11. Output Voltage vs. Output Current

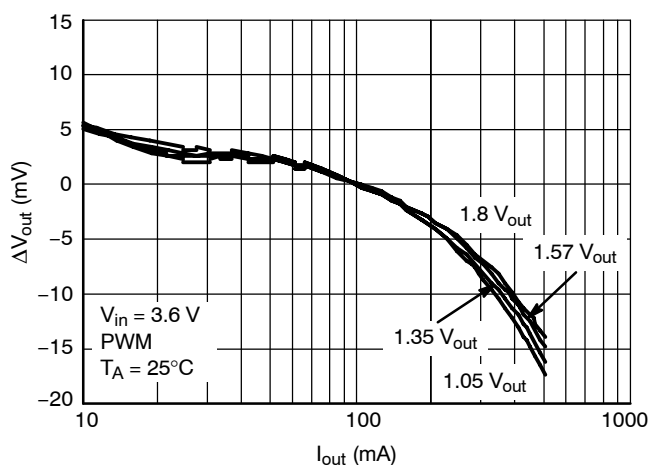


Figure 12. Load Regulation in PWM Mode

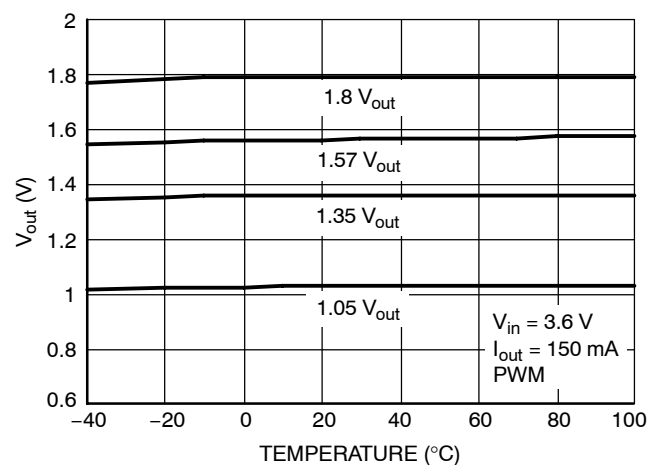


Figure 13. Output Voltage vs. Temperature

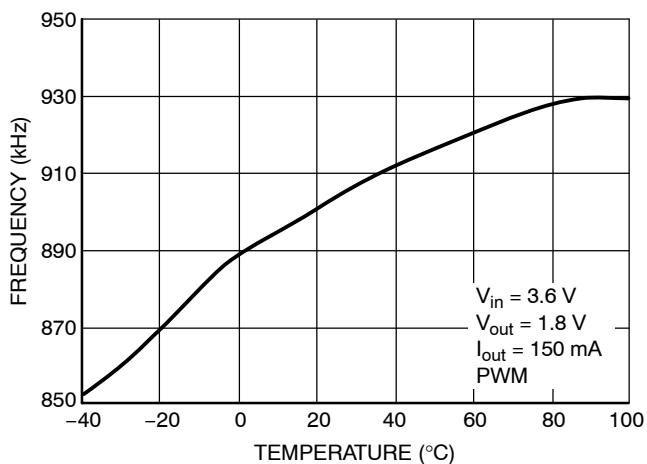


Figure 14. Oscillator Frequency vs. Temperature

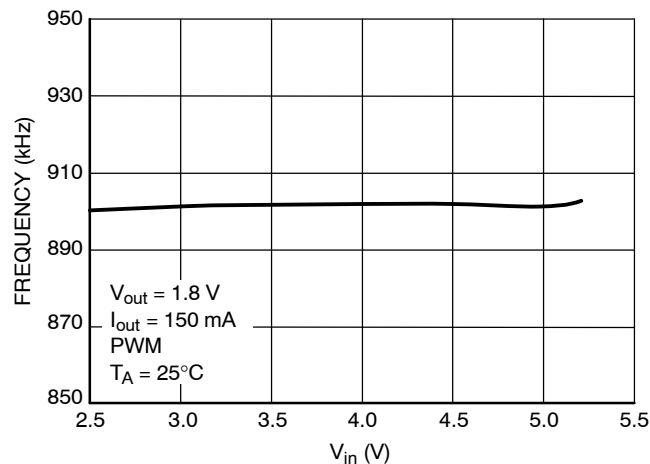


Figure 15. Oscillator Frequency vs. Input Voltage

NCP1510A

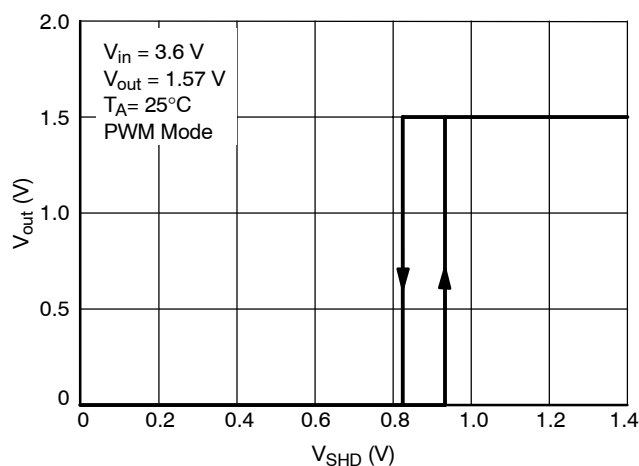


Figure 16. Output Voltage vs. Shutdown Pin Voltage

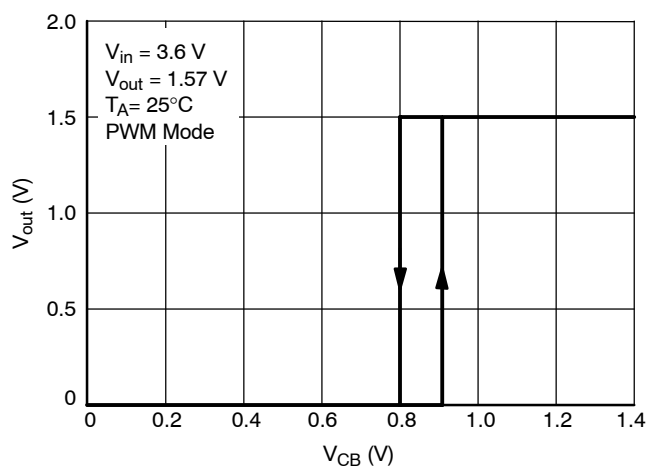


Figure 17. Transition Level of CB Pins

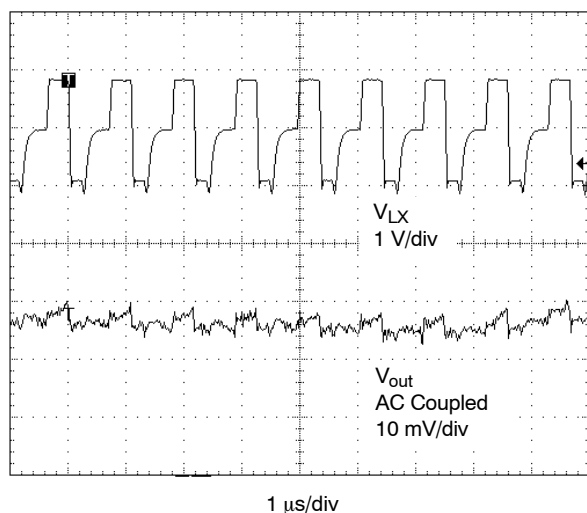


Figure 18. Light Load PWM Switching Waveform
 $(V_{in} = 3.6 \text{ V}, V_{out} = 1.8 \text{ V}, I_{out} = 30 \text{ mA})$

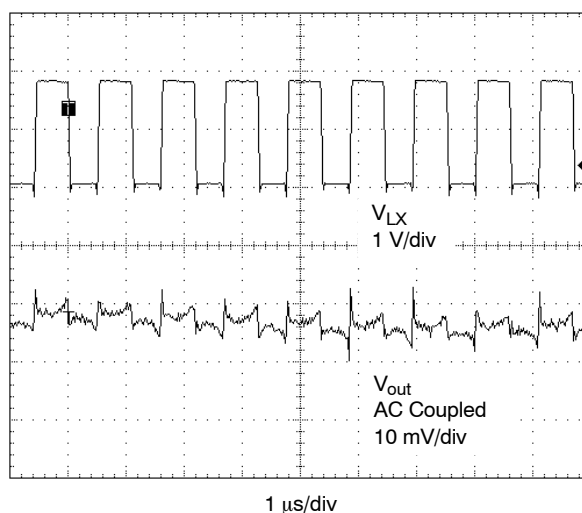


Figure 19. Heavy Load PWM Switching Waveform
 $(V_{in} = 3.6 \text{ V}, V_{out} = 1.8 \text{ V}, I_{out} = 300 \text{ mA})$

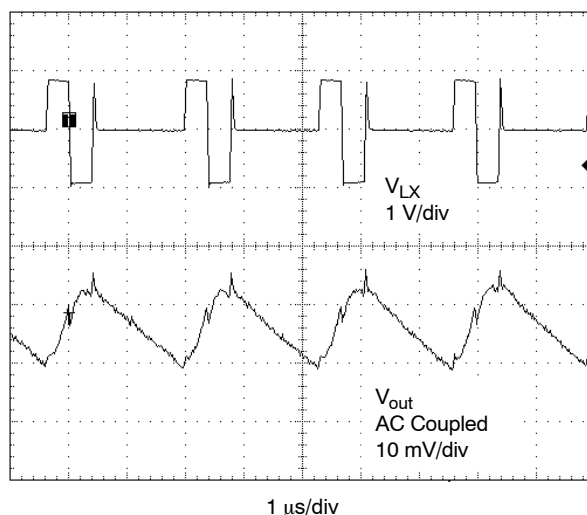


Figure 20. Pulsed Mode Switching Waveform
 $(V_{in} = 3.6 \text{ V}, V_{out} = 1.8 \text{ V}, I_{out} = 30 \text{ mA})$

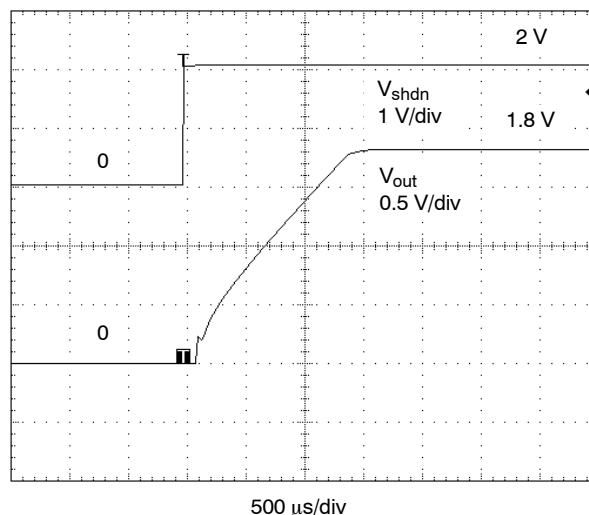


Figure 21. Soft-Start
 $(V_{in} = 3.6 \text{ V}, V_{out} = 1.8 \text{ V}, I_{out} = 150 \text{ mA})$

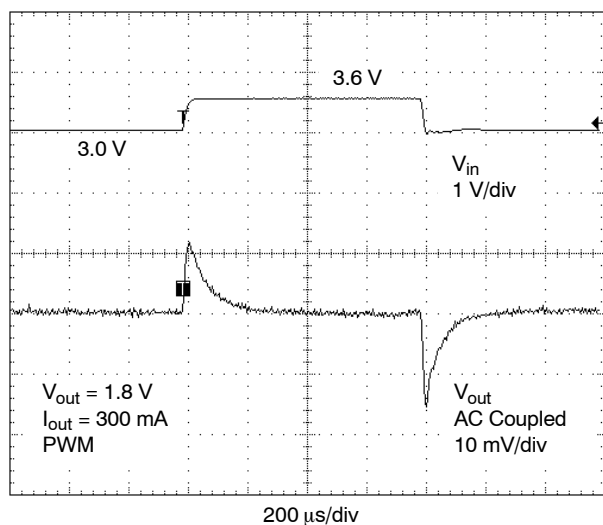


Figure 22. Line Transient Response for PWM

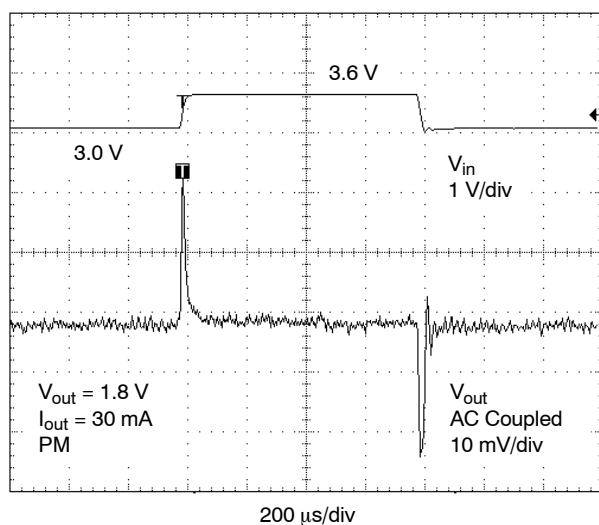


Figure 23. Line Transient Response for PM

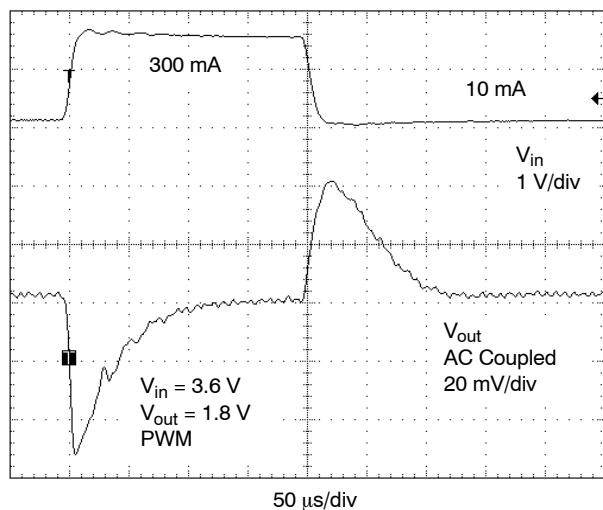


Figure 24. Load Transient Response

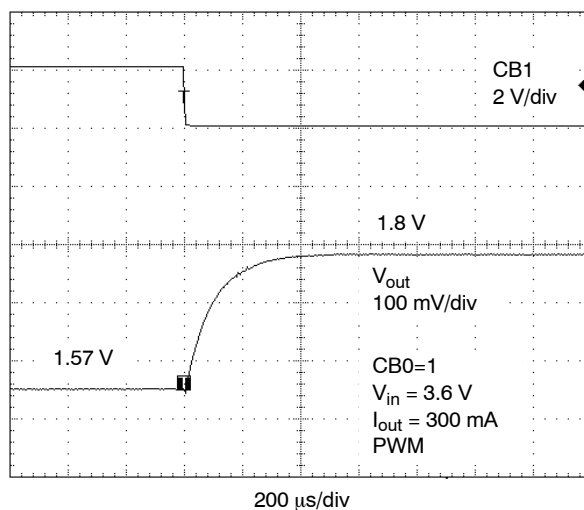


Figure 25. Output Voltage Transition from 1.57 V to 1.8 V

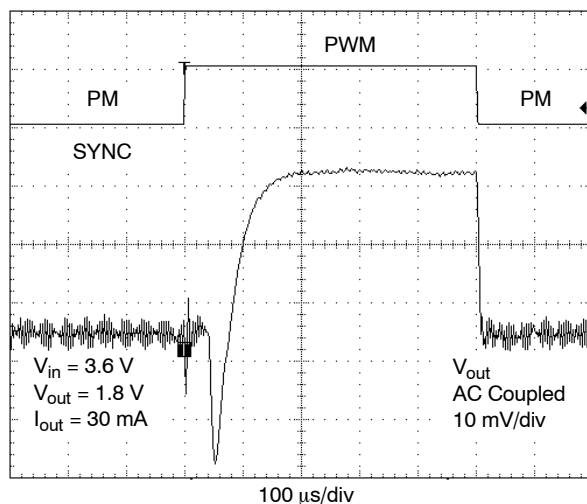


Figure 26. Transition between PWM and PM

DETAILED OPERATING DESCRIPTION

Overview

The NCP1510A is a monolithic micro-power high frequency PWM step-down DC-DC converter specifically optimized for applications requiring high efficiency and a small PCB footprint such as portable battery powered products. It integrates synchronous rectification to improve efficiency as well as eliminate the external Schottky diode. High switching frequency allows for a low profile inductor and capacitors to be used. Four digital selectable output voltages (1.05, 1.35, 1.57 and 1.8 V) can be generated from the input supply that can range from 2.7–5.2 V. All loop compensation is integrated as well further reducing the external component count as well.

The DC-DC converter has two operating modes (normal PWM, pulsed switching), which are intended to allow for optimum efficiency under either light (up to 30 mA) or heavy loads. The user determines the operating mode by controlling the SYNC input. In addition the SYNC input can be used to synchronize the PWM to an external system clock signal in the range of 500–1000 kHz.

PWM Operating Mode

The NCP1510A can be set to current mode PWM operation by connecting SYNC pin to V_{CC} . In this mode, the output voltage is regulated by modulating the on-time pulse width of the main switch Q1 at a fixed frequency of 1.0 MHz. The switching of the PMOS Q1 is controlled by a flip-flop driven by the internal oscillator and a comparator that compares the error signal from an error amplifier with the sum of the sensed current signal and compensation ramp. At the beginning of each cycle, the main switch Q1 is turned ON by the rising edge of the internal oscillator clock. The inductor current ramps up until the sum of the current sense signal and compensation ramp becomes higher than the error voltage amplifier. Once this has occurred, the PWM comparator resets the flip-flop, Q1 is turned OFF and the synchronous switch Q2 is turned ON. Q2 replaces the external Schottky diode to reduce the conduction loss and improve the efficiency. To avoid overall power loss, a certain amount of dead time is introduced to ensure Q1 is completely turned OFF before Q2 is being turned ON.

In continuous conduction mode (CCM), Q1 is turned ON after Q2 is completely turned OFF to start a new clock cycle. In discontinuous conduction mode (DCM), the zero crossing comparator (ZLC) will turn off Q2 when the inductor current drops to zero.

Overvoltage Protection

The overvoltage protection circuit is present in PWM mode to prevent the output voltage from going too high under light load or fast load transient conditions. The output overvoltage threshold is 5% above nominal set value. If the output voltage rises above 5% of the nominal

value, the OVP comparator is activated and switch Q1 is turned OFF. Switching will continue when the output voltage falls below the threshold of OVP comparator.

Pulsed Mode (PM)

Under light load conditions (< 30 mA), The NCP1510A can be configured to enter a low current pulsed mode operation to reduce power consumption. This is accomplished by applying a logic LOW to the SYNC pin. The output regulation is implemented by pulse frequency modulation. If the output voltage drops below the threshold of PM comparator (typically $V_{nom}-2\%$), a new cycle will be initiated by the PM comparator to turn on the switch Q1. Q1 remains ON until the peak inductor current reaches 200 mA (nom). Then ILIM comparator goes high to switch off Q1. After a short dead time delay, switch rectifier Q2 is turn ON. The zero crossing comparator will detect when the inductor current drops to zero and send the signal to turn off Q2. The output voltage continues to decrease through discharging the output capacitor. When the output voltage falls below the threshold of the PM comparator again, a new cycle starts immediately.

Cycle-by-Cycle Current Limit

From the block diagram (Figure 3), an ILIM comparator is used to realize cycle-by-cycle current limit protection. The comparator compares the LX pin voltage with the reference voltage from the SENFET, which is biased by a constant current. If the inductor current reaches the limit, the ILIM comparator detects the LX voltage falling below the reference voltage from the SENFET and releases the signal to turn off the switch Q1. The cycle-by-cycle current limit is set at 800 mA (nom) in PWM and 200 mA in PM.

Frequency Synchronization and Operating Mode Selection

The SYNC pin can also be used for frequency synchronization by connecting it with an external clock signal. It operates in PWM mode when synchronized to an external clock. The switching cycle initiates by the rising edge of the clock. The 500 kHz to 1000 kHz synchronization clock signal should be between 0.4 V and 1.2 V.

Gating on and off the clock, the SYNC pin can also be used to select between PM and PWM modes. It allows efficient dynamical power management by adjusting the converter operation to the specific system requirement. Set SYNC pin low to select PM mode at light load conditions (up to 30 mA) and set SYNC pin high or connect with external clock to select PWM mode at heavy load condition to achieve optimum efficiency. Table 1 shows the mode selection with three different SYNC pin states.

Table 1. Operating Mode Selection

SYNC Pin State	Operating Mode
LOW	Pulsed Mode (PM)
HIGH	PWM, 1 MHz Switch Frequency
CLOCK	PWM, Frequency Synchronization

Output Voltage Selection

The output voltage is digitally programmed to one of four voltage levels depending on the logic state of CB0 and CB1. Therefore if the NCP1510A's load, such as a digital cellular phone's baseband processor, supports dynamic power management, the device can lower or raise its core voltage under software control. When combined with the pulsed current mode function in low load situations, this active voltage management further stretches the useful operating life of the handset battery between charges.

The output voltage levels are listed in Table 2. The CB0 has a pull down resistor and the CB1 has a pullup resistor. The default output voltage is 1.35 V when CB0 and CB1 are floating.

Table 2. Truth Table for CB0 and CB1 with the corresponding output voltage

CB0	CB1	Vout(V)
0	0	1.05
0	1	1.35
1	1	1.57
1	0	1.8

Soft-Start

The NCP1510A uses soft-start to limit the inrush current when the device is initially powered up or enabled. Soft-start is implemented by gradually increasing the reference voltage until it reaches the full reference voltage. During startup, a pulsed current source charges the internal soft-start capacitor to provide gradually increasing reference voltage for the PWM loop. When the voltage across the capacitor ramps up to the nominal reference voltage, the pulsed current source will be switched off and the reference voltage will switch to the regular reference voltage.

Shutdown Mode

When the SHD pin has a voltage applied of less than 0.4 V, the NCP1510A will be disabled. In shutdown mode, the internal reference, oscillator and most of the control circuitries are turned off. Therefore, the typical current consumption will be 0.1 μ A (typical value).

Applying a voltage above 1.2 V to SHD pin will enable the device for normal operation. The device will go through soft-start to normal operation.

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. If the junction temperature exceeds 160°C, the device shuts down. In this mode switch Q1 and Q2 and the control circuits are all turned off. The device restarts in soft-start after the temperature drops below 135°C. This feature is provided to prevent catastrophic failures from accidental device overheating and it is not intended as a substitute for proper heatsinking.

APPLICATIONS INFORMATION

Component Selection

Input Capacitor Selection

In PWM operating mode, the input current is pulsating with large switching noise. Using an input bypass capacitor reduces the peak current transients drawn from the input supply source, thereby reducing switching noise significantly. The capacitance needed for the input bypass capacitor depends on the source impedance of the input supply. The RMS capacitor current is calculated as:

$$I_{RMS} \approx I_O \sqrt{D \cdot D'} \quad (\text{eq. 1})$$

where:

D = duty cycle, which equals V_{out}/V_{in} , and $D' = 1 - D$.

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is $I_{O,max}/2$.

A low profile ceramic capacitor of 10 μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to the V_{CC} pin.

Inductor Value Selection

Selecting the proper inductor value is based on the desired ripple current. The relationship between the inductance and the inductor ripple current is given by the equation below.

$$\Delta i_L = \frac{V_{out}}{L f_s} \left(1 - \frac{V_{out}}{V_{in}} \right) \quad (\text{eq. 2})$$

The DC current of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. For NCP1510A, the compensation is internally fixed and a fixed 6.8 μH inductor is needed for most of the applications. For better efficiency, choose a low DC resistance inductor.

Output Capacitor Selection

Selecting the proper output capacitor is based on the desired output ripple voltage. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output ripple voltage is given by:

$$\Delta V_C = \Delta i_L \cdot \left(\text{ESR} + \frac{1}{4f_s C_{out}} \right) \quad (\text{eq. 3})$$

The RMS output capacitor current is given by:

$$I_{RMS}(C_{out}) = \frac{V_O \cdot (1 - D)}{2\sqrt{3} \cdot L \cdot f_s} \quad (\text{eq. 4})$$

Where f_s is the switching frequency and ESR is the effective series resistance of the output capacitor. A low ESR, 22 μF ceramic capacitor is recommended for NCP1510A in most of applications. For example, with TDK C2012X5R0J226 output capacitor, the output ripple is less than 10 mV at 300 mA.

Design Example

As a design example, assume that the NCP1510A is used in a single lithium-ion battery application. The input voltage, V_{in} , is 3.0 V to 4.2 V. Output condition is V_{out} at 1.8 V with a typical load current of 120 mA and a maximum of 300 mA. For NCP1510A, the inductor has a predetermined value, 6.8 μH . The inductor ESR will factor into the overall efficiency of the converter. The inductor needs to be selected by the required peak current.

Equation 5 is the basic equation for an inductor and describes the voltage across the inductor. The inductance value determines the slope of the current of the inductor.

$$\frac{V_L}{L} = \frac{di_L}{dt} \quad (\text{eq. 5})$$

Equation 5 is rearranged to solve for the change in current for the on-time of the converter in Continuous Conduction Mode.

$$\begin{aligned} i_{L, pk-pk} &= \frac{(V_{in} - V_{out})}{L} \cdot DT_s \\ &= \frac{(V_{in} - V_{out})}{L} \cdot \frac{V_{in}}{V_{out}} \cdot \frac{1}{f_s} \quad (\text{eq. 6}) \\ i_{L, max} &= I_{O, max} + \frac{\Delta i_{L, pk-pk}}{2} \end{aligned}$$

Utilizing Equations 6, the peak-to-peak inductor current is calculated using the following worst-case conditions.

$$V_{in, max} = 4.2 \text{ V}, V_{out} = 1.8 \text{ V}, f_s = 1 \text{ MHz}-20\%,$$

$$L = 6.8 \mu\text{H}-10\%, i_{L, pk-pk} = 211 \text{ mA}, i_{L, max} = 405 \text{ mA}$$

Therefore, the inductor must have a maximum current exceeding 405 mA.

Since the compensation is fixed internally in the IC, the input and output capacitors as well as the inductor have a predetermined value too: $C_{in} = 10 \mu\text{F}$ and $C_{out} = 22 \mu\text{F}$. Low ESR capacitors are needed for best performance. Therefore, ceramic capacitors are recommended.

NCP1510A

PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise and unwanted feedback that can affect the performance of the converter. Hints suggested below can be used as a guideline in most situations.

1. Use star-ground connection to connect the IC ground nodes and capacitor GND nodes together at one point. Keep them as close as possible, and then connect this to the ground plane through several vias. This will reduce noise in the ground plane by preventing the switching currents from flowing through the ground plane.

2. Place the power components (i.e., input capacitor, inductor and output capacitor) as close together as possible

for best performance. All connecting traces must be short, direct, and wide to reduce voltage errors caused by resistive losses through the traces.

3. Separate the feedback path of the output voltage from the power path. Keep this path close to the NCP1510A circuit. And also route it away from noisy components. This will prevent noise from coupling into the voltage feedback trace.

4. Place the DC-DC converter away from noise sensitive circuitry, such as RF circuits.

The following shows the NCP1510A demo board layout and bill of materials:

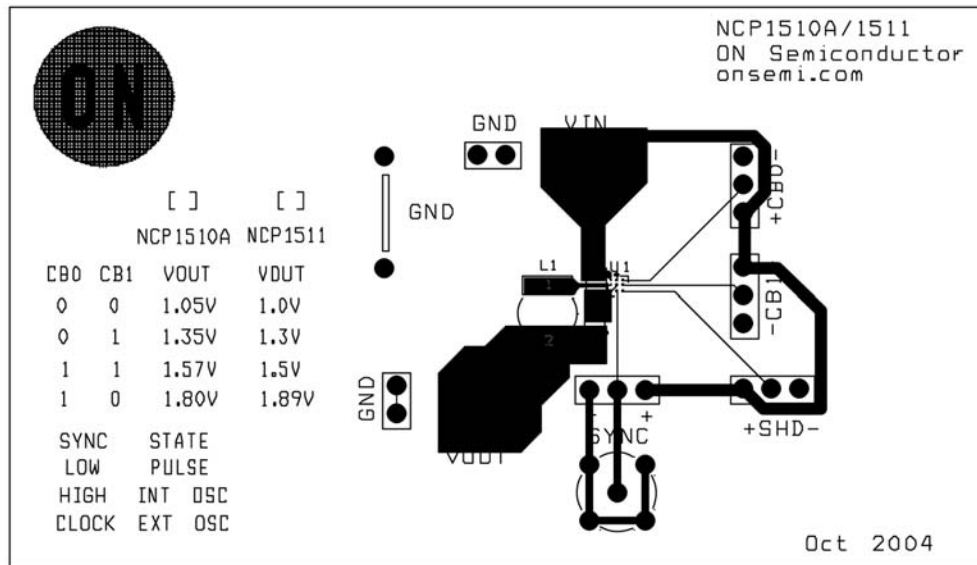


Figure 27. Top and Silkscreen Layer

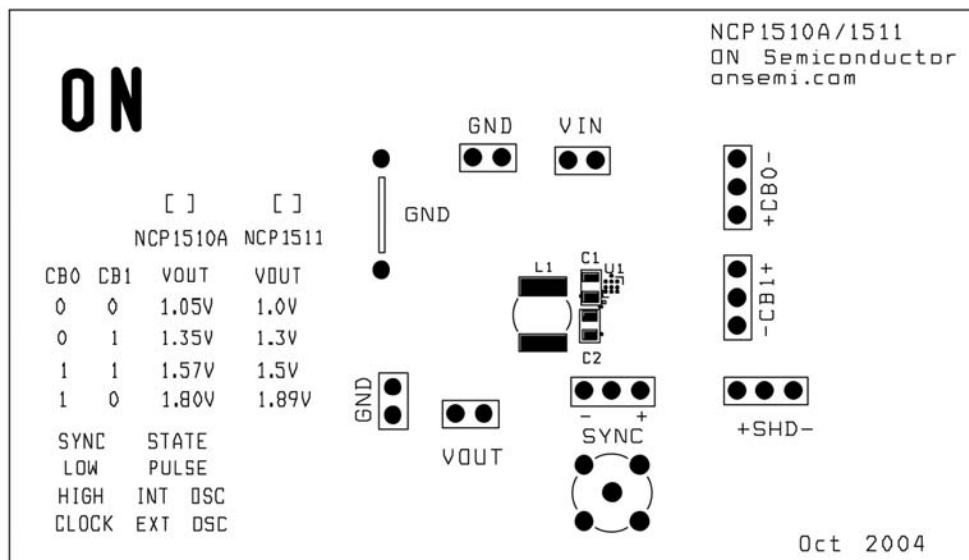


Figure 28. Soldermask Top and Silkscreen Layer

NCP1510A

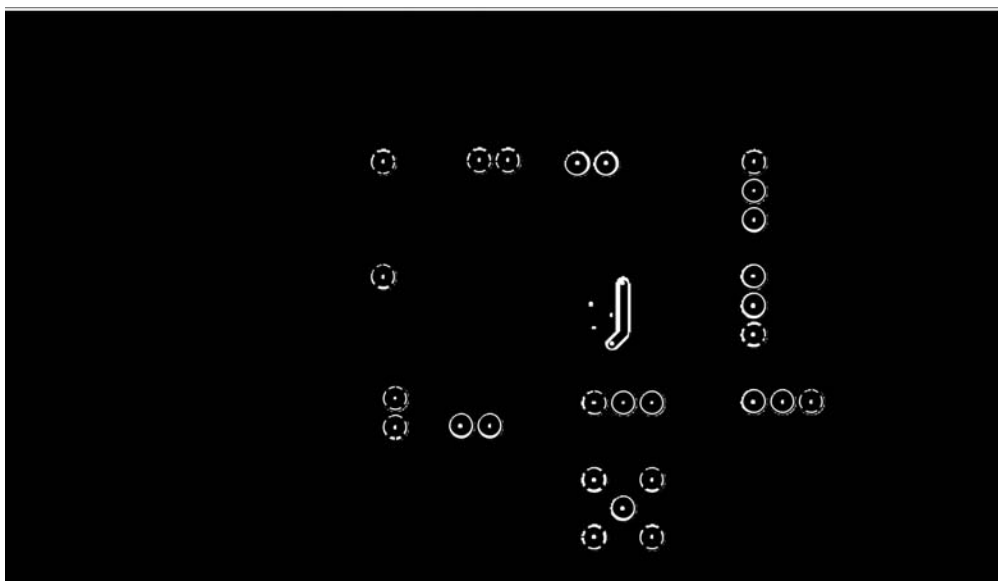


Figure 29. Bottom Layer

Table 3. Bill of Materials

Component	Value	Manufacturer	Part Number	Size (mm)	I _{out} (mA)	ESR (mΩ)
C _{in}	10 μF, X5R, 6.3 V	TDK Murata	C2012X5R0J106 GRM21BR60J106	2.0 x 1.25 x 1.25	–	–
C _{out}	22 μF, X5R, 6.3 V	TDK Murata	C2012X5R0J226 GRM21BR60J226	2.0 x 1.25 x 1.25	–	–
L	6.8 μH	TDK Coilcraft Coilcraft Sumida	VLCF4020–6R8 0805PS–682 LPO4812 CLS4D11	4.0 x 4.0 x 2.0 3.4 x 3.0 x 1.8 4.8 x 4.8 x 1.2 4.9 x 4.9 x 1.2	500** 210* 340* 500**	146 1260 225 220

*Output current calculated from $V_{CC} = 4.2 V_{max}$, $1.5 V_{out}$ and Freq = 700 kHz (1.0 MHz – 20 %).

**Calculated output current from $V_{CC} = 4.2 V_{max}$ and Freq = 700 kHz exceeds 640 mA ($I_{lim} - 20\%$). Therefore maximum output for these conditions shown as 500 mA.

NCP1511

Up to 500 mA, High Efficiency Synchronous Step-Down DC-DC Converter in Chip Scale Package

The NCP1511 step-down PWM DC-DC converter is optimized for portable applications powered from 1-cell Li-ion or 3-cell Alkaline/NiCd/NiMH batteries. This DC-DC converter utilizes a current-mode control architecture for easy compensation and better line regulation. It also uses synchronous rectification to increase efficiency and reduce external part count. The NCP1511 optimizes efficiency in light load conditions when switched from a normal PWM mode to a "pulsed switching" mode. The device also has a built-in oscillator for the PWM circuitry, or it can be synchronized to an external 500 kHz to 1000 kHz clock signal. Finally, it includes an integrated soft-start, cycle-by-cycle current limiting, and thermal shutdown protection. The NCP1511 is available in a chip scale package.

Features

- High Efficiency:
 - 93% for 1.89 V Output at 3.6 V Input and 150 mA Load Current
 - 92% for 1.89 V Output at 3.6 V Input and 300 mA Load Current
- Digital Programmable Output Voltages: 1.0, 1.3, 1.5 or 1.89 V
- Output Current up to 500 mA at $V_{in} = 3.6$ V
- Low Quiescent Current of 14 μ A in Pulsed Switching Mode
- Low 0.1 μ A Shutdown Current
- -30°C to 85°C Operation Temperature
- Ceramic Input/Output Capacitor
- 9 Pin Chip Scale Package
- Pb-Free Package is Available

Applications

- Cellular Phones, Smart Phones and PDAs
- Digital Still Cameras
- MP3 Players and Portable Audio Systems
- Wireless and DSL Modems
- Portable Equipment

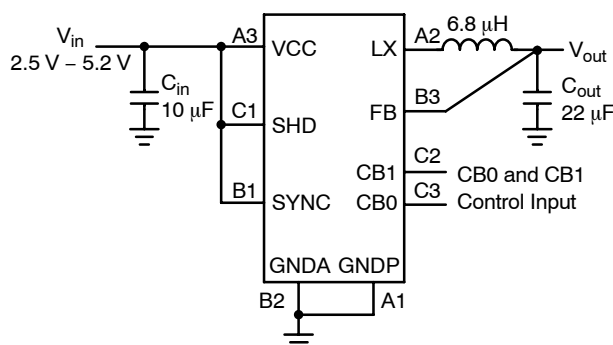


Figure 1. Typical Application Circuit



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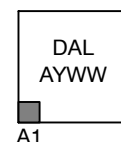


A1

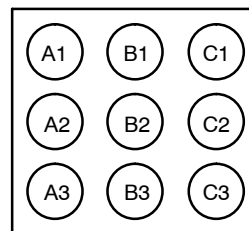
9 PIN
MICRO BUMP
FC SUFFIX
CASE 499AC

XX = Device Code
A = Assembly Location
Y = Year
WW = Work Week

MARKING DIAGRAM



PIN CONNECTIONS



(Bottom View)

Pin: A1 - GNDD
A2 - LX
A3 - VCC
B1 - SYNC
B2 - GNDA
B3 - FB
C1 - SHD
C2 - CB1
C3 - CB0

ORDERING INFORMATION

Device	Package	Shipping†
NCP1511FCT1	Micro Bump	3000 Tape & Reel
NCP1511FCT1G	Micro Bump (Pb-Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

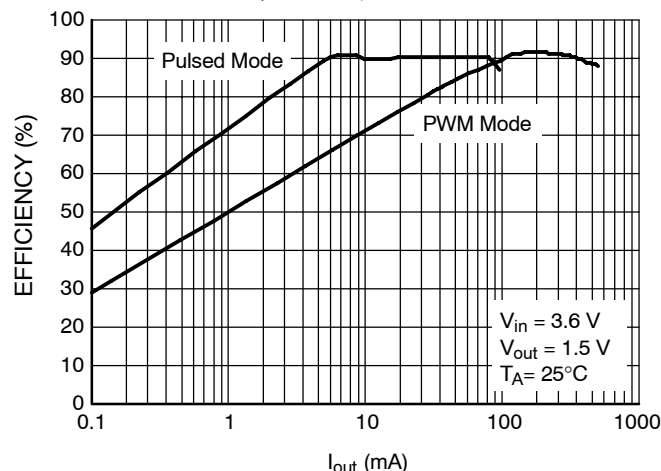


Figure 2. Efficiency vs. Output Current

NCP1511

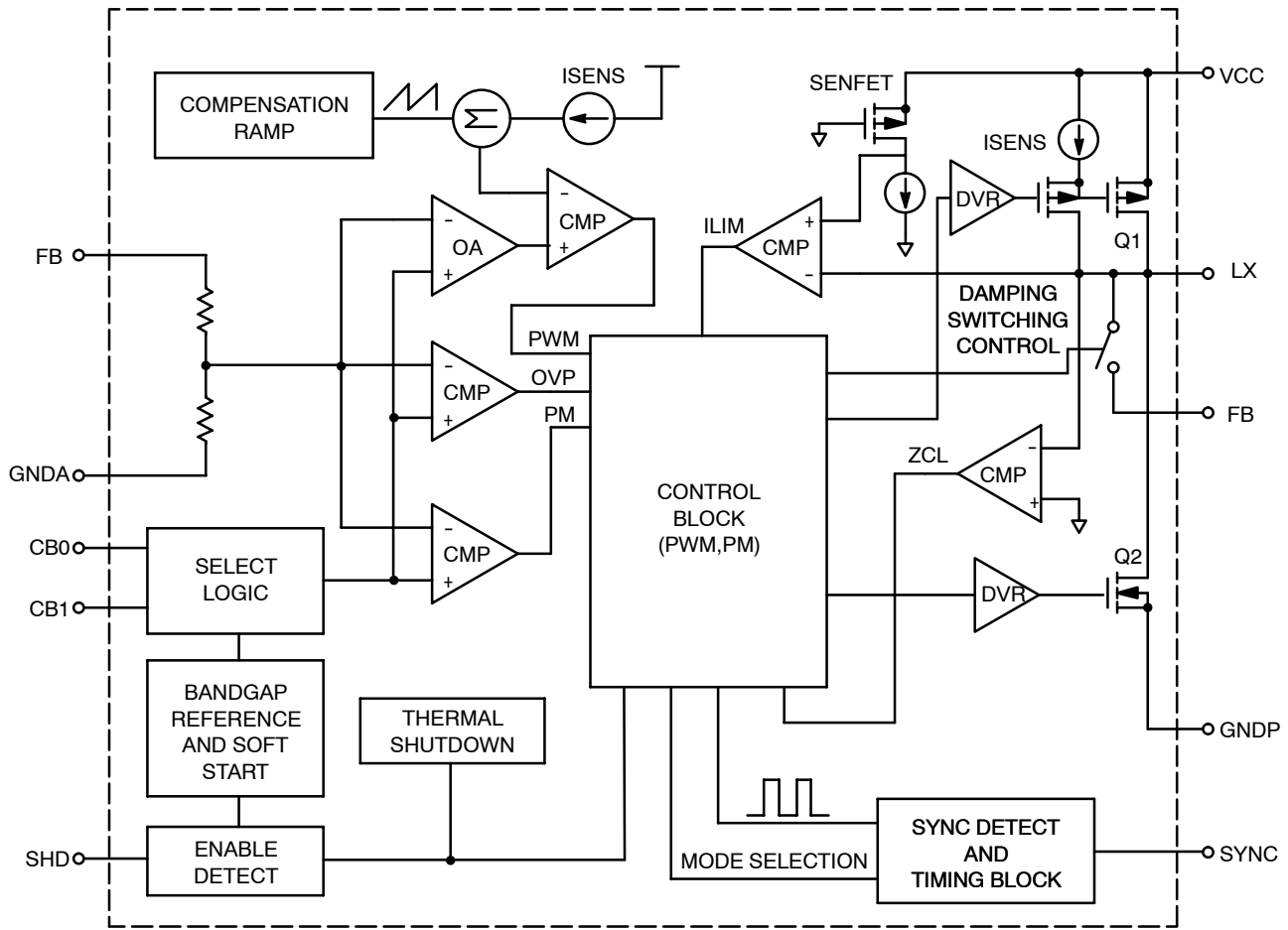


Figure 3. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Type	Description
A1	GNDP	Power Ground	Ground Connection for the NFET Power Stage.
A2	LX	Analog Output	Connection from Power Pass Elements to the Inductor.
A3	V _{CC}	Analog Input	Power Supply Input for Power and Analog V _{CC} .
B1	SYNC	Analog Input	Synchronization input for the PWM converter. If a clock signal is present, the converter uses the rising edge for the turn on. If this pin is low, the converter is in the Pulsed mode. If this pin is high, the converter uses the internal oscillator for the PWM mode. This pin contains an internal pull down resistor.
B2	GND	Analog Ground	Ground connection for the Analog Section of the IC. This is the GND for the FB, Ref, Sync, CB, and SHD pins.
B3	FB	Analog Input	Feedback Voltage from the Output of the Power Supply.
C1	SHD	Analog Input	Enable for Switching Regulator. This Pin is Active High to enable the NCP1511. The SHD Pin has an internal pull down resistor to force the converter off if this pin is not connected to the external circuit.
C2	CB1	Analog Input	Selects V _{out} . This pin contains an internal pull up resistor.
C3	CB0	Analog Input	Selects V _{out} . This pin contains an internal pull down resistor.

NCP1511

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Maximum Voltage All Pins	$V_{\max}$	5.5	V
Maximum Operating Voltage All Pins	$V_{\max}$	5.2	V
Thermal Resistance, Junction-to-Air (Note 1)	$R_{\theta JA}$	159	°C/W
Operating Ambient Temperature Range	T_A	–30 to 85	°C
ESD Withstand Voltage	V_{ESD}	Human Body Model (Note 2) > 2500	V
		Machine Model (Note 2) > 150	
Moisture Sensitivity	MSL	Level 1	
Storage Temperature Range	T_{stg}	–55 to 150	°C
Junction Operating Temperature	T_J	–30 to 125	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- For the 9-Pin Micro Bump package, the $R_{\theta JA}$ is highly dependent of the PCB heatsink area. $R_{\theta JA} = 159^{\circ}\text{C/W}$ with 50 mm² PCB heatsink area.
- This device series contains ESD protection and exceeds the following tests:
Human Body Model, 100 pF discharge through a 1.5 k Ω following specification JESD22/A114.
Machine Model, 200 pF discharged through all pins following specification JESD22/A115.
Latchup as per JESD78 Class II: > 100 mA.

NCP1511

ELECTRICAL CHARACTERISTICS ($V_{in} = 3.6\text{ V}$, $V_o = 1.5\text{ V}$, $T_A = 25^\circ\text{C}$, $F_{syn} = 600\text{ kHz}$ 50% Duty Cycle square wave for PWM mode; $T_A = -30$ to 85°C for Min/Max values, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit

VCC Pin

Quiescent Current of Sync Mode, $I_{out} = 0\text{ mA}$	Iq PWM	–	175	–	μA
Quiescent Current of PWM Mode, $I_{out} = 0\text{ mA}$	Iq PWM	–	185	–	μA
Quiescent Current of Pulsed Mode, $I_{out} = 0\text{ mA}$	Iq Pulsed	–	14	–	μA
Quiescent Current, SHD Low	Iq Off	–	0.1	1.0	μA
Input Voltage Range (Note 3)	Vin	2.5	–	5.2	V

Sync Pin

Input Voltage	Vsync	–0.3	–	$V_{cc} + 0.3$	V
Frequency Operational Range	Fsync	500	600	1000	kHz
Minimum Synchronization Pulse Width	Dcsync Min	–	30	–	%
Maximum Synchronization Pulse Width	Dcsync Max	–	70	–	%
SYNC “H” Voltage Threshold	Vsynch	–	920	1200	mV
SYNC “L” Voltage Threshold	Vsyncl	400	830	–	mV
SYNC “H” Input Current, $V_{sync} = 3.6\text{ V}$	Isynch	–	2.2	–	μA
SYNC “L” Input Current, $V_{sync} = 0\text{ V}$	Isyncl	–0.5	–	–	μA

Output Level Selection Pins

Input Voltage	Vcb	–0.3	–	$V_{cc} + 0.3$	V
CB0, CB1 “H” Voltage Threshold	Vcb h	–	920	1200	mV
CB0, CB1 “L” Voltage Threshold	Vcb l	400	830	–	mV
CB0 “H” Input Current, $CB = 3.6\text{ V}$	Icb0 h	–	2.2	–	μA
CB0 “L” Input Current, $CB = 0\text{ V}$	Icb0 l	–0.5	–	–	μA
CB1 “H” Input Current, $CB = 3.6\text{ V}$	Icb1 h	–	0.3	1.0	μA
CB1 “L” Input Current, $CB = 0\text{ V}$	Icb1 l	–	–2.2	–	μA

Shutdown Pin

Input Voltage	Vshd	–0.3	–	$V_{cc} + 0.3$	V
SHD “H” Voltage Threshold	Vshd h	–	920	1200	mV
SHD “L” Voltage Threshold	Vshd l	400	830	–	mV
SHD “H” Input Current, $SHD = 3.6\text{ V}$	Ishd h	–	2.2	–	μA
SHD “L” Input Current, $SHD = 0\text{ V}$	Ishd l	–0.5	–	–	μA

Feedback Pin

Input Voltage	Vfb	–0.3	–	$V_{cc} + 0.3$	V
Input Current, $V_{fb} = 1.5\text{ V}$	Ifb	–	5.0	7.5	μA

Sync PWM Mode Characteristics

Switching P-FET Current Limit	I lim	–	800	–	mA
Minimum On Time	Ton min	–	75	–	nsec
Rdson Switching P-FET and N_FET	Rdson	–	0.23	–	Ω
Switching P-FET and N-FET Leakage Current	Ileak	–	0	1.0	μA
Output Overvoltage Threshold	Vo	–	5.0	–	%

3. Recommended maximum input voltage is 5 V when the device frequency is synchronized with an external clock signal.

NCP1511

ELECTRICAL CHARACTERISTICS (continued) ($V_{in} = 3.6\text{ V}$, $V_o = 1.5\text{ V}$, $T_A = 25^\circ\text{C}$, $F_{syn} = 600\text{ kHz}$ 50% Duty Cycle square wave for PWM mode; $T_A = -30\text{ to }85^\circ\text{C}$ for Min/Max values, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit

Sync PWM Mode Characteristics (continued)

Feedback Voltage Accuracy, V_{out} Set = 1.0 V CB0 = L, CB1 = L	V_{out}	0.950	1.000	1.050	V
Feedback Voltage Accuracy, V_{out} Set = 1.3 V CB0 = L, CB1 = H	V_{out}	1.261	1.300	1.339	V
Feedback Voltage Accuracy, V_{out} Set = 1.5 V CB0 = H, CB1 = H	V_{out}	1.450	1.500	1.550	V
Feedback Voltage Accuracy, V_{out} Set = 1.89 V CB0 = H CB1 = L	V_{out}	1.833	1.890	1.947	V
Load Transient Response 10 to 100 mA Load Step	V_{out}	–	35	–	mV
Line Transient Response, $I_{out} = 100\text{ mA}$ 3.0 to 3.6 V_{in} Line Step	V_{out}	–	± 10	–	mVpp

PWM Mode with Internal Oscillator Characteristics

Switching P-FET Current Limit	I_{lim}	–	800	–	mA
Minimum On Time	$T_{on\ min}$	–	75	–	nsec
Internal Oscillator Frequency	F_{osc}	700	900	1200	kHz
R_{dson} Switching P-FET and N_{FET}	R_{dson}	–	0.23	–	Ω
Switching P-FET and N-FET Leakage Current	I_{leak}	–	0	1.0	μA
Output Overvoltage Threshold	V_o	–	5.0	–	%
Feedback Voltage Accuracy, V_{out} Set = 1.0 V CB0 = L, CB1 = L	V_{out}	0.950	1.000	1.050	V
Feedback Voltage Accuracy, V_{out} Set = 1.3 V CB0 = L, CB1 = H	V_{out}	1.261	1.300	1.339	V
Feedback Voltage Accuracy, V_{out} Set = 1.5 V CB0 = H, CB1 = H	V_{out}	1.450	1.500	1.550	V
Feedback Voltage Accuracy, V_{out} Set = 1.89 V CB0 = H CB1 = L	V_{out}	1.833	1.890	1.947	V
Load Transient Response 10 to 100 mA Load Step	V_{out}	–	35	–	mV
Line Transient Response, $I_{out} = 100\text{ mA}$ 3.0 to 3.6 V_{in} Line Step	V_{out}	–	± 10	–	mVpp

Pulsed Mode Characteristics

On Time	T_{on}	–	660	–	nsec
Output Ripple Voltage, $I_{out} = 100\text{ }\mu\text{A}$	V_{out}	–	22	–	mV
Feedback Voltage Accuracy, V_{out} Set = 1.0 V CB0 = L, CB1 = L	V_{out}	0.930	1.000	1.070	V
Feedback Voltage Accuracy, V_{out} Set = 1.3 V CB0 = L, CB1 = H	V_{out}	1.241	1.300	1.359	V
Feedback Voltage Accuracy, V_{out} Set = 1.5 V CB0 = H, CB1 = H	V_{out}	1.430	1.500	1.570	V
Feedback Voltage Accuracy, V_{out} Set = 1.89 V CB0 = H CB1 = L	V_{out}	1.813	1.890	1.967	V

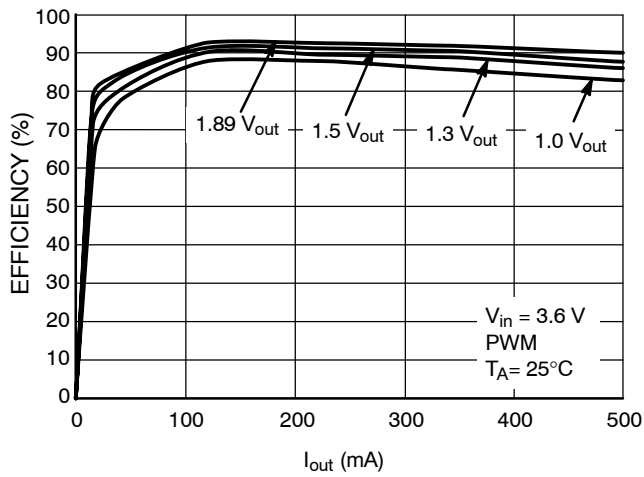


Figure 4. Efficiency vs. Output Current in PWM Mode

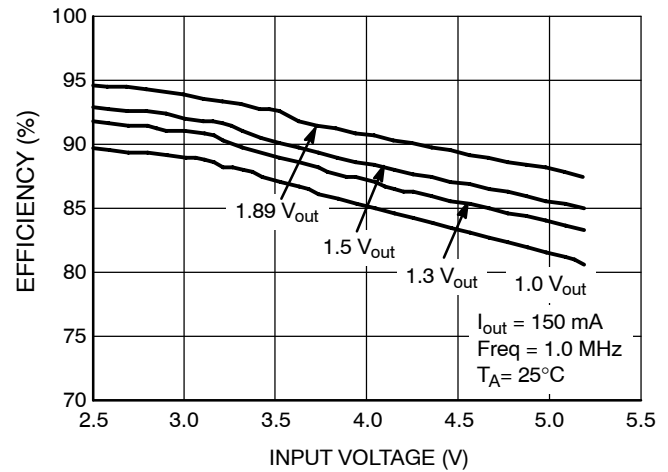


Figure 5. Efficiency vs. Input Voltage in PWM Mode

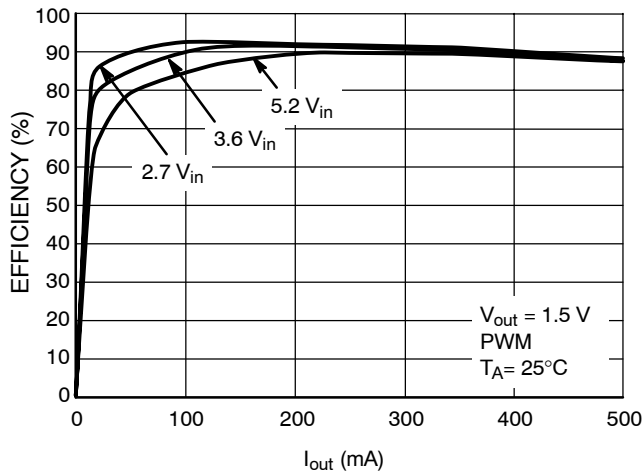


Figure 6. Efficiency vs. Output Current at Different Input Voltage

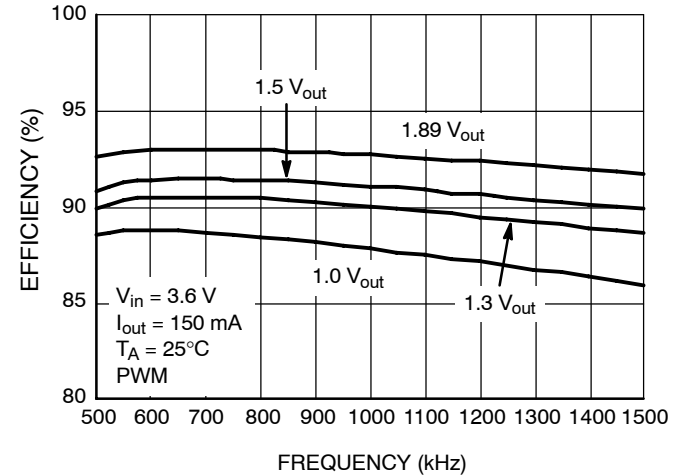


Figure 7. Efficiency vs. Frequency at $I_{out} = 150 \text{ mA}$

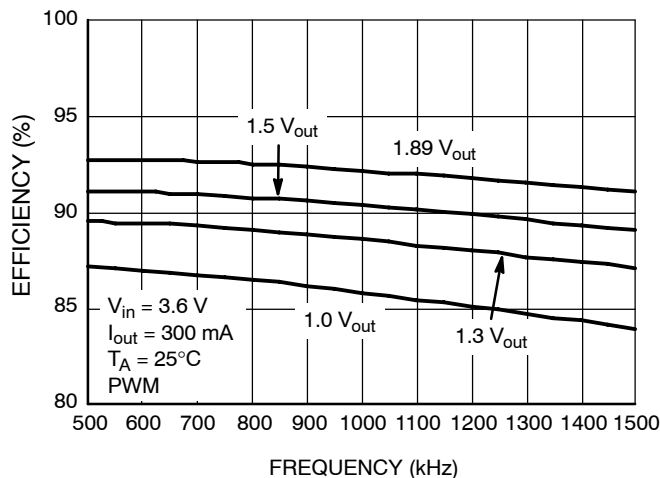


Figure 8. Efficiency vs. Frequency at $I_{out} = 300 \text{ mA}$

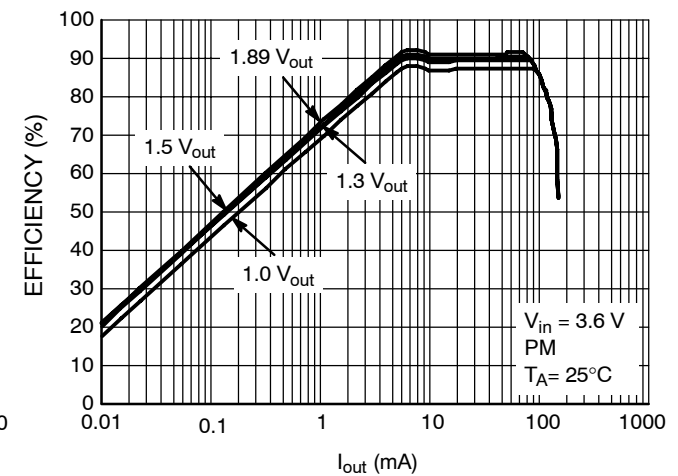


Figure 9. Efficiency vs. Output Current in Pulsed Mode

NCP1511

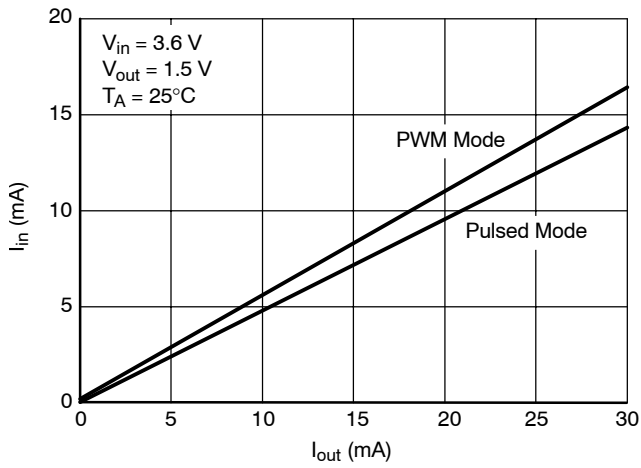


Figure 10. Input Current Comparison

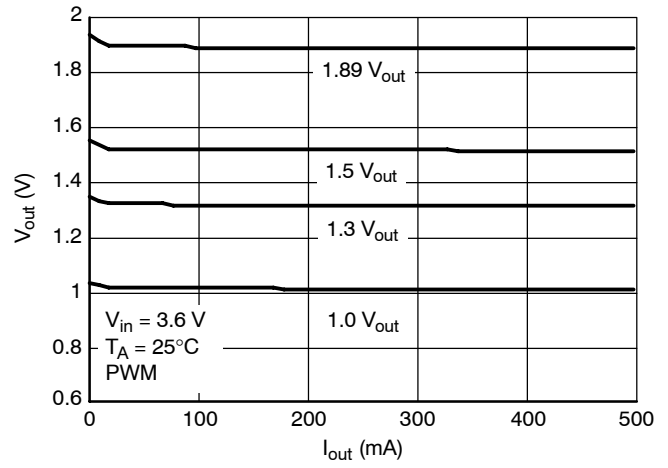


Figure 11. Output Voltage vs. Output Current

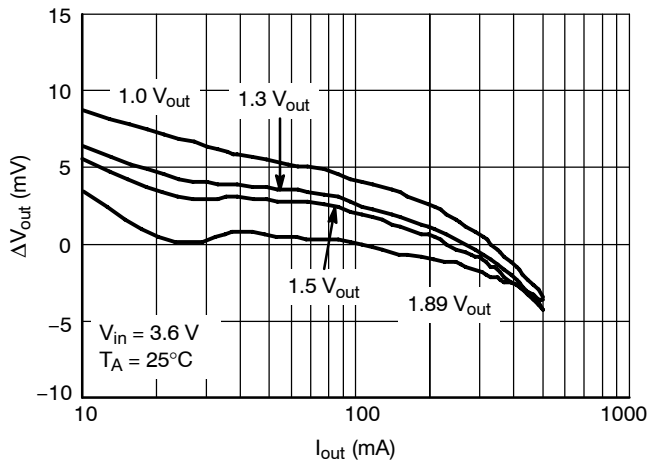


Figure 12. Load Regulation in PWM Mode

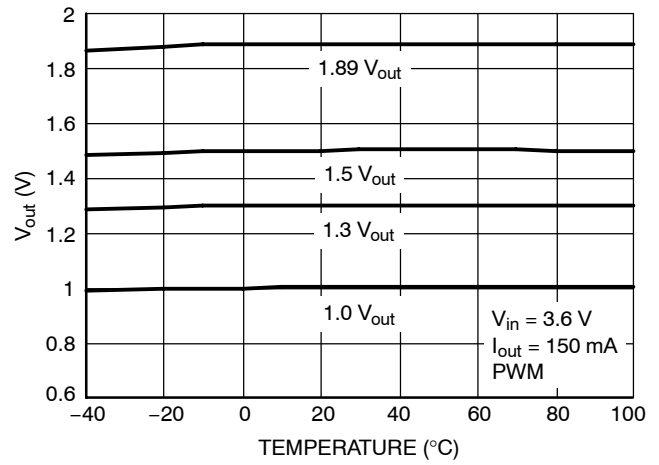


Figure 13. Output Voltage vs. Temperature

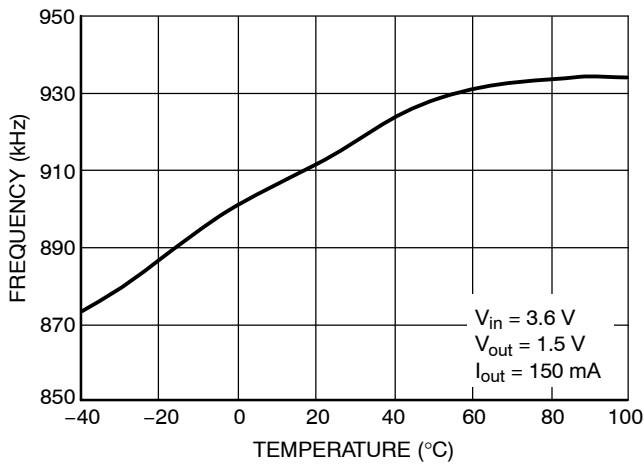


Figure 14. Oscillator Frequency vs. Temperature

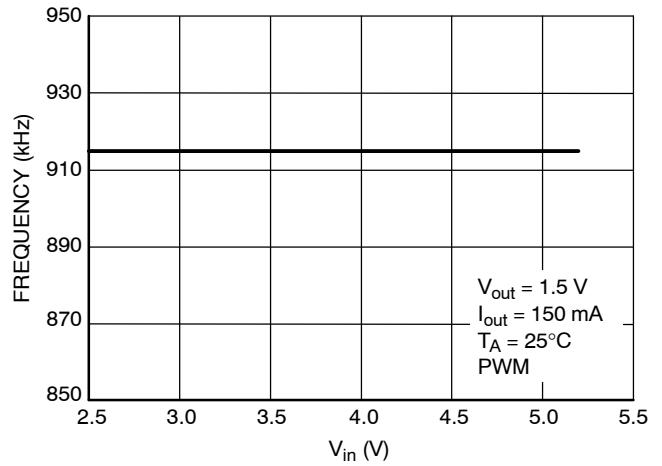


Figure 15. Oscillator Frequency vs. Input Voltage

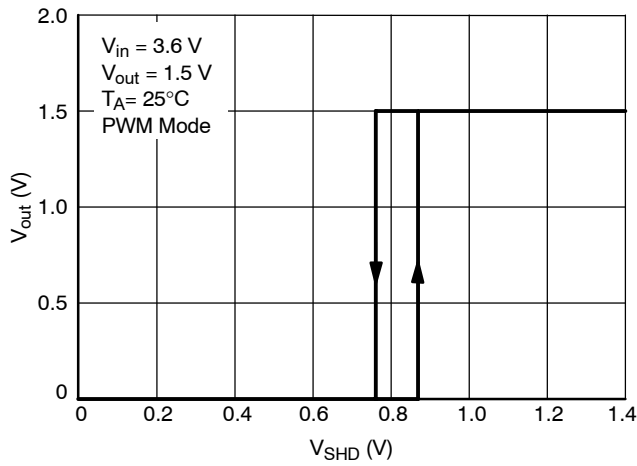


Figure 16. Output Voltage vs. Shutdown Pin Voltage

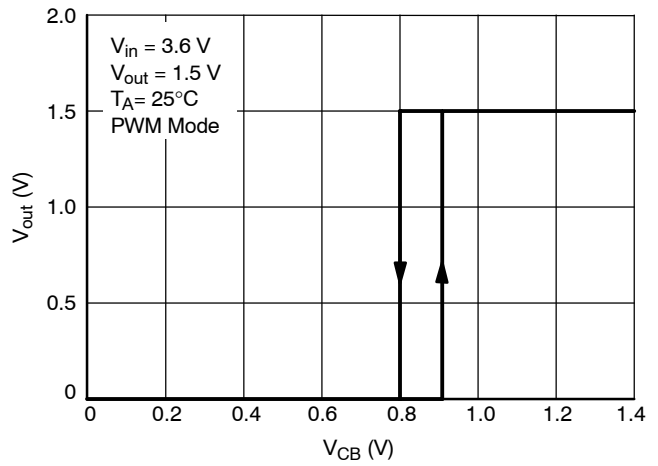


Figure 17. Transition Level of CB Pins

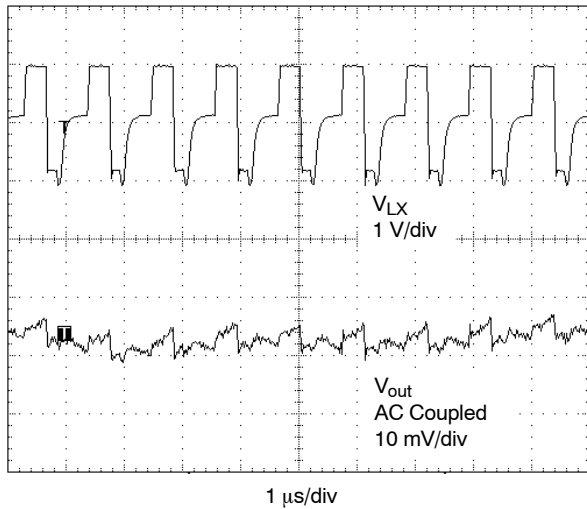


Figure 18. Light Load PWM Switching Waveform
($V_{in} = 3.6 \text{ V}$, $V_{out} = 1.5 \text{ V}$, $I_{out} = 30 \text{ mA}$)

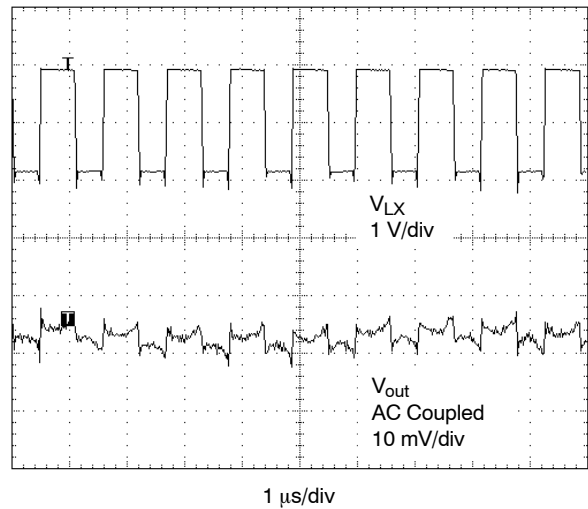


Figure 19. Heavy Load PWM Switching Waveform
($V_{in} = 3.6 \text{ V}$, $V_{out} = 1.5 \text{ V}$, $I_{out} = 300 \text{ mA}$)

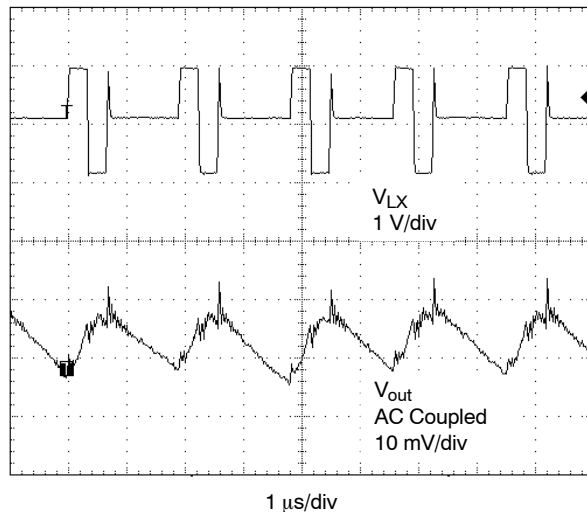


Figure 20. Pulsed Mode Switching Waveform
($V_{in} = 3.6 \text{ V}$, $V_{out} = 1.5 \text{ V}$, $I_{out} = 30 \text{ mA}$)

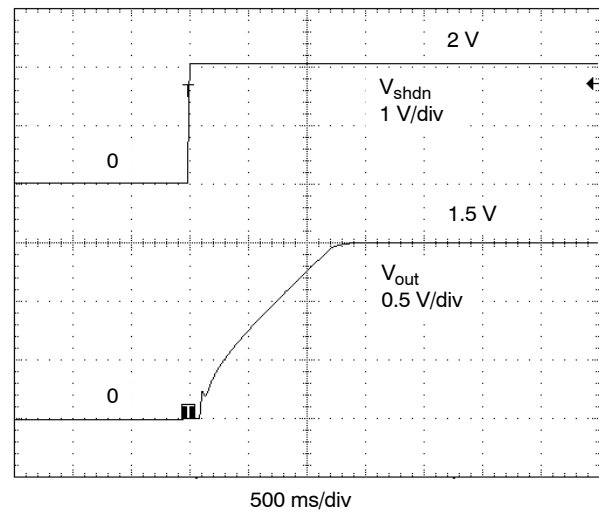


Figure 21. Soft-Start
($V_{in} = 3.6 \text{ V}$, $V_{out} = 1.5 \text{ V}$, $I_{out} = 150 \text{ mA}$)

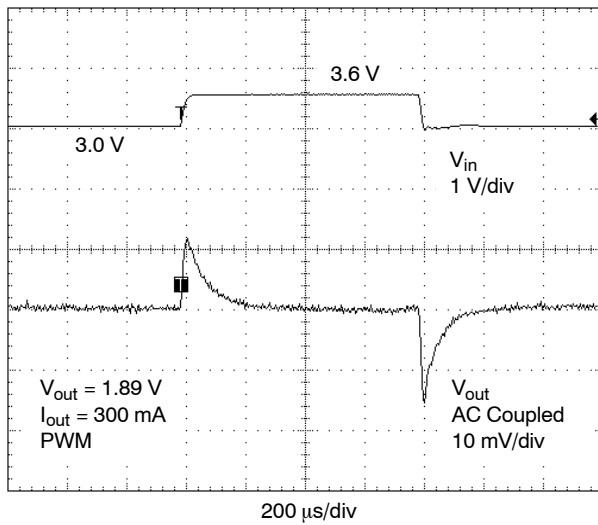


Figure 22. Line Transient Response for PWM

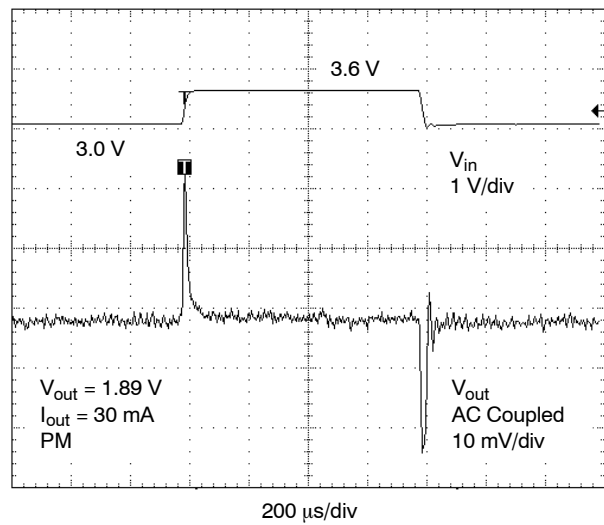


Figure 23. Line Transient Response for PM

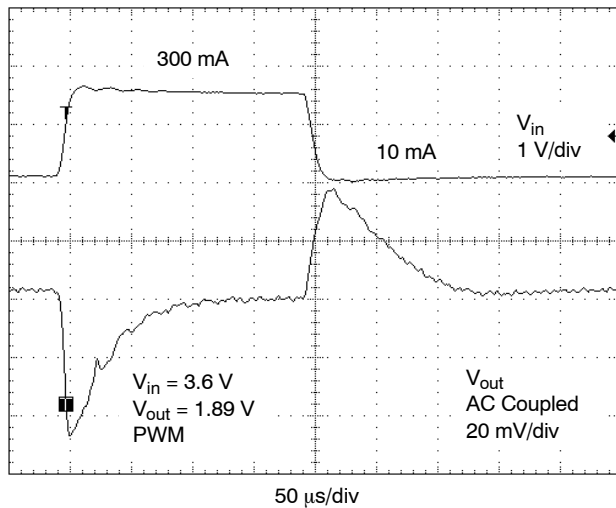


Figure 24. Load Transient Response

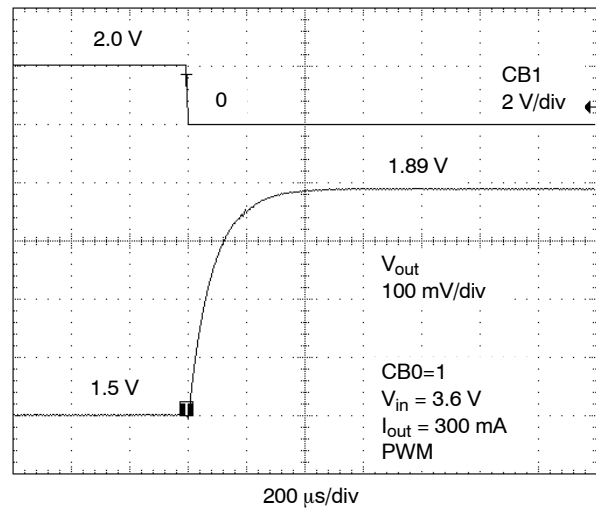


Figure 25. Output Voltage Transition from 1.5 V to 1.89 V

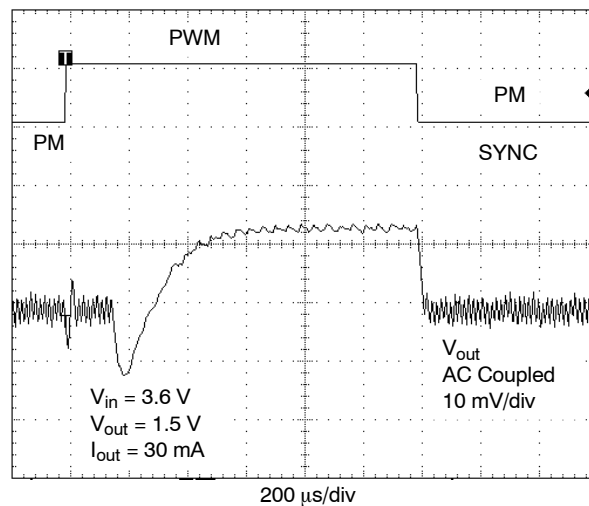


Figure 26. Transition between PWM and PM

DETAILED OPERATING DESCRIPTION

Overview

The NCP1511 is a monolithic micro-power high frequency PWM step-down DC-DC converter specifically optimized for applications requiring high efficiency and a small PCB footprint such as portable battery powered products. It integrates synchronous rectification to improve efficiency as well as eliminate the external Schottky diode. High switching frequency allows for a low profile inductor and capacitors to be used. Four digital selectable output voltages (1.0, 1.3, 1.5 and 1.89 V) can be generated from the input supply that can range from 2.7–5.2 V. All loop compensation is integrated as well further reducing the external component count as well.

The DC-DC converter has two operating modes (normal PWM, pulsed switching), which are intended to allow for optimum efficiency under either light (up to 30 mA) or heavy loads. The user determines the operating mode by controlling the SYNC input. In addition the SYNC input can be used to synchronize the PWM to an external system clock signal in the range of 500–1000 kHz.

PWM Operating Mode

The NCP1511 can be set to current mode PWM operation by connecting SYNC pin to V_{CC}. In this mode, the output voltage is regulated by modulating the on-time pulse width of the main switch Q1 at a fixed frequency of 1.0 MHz. The switching of the PMOS Q1 is controlled by a flip-flop driven by the internal oscillator and a comparator that compares the error signal from an error amplifier with the sum of the sensed current signal and compensation ramp. At the beginning of each cycle, the main switch Q1 is turned ON by the rising edge of the internal oscillator clock. The inductor current ramps up until the sum of the current sense signal and compensation ramp becomes higher than the error voltage amplifier. Once this has occurred, the PWM comparator resets the flip-flop, Q1 is turned OFF and the synchronous switch Q2 is turned ON. Q2 replaces the external Schottky diode to reduce the conduction loss and improve the efficiency. To avoid overall power loss, a certain amount of dead time is introduced to ensure Q1 is completely turned OFF before Q2 is being turned ON.

In continuous conduction mode (CCM), Q1 is turned ON after Q2 is completely turned OFF to start a new clock cycle. In discontinuous conduction mode (DCM), the zero crossing comparator (ZLC) will turn off Q2 when the inductor current drops to zero.

Overvoltage Protection

The overvoltage protection circuit is present in PWM mode to prevent the output voltage from going too high under light load or fast load transient conditions. The output overvoltage threshold is 5% above nominal set value. If the output voltage rises above 5% of the nominal

value, the OVP comparator is activated and switch Q1 is turned OFF. Switching will continue when the output voltage falls below the threshold of OVP comparator.

Pulsed Mode (PM)

Under light load conditions (< 30 mA), the NCP1511 can be configured to enter a low current pulsed mode operation to reduce power consumption. This is accomplished by applying a logic LOW to the SYNC pin. The output regulation is implemented by pulse frequency modulation. If the output voltage drops below the threshold of PM comparator (typically V_{nom}–2%), a new cycle will be initiated by the PM comparator to turn on the switch Q1. Q1 remains ON until the peak inductor current reaches 200 mA (nom). Then ILIM comparator goes high to switch off Q1. After a short dead time delay, switch rectifier Q2 is turn ON. The zero crossing comparator will detect when the inductor current drops to zero and send the signal to turn off Q2. The output voltage continues to decrease through discharging the output capacitor. When the output voltage falls below the threshold of the PM comparator again, a new cycle starts immediately.

Cycle-by-Cycle Current Limit

From the block diagram, an ILIM comparator is used to realize cycle-by-cycle current limit protection. The comparator compares the LX pin voltage with the reference voltage from the SENFET, which is biased by a constant current. If the inductor current reaches the limit, the ILIM comparator detects the LX voltage falling below the reference voltage from the SENFET and releases the signal to turn off the switch Q1. The cycle-by-cycle current limit is set at 800 mA (nom) in PWM and 200 mA in PM.

Frequency Synchronization and Operating Mode Selection

The SYNC pin can also be used for frequency synchronization by connecting it with an external clock signal. It operates in PWM mode when synchronized to an external clock. The switching cycle initiates by the rising edge of the clock. The 500 kHz to 1000 kHz synchronization clock signal should be between 0.4 V and 1.2 V.

Gating on and off the clock, the SYNC pin can also be used to select between PM and PWM modes. It allows efficient dynamical power management by adjusting the converter operation to the specific system requirement. Set SYNC pin low to select PM mode at light load conditions (up to 30 mA) and set SYNC pin high or connect with external clock to select PWM mode at heavy load condition to achieve optimum efficiency. Table 1 shows the mode selection with three different SYNC pin states.

Table 1. Operating Mode Selection

SYNC Pin State	Operating Mode
LOW	Pulsed Mode (PM)
HIGH	PWM, 1 MHz Switch Frequency
CLOCK	PWM, Frequency Synchronization

Output Voltage Selection

The output voltage is digitally programmed to one of four voltage levels depending on the logic state of CB0 and CB1. Therefore if the NCP1511's load, such as a digital cellular phone's baseband processor, supports dynamic power management, the device can lower or raise its core voltage under software control. When combined with the pulsed current mode function in low load situations, this active voltage management further stretches the useful operating life of the handset battery between charges.

The output voltage levels are listed in Table 2. The CB0 has a pull down resistor and the CB1 has a pullup resistor. The default output voltage is 1.3 V when CB0 and CB1 are floating.

Table 2. Truth Table for CB0 and CB1 with the Corresponding Output Voltage

CB0	CB1	Vout(V)
0	0	1.0
0	1	1.3
1	1	1.5
1	0	1.89

Soft-Start

The NCP1511 uses soft-start to limit the inrush current when the device is initially powered up or enabled. Soft-start is implemented by gradually increasing the reference voltage until it reaches the full reference voltage. During startup, a pulsed current source charges the internal soft-start capacitor to provide gradually increasing reference voltage for the PWM loop. When the voltage across the capacitor ramps up to the nominal reference voltage, the pulsed current source will be switched off and the reference voltage will switch to the regular reference voltage.

Shutdown Mode

When the SHD pin has a voltage applied of less than 0.4 V, the NCP1511 will be disabled. In shutdown mode, the internal reference, oscillator and most of the control circuitries are turned off. Therefore, the typical current consumption will be 0.1 μ A (typical value).

Applying a voltage above 1.2 V to SHD pin will enable the device for normal operation. The device will go through soft-start to normal operation.

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. If the junction temperature exceeds 160°C, the device shuts down. In this mode switch Q1 and Q2 and the control circuits are all turned off. The device restarts in soft-start after the temperature drops below 135°C. This feature is provided to prevent catastrophic failures from accidental device overheating and it is not intended as a substitute for proper heatsinking.

APPLICATIONS INFORMATION

Component Selection

Input Capacitor Selection

In PWM operating mode, the input current is pulsating with large switching noise. Using an input bypass capacitor reduces the peak current transients drawn from the input supply source, thereby reducing switching noise significantly. The capacitance needed for the input bypass capacitor depends on the source impedance of the input supply. The RMS capacitor current is calculated as:

$$I_{RMS} \approx I_O \sqrt{D \cdot D'} \quad (\text{eq. 1})$$

where:

D = duty cycle, which equals V_{out}/V_{in} , and $D' = 1 - D$.

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is $I_{O,max}/2$.

A low profile ceramic capacitor of 10 μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to the V_{CC} pin.

Inductor Value Selection

Selecting the proper inductor value is based on the desired ripple current. The relationship between the inductance and the inductor ripple current is given by the equation below.

$$\Delta i_L = \frac{V_{out}}{L f_s} \left(1 - \frac{V_{out}}{V_{in}} \right) \quad (\text{eq. 2})$$

The DC current of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. For NCP1511, the compensation is internally fixed and a fixed 6.8 μH inductor is needed for most of the applications. For better efficiency, choose a low DC resistance inductor.

Output Capacitor Selection

Selecting the proper output capacitor is based on the desired output ripple voltage. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output ripple voltage is given by:

$$\Delta V_C = \Delta i_L \cdot \left(\text{ESR} + \frac{1}{4f_s C_{out}} \right) \quad (\text{eq. 3})$$

The RMS output capacitor current is given by:

$$I_{RMS}(C_{out}) = \frac{V_O \cdot (1 - D)}{2\sqrt{3} \cdot L \cdot f_s} \quad (\text{eq. 4})$$

Where f_s is the switching frequency and ESR is the effective series resistance of the output capacitor. A low ESR, 22 μF ceramic capacitor is recommended for NCP1511 in most of applications. For example, with TDK C2012X5R0J226 output capacitor, the output ripple is less than 10 mV at 300 mA.

Design Example

As a design example, assume that the NCP1511 is used in a single lithium-ion battery application. The input voltage, V_{in} , is 3.0 V to 4.2 V. Output condition is V_{out} at 1.5 V with a typical load current of 120 mA and a maximum of 300 mA. For NCP1511, the inductor has a predetermined value, 6.8 μH . The inductor ESR will factor into the overall efficiency of the converter. The inductor needs to be selected by the required peak current.

Equation 5 is the basic equation for an inductor and describes the voltage across the inductor. The inductance value determines the slope of the current of the inductor.

$$\frac{V_L}{L} = \frac{di_L}{dt} \quad (\text{eq. 5})$$

Equation 5 is rearranged to solve for the change in current for the on-time of the converter in Continuous Conduction Mode.

$$\begin{aligned} i_{L, pk-pk} &= \frac{(V_{in} - V_{out})}{L} \cdot DT_s \\ &= \frac{(V_{in} - V_{out})}{L} \cdot \frac{V_{in}}{V_{out}} \cdot \frac{1}{f_s} \\ i_{L, max} &= I_{O, max} + \frac{\Delta i_{L, pk-pk}}{2} \end{aligned} \quad (\text{eq. 6})$$

Utilizing Equations 6, the peak-to-peak inductor current is calculated using the following worst-case conditions.

$$V_{in, max} = 4.2 \text{ V}, V_{out} = 1.5 \text{ V}, f_s = 1 \text{ MHz}-20\%,$$

$$L = 6.8 \mu\text{H}-10\%, i_{L, pk-pk} = 197 \text{ mA}, i_{L, max} = 399 \text{ mA}$$

Therefore, the inductor must have a maximum current exceeding 405 mA.

Since the compensation is fixed internally in the IC, the input and output capacitors as well as the inductor have a predetermined value too: $C_{in} = 10 \mu\text{F}$ and $C_{out} = 22 \mu\text{F}$. Low ESR capacitors are needed for best performance. Therefore, ceramic capacitors are recommended.

NCP1511

PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise and unwanted feedback that can affect the performance of the converter. Hints suggested below can be used as a guideline in most situations.

1. Use star-ground connection to connect the IC ground nodes and capacitor GND nodes together at one point. Keep them as close as possible. And then connect this to the ground plane through several vias. This will reduce noise in the ground plane by preventing the switching currents from flowing through the ground plane.

2. Place the power components (i.e., input capacitor, inductor and output capacitor) as close together as possible

for best performance. All connecting traces must be short, direct, and wide to reduce voltage errors caused by resistive losses through the traces.

3. Separate the feedback path of the output voltage from the power path. Keep this path close to the NCP1511 circuit. And also route it away from noisy components. This will prevent noise from coupling into the voltage feedback trace.

4. Place the DC-DC converter away from noise sensitive circuitry, such as RF circuits.

The following shows the NCP1511 demo board layout and bill of materials:

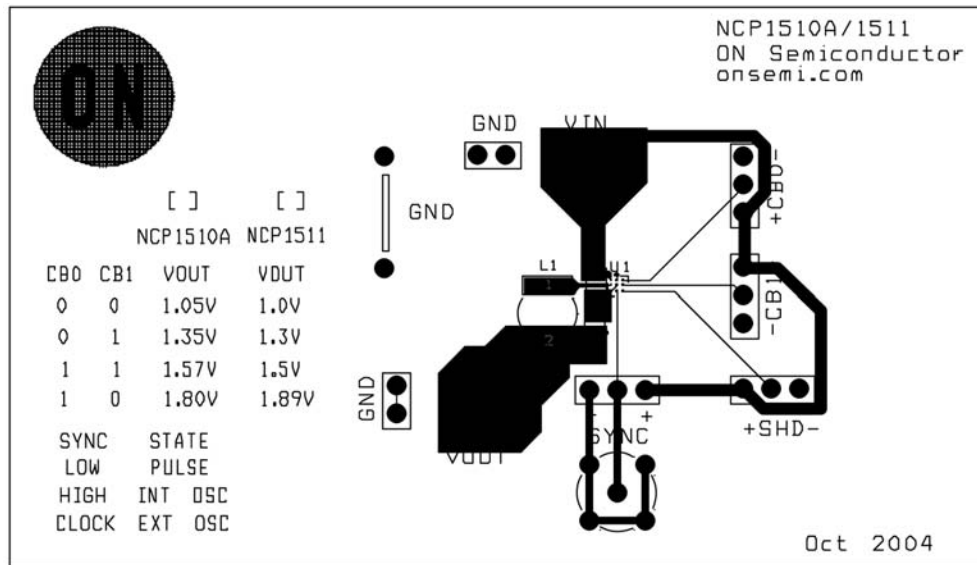


Figure 27. Top and Silkscreen Layer

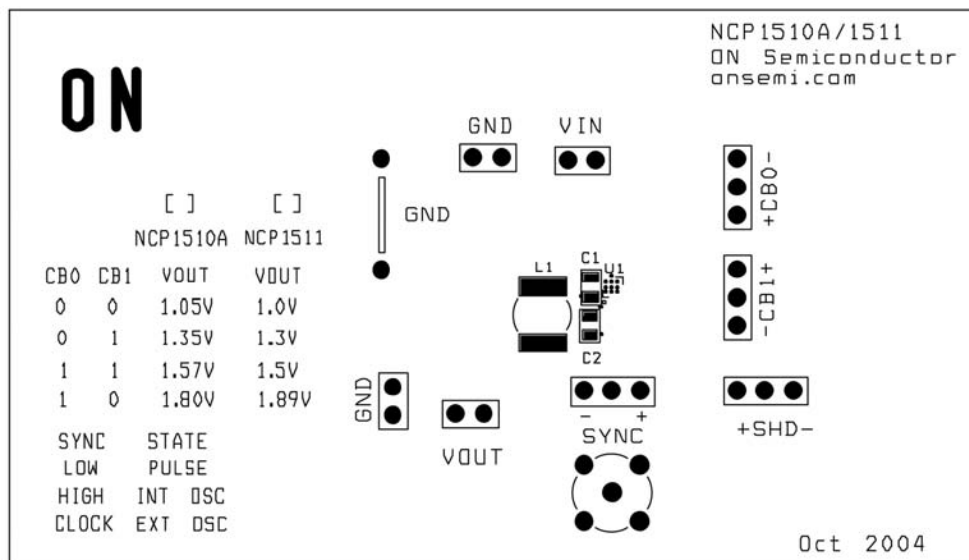


Figure 28. Soldermask Top and Silkscreen Layer

NCP1511

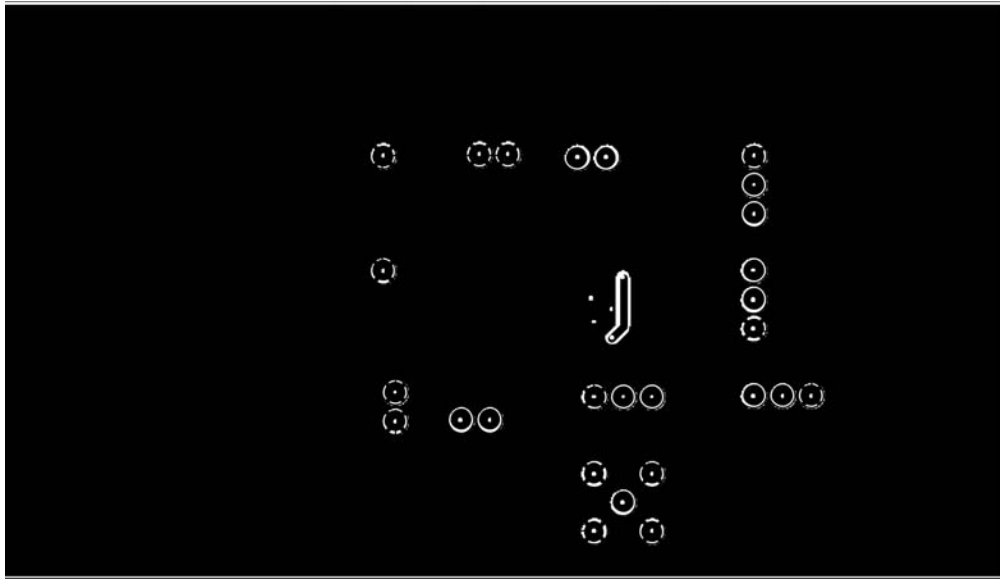


Figure 29. Bottom Layer

Table 3. Bill of Materials

Component	Value	Manufacturer	Part Number	Size (mm)	I _{out} (mA)	ESR (mΩ)
C _{in}	10 μF, X5R, 6.3 V	TDK Murata	C2012X5R0J106 GRM21BR60J106	2.0 x 1.25 x 1.25	–	–
C _{out}	22 μF, X5R, 6.3 V	TDK Murata	C2012X5R0J226 GRM21BR60J226	2.0 x 1.25 x 1.25	–	–
L	6.8 μH	TDK	VLCF4020–6R8	4.0 x 4.0 x 2.0	500**	146
		Coilcraft	0805PS–682	3.4 x 3.0 x 1.8	210*	1260
		Coilcraft	LPO4812	4.8 x 4.8 x 1.2	340*	225
		Sumida	CLS4D11	4.9 x 4.9 x 1.2	500**	220

*Output current calculated from $V_{CC} = 4.2 V_{max}$, $1.5 V_{out}$ and Freq = 700 kHz (1.0 MHz – 20 %).

**Calculated output current from $V_{CC} = 4.2 V_{max}$ and Freq = 700 kHz exceeds 640 mA ($I_{lim} - 20\%$). Therefore maximum output for these conditions shown as 500 mA.

NCP1530

600 mA PWM/PFM Step-Down Converter with External Synchronization Pin

The NCP1530 is a PWM/PFM non-synchronous step-down (Buck) DC-DC converter for usage in systems supplied from 1-cell Li-ion, or 2 or more cells Alkaline/NiCd/NiMH batteries. It can operate in Constant-Frequency PWM mode or PWM/PFM mode in which the controller will automatically switch to PFM mode operation at low output loads to maintain high efficiency. The switching frequency can also be synchronized to external clock between 600 kHz and 1.2 MHz. The maximum output current is up to 600 mA. Applying an external synchronizing signal to SYN pin can supersede the PFM operation.

The NCP1530 consumes only 47 μ A (typ) of supply current ($V_{OUT} = 3.0$ V, no switching) and can be forced to shutdown mode by bringing the enable input (EN) low. In shutdown mode, the regulator is disabled and the shutdown supply current is reduced to 0.5 μ A (typ). Other features include built-in undervoltage lockout, internal thermal shutdown, an externally programmable soft-start time and output current limit protection. The NCP1530 operates from a maximum input voltage of 5.0 V and is available in a space saving, low profile Micro8™ package.

Features

- Pb-Free Package is Available
- High Conversion Efficiency, up to 92% at $V_{IN} = 4.3$ V, $V_{OUT} = 3.3$ V, $I_{OUT} = 300$ mA
- Current-Mode PWM Control
- Automatic PWM/PFM Mode for Current Saving at Low Output Loads
- Internal Switching Transistor Support 600 mA Output Current ($V_{IN} = 5.0$ V, $V_{OUT} = 3.3$ V)
- High Switching Frequency (600 kHz), Support Small Size Inductor and Capacitor, Ceramic Capacitors Can be Used
- Synchronize to External Clock Signal up to 1.2 MHz
- 100% Duty Cycle for Maximum Utilization of the Supply Source
- Programmable Soft-Start Time through External Chip Capacitor
- Externally Accessible Voltage Reference
- Built-In Input Undervoltage Lockout
- Built-In Output Overvoltage Protection
- Power Saving Shutdown Mode
- Space Saving, Low Profile Micro8 Package

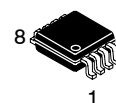
Typical Applications

- PDAs
- Digital Still Camera
- Cellular Phone and Radios
- Portable Test Equipment
- Portable Scanners
- Portable Audio Systems



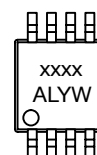
ON Semiconductor®

<http://onsemi.com>



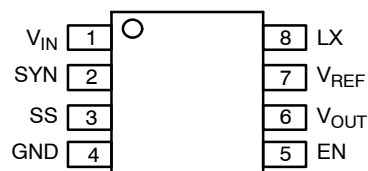
Micro8™
DM SUFFIX
CASE 846A

MARKING DIAGRAM



xxxx = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 466 of this data sheet.

NCP1530

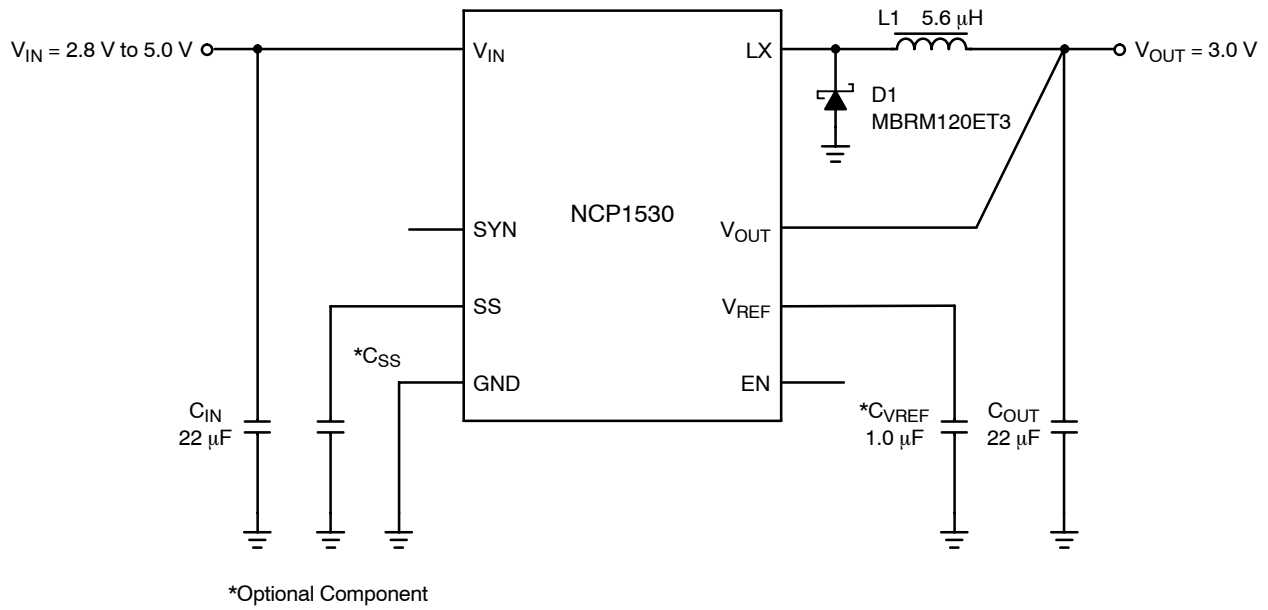


Figure 1. Typical Step-Down Converter Application

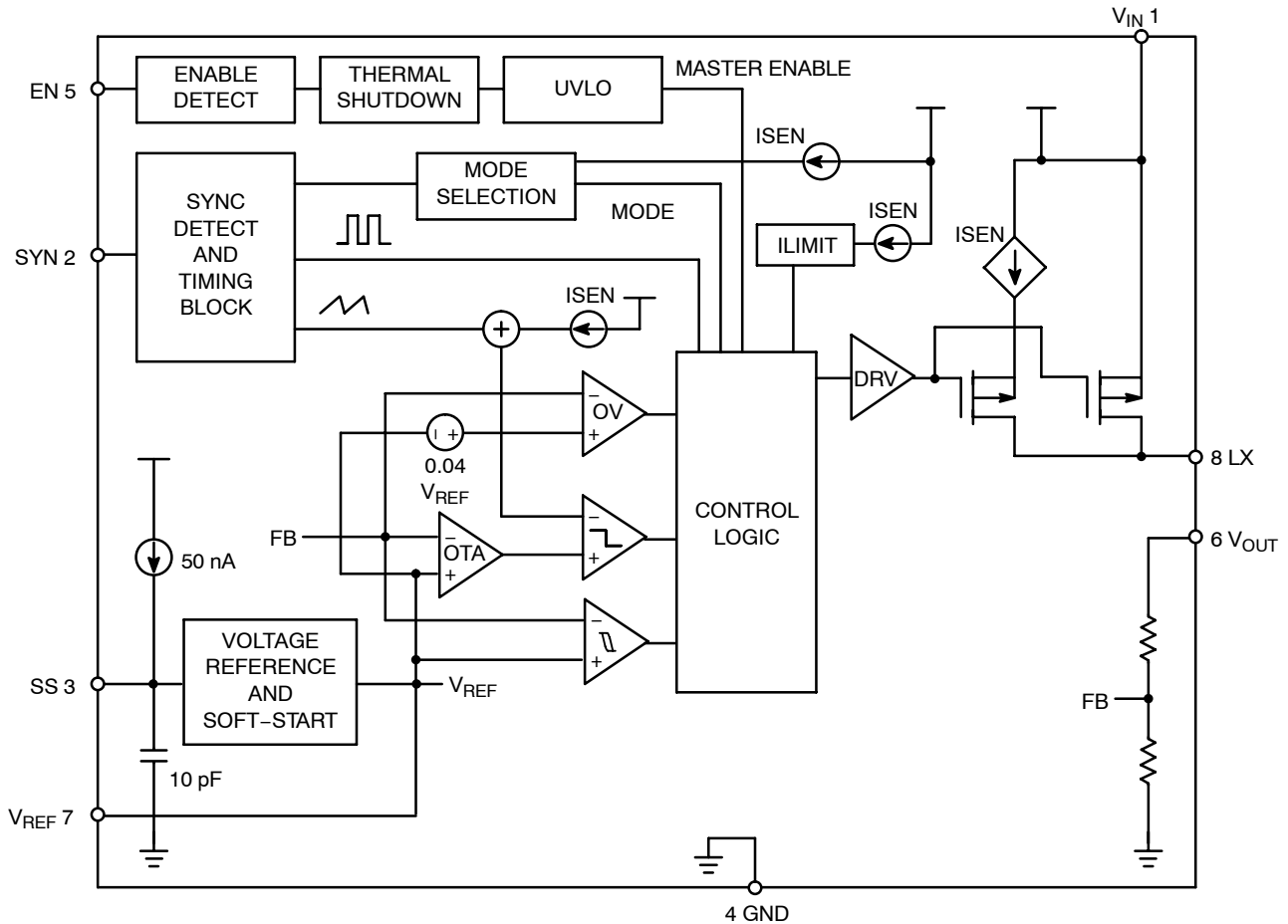


Figure 2. Simplified Functional Block Diagram

PIN FUNCTION DESCRIPTIONS

Pin	Symbol	Description
1	V_{IN}	Unregulated Supply Input.
2	SYNC	Oscillator Synchronization and Mode Selection Input. SYNC = GND (Automatic PWM/PFM mode) The converter operates at 600 kHz fixed-frequency PWM mode primarily, and automatically switches to variable-frequency PFM mode at small output loads for power saving. SYNC = V_{IN} (Constant-Frequency PWM mode) The converter operates at 600 kHz fixed-frequency PWM mode always. SYNC = External clock signal between 600 to 1200 kHz. The converter will be synchronized with the external clock signal. The SYNC pin is internally pulled to GND.
3	SS	Soft-Start Timing control pin. An external soft-start capacitor can be connected to this pin if extended soft-start is required. A 50 nA current will be sourced from this pin to charge up the capacitor during startup and gently ramps the device into service to prevent output voltage overshoot. If this pin is floated, built-in 500 μ s (typ.) soft-start will be activated.
4	GND	Ground Terminal.
5	EN	Active-High Enable Input. Active to enable the device. Bring this pin to GND and the quiescent current is reduced to less than 0.5 μ A. This pin is internally pulled to V_{IN} .
6	V_{OUT}	Feedback Terminal. The output voltage is sensed by this pin.
7	V_{REF}	Connected to voltage reference decoupling capacitor. For noise non-sensitive applications, the internal voltage reference can operate without decoupling capacitor.
8	LX	Inductor Terminal. This pin is connected to the drains of the internal P-channel switching transistors. The inductor must be connected between this pin and the output terminal.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply (Pin 1)	V_{IN}	-0.3 to 6	V
Input/Output Pins (Pins 2-4 & Pins 7-8)	V_{IO}	-0.3 to 6	V
Thermal Characteristics Micro8 Plastic Package Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	240	$^{\circ}\text{C/W}$
Operating Junction Temperature Range	T_J	0 to +150	$^{\circ}\text{C}$
Operating Ambient Temperature Range	T_A	0 to +85	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^{\circ}\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

4. This device series contains ESD protection and exceeds the following tests:
 Human Body Model (HBM) ± 2.0 kV per JEDEC standard: JESD22-A114.
 Machine Model (MM) ± 200 V per JEDEC standard: JESD22-A115.
5. Latchup Current Maximum Rating: ± 150 mA per JEDEC standard: JESD78.
6. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.

NCP1530

ELECTRICAL CHARACTERISTICS ($V_{IN} = V_R + 1.0$ V, test circuit, refer to Figure 1, $C_{SS} = NC$ and $C_{VREF} = 1.0$ μ F, $T_A = 25^\circ$ C for typical value, 0° C $\leq T_A \leq 85^\circ$ C for min/max values unless otherwise noted.) * V_R is the factory-programmed output voltage setting.

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage	V_{IN}	$1.1 V_R$	–	5.0	V
Output Voltage ($I_{load} = 150$ mA, $V_R + 1.0$ V $< V_{IN} < 5.0$ V) (Note 7) NCP1530DM25R2 NCP1530DM27R2 NCP1530DM30R2 NCP1530DM33R2	V_{OUT}	2.425 2.619 2.910 3.201	2.5 2.7 3.0 3.3	2.575 2.781 3.090 3.399	V
Maximum Output Current ($V_{IN} = 5.0$ V, $V_{OUT} = 3.0$ V) (Note 8)	$I_{OUT(max)}$	600	–	–	mA
Supply Current ($V_{IN} = V_R + 1.0$ V, No Load, EN and SYN Pins NC)	I_{IN}	–	45	95	μ A
Shutdown Supply Current ($V_{IN} = 5.0$ V, No Load, $V_{EN} = 0$ V)	I_{SHDN}	–	0.5	1.0	μ A
LX Pin Leakage Current (No Load, $V_{EN} = 0$ V)	I_{LX}	–	–	1.0	μ A
Internal P-FET ON Resistance at LX Pin ($V_{IN} = V_R + 1.0$ V, $I_{Load} = 150$ mA)	$R_{DS(ON)}$	–	0.3	0.5	Ω
Oscillator Frequency ($V_{IN} = V_{EN} = V_R + 1.0$ V, $I_{Load} = 100$ mA, SYN Pin NC)	f_{OSC}	480	600	720	kHz
Maximum PWM Duty Cycle (Note 8)	$D_{MAX-PWM}$	–	–	100	%
PFM to PWM Switch-Over Current Threshold ($V_{IN} = 4.5$ V, SYN Pin NC, $L = 5.6$ μ H, $C_{OUT} = 22$ μ F) (Note 8) NCP1530DM25R2 NCP1530DM27R2 NCP1530DM30R2 NCP1530DM33R2	$I_{PFM-PWM}$	– – – –	83 90 100 102	– – – –	mA
PWM to PFM Switch-Over Current Threshold ($V_{IN} = 4.5$ V, SYN Pin NC, $L = 5.6$ μ H, $C_{OUT} = 22$ μ F) (Note 8) NCP1530DM25R2 NCP1530DM27R2 NCP1530DM30R2 NCP1530DM33R2	$I_{PWM-PFM}$	– – – –	27 38 39 48	– – – –	mA
Input Undervoltage Lockout Threshold	V_{UVLO}	–	2.0	2.45	V
Reference Voltage ($V_{IN} = V_R + 1.0$ V, $C_{VREF} = 1.0$ μ F)	V_{REF}	1.184	1.20	1.216	V
Reference Voltage Temperature Coefficient ($V_{IN} = V_R + 1.0$ V, $C_{VREF} = 1.0$ μ F) (Note 8)	TC_{VREF}	–	0.03	–	mV/ $^\circ$ C
Reference Voltage Load Current ($V_{IN} = V_R + 1.0$ V, $C_{VREF} = 1.0$ μ F) (Note 9)	I_{VREF}	5.0	–	–	mA
Enable Logic High Threshold Voltage ($V_{IN} = V_R + 1.0$ V, $I_{Load} = 0$ mA)	V_{EN-H}	–	1.5	1.85	V
Enable Logic Low Threshold Voltage ($V_{IN} = V_R + 1.0$ V, $I_{Load} = 0$ mA)	V_{EN-L}	0.5	1.2	–	V
PWM Minimum On-Time (Note 8)	t_{PWM-ON}	–	100	–	ns
PWM OV Protection Level	% V_{OV}	–	6.0	12	%
PWM Cycle-by-Cycle Current Limit (Note 8)	I_{LIM}	–	1.5	–	A
Built-in Soft-Start Time ($V_{OUT} = 3.0$ V, SS Pin NC) (Note 8)	t_{SS}	–	500	–	μ s
Thermal Shutdown Threshold ($V_{IN} = 3.5$ V, $I_{Load} = 0$ mA) (Note 8)	TH_{SHD}	–	145	–	$^\circ$ C
Thermal Shutdown Hysteresis ($V_{IN} = 3.5$ V, $I_{Load} = 0$ mA) (Note 8)	TH_{HSYS}	–	15	–	$^\circ$ C

7. Tested at $V_{IN} = V_R + 1.0$ V in production only. Full V_{IN} range guaranteed by design.
8. Parameter guaranteed by design only, not tested in production.
9. Loading capability decreases with V_{OUT} decreases.

TYPICAL OPERATING CHARACTERISTICS ($V_{IN} = V_R + 1.0\text{ V}$, test circuit, refer to Figure 1, $C_{SS} = \text{NC}$ and $C_{VREF} = 1.0\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$ for typical value, $0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for min/max values unless otherwise noted.) * V_R is the factory-programmed output voltage setting.

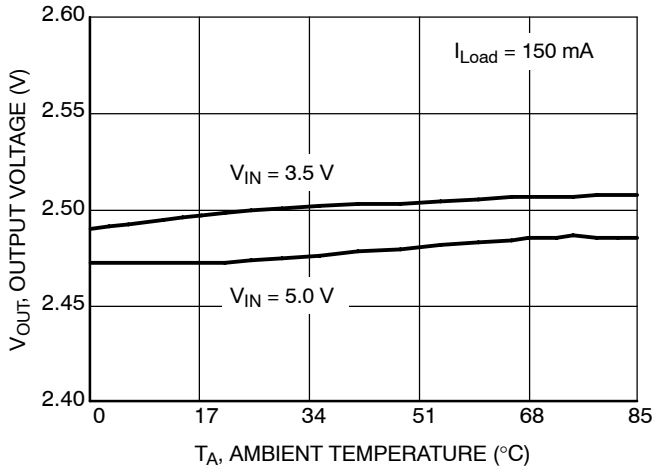


Figure 3. Output Voltage vs. Ambient Temperature ($V_{OUT} = 2.5\text{ V}$)

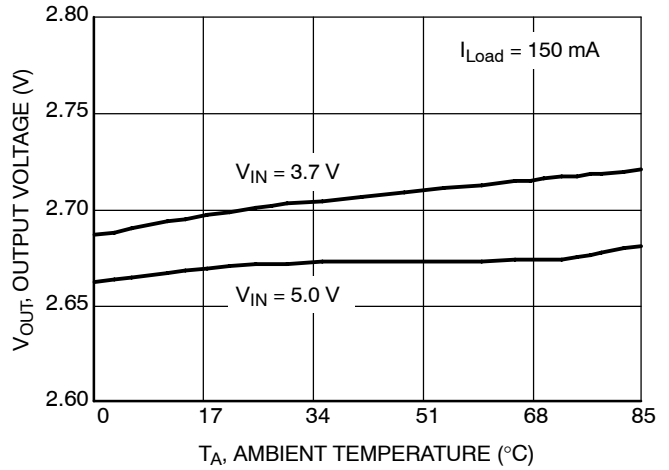


Figure 4. Output Voltage vs. Ambient Temperature ($V_{OUT} = 2.7\text{ V}$)

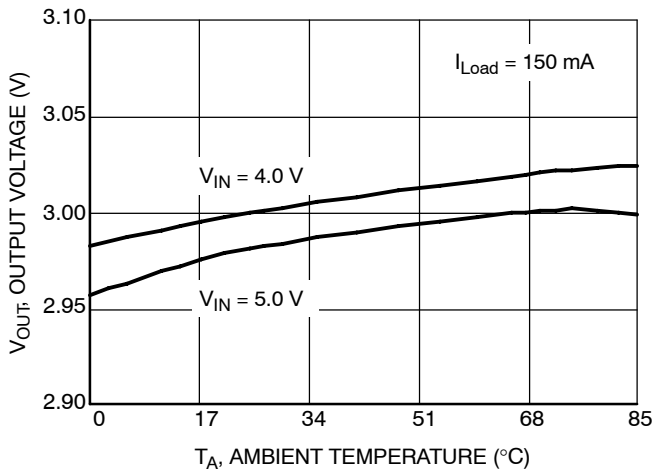


Figure 5. Output Voltage vs. Ambient Temperature ($V_{OUT} = 3.0\text{ V}$)

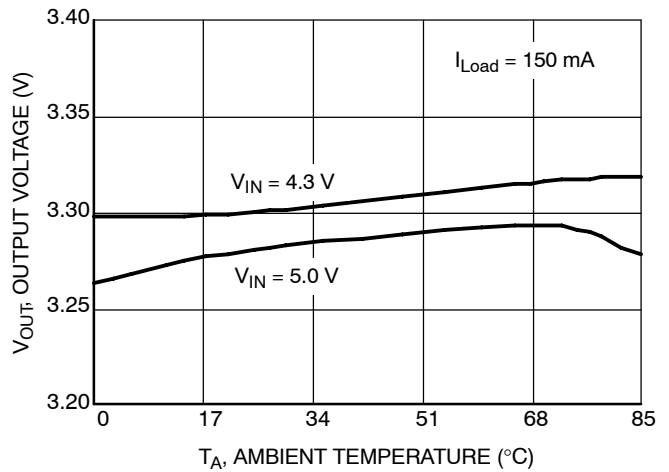


Figure 6. Output Voltage vs. Ambient Temperature ($V_{OUT} = 3.3\text{ V}$)

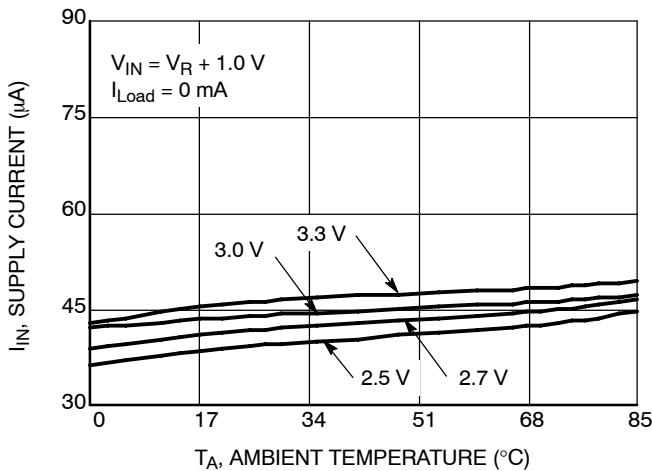


Figure 7. Supply Current vs. Ambient Temperature

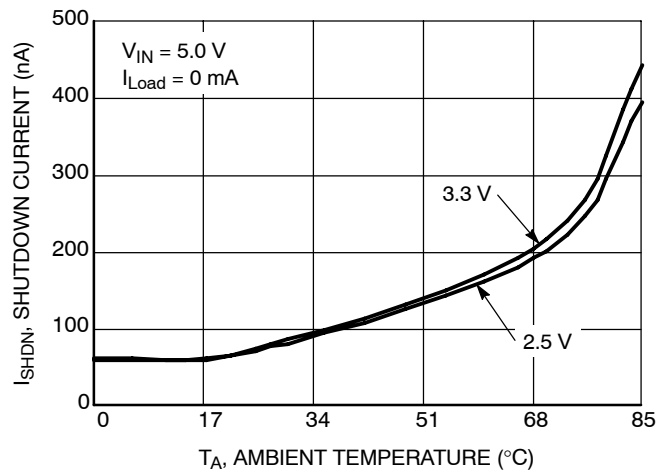


Figure 8. Shutdown Current vs. Ambient Temperature

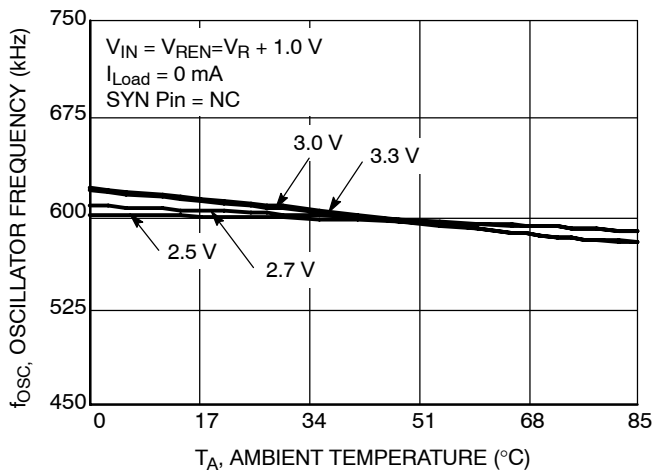


Figure 9. Oscillator Frequency vs. Ambient Temperature

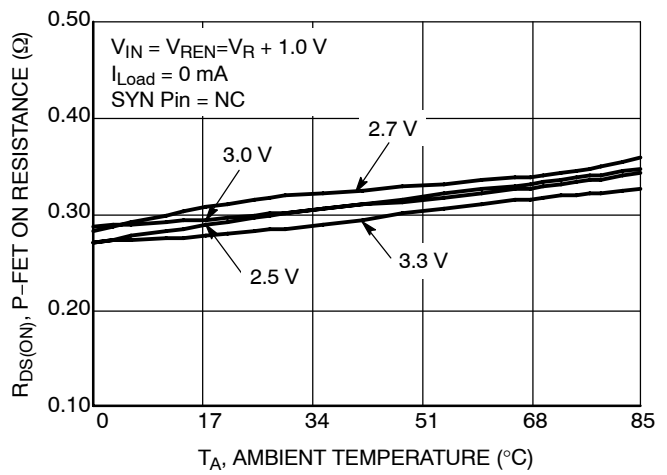


Figure 10. P-FET ON Resistance vs. Ambient Temperature

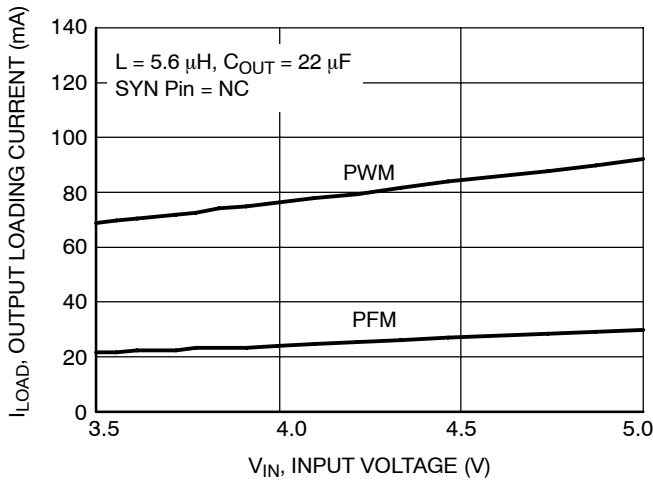


Figure 11. PWM/PFM Switchover Current Thresholds vs. Input Voltage ($V_{OUT} = 2.5 \text{ V}$)

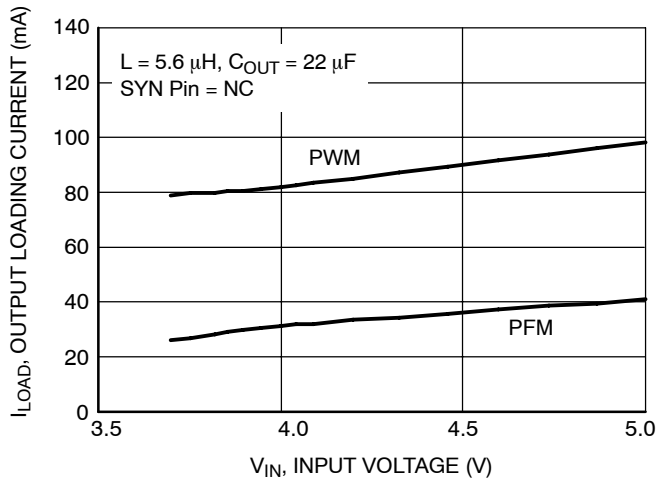


Figure 12. PWM/PFM Switchover Current Thresholds vs. Input Voltage ($V_{OUT} = 2.7 \text{ V}$)

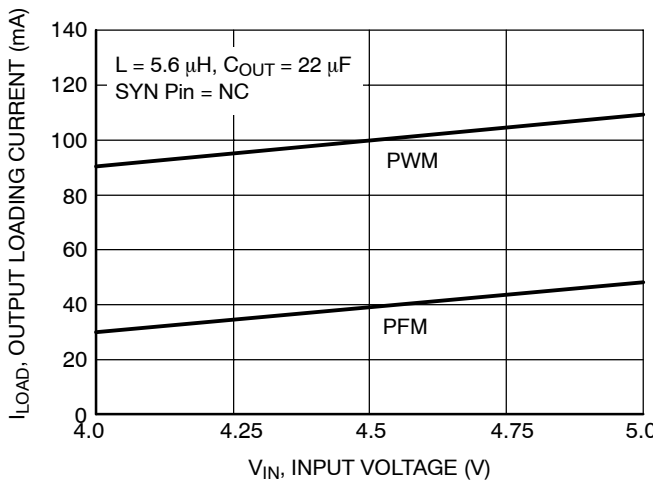


Figure 13. PWM/PFM Switchover Current Thresholds vs. Input Voltage ($V_{OUT} = 3.0 \text{ V}$)

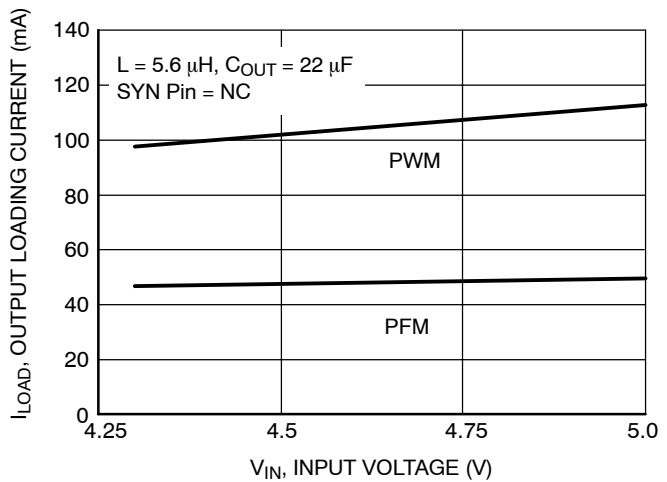


Figure 14. PWM/PFM Switchover Current Thresholds vs. Input Voltage ($V_{OUT} = 3.3 \text{ V}$)

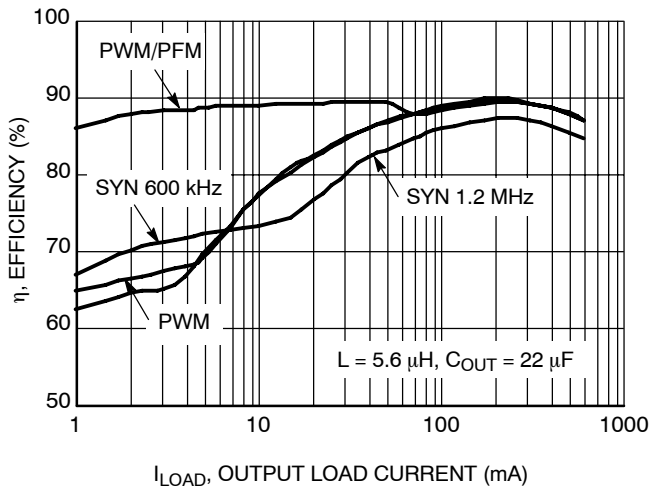


Figure 15. Efficiency vs. Output Load Current
($V_{IN} = 3.5\text{ V}$, $V_{OUT} = 2.5\text{ V}$)

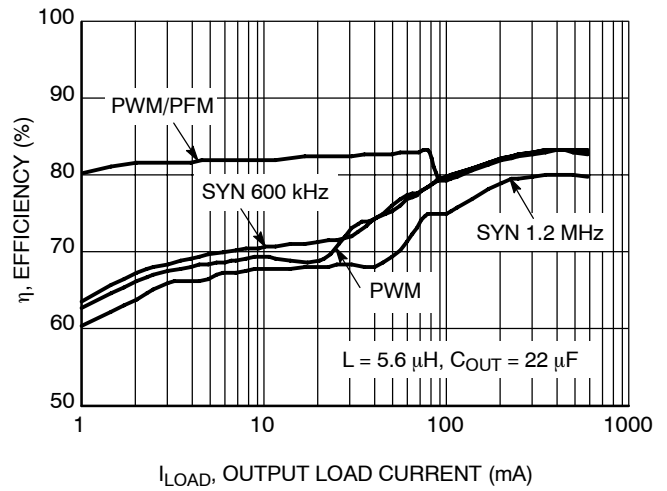


Figure 16. Efficiency vs. Output Load Current
($V_{IN} = 5.0\text{ V}$, $V_{OUT} = 2.5\text{ V}$)

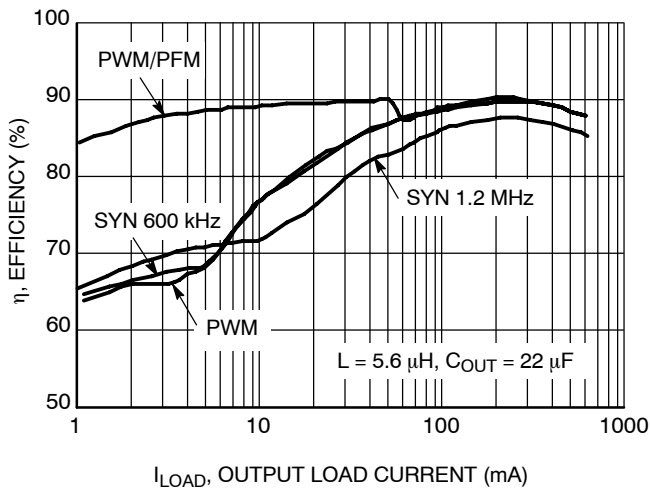


Figure 17. Efficiency vs. Output Load Current
($V_{IN} = 3.7\text{ V}$, $V_{OUT} = 2.7\text{ V}$)

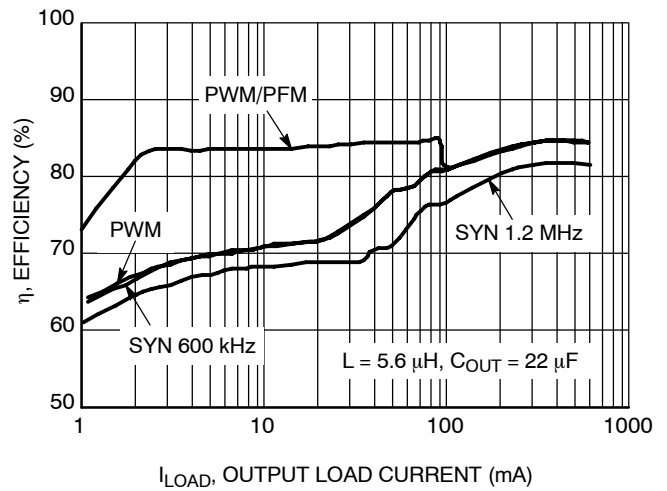


Figure 18. Efficiency vs. Output Load Current
($V_{IN} = 5.0\text{ V}$, $V_{OUT} = 2.7\text{ V}$)

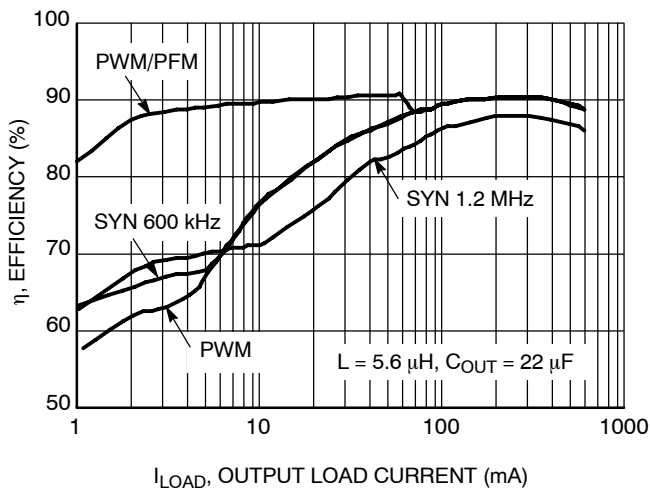


Figure 19. Efficiency vs. Output Load Current
($V_{IN} = 4.0\text{ V}$, $V_{OUT} = 3.0\text{ V}$)

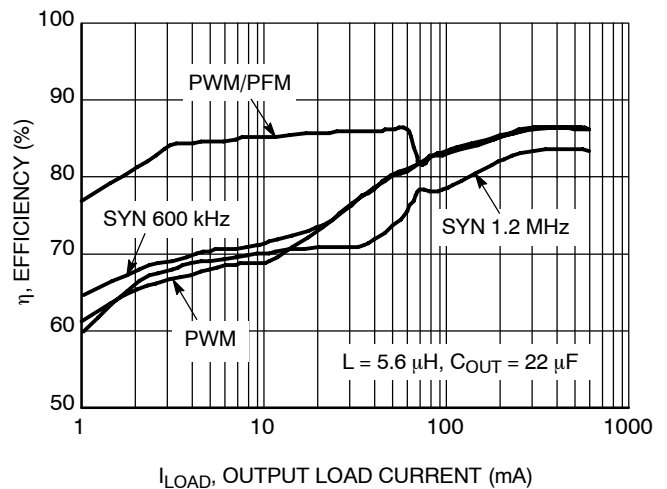


Figure 20. Efficiency vs. Output Load Current
($V_{IN} = 5.0\text{ V}$, $V_{OUT} = 3.0\text{ V}$)

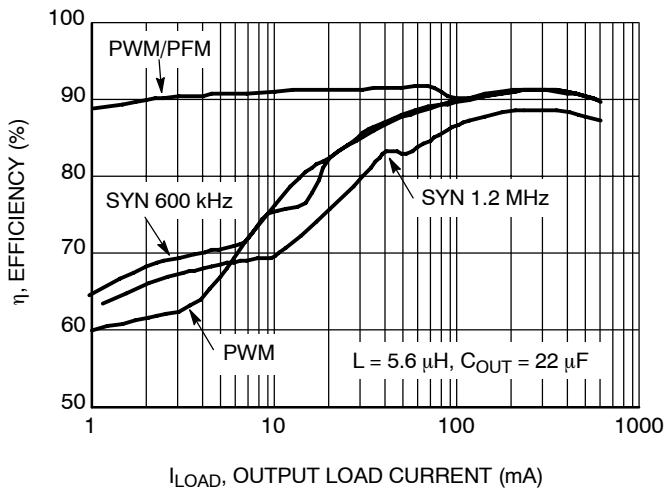


Figure 21. Efficiency vs. Output Load Current
($V_{IN} = 4.3\text{ V}$, $V_{OUT} = 3.3\text{ V}$)

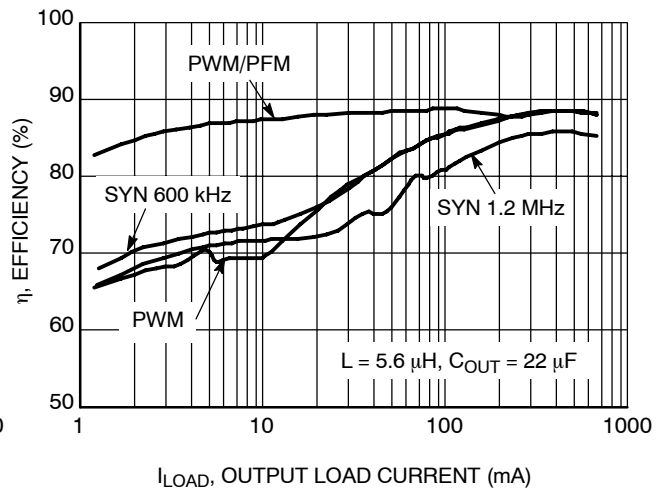


Figure 22. Efficiency vs. Output Load Current
($V_{IN} = 5.0\text{ V}$, $V_{OUT} = 3.3\text{ V}$)

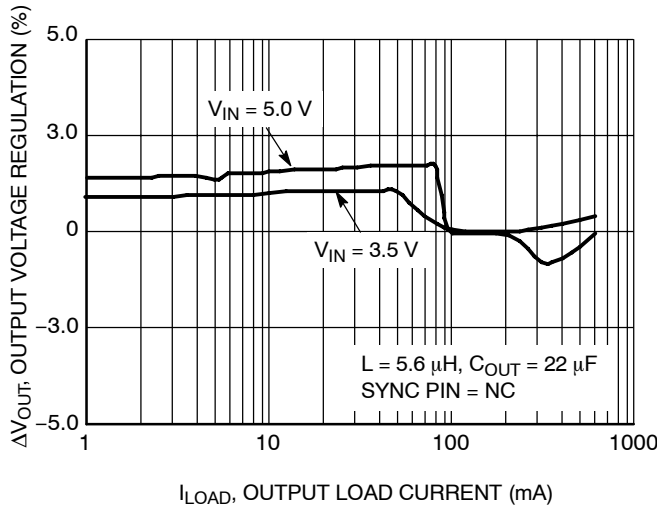


Figure 23. Output Voltage Regulation vs. Output Load Current
($V_{OUT} = 2.5\text{ V}$)

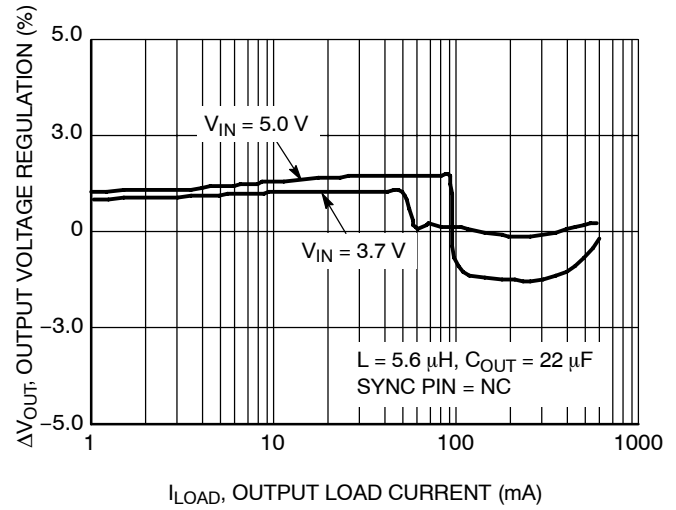


Figure 24. Output Voltage Regulation vs. Output Load Current
($V_{OUT} = 2.7\text{ V}$)

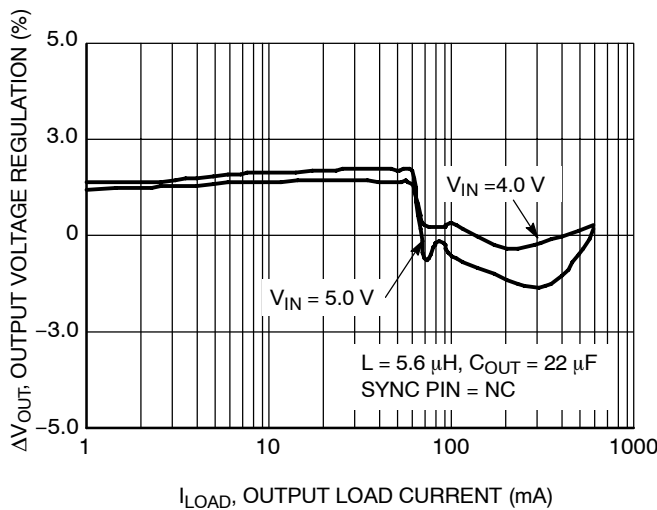


Figure 25. Output Voltage Regulation vs. Output Load Current
($V_{OUT} = 3.0\text{ V}$)

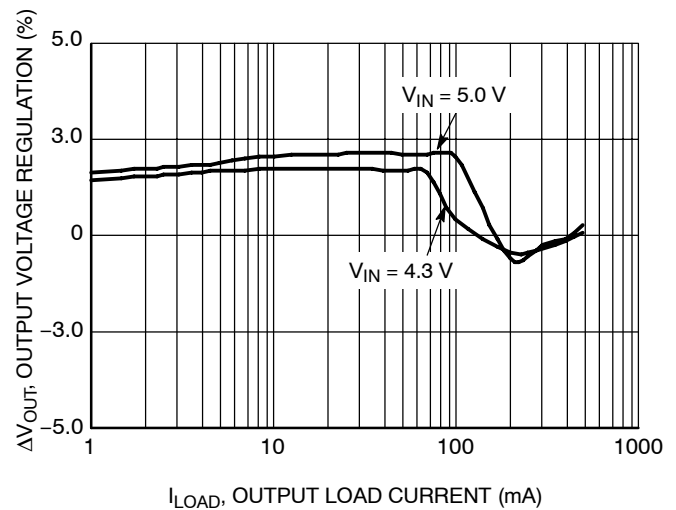
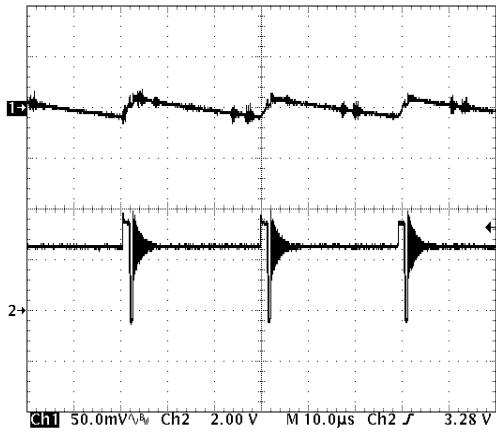


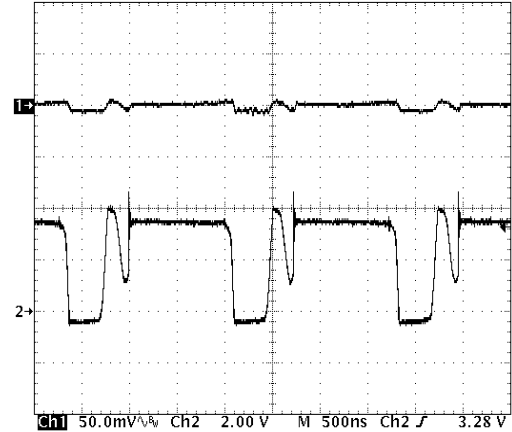
Figure 26. Output Voltage Regulation vs. Output Load Current
($V_{OUT} = 3.3\text{ V}$)



($V_{IN} = 3.5\text{ V}$, $V_{OUT} = 2.5\text{ V}$, $I_{LOAD} = 10\text{ mA}$)

Upper Trace: Output Voltage Ripple, 50 mV/div.
Lower Trace: LX Pin Switching Waveform, 2.0 V/div.

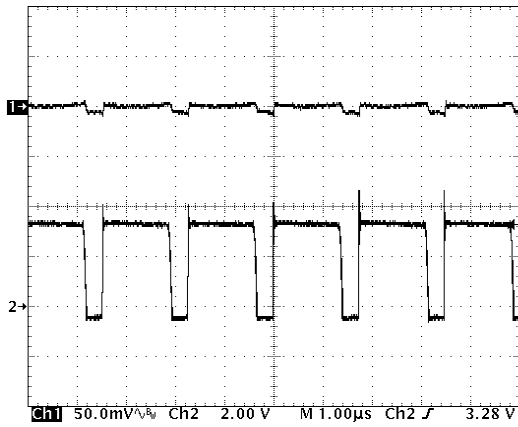
Figure 27. PFM Switching Waveform and Output Ripple for $V_{OUT} = 2.5\text{ V}$



($V_{IN} = 3.5\text{ V}$, $V_{OUT} = 2.5\text{ V}$, $I_{LOAD} = 80\text{ mA}$)

Upper Trace: Output Voltage Ripple, 50 mV/div.
Lower Trace: LX Pin Switching Waveform, 2.0 V/div.

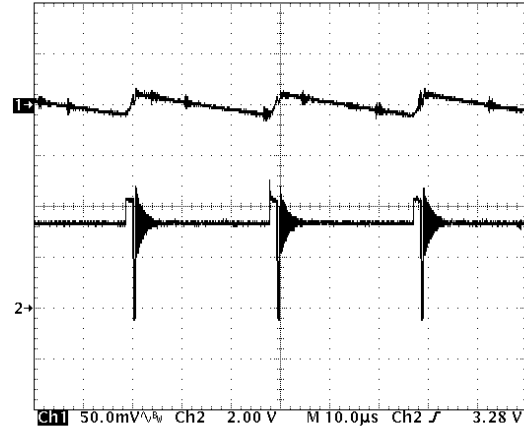
Figure 28. DCM PWM Switching Waveform and Output Ripple for $V_{OUT} = 2.5\text{ V}$



($V_{IN} = 3.5\text{ V}$, $V_{OUT} = 2.5\text{ V}$, $I_{LOAD} = 600\text{ mA}$)

Upper Trace: Output Voltage Ripple, 50 mV/div.
Lower Trace: LX Pin Switching Waveform, 2.0 V/div.

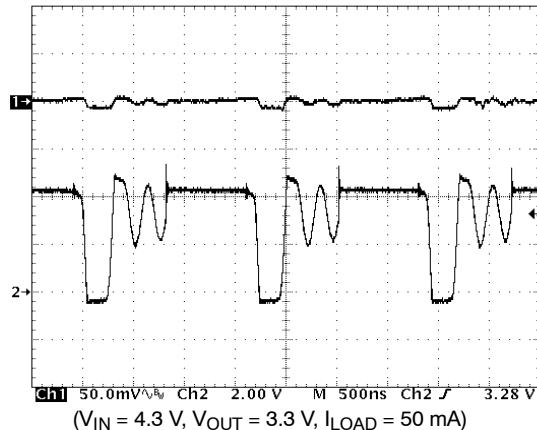
Figure 29. CCM PWM Switching Waveform and Output Ripple for $V_{OUT} = 2.5\text{ V}$



($V_{IN} = 4.3\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 10\text{ mA}$)

Upper Trace: Output Voltage Ripple, 50 mV/div.
Lower Trace: LX Pin Switching Waveform, 2.0 V/div.

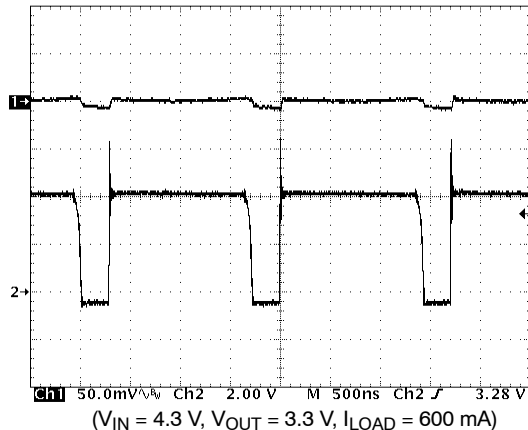
Figure 30. PFM Switching Waveform and Output Ripple for $V_{OUT} = 3.3\text{ V}$



($V_{IN} = 4.3\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 50\text{ mA}$)

Upper Trace: Output Voltage Ripple, 50 mV/div.
Lower Trace: LX Pin Switching Waveform, 2.0 V/div.

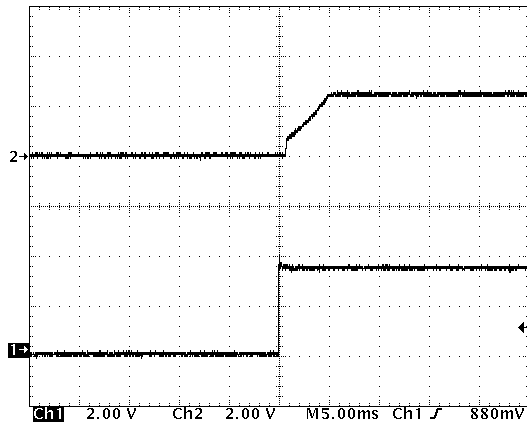
Figure 31. DCM PWM Switching Waveform and Output Ripple for $V_{OUT} = 3.3\text{ V}$



($V_{IN} = 4.3\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 600\text{ mA}$)

Upper Trace: Output Voltage Ripple, 50 mV/div.
Lower Trace: LX Pin Switching Waveform, 2.0 V/div.

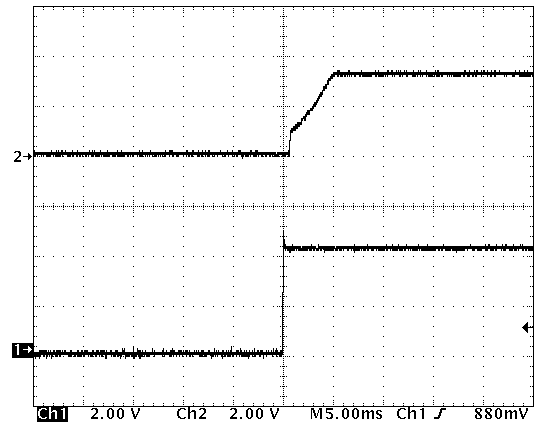
Figure 32. CCM PWM Switching Waveform and Output Ripple for $V_{OUT} = 3.3\text{ V}$



($V_{IN} = 3.5\text{ V}$, $V_{OUT} = 2.5\text{ V}$, $C_{SS} = 100\text{ pF}$, No load)

Upper Trace: Output Voltage, 2.0 V/Div.
Lower Trace: EN Pin Waveform, 2.0 V/Div.
Time Scale: 5.0 ms/Div.

**Figure 33. Soft-Start Output Voltage
Waveform for $V_{OUT} = 2.5\text{ V}$**



($V_{IN} = 4.3\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $C_{SS} = 100\text{ pF}$, No load)

Upper Trace: Output Voltage, 2.0 V/Div.
Lower Trace: EN Pin Waveform, 2.0 V/Div.
Time Scale: 5.0 ms/Div.

**Figure 34. Soft-Start Output Voltage
Waveform for $V_{OUT} = 3.3\text{ V}$**

DETAILED OPERATING DESCRIPTION

Introduction

The NCP1530 series are step-down converters with a smart control scheme that operates with 600 kHz fixed Pulse Width Modulation (PWM) at moderate to heavy load currents, so that high efficiency, noise free output voltage can be generated. In order to improve the system efficiency at light loads, this device can be configured to work in auto-mode. In auto-mode operation, the control unit will detect the loading condition and switch to power saving Pulse Frequency Modulation (PFM) control scheme at light load. With these enhanced features, the converter can achieve high operating efficiency for all loading conditions. Additionally, the switching frequency can also be synchronized to external clock signal in between 600 kHz to 1.2 MHz range. The converter uses peak current mode PWM control as a core, with the high switching frequency incorporated. Good line and load regulation can be achieved easily with small value ceramic input and output capacitors. Internal integrated compensation voltage ramp ensures stable operation at all operating modes. NCP1530 series are designed to support up to 600 mA output current with cycle-by-cycle current limit protection.

The Internal Oscillator

The oscillator that governs the switching of the PWM control cycle is self contained and no external timing component is required to setup the switching frequency. For PWM mode and auto-mode operation, all timing signals required for proper operation are derived from the internal oscillator. The internal fix frequency oscillator is trimmed to run at 600 kHz $\pm$ 20% over full temperature range. In case the device is forced to operate at Synchronization mode by applying an external clock signal to SYN pin (pin 2), the external clock signal will supersede the internal oscillator and take charge of the switching operation.

Voltage Reference and Soft-Start

An internal high accuracy voltage reference is included in NCP1530. This reference voltage governs all internal reference levels in various functional blocks required for proper operation. This reference voltage is precisely trimmed to 1.2 V $\pm$ 1.5% over full temperature range. The reference voltage can be accessed externally at V_{REF} pin (pin 7), with an external capacitor, C_{REF} of 1.0 μ F, providing up to 5.0 mA of loading. Additionally, NCP1530 has a Soft-Start circuit built around the voltage reference block that provide limits to the inrush current during start-up by

controlling the ramp up of the internal voltage reference. The soft-start time can be user adjusted by an external capacitor, C_{SS}, connecting to the SS pin (pin 3). During converter powerup, a 50 nA current flowing out from the SS pin will charge-up the timing capacitor. The voltage across the SS pin controls the ramp up of the internal reference voltage by slowly releasing it until the nominal value is reached. For an external timing capacitor of value C_{SS} = 100 pF, the soft-start time is about 5.0 ms including the small logic delay time, Figure 33 and 34. In the case where the SS pin is left floating, a small built-in capacitor together with other parasitic capacitance will provide a minimum intrinsic soft-start time of 500 μ s. As the soft-start function is implemented by simple circuitry, the final timing depends on non-linear functions, where accurate determination of the soft-start timing is impossible. However, for simplicity, the empirical formula below can be used to estimate the soft-start time with respect to the value of the external capacitor.

$$t_{SS} \text{ in } \mu\text{s} \approx 50 \times C_{SS} \text{ in pF} + 500 \mu\text{s}$$

Current Mode Pulse-Width Modulation (PWM) Control Scheme

With the SYN pin (pin 2) connected to V_{IN}, the converter will set to operate at constant switching frequency PWM mode. NCP1530 uses peak current mode control scheme to achieve good line and load regulation. The high switching frequency, 600 kHz, and a carefully compensated internal control loop, allows the use of low profile small value ceramic type input and output capacitor for stable operation. In current mode operation, the required ramp function is generated by sensing the inductor current (ISEN) and comparing with the voltage loop error amplifier (OTA) output. The OTA output is derived from feedback from the output voltage pin (V_{OUT} – Pin 6) and the internal reference voltage (V_{REF} – Pin 7). See Figure 2. On a cycle-by-cycle basis, the duty cycle is controlled to keep the output voltage within regulation. The current mode approach has outstanding line regulation performance and good overall system stability. Additionally, by monitoring the inductor current, a cycle-by-cycle current limit protection is implemented. Constant Frequency PWM scheme reduces output ripple and noise, which is one of the important characteristics for noise sensitive communication applications. The high switching frequency allows the use of small size surface mount components that saves significant PC board area and improves layout compactness and EMI performance.

Power Saving Pulse–Frequency–Modulation (PFM) Control Scheme

With the SYN pin (pin 2) connected to ground or left open, the converter will operate in PWM/PFM auto mode. Under this operating mode, NCP1530 will stay in constant frequency PWM operation in moderate to heavy load conditions. When the load decreases down to a threshold point, the operation will switch to the power saving PFM operation automatically. The switchover mechanism depends on the input voltage, output voltage and the inductor current level. The mode change circuit will determine whether the converter should be operated in PWM or PFM mode. In order to maintain stable and smooth switching mode transition, a small hysteresis on the load current level for mode transition was implemented. The detailed mode transition characteristics for each voltage option are illustrated in Figures 11 and 14. PFM mode operation provides high conversion efficiency even at very light loading conditions. In PFM mode, most of the circuits inside the device will be turned off and the converter operates just as a simple voltage hysteretic converter. When the load current increases, the converter returns to PWM mode automatically.

External Synchronization Control

The NCP1530 has an internal fixed frequency oscillator of 600 kHz or can be synchronized to an external clock signal at SYN pin (pin 2). Connecting the SYN pin with an external clock signal will force the converter to operate in a pure PWM mode and the switching frequency will be synchronized. The external clock signal should be in the range of 600 kHz to 1.2 MHz and the pulse width should not be less than 300 ns. The detection of the pulse train is edge sensitive and independent of duty ratio. In the case where the external clock frequency is too low, the detection circuit may not be able to follow and will treat it as a disturbance, thus affecting the converters normal operation. The internal control circuit detects the rising edge of the pulse train and the switching frequency synchronized to the external clock signal. If the external clock signal ceases for several clock cycles, the converter will switch back to use the internal oscillator automatically.

Power Saving Shutdown Mode

NCP1530 can be disabled whenever the EN pin (pin 5) is tied to ground. In shutdown mode, the internal reference, oscillator and most of the control circuitries are turned off. With the device put in shutdown mode, the device current consumption will be as low as 0.5 μ A (typ).

Input Undervoltage Lockout Protection (UVLO)

To prevent the P–Channel MOSFETs from operating below safe input voltage levels, an Undervoltage Lockout protection is incorporated in NCP1530. Whenever the input voltage, V_{IN} drops below approximately 2.0 V, the protection circuitry will be activated and the converter operation will be stopped.

Output Overvoltage Protection (OVP)

In order to prevent the output voltage from going to high (when the load current is close to zero in a pure PWM mode and other abnormal conditions), an Output Overvoltage protection circuit is included in the NCP1530. In case the output voltage is higher than its nominal level by more than 12% maximum, the protection circuitry will stop the switching immediately.

Internal Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. The protection will be activated at about 145°C with a hysteresis of 15°C. This feature is provided to prevent failures from unexpected overheating.

Input Capacitor Selection

For a PWM converter operating in continuous current mode, the input current of the converter is a square wave with a duty ratio of approximately V_{OUT}/V_{IN} . The pulsating nature of the input current transient can be a source of EMI noise and system instability. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly. The capacitance needed for the input bypass capacitor depends on the source impedance of the input supply. For NCP1530, a low ESR, low profile ceramic capacitor of 22 μ F can be used for most of the cases. For effective bypass results, the input capacitor should be placed just next to V_{IN} pin (pin 1) whenever it is possible.

Inductor Value Selection

Selecting the proper inductance for the power inductor is a trade-off between inductor's physical sizes, transient response, power delivering capability, output voltage ripple and power conversion efficiency. Low value inductor saves cost, PC board space and provides fast transient response, however suffers high inductor ripple current, core loss and lower overall conversion efficiency. The relationship between the inductance and the inductor ripple current is given by the equation in below.

$$L = \frac{T_{ON}(V_{IN} - R_{DS(ON)} \times I_{OUT} - V_{OUT})}{I_{L\_RIPPLE(P-P)}}$$

Where L is the inductance required;

T_{ON} is the nominal ON time within a switching cycle;

$R_{DS(ON)}$ is the ON resistance of the internal MOSFET;

V_{IN} is the worst-case input voltage;

V_{OUT} is the output voltage;

I_{OUT} is the maximum allowed loading current;

$I_{L\_RIPPLE(P-P)}$ is the acceptable inductor current ripple level.

For ease of application, the previous equation was plotted in Figure 35 to help end user to select the right inductor for specific application. As a rule of thumb, the user needs to be aware of the maximum peak inductor current and should be designed not to exceed the saturation limit of the inductor selected. Low inductance can supply higher output current, but suffers higher output ripple and reduced efficiency, but it limits the output current capability. On the other hand, high inductance can improve output ripple and efficiency, at the same time, it also limits the output current capability. One other critical parameter of the inductor is its DC resistance. This resistance can introduce unwanted power loss and hence reduce overall efficiency. The basic rule is selecting an inductor with lowest DC resistance within the board space limitation.

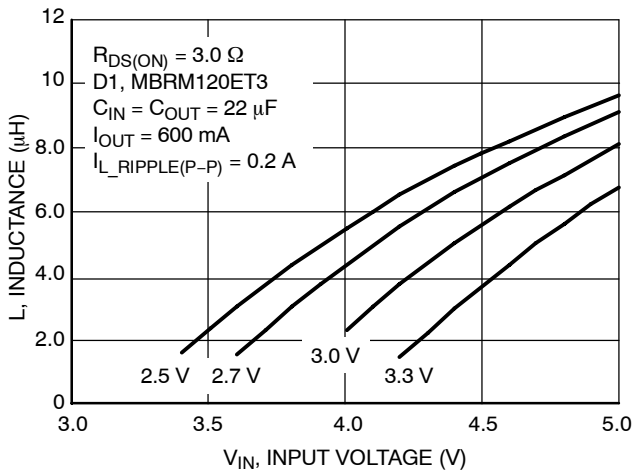


Figure 35. Inductor Selection Chart

Flywheel Diode Selection

The flywheel diode is turned on and carries load current during the off time. At high input voltages, the diode conducts most of the time. In the case where V_{IN} approaches V_{OUT} , the diode conducts only a small fraction of the cycle. While the output terminals are shorted, the diode will be subject to its highest stress. Under this condition, the diode must be able to safely handle the peak current circulating in the loop. So, it is important to select a flywheel diode that can meet the diode peak current and average power dissipation requirements. Under normal conditions, the average current conducted by the flywheel diode is given by,

$$I_D = \frac{V_{IN} - V_{OUT}}{V_{IN} + V_F} \times I_{OUT}$$

Where I_D is the average diode current and V_F is the forward voltage drop of the diode.

A low forward voltage drop and fast switching diode must also be used to optimize converter efficiency. Schottky diodes are a good choice for low forward drop and fast switching times.

Output Capacitor Selection

Selection of the output capacitor, C_{OUT} is primarily governed by the required effective series resistance (ESR) of the capacitor. Typically, once the ESR requirement is met, the capacitance will be adequate for filtering. The output voltage ripple, V_{RIPPLE} is approximated by,

$$V_{RIPPLE} \approx I_{L\_RIPPLE(P-P)} \times \left(ESR + \frac{1}{4 \times F_{OSC} C_{OUT}} \right)$$

Where F_{OSC} is the switching frequency and ESR is the effective series resistance of the output capacitor.

From equation in above, it can be noted that the output voltage ripple is contributed to by two parts. For most of the cases, the major contributor is the capacitor's ESR. Ordinary aluminum-electrolytic capacitors have high ESR and should be avoided. High quality Low ESR aluminum-electrolytic capacitors are acceptable and relatively inexpensive. Low ESR tantalum capacitors are another alternative. For even better performance, surface mounted ceramic capacitors can be used. Ceramic capacitors have lowest ESR among all choices. The NCP1530 is internally compensated for stable operation with low ESR ceramic capacitors. However, ordinary multi-layer ceramic capacitors have poor temperature and frequency performance, for switching applications, so only high quality, grade X5R and X7R ceramic capacitors can be used.

PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise and unwanted feedbacks that can affect the performance of the converter. Hints suggested below can be used as a guideline in most situations.

Grounding

Star-ground connection should be used to connect the output power return ground, the input power return ground and the device power ground together at one point. All high current running paths must be thick enough for current flowing through and producing insignificant voltage drop along the path.

Components Placement

Power components, i.e. input capacitor, inductor and output capacitor, must be placed as close together as possible. All connecting traces must be short, direct and thick. High current flowing and switching paths must be kept away from the feedback (V_{OUT} , pin 6) terminal to avoid unwanted injection of noise into the feedback path.

Feedback Path

Feedback of the output voltage must be a separate trace separated from the power path. The output voltage sensing trace to the feedback (V_{OUT} , pin 6) pin should be connected to the output voltage directly at the anode of the output capacitor.

NCP1530

ORDERING INFORMATION

Device	Output Voltage	Device Marking	Package	Shipping [†]
NCP1530DM25R2	2.5 V	DAAA	Micro8	4000 Units Per 7 Inch Reel
NCP1530DM27R2	2.7 V	DAAB		
NCP1530DM30R2	3.0 V	DAAC		
NCP1530DM30R2G	3.0 V	DAAC	Micro8 (Pb-Free)	
NCP1530DM33R2	3.3 V	DAAD	Micro8	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: The ordering information lists four standard output voltage device options. Additional device with output voltage ranging from 2.5 V to 3.5 V in 100 mV increments can be manufactured. Contact your ON Semiconductor representative for availability.

NCP1550

600 kHz PWM/PFM Step-Down DC-DC Controller

The NCP1550 is a monolithic micropower high frequency voltage mode step-down controller IC, specially designed for battery operated hand-held electronic products. With appropriate external P-type MOSFET, the device can provide up to 2.0 A loading current with high conversion efficiency. The device operates in Constant-Frequency PWM mode at normal operation, that ensures low output ripple noise, and which will automatically switch to PFM mode at low output loads for higher efficiency. Additionally, value-added features of Chip Enable to reduce IC Off-State current and integrated feedback resistor network, make it the best choice for portable applications. The device is designed to operate for voltage regulation with minimum external components and board space. This device is available in a TSOP-5 package with six standard output voltage options.

Features

- Pb-Free Packages are Available
- High Efficiency 92%, Typical
- Low Quiescent Bias Current of 50 μ A (Typical at PFM Mode with No Load)
- Output Voltage Options from 1.8 V to 3.3 V with High Accuracy $\pm 2.0\%$
- Low Output Voltage Ripple, 50 mV, Typical
- PWM Switching Frequency at 600 kHz
- Automatic PWM/PFM Switchover at Light Load Condition
- Very Low Dropout Operation, 100% Max. Duty Cycle
- Chip Enable Pin with On-Chip 150 nA Pullup Current Source
- Low Shutdown Current, 0.3 μ A, Typical
- Input Voltage Range from 2.45 V to 5.5 V
- Built-in Soft-Start
- Internal Undervoltage Lockout (UVLO) Protection
- Low Profile and Minimum External Components
- Micro Miniature TSOP-5 Package

Typical Applications

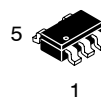
- Personal Digital Assistant (PDA)
- Camcorders and Digital Still Camera
- Hand-Held Instrument
- Distributed Power System
- Computer Peripheral
- Conversion from Four NiMH or NiCd or One Lithium-ion Cells to 3.3 V/1.8 V



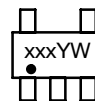
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MARKING DIAGRAM

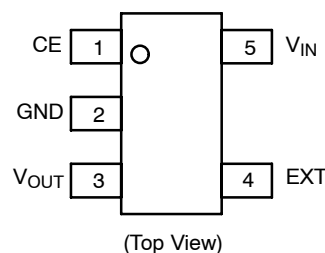


**TSOP-5
SN SUFFIX
CASE 483**



xxx = Device Code
Y = Year
W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 482 of this data sheet.

NCP1550

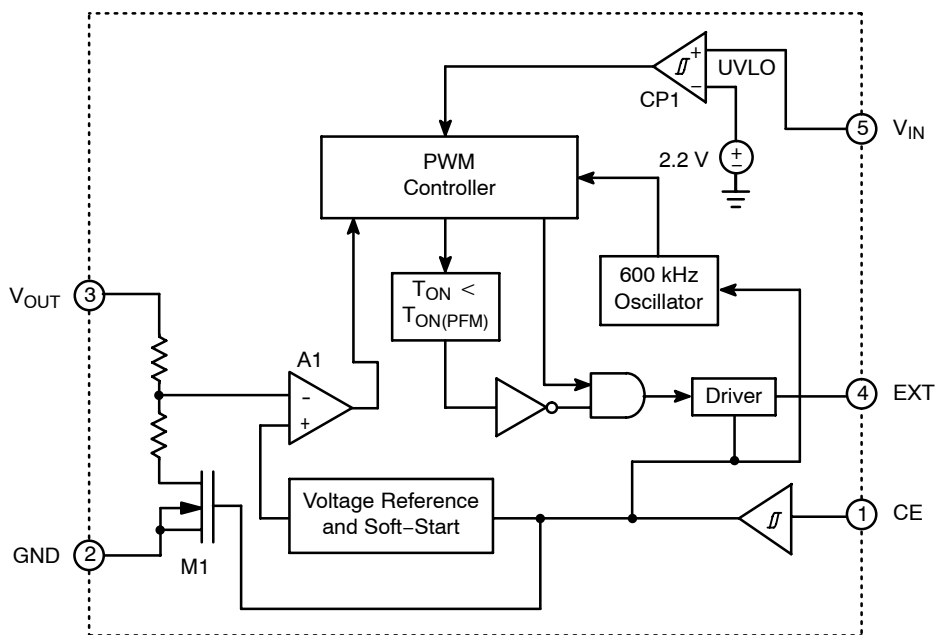


Figure 1. Simplified Block Diagram

PIN FUNCTION DESCRIPTIONS

Pin	Symbol	Description
1	CE	Chip Enable pin, active high (internal pullup current source). By connecting this pin to GND, the switching operation of the controller will be stopped.
2	GND	Ground Connection
3	V _{OUT}	Output voltage monitoring input. This pin must be connected to the regulated output node as a feedback to on-chip control circuitry. V _{OUT} is internally connected to the on-chip voltage divider that determines the output voltage level.
4	EXT	Gate drive for external P-MOSFET
5	V _{IN}	Power supply input

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Device Power Supply, V_{IN} (Pin 5)	V_{IN}	−0.3 to 6.0	V
Input/Output Pins CE (Pin 1) V_{OUT} (Pin 3) EXT (Pin 4)	V_{CE} V_{OUT} V_{EXT}	−0.3 to 6.0 −0.3 to 6.0 −0.3 to 6.0	V
Thermal Characteristics TSOP−5 Plastic Package, Case 483−01 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	250	°C/W
Operating Junction Temperature Range	T_J	−40 to +150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

NOTE: ESD data available upon request.

10. This device series contains ESD protection and exceeds the following tests:
Human Body Model (HBM) ± 2.0 kV per JEDEC standard: JESD22-A114.

Machine Model (MM) $\pm 200V$ per JEDEC standard: JESD22-A115.

11. Latchup Current Maximum Rating: 150 mA per JEDEC standard: JESD78.

12. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.

NCP1550

ELECTRICAL CHARACTERISTICS ($V_{IN} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$ for typical value, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for min/max values unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
TOTAL DEVICE					
Input Voltage	V_{IN}	2.45	–	5.50	V
Output Voltage ($I_{LOAD} = 0\text{ mA}$, $T_A = 25^\circ\text{C}$)	V_{OUT}				V
NCP1550SN18T1		1.764	1.8	1.836	
NCP1550SN19T1		1.862	1.9	1.938	
NCP1550SN25T1		2.450	2.5	2.550	
NCP1550SN27T1		2.646	2.7	2.754	
NCP1550SN30T1		2.940	3.0	3.060	
NCP1550SN33T1		3.234	3.3	3.366	
Input Current into V_{OUT} Pin	I_{VOUT}				μA
NCP1550SN18T1		–	2.5	4.0	
NCP1550SN19T1		–	2.5	4.0	
NCP1550SN25T1		–	2.5	4.0	
NCP1550SN27T1		–	2.5	4.0	
NCP1550SN30T1		–	2.5	4.0	
NCP1550SN33T1		–	2.5	4.0	
Temperature Coefficient	$\Delta V_{OUT}/\Delta T$	–	100	–	ppm/ $^\circ\text{C}$
Operating Current ($V_{IN} = 5.0\text{ V}$, $V_{CE} = 5.0\text{ V}$, No External Components)	I_{DD}				μA
NCP1550SN18T1		–	50	80	
NCP1550SN19T1		–	50	80	
NCP1550SN25T1		–	50	80	
NCP1550SN27T1		–	50	80	
NCP1550SN30T1		–	50	80	
NCP1550SN33T1		–	50	80	
Off-State Current ($V_{IN} = 5.0\text{ V}$, $V_{CE} = 0\text{ V}$, $T_A = 25^\circ\text{C}$)	I_{OFF}				μA
NCP1550SN18T1		–	0.3	0.5	
NCP1550SN19T1		–	0.3	0.5	
NCP1550SN25T1		–	0.3	0.5	
NCP1550SN27T1		–	0.3	0.5	
NCP1550SN30T1		–	0.3	0.5	
NCP1550SN33T1		–	0.3	0.5	

OSCILLATOR

Frequency	F_{OSC}	510	600	690	kHz
Frequency Temperature Coefficient ($T_A = -40^\circ\text{C}$ to 85°C)	$\Delta F_{OSC}/\Delta T_A$	–	0.11	–	%/ $^\circ\text{C}$
Maximum Duty Cycle	D_{MAX}	100	–	–	%
PWM/PFM Switchover ON Time Threshold (Note 13)	$T_{ON(PFM)}$	167	320	500	ns
Soft-Start Delay Time (Note 13)	T_{SS}	–	8.0	–	ms
Protection Delay Time (Auto Restart)	T_{prot}	–	8.0	–	ms

OUTPUT DRIVE (PIN 4)

EXT “H” Output Current ($V_{EXT} = V_{IN} - 0.4\text{ V}$)	I_{EXTH}	–	–60	–	mA
EXT “L” Output Current ($V_{EXT} = 0.4\text{ V}$)	I_{EXTL}	–	100	–	mA
EXT “L–H” Rise Time ($C_{LOAD} = 1000\text{ pF}$) ($V_{IN} = 5.0\text{ V}$)	T_r	–	65	–	ns
EXT “H–L” Fall Time ($C_{LOAD} = 1000\text{ pF}$) ($V_{IN} = 5.0\text{ V}$)	T_f	–	40	–	ns
EXT “L–H” Rise Time ($C_{LOAD} = 5.0\text{ nF}$) ($V_{IN} = 5.0\text{ V}$)	T_r	–	140	–	ns
EXT “H–L” Fall Time ($C_{LOAD} = 5.0\text{ nF}$) ($V_{IN} = 5.0\text{ V}$)	T_f	–	90	–	ns

13. PWM/PFM Switchover ON Time Threshold min/max guaranteed by design only.

NCP1550

ELECTRICAL CHARACTERISTICS (continued) ($V_{IN} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$ for typical value, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for min/max values unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CE (PIN 1)					
CE "H" Input Voltage	V_{CEH}	1.3	–	–	V
CE "L" Input Voltage	V_{CEL}	–	–	0.3	V
CE "H" Input Current ($V_{IN} = V_{CE} = 5.0\text{ V}$)	I_{CEH}	–0.5	0	0.5	μA
CE "L" Input Current ($V_{IN} = 5.0$, $V_{CE} = 0\text{ V}$)	I_{CEL}	–0.5	0.15	0.5	μA
Undervoltage Lockout					
Undervoltage Lockout Threshold	V_{UVLO}	1.60	2.20	2.40	V
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	–	50	–	mV

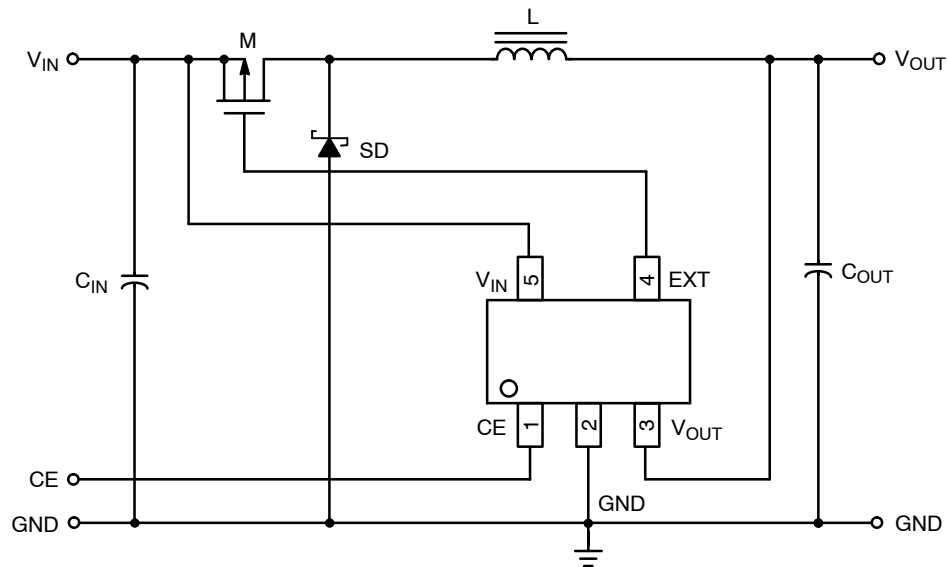


Figure 2. Typical Application Diagram

NCP1550

TYPICAL OPERATING CHARACTERISTICS

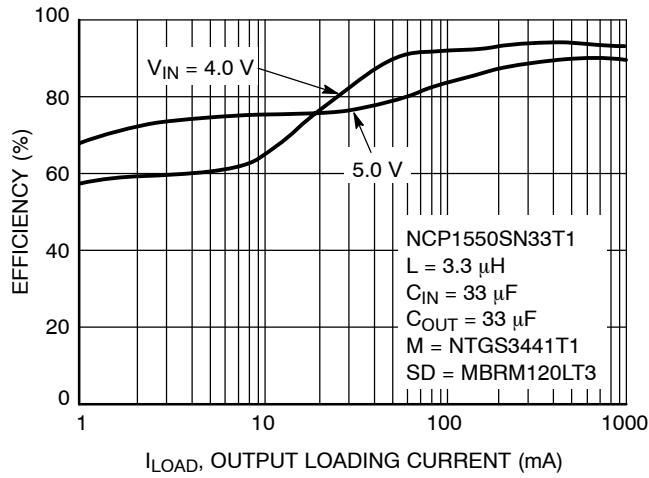


Figure 3. Efficiency versus Load Current

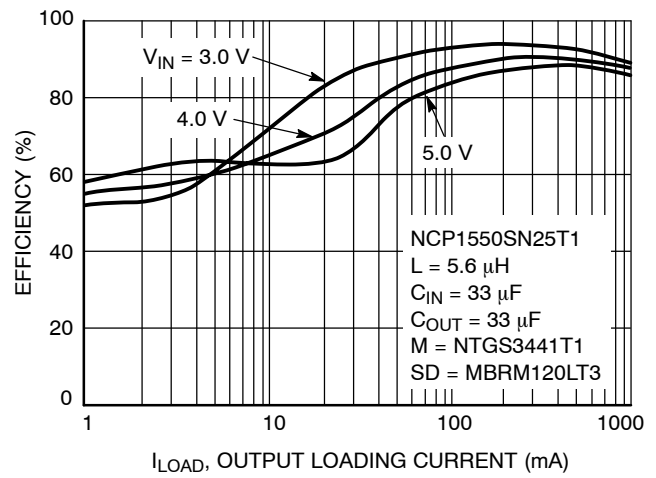


Figure 4. Efficiency versus Load Current

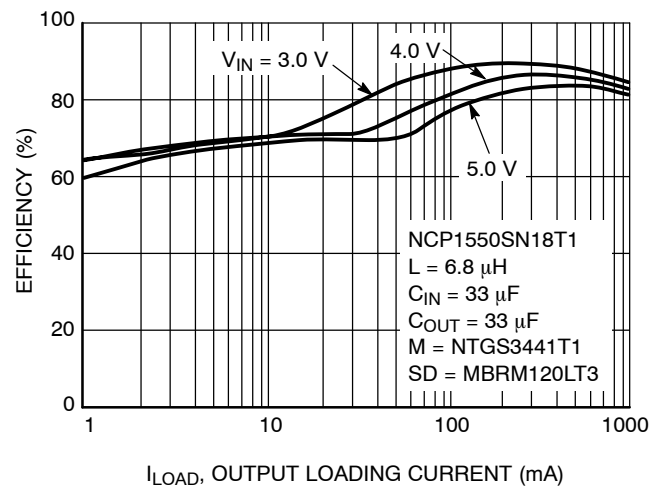


Figure 5. Efficiency versus Load Current

TYPICAL OPERATING CHARACTERISTICS

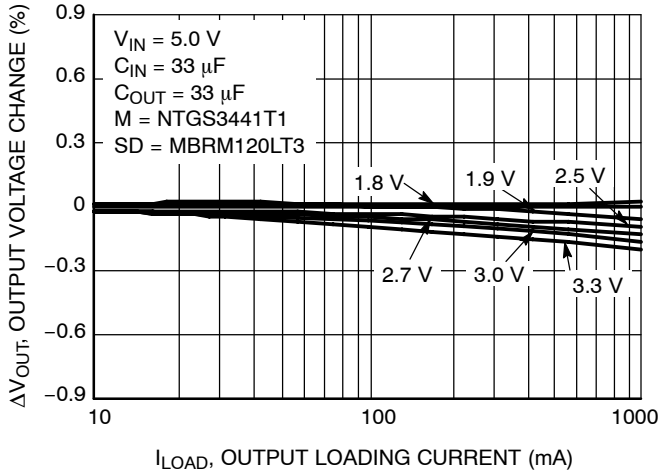


Figure 6. Output Voltage Change versus Load Current

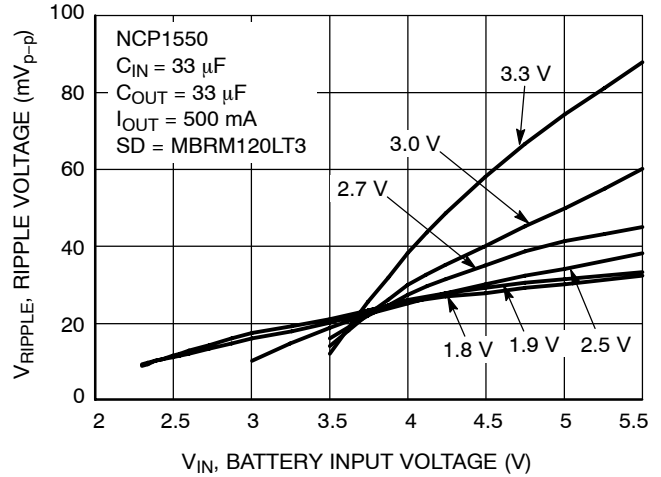


Figure 7. Output Ripple Voltage versus Input Voltage

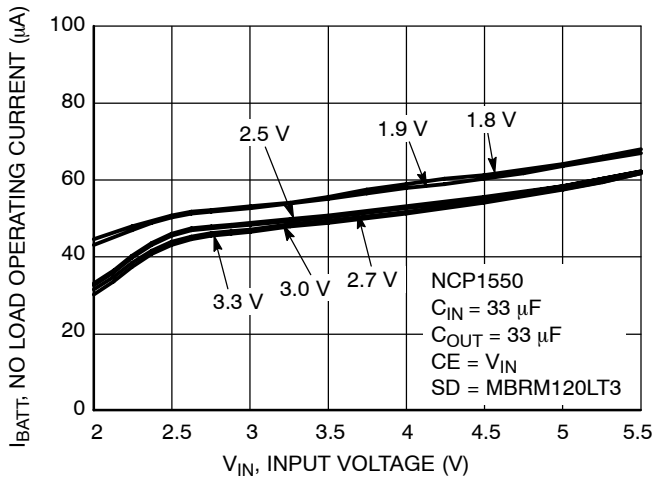


Figure 8. No Load Operating Current versus Input Voltage

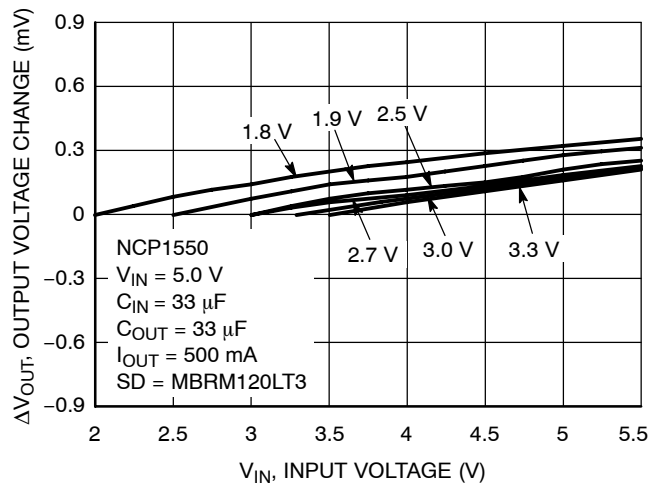


Figure 9. Output Voltage Change versus Input Voltage

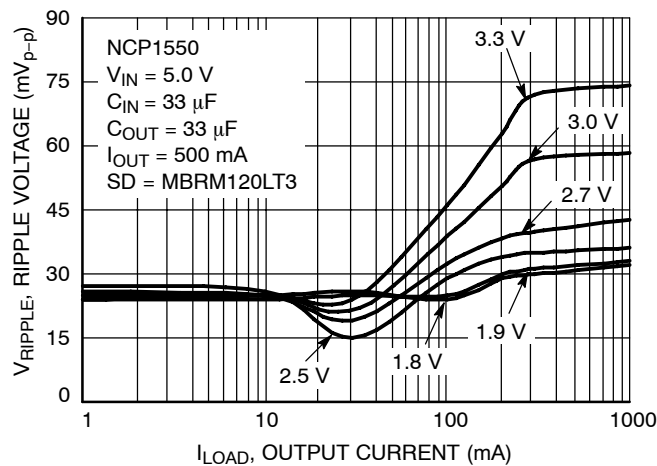
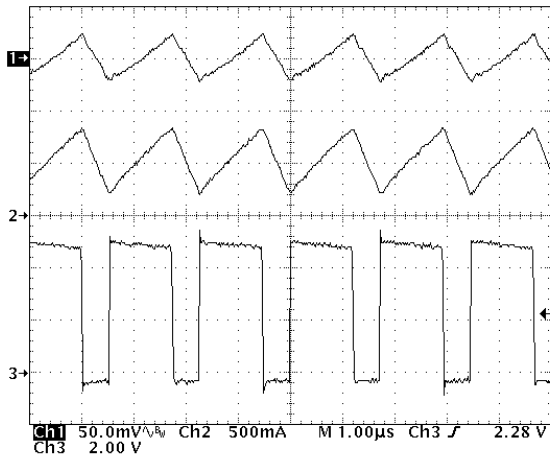


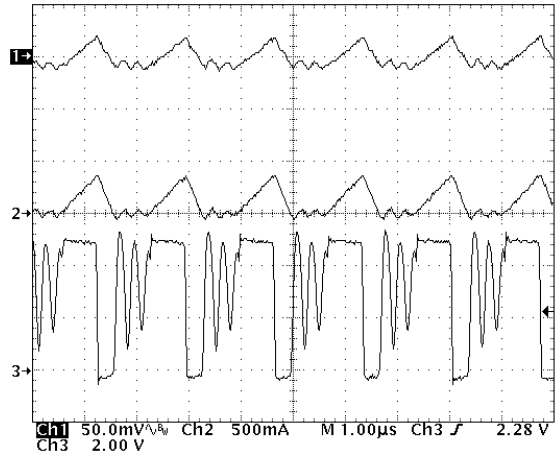
Figure 10. Output Ripple Voltage versus Output Current



($V_{IN} = 5.0 \text{ V}$, $I_{LOAD} = 500 \text{ mA}$, $L = 3.3 \mu\text{H}$, $C_{OUT} = 100 \mu\text{F}$)

Upper Trace: Output Voltage Ripple, 50 mV/Division
Middle Trace: Inductor Current, I_L , 500 mA/Division
Lower Trace: Voltage at Cathode of Schottky Diode, 2.0 V/Division

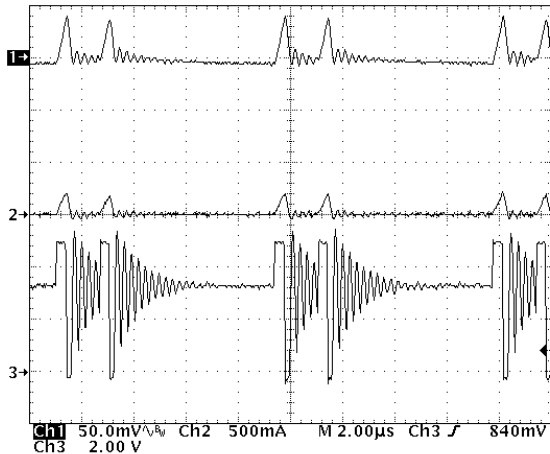
Figure 11. Continuous Conduction Mode PWM Switching Waveform for $V_{OUT} = 3.3 \text{ V}$



($V_{IN} = 5.0 \text{ V}$, $I_{LOAD} = 100 \text{ mA}$, $L = 3.3 \mu\text{H}$, $C_{OUT} = 100 \mu\text{F}$)

Upper Trace: Output Voltage Ripple, 50 mV/Division
Middle Trace: Inductor Current, I_L , 500 mA/Division
Lower Trace: Voltage at Cathode of Schottky Diode, 2.0 V/Division

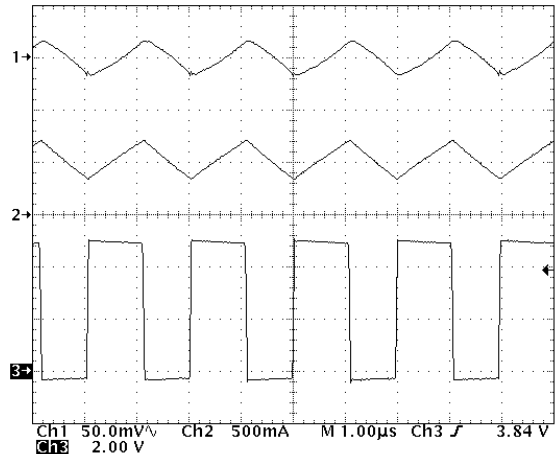
Figure 12. Discontinuous Conduction Mode PWM Switching Waveform for $V_{OUT} = 3.3 \text{ V}$



($V_{IN} = 5.0 \text{ V}$, $I_{LOAD} = 10 \text{ mA}$, $L = 3.3 \mu\text{H}$, $C_{OUT} = 100 \mu\text{F}$)

Upper Trace: Output Voltage Ripple, 50 mV/Division
Middle Trace: Inductor Current, I_L , 500 mA/Division
Lower Trace: Voltage at Cathode of Schottky Diode, 2.0 V/Division

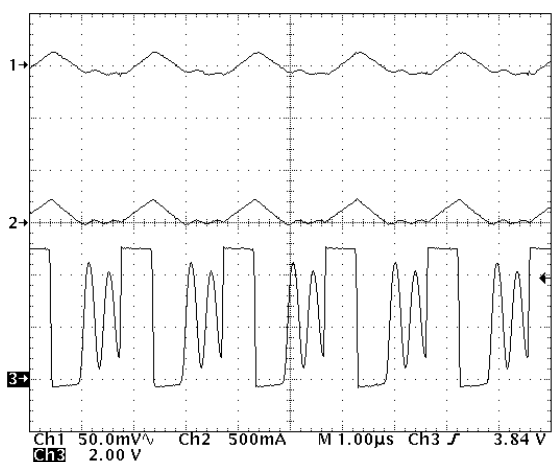
Figure 13. Discontinuous Conduction Mode PFM Switching Waveform for $V_{OUT} = 3.3 \text{ V}$



($V_{IN} = 5.0 \text{ V}$, $I_{LOAD} = 500 \text{ mA}$, $L = 5.6 \mu\text{H}$, $C_{OUT} = 33 \mu\text{F}$)

Upper Trace: Output Voltage Ripple, 50 mV/Division
Middle Trace: Inductor Current, I_L , 500 mA/Division
Lower Trace: Voltage at Cathode of Schottky Diode, 2.0 V/Division

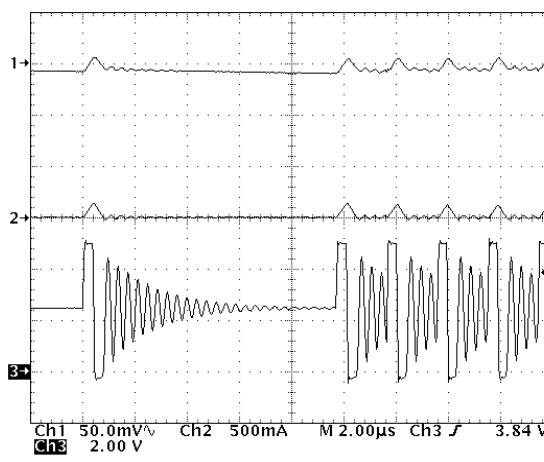
Figure 14. Continuous Conduction Mode PWM Switching Waveform for $V_{OUT} = 2.5 \text{ V}$



($V_{IN} = 5.0 \text{ V}$, $I_{LOAD} = 100 \text{ mA}$, $L = 5.6 \mu\text{H}$, $C_{OUT} = 33 \mu\text{F}$)

Upper Trace: Output Voltage Ripple, 50 mV/Division
Middle Trace: Inductor Current, I_L , 500 mA/Division
Lower Trace: Voltage at Cathode of Schottky Diode, 2.0 V/Division

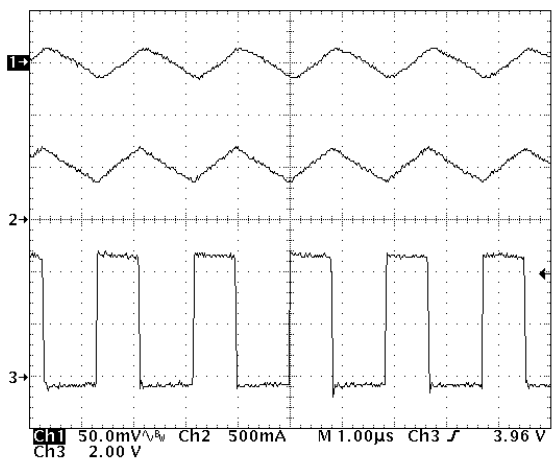
Figure 15. Discontinuous Conduction Mode PWM Switching Waveform for $V_{OUT} = 2.5 \text{ V}$



($V_{IN} = 5.0 \text{ V}$, $I_{LOAD} = 30 \text{ mA}$, $L = 5.6 \mu\text{H}$, $C_{OUT} = 33 \mu\text{F}$)

Upper Trace: Output Voltage Ripple, 50 mV/Division
Middle Trace: Inductor Current, I_L , 500 mA/Division
Lower Trace: Voltage at Cathode of Schottky Diode, 2.0 V/Division

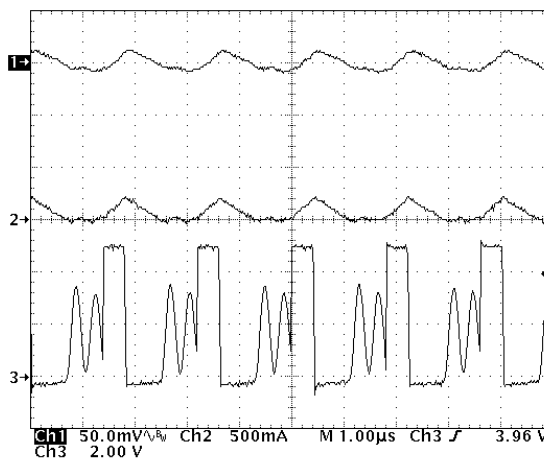
Figure 16. Discontinuous Conduction Mode PFM Switching Waveform for $V_{OUT} = 2.5 \text{ V}$



($V_{IN} = 5.0 \text{ V}$, $I_{LOAD} = 500 \text{ mA}$, $L = 6.8 \mu\text{H}$, $C_{OUT} = 33 \mu\text{F}$)

Upper Trace: Output Voltage Ripple, 50 mV/Division
Middle Trace: Inductor Current, I_L , 500 mA/Division
Lower Trace: Voltage at Cathode of Schottky Diode, 2.0 V/Division

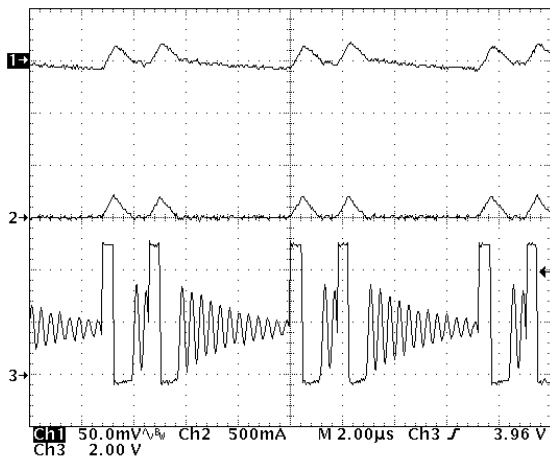
Figure 17. Continuous Conduction Mode PWM Switching Waveform for $V_{OUT} = 1.8 \text{ V}$



($V_{IN} = 5.0 \text{ V}$, $I_{LOAD} = 60 \text{ mA}$, $L = 6.8 \mu\text{H}$, $C_{OUT} = 33 \mu\text{F}$)

Upper Trace: Output Voltage Ripple, 50 mV/Division
Middle Trace: Inductor Current, I_L , 500 mA/Division
Lower Trace: Voltage at Cathode of Schottky Diode, 2.0 V/Division

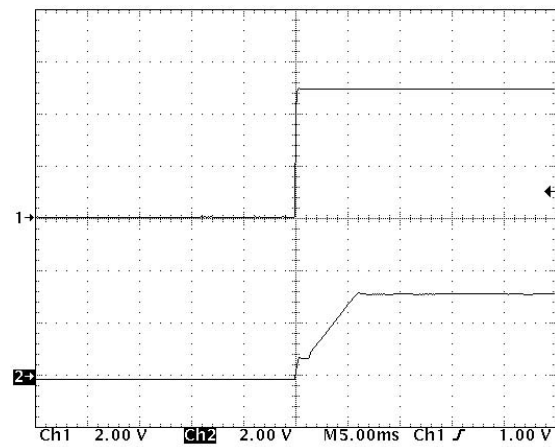
Figure 18. Discontinuous Conduction Mode PWM Switching Waveform for $V_{OUT} = 1.8 \text{ V}$



($V_{IN} = 5.0 \text{ V}$, $I_{LOAD} = 30 \text{ mA}$, $L = 6.8 \mu\text{H}$, $C_{OUT} = 33 \mu\text{F}$)

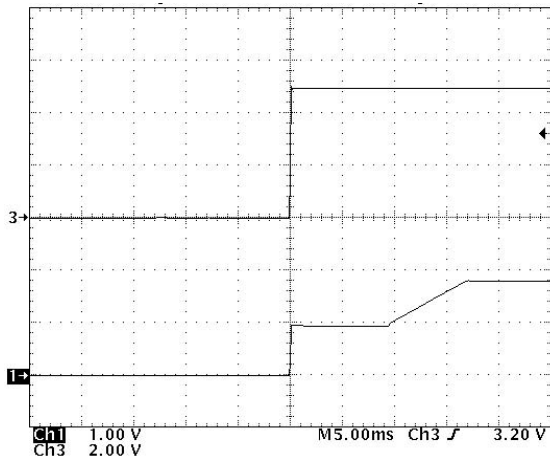
Upper Trace: Output Voltage Ripple, 50 mV/Division
Middle Trace: Inductor Current, I_L , 500 mA/Division
Lower Trace: Voltage at Cathode of Schottky Diode, 2.0 V/Division

Figure 19. Discontinuous Conduction Mode PFM Switching Waveform for $V_{OUT} = 1.8 \text{ V}$



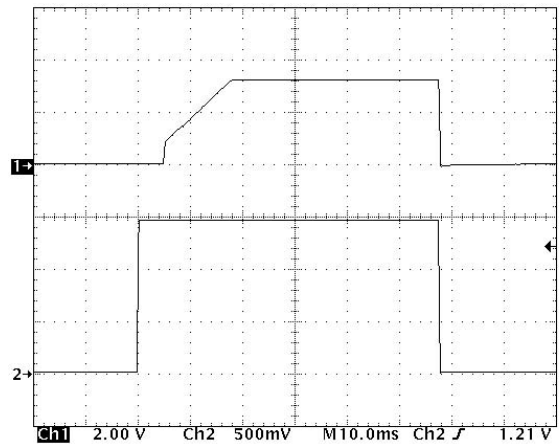
Upper Trace: Input Voltage, 2.0 V/Division
Lower Trace: Output Voltage, 2.0 V/Division

Figure 20. Startup Transient Response for $V_{OUT} = 3.3 \text{ V}$



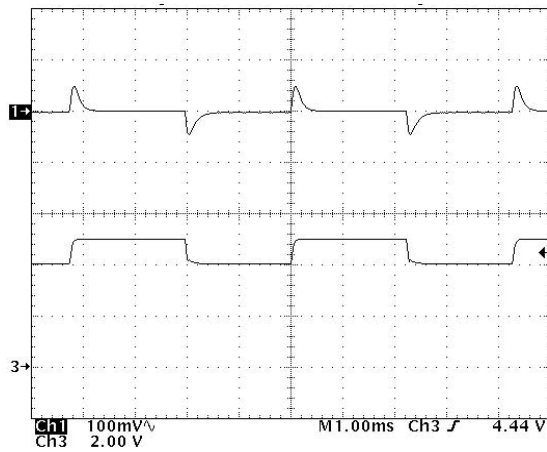
Upper Trace: Input Voltage, 2.0 V/Division
Lower Trace: Output Voltage, 1.0 V/Division

Figure 21. Startup Transient Response for $V_{OUT} = 1.8 \text{ V}$



Upper Trace: Output Voltage Waveform, 2.0 V/Division
Lower Trace: Chip Enable/Disable Pin Waveform, 0.5 V/Division

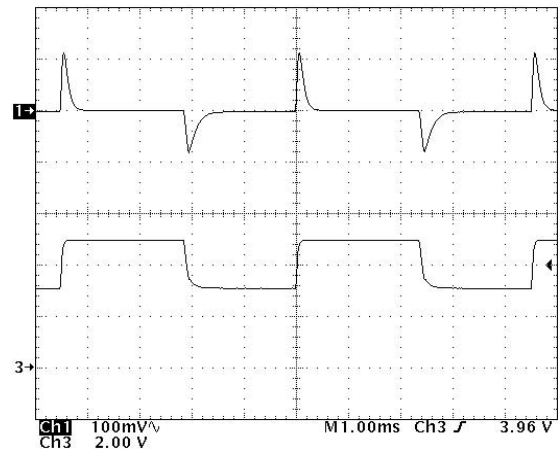
Figure 22. Chip Enable/Disable Output Voltage Waveform



($V_{IN} = 4.0$ to 5.0 V, $L = 3.3$ μ H, $C_{OUT} = 33$ μ F, $I_{LOAD} = 1.0$ A)

Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Input Voltage, 2.0 V/Division

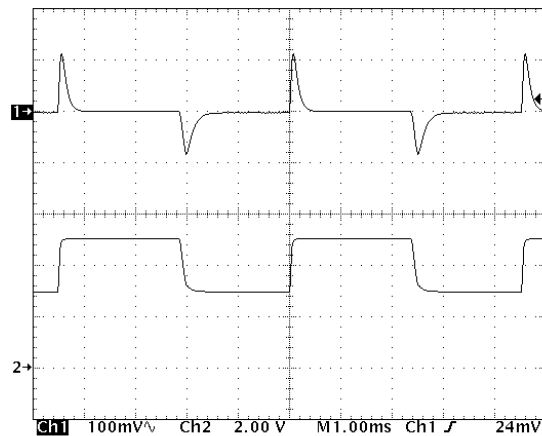
Figure 23. Line Transient Response for $V_{OUT} = 3.3$ V



($V_{IN} = 3.0$ to 5.0 V, $L = 5.6$ μ H, $C_{OUT} = 33$ μ F, $I_{LOAD} = 1.0$ A)

Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Input Voltage, 2.0 V/Division

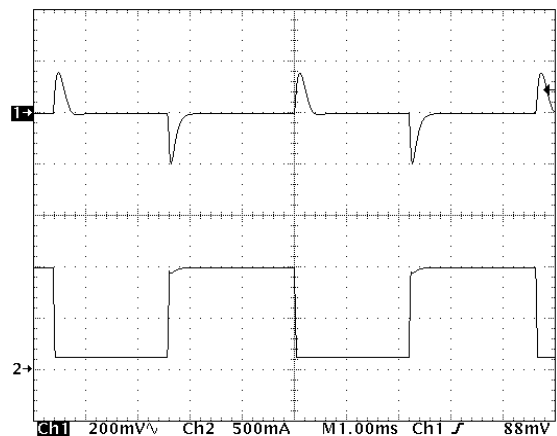
Figure 24. Line Transient Response for $V_{OUT} = 2.5$ V



($V_{IN} = 3.0$ to 5.0 V, $L = 6.8$ μ H, $C_{OUT} = 33$ μ F, $I_{LOAD} = 1.0$ A)

Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Input Voltage, V_{IN} , 2.0 V/Division

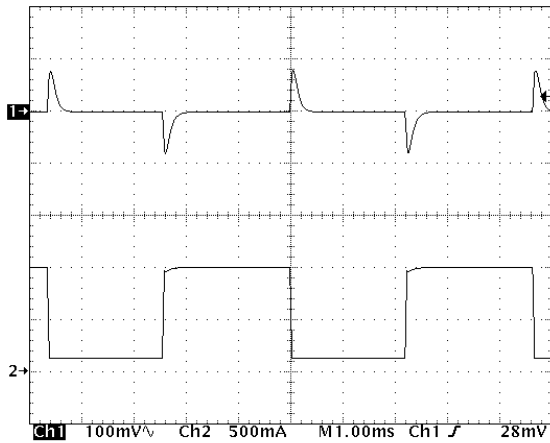
Figure 25. Line Transient Response for $V_{OUT} = 1.8$ V



($V_{IN} = 5.0$ V, $I_{LOAD} = 100$ mA to 1.0 A, $L = 3.3$ μ H, $C_{OUT} = 33$ μ F)

Upper Trace: Output Voltage Ripple, 200 mV/Division
Lower Trace: Load Current, I_{LOAD} , 500 mA/Division

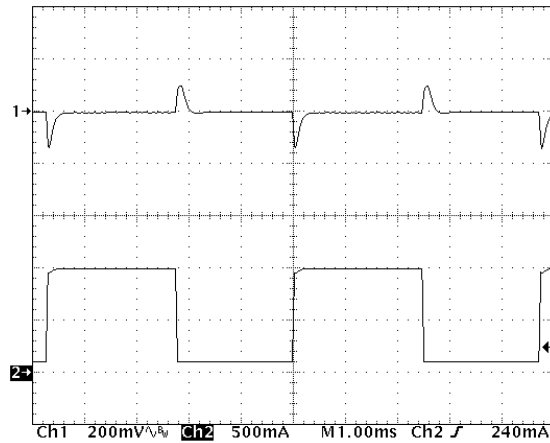
Figure 26. Load Transient Response for $V_{OUT} = 3.3$ V



($V_{IN} = 5.0 \text{ V}$, $I_{LOAD} = 100 \text{ mA to } 1.0 \text{ A}$, $L = 5.6 \mu\text{H}$, $C_{OUT} = 33 \mu\text{F}$)

Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Load Current, I_{LOAD} , 500 mA/Division

Figure 27. Load Transient Response for $V_{OUT} = 2.5 \text{ V}$



($V_{IN} = 5.0 \text{ V}$, $I_{LOAD} = 100 \text{ mA to } 1.0 \text{ A}$, $L = 6.8 \mu\text{H}$, $C_{OUT} = 33 \mu\text{F}$)

Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Load Current, I_{LOAD} , 500 mA/Division

Figure 28. Load Transient Response for $V_{OUT} = 1.8 \text{ V}$

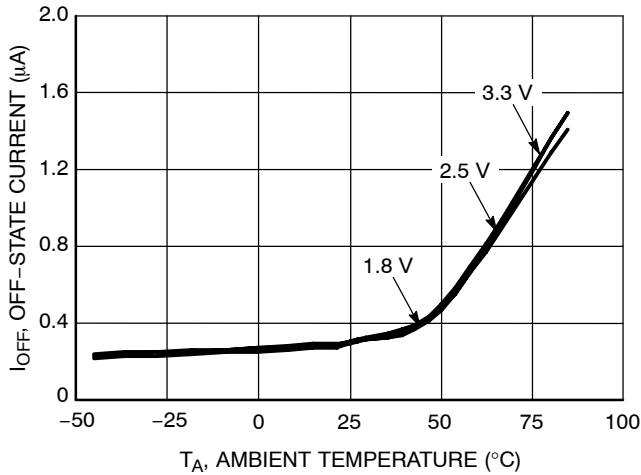


Figure 29. Off-Stage Current versus Ambient Temperature

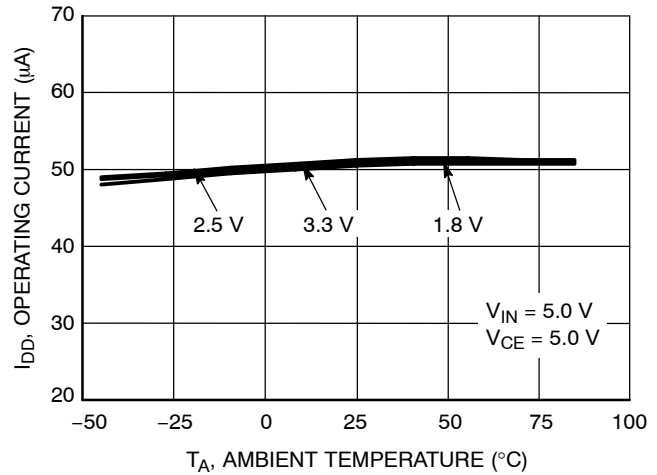


Figure 30. Operating Current versus Ambient Temperature

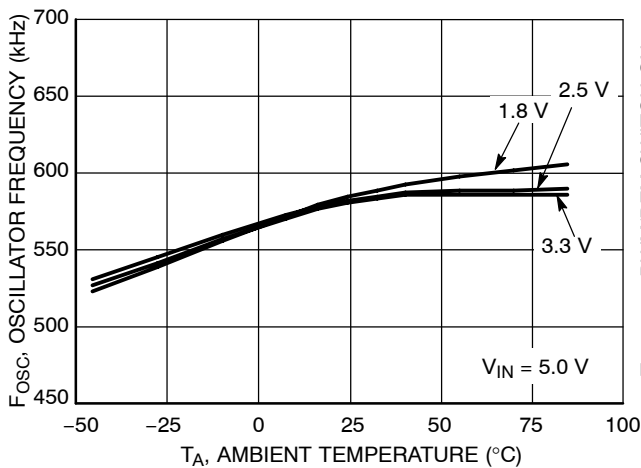


Figure 31. Oscillator Frequency versus Ambient Temperature

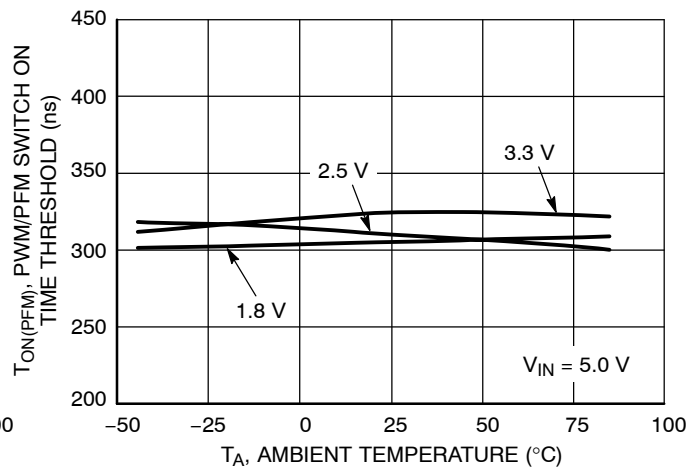


Figure 32. PWM/PFM Switch ON Time Threshold versus Ambient Temperature

NCP1550

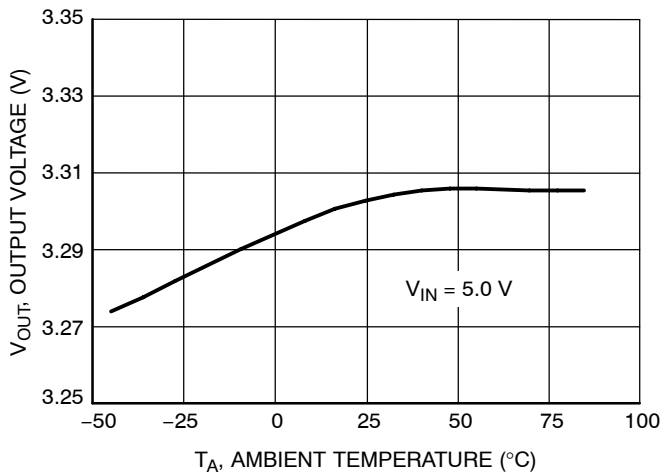


Figure 33. NCP1550SN33T1 Output Voltage versus Ambient Temperature

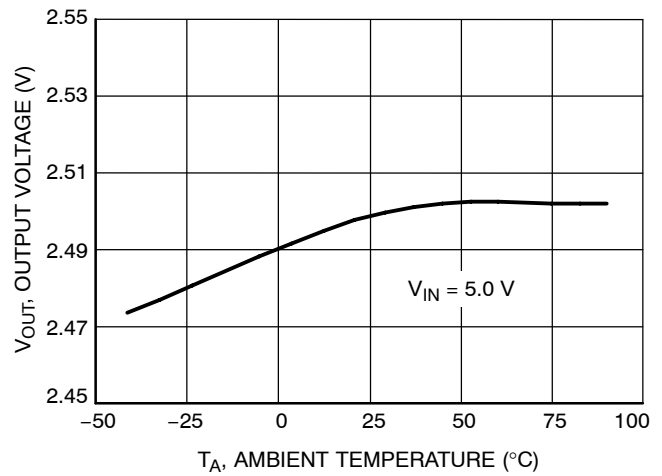


Figure 34. NCP1550SN25T1 Output Voltage versus Ambient Temperature

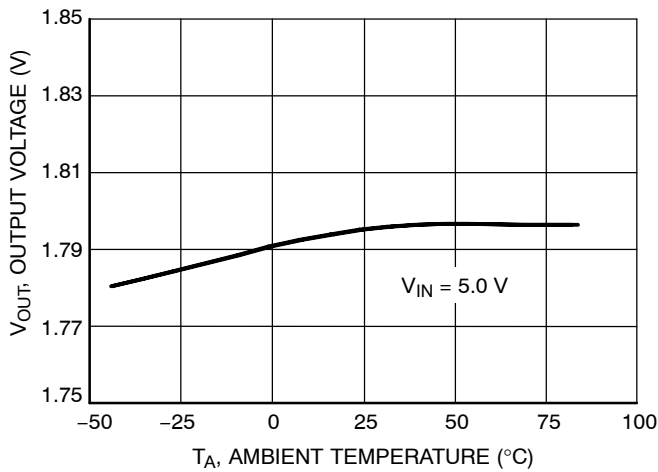


Figure 35. NCP1550SN18T1 Output Voltage versus Ambient Temperature

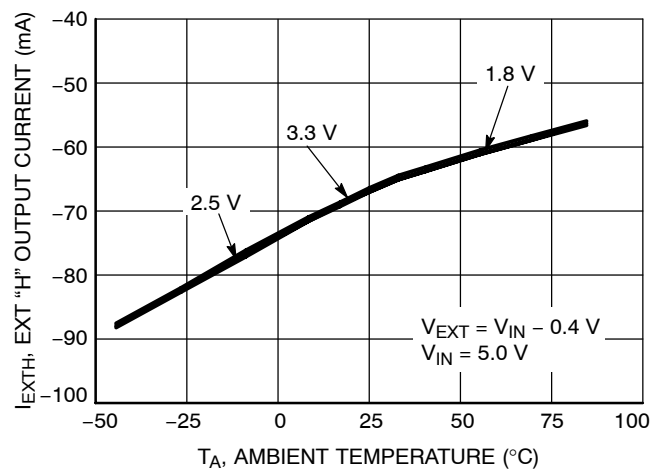


Figure 36. NCP1550 EXT "H" Output Current versus Ambient Temperature

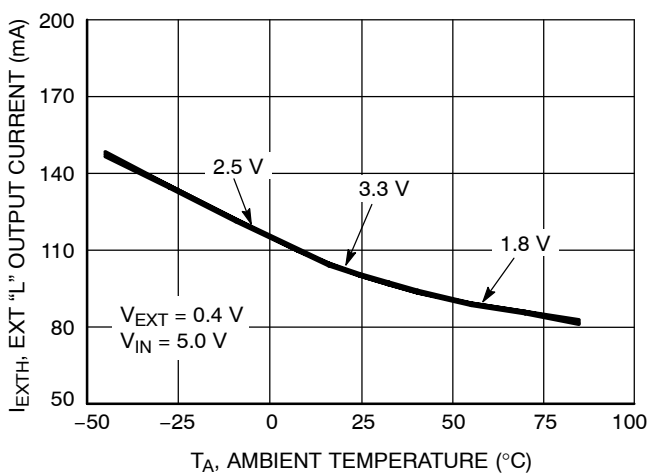


Figure 37. NCP1550 EXT "L" Output Current versus Ambient Temperature

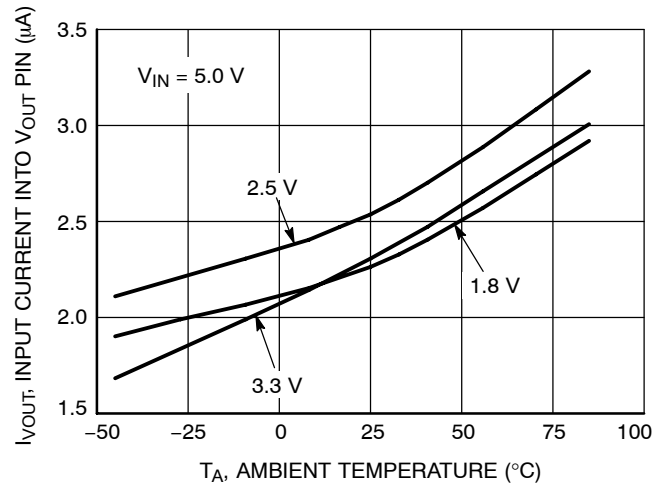


Figure 38. NCP1550 Input Current into V_{OUT} Pin versus Ambient Temperature

DETAILED OPERATING DESCRIPTION

Detailed Operating Description

The NCP1550 series are step-down (Buck) DC-DC controllers designed primarily for use in portable applications powered by battery cells. With an appropriate external P-channel MOSFET connected, the device can provide up to 2 A loading current with high conversion efficiency. The NCP1550 series using an unique control scheme combines the advantages of Pulse-Frequency-Modulation (PFM) that can provide excellent efficiency even at light loading conditions and Constant-Frequency Pulse-Width-Modulation that can achieve high efficiency and low output voltage ripple at heavy loads. The NCP1550 working at high switching frequency makes it possible to use small size surface mount inductor and capacitors to reduce PCB area and provide better interference handling for noise sensitive applications. The simplified functional blocks of the device are shown in Figure 1 and descriptions for each of the functions are given below.

The Internal Oscillator

An oscillator that governs the switching of a PWM control cycles is required. NCP1550 have an internal Fixed-Frequency oscillator. The oscillator frequency is trimmed to 600 kHz with an accuracy of $\pm 15\%$. All other timing signals needed for operation are derived from this oscillator signal.

Voltage Reference and Soft-Start

An internal high accuracy voltage reference is included in NCP1550. This reference voltage is connected to the inverting input terminal of the error amplifier, A1, which compared with portion of the output voltage, V_{OUT} derived from an integrated voltage divider with precise trimming to give the required output voltage at $\pm 2\%$ accuracy. NCP1550 also comes with a built-in soft-start circuit that controls the ramping up of the internal reference voltage during the power-up of the converter. This function effectively enables the output voltage to rise gradually over the specified soft-start time, 8 msec typical. This prevents the output voltage from overshooting during start-up of the converter.

Voltage Mode Pulse-Width-Modulation (PWM) Control Scheme

For normal operation, NCP1550 is working in Constant-Frequency Pulse-Width-Modulation (PWM) Voltage Mode Control. The controller operates with the internal oscillator, which generates the required ramp function to compare with the output of the error amplifier, A1. The error amplifier compares the internally divided-down output voltage with the voltage reference to

produce an error voltage at its output. This error voltage is compared with the ramp function to generate the control pulse to drive the external power switch. On a cycle-by-cycle basis, the greater the error voltage, the longer the switch is held on. Hence, corresponding corrective action will be made to keep the output voltage within regulation. Constant-Frequency PWM reduces output voltage ripple and noise, which is one of the important characteristics for noise sensitive communication applications. The high switching frequency allows small size surface mount components to improve layout compactness and reduce PC board area, and eliminate audio and emission interference.

Power-Saving Pulse-Frequency-Modulation (PFM) Control Scheme

While the loading is decreasing, the converter enters the Discontinuous Conduction Mode (DCM) operation, which means the inductor current will decrease to zero before the next switching cycle starts. In DCM operation, the ON time for each switching cycle will decrease significantly when the output current decreases. In order to maintain a high conversion efficiency even at light load conditions, the ON time for each switching cycle is closely monitored and for any ON time smaller than the preset value, 320 nsec, the switching pulse will be skipped. As a result, when the loading current is small, the converter will be operating in a "Constant ON time (320 nsec nominal), variable OFF time" Pulse-Frequency Modulation (PFM) mode. This innovative control scheme improves the conversion efficiency for the system at light load and standby operating conditions hence extend the operating life of the battery.

Low Power Shutdown Mode

NCP1550 can be disabled whenever the CE pin (Pin 1) is tied to GND. In shutdown, the internal reference, oscillator, control circuitry, driver and internal feedback voltage divider are turned off and the output voltage falls to 0 V. During the shutdown mode, as most of the internal functions are stopped and current paths are cut-off, the device consume extremely small current in this condition.

Under-Voltage Lockout (UVLO)

To prevent operation of the P-Channel MOSFET below safe input voltage levels, an Undervoltage Lockout is incorporated into the NCP1550. When the input supply voltage drops below approximately 2.2 V, the comparator, CP1 will turn-off the control circuitry and shut the converter down.

APPLICATIONS INFORMATION

Inductor Value Calculation

Selecting the proper inductance is a trade-off between inductor's physical size, transient respond and power conversion requirements. Lower value inductor saves cost, PC board space and providing faster transient response, but result in higher ripple current and core losses. Considering an application with loading current, $I_{OUT} = 0.5$ A and the inductor ripple current, $I_{L-RIPPLE(P-P)}$ is designed to be less than 40% of the load current, i.e. 0.5 A $\times$ 40% = 0.2 A. The relationship between the inductor value and inductor ripple current is given by,

$$L = \frac{TON * (VIN - R_{DS(ON)} \times I_{OUT} - V_{OUT})}{I_{L-RIPPLE(P-P)}} \quad (\text{eq. 1})$$

Where $R_{DS(ON)}$ is the ON resistance of the external P-channel MOSFET. Figure 39 is a plot for recommended inductance against nominal input voltage for different output options.

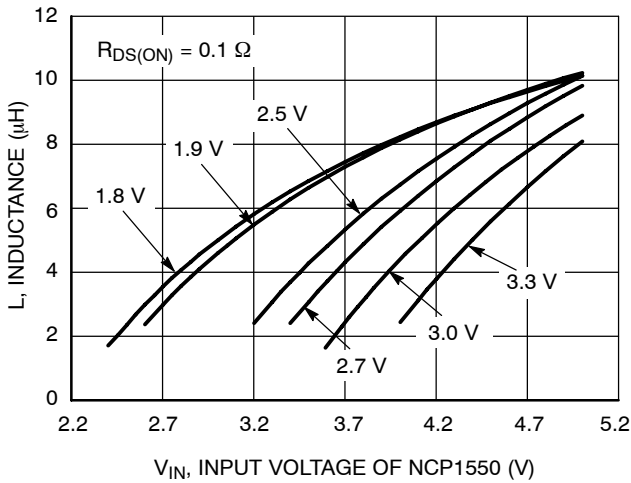


Figure 39. Inductor Selection Chart

P-Channel Power MOSFET Selection

An external P-Channel power MOSFET must be used with the NCP1550. The key selection criteria for the power MOSFET are the gate threshold, V_{GS} , the "ON" resistance, $R_{DS(ON)}$ and its total gate charge, Q_T . For low input voltage operation, we need to select a low gate threshold device that can work down to the minimum input voltage level. $R_{DS(ON)}$ determines the conduction losses for each switching cycle, the lower the ON resistance, the higher the efficiency can be achieved. A power MOSFET with lower gate charge can give lower switching losses but the fast transient can cause unwanted EMI to the system. Compromise in between is required during the design stage. For 1.0 A and 2.0 A load current, NTGS3441T1 and NTGS3443T1 are tested to be appropriate for most applications.

Flywheel Diode Selection

The flywheel diode is turned on and carries load current during the off time. The average diode current depends on the P-Channel switch duty cycle. At high input voltages, the diode conducts most of the time. In case of V_{IN} approaches V_{OUT} , the diode conducts only a small fraction of the cycle. While the output terminals are shorted, the diode will subject to its highest stress. Under this condition, the diode must be able to safely handle the peak current circulating in the loop. So, it is important to select a flywheel diode that can meet the diode peak current and average power dissipation requirements. Under normal conditions, the average current conducted by the flywheel diode is given by:

$$I_D = \frac{V_{IN} - V_{OUT}}{V_{IN} + V_F} \times I_{OUT} \quad (\text{eq. 2})$$

Where I_D is the average diode current and V_F is the forward diode voltage drop.

A fast switching diode must also be used to optimize efficiency. Schottky diodes are a good choice for low forward drop and fast switching times.

Input and Output Capacitor Selection (C_{IN} and C_{OUT})

In continuous mode operation, the source current of the P-Channel MOSFET is a square wave of duty cycle $(V_{OUT} + V_F)/V_{IN}$. To prevent large input voltage transients, a low ESR input capacitor that can support the maximum RMS input current must be selected. The maximum RMS input current, $I_{RMS(MAX)}$ can be estimated by the equation in below:

$$I_{RMS(MAX)} \approx I_{OUT} \times \frac{V_{OUT}(V_{IN} - V_{OUT})^{\frac{1}{2}}}{V_{IN}} \quad (\text{eq. 3})$$

Above estimation has a maximum value at $V_{IN} = 2V_{OUT}$, where $I_{RMS(MAX)} = I_{OUT}/2$. As a general practice, this simple worst-case condition is used for design.

Selection of the output capacitor, C_{OUT} is primarily governed by the required effective series resistance (ESR) of the capacitor. Typically, once the ESR requirement is met, the capacitance will be adequate for filtering. The output voltage ripple, V_{RIPPLE} is approximated by:

$$V_{RIPPLE} \approx I_{L-RIPPLE(P-P)} \times \left(ESR + \frac{1}{4 F_{OSC} C_{OUT}} \right) \quad (\text{eq. 4})$$

Where F_{OSC} is the switching frequency and ESR is the effective series resistance of the output capacitor.

From equation (4), it can be noted that the output voltage ripple contributed by two parts. For most of the case, the major contributor is the capacitor ESR. Ordinary aluminum-electrolytic capacitors have high ESR and should be avoided. Higher quality Low ESR

aluminum–electrolytic capacitors are acceptable and relatively inexpensive. For even better performance, Low ESR tantalum capacitors should be used. Surface–mount tantalum capacitors are better and provide neat and compact solution for space sensitive applications.

PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise and unwanted feedbacks that can affect the performance of the converter. Suggested hints below can be used as a guideline in most situations.

Grounding

Star–ground connection should be used to connect the output power return ground, the input power return ground and the device power ground together at one point. All high current running paths must be thick enough for current

flowing through and producing insignificant voltage drop along the path. Feedback signal path must be separated from the main current path and sensing directly at the anode of the output capacitor.

Components Placement

Power components, i.e. input capacitor, inductor and output capacitor, must be placed as close together as possible. All connecting traces must be short, direct and thick. High current flowing and switching paths must be kept away from the feedback (V_{OUT} , pin 3) terminal to avoid unwanted injection of noise into the feedback path.

Feedback Path

Feedback of the output voltage must be a separate trace separated from the power path. The output voltage sensing trace to the feedback (V_{OUT} , pin 3) pin should be connected to the output voltage directly at the anode of the output capacitor.

External Component Reference Data

Device	V_{OUT}	Inductor Model	Inductor (L)	External MOSFET (M)	Diode (SD)	Output and Input Capacitor C_{OUT}/C_{IN}
NCP1550SN18T1	1.8 V	CDD5D23 6R8 (1A) CDRH6D38 6R8 (2A) Sumida	6.8 μ H	NTGS3441T1 (1A) NTGS3443T1 (2A) ON Semiconductor	MBRM120LT3 ON Semiconductor	33 μ F/33 μ F (1A) 68 μ F/33 μ F (2A) KEMET (T494 series)
NCP1550SN19T1	1.9 V	CDC5D23 6R8 (1A) CDRH6D38 6R8 (2A) Sumida	6.8 μ H	NTGS3441T1 (1A) NTGS3443T1 (2A) ON Semiconductor	MBRM120LT3 ON Semiconductor	33 μ F/33 μ F (1A) 68 μ F/33 μ F (2A) KEMET (T494 series)
NCP1550SN25T1	2.5 V	CDC5D23 5R6 (1A) CDRH6D38 5R0 (2A) Sumida	5.6 μ H 5.0 μ H	NTGS3441T1 (1A) NTGS3443T1 (2A) ON Semiconductor	MBRM120LT3 ON Semiconductor	33 μ F/33 μ F (1A) 68 μ F/33 μ F (2A) KEMET (T494 series)
NCP1550SN27T1	2.7 V	CDC5D23 5R6 (1A) CDRH6D38 5R0 (2A) Sumida	5.6 μ H 5.0 μ H	NTGS3441T1 (1A) NTGS3443T1 (2A) ON Semiconductor	MBRM120LT3 Semiconductor	33 μ F/33 μ F (1A) 68 μ F/33 μ F (2A) KEMET (T494 series)
NCP1550SN30T1	3.0 V	CDC5D23 4R7 (1A) CDRH6D28 5R0 (2A) Sumida	5.6 μ H 5.0 μ H	NTGS3441T1 (1A) NTGS3443T1 (2A) ON Semiconductor	MBRM120LT3 ON Semiconductor	33 μ F/33 μ F (1A) 68 μ F/33 μ F (2A) KEMET (T494 series)
NCP1550SN33T1	3.3 V	CD43 3R3 (1A) CDRH6D38 3R3 (2A) Sumida	3.3 μ H	NTGS3441T1 (1A) NTGS3443T1 (2A) ON Semiconductor	MBRM120LT3 ON Semiconductor	68 μ F/33 μ F (1A) 100 μ F/68 μ F (2A) KEMET (T494 series)

NCP1550

ORDERING INFORMATION

Part Number	Output Voltage (V _{OUT})	Switching Frequency	Device Marking	Package	Shipping [†]
NCP1550SN33T1	3.3 V	600 kHz	DCD	TSOP-5	3000 Tape & Reel
NCP1550SN33T1G	3.3 V		DCD	TSOP-5 (Pb-Free)	
NCP1550SN30T1	3.0 V		DBF	TSOP-5	
NCP1550SN27T1	2.7 V		DCB	TSOP-5	
NCP1550SN25T1	2.5 V		DCA	TSOP-5	
NCP1550SN19T1	1.9 V		DBE	TSOP-5	
NCP1550SN18T1	1.8 V		DBZ	TSOP-5	
NCP1550SN18T1G	1.8 V		DBZ	TSOP-5 (Pb-Free)	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP1571

Low Voltage Synchronous Buck Controller

The NCP1571 is a low voltage buck controller. It provides the control for a DC–DC power solution producing an output voltage as low as 0.980 V over a wide current range. The NCP1571–based solution is powered from 12 V with the output derived from a 2–7 V supply. It contains all required circuitry for a synchronous NFET buck regulator using the V^2 ™ control method to achieve the fastest possible transient response and best overall regulation. NCP1571 operates at a fixed internal 200 kHz frequency and is packaged in an SOIC–8.

This device provides undervoltage lockout protection, Soft–Start, Power Good with delay, and built–in adaptive non–overlap. During undervoltage lockout, the NCP1571 controller allows the power supply output to drift down, allowing the load time to shut off. This operation distinguishes the NCP1571 from other parts in its family.

Features

- Pb–Free Package is Available
- 0.980 V $\pm$ 1.0% Reference Voltage
- V^2 Control Topology
- 200 ns Transient Response
- Programmable Soft–Start
- Power Good
- Programmable Power Good Delay
- 40 ns Gate Rise and Fall Times (3.3 nF Load)
- Adaptive FET Non–Overlap Time
- Fixed 200 kHz Oscillator Frequency
- Undervoltage Lockout Holds Both Gate Outputs Low
- On/Off Control Through Use of the COMP Pin
- Overvoltage Protection through Synchronous MOSFETs
- Synchronous N–Channel Buck Design
- Dual Supply, 12 V Control, 2–7 V Power Source



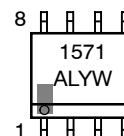
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM

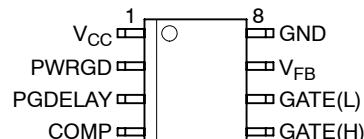


**SOIC–8
D SUFFIX
CASE 751**



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP1571D	SOIC–8	98 Units/Rail
NCP1571DR2	SOIC–8	2500 Tape & Reel
NCP1571DR2G	SOIC–8 (Pb–Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP1571

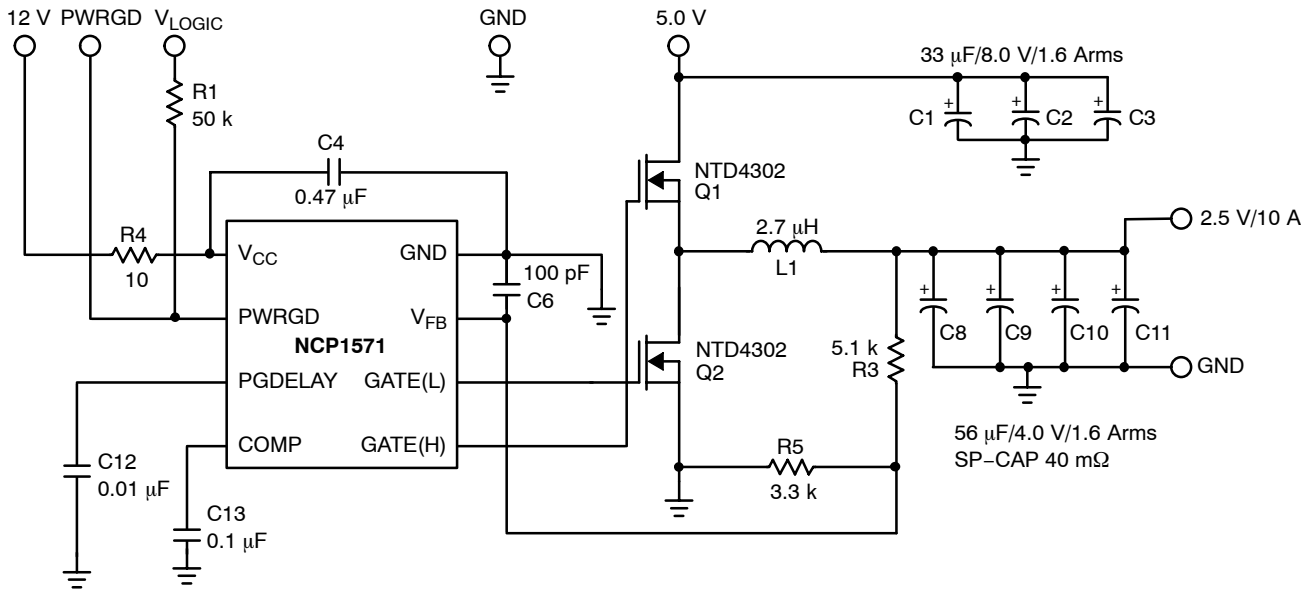


Figure 1. Applications Circuit

MAXIMUM RATINGS

Rating	Value	Unit
Operating Junction Temperature	150	°C
Storage Temperature Range	–65 to 150	°C
ESD Susceptibility (Human Body Model)	2.0	kV
Lead Temperature Soldering:	Reflow: (Note 1)	230 peak
Moisture Sensitivity Level	2	–
Package Thermal Resistance, SOIC–8		
Junction-to-Case, $R_{\theta JC}$	48	°C/W
Junction-to-Ambient, $R_{\theta JA}$	165	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. 60 second maximum above 183°C.

MAXIMUM RATINGS

Pin Name	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
IC Power Input	V_{CC}	15 V	–0.5 V	N/A	1.5 A Peak 450 mA DC
Compensation Capacitor	COMP	6.0 V	–0.5 V	10 mA	10 mA
Voltage Feedback Input	V_{FB}	6.0 V	–0.5 V	1.0 mA	1.0 mA
Power Good Output	PWRGD	15 V	–0.5 V	1.0 mA	20 mA
Power Good Delay	PGDELAY	6.0 V	–0.5 V	1.0 mA	10 mA
High-Side FET Driver	GATE(H)	15 V	–0.5 V –2.0 V for 50 ns	1.5 A Peak 200 mA DC	1.5 A Peak 200 mA DC
Low-Side FET Driver	GATE(L)	15 V	–0.5 V –2.0 V for 50 ns	1.5 A Peak 200 mA DC	1.5 A Peak 200 mA DC
Ground	GND	0.5 V	–0.5 V	1.5 A Peak 450 mA DC	N/A

NCP1571

ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $11.4\text{ V} < V_{CC} < 12.6\text{ V}$, $C_{\text{GATE(H)}} = C_{\text{GATE(L)}} = 3.3\text{ nF}$, $C_{\text{PGDELAY}} = 0.01\text{ }\mu\text{F}$, $C_{\text{COMP}} = 0.1\text{ }\mu\text{F}$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Error Amplifier					
V_{FB} Bias Current	$V_{\text{FB}} = 0\text{ V}$	–	0.2	2.0	μA
COMP Source Current	COMP = 1.5 V, $V_{\text{FB}} = 0.8\text{ V}$	15	30	60	μA
COMP Sink Current	COMP = 1.5 V, $V_{\text{FB}} = 1.2\text{ V}$	15	30	60	μA
Reference Voltage	COMP = V_{FB} $T_J < 25^{\circ}\text{C}$	0.970 0.965	0.980 0.980	0.990 0.995	V V
COMP Max Voltage	$V_{\text{FB}} = 0.8\text{ V}$	2.4	2.7	–	V
COMP Min Voltage	$V_{\text{FB}} = 1.2\text{ V}$	–	0.1	0.2	V
COMP Fault Discharge Current at UVLO	COMP = 1.2 V, $V_{CC} = 6.9\text{ V}$	0.5	1.7	–	mA
COMP Fault Discharge Threshold to Reset UVLO	–	0.1	0.25	0.3	V
Open Loop Gain	–	–	98	–	dB
Unity Gain Bandwidth	–	–	20	–	kHz
PSRR @ 1.0 kHz	–	–	70	–	dB
Output Transconductance	–	–	32	–	mmho
Output Impedance	–	–	2.5	–	$\text{M}\Omega$

GATE(H) and GATE(L)

Rise Time	$1.0\text{ V} < \text{GATE(L)}, \text{GATE(H)} < V_{CC} - 2.0\text{ V}$	–	40	80	ns
Fall Time	$V_{CC} - 2.0\text{ V} < \text{GATE(L)}, \text{GATE(H)} < 1.0\text{ V}$	–	40	80	ns
GATE(H) to GATE(L) Delay	$\text{GATE(H)} < 2.0\text{ V}, \text{GATE(L)} > 2.0\text{ V}$	40	60	100	ns
GATE(L) to GATE(H) Delay	$\text{GATE(L)} < 2.0\text{ V}, \text{GATE(H)} > 2.0\text{ V}$	40	60	100	ns
Minimum Pulse Width	$\text{GATE(X)} = 4.0\text{ V}$	–	250	–	ns
High Voltage (AC)	Measure GATE(L) or GATE(H) $0.5\text{ nF} < C_{\text{GATE(H)}} = C_{\text{GATE(L)}} < 10\text{ nF}$ Note 2	$V_{CC} - 0.5$	V_{CC}	–	V
Low Voltage (AC)	Measure GATE(L) or GATE(H) $0.5\text{ nF} < C_{\text{GATE(H)}} = C_{\text{GATE(L)}} < 10\text{ nF}$ Note 2	–	0	0.5	V
GATE(H)/(L) Pulldown	Resistance to GND. Note 2	20	50	115	$\text{k}\Omega$

Power Good

Lower Threshold, V_O Rising	$T_J < 25^{\circ}\text{C}$	0.852 0.847	0.882 0.882	0.912 0.917	V V
Lower Threshold, V_O Falling	$T_J < 25^{\circ}\text{C}$	0.663 0.658	0.685 0.685	0.709 0.714	V V
PWRGD Low Voltage	$I_{\text{SINK}} = 1.0\text{ mA}, V_{\text{FB}} = 0\text{ V}$	–	0.15	0.4	V
Delay Charge Current	$\text{PGDELAY} = 2.0\text{ V}$	7.0	12	18	μA
Delay Clamp Voltage	–	3.45	4.0	4.3	V
Delay Charge Threshold	Ramp PGDELAY, Monitor PWRGD	3.1	3.3	3.5	V
Delay Discharge Current at UVLO	$\text{PGDELAY} = 0.5\text{ V}, V_{CC} = 6.9\text{ V}$	0.5	2.0	–	mA

2. Guaranteed by design. Not tested in production.

NCP1571

ELECTRICAL CHARACTERISTICS (continued) ($0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $11.4\text{ V} < V_{CC} < 12.6\text{ V}$, $C_{\text{GATE(H)}} = C_{\text{GATE(L)}} = 3.3\text{ nF}$, $C_{\text{PGDELAY}} = 0.01\text{ }\mu\text{F}$, $C_{\text{COMP}} = 0.1\text{ }\mu\text{F}$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit

Power Good

Delay Discharge Threshold to Reset UVLO	PGDELAY = 0.5 V, $V_{CC} = 12\text{ V}$ to 6.9 to 12 V, Ramp PGDELAY to 0.1 V, Monitor I (PGDELAY)	0.1	0.25	0.3	V
“Good” Signal Delay	With 0.01 μF . Note 3	1.0	3.0	5.0	ms

PWM Comparator

PWM Comparator Offset	$V_{FB} = 0\text{ V}$, Increase COMP Until GATE(H) Starts Switching	0.475	0.525	0.575	V
Ramp Max Duty Cycle	–	–	80	–	%
Artificial Ramp	Duty Cycle = 50%	18	25	35	mV
Transient Response	COMP = 1.5 V, V_{FB} 20 mV Overdrive. Note 3	–	200	300	ns
V_{FB} Input Range	Note 3	0	–	1.4	V

Oscillator

Switching Frequency	–	150	200	250	kHz

General Electrical Specifications

V_{CC} Supply Current	COMP = 0 V (No Switching)	–	10	15	mA
Start Threshold	GATE(H) Switching, COMP Charging	8.0	8.5	9.0	V
Stop Threshold	GATE(H) Not Switching, COMP Discharging	7.0	7.5	8.0	V
Hysteresis	Start – Stop	0.75	1.0	1.25	V

3. Guaranteed by design. Not tested in production.

PACKAGE PIN DESCRIPTION

PACKAGE PIN #	PIN SYMBOL	FUNCTION
1	V_{CC}	Power supply input.
2	PWRGD	Open collector output goes low when V_{FB} is out of regulation. User must externally limit current into this pin to less than 20 mA.
3	PGDELAY	External capacitor programs PWRGD low-to-high transition delay.
4	COMP	Error amp output. PWM comparator reference input. A capacitor to LGND provides error amp compensation and Soft-Start. Pulling pin < 0.475 V locks gate outputs to a zero percent duty cycle state.
5	GATE(H)	High-side switch FET driver pin. Capable of delivering peak currents of 1.5 A.
6	GATE(L)	Low-side synchronous FET driver pin. Capable of delivering peak currents of 1.5 A.
7	V_{FB}	Error amplifier and PWM comparator input.
8	GND	Power supply return.

NCP1571

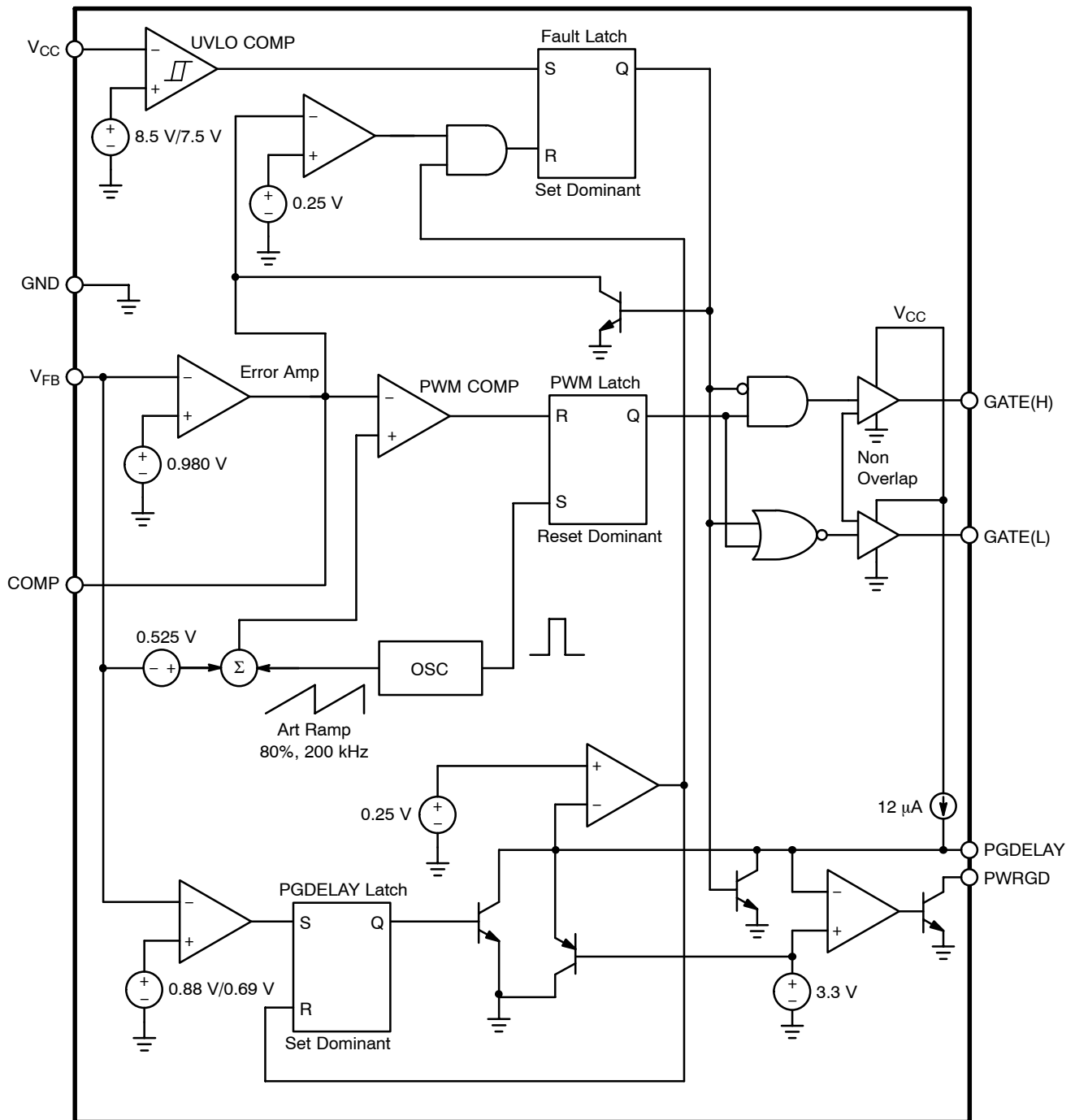


Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

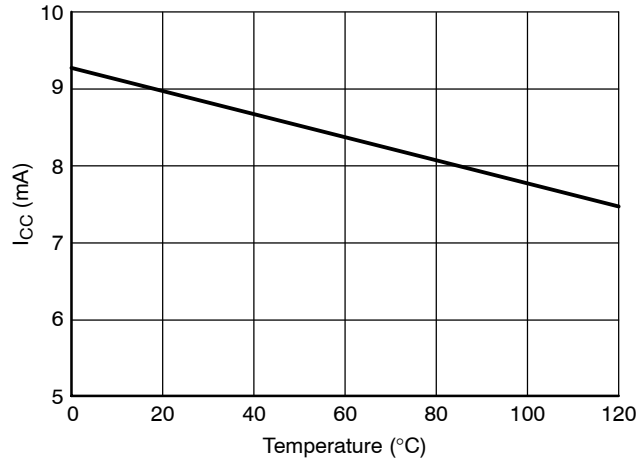


Figure 3. Supply Current vs. Temperature

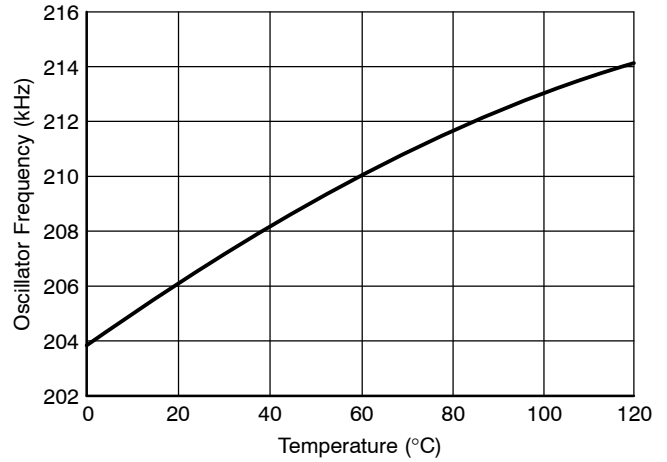


Figure 4. Oscillator Frequency vs. Temperature

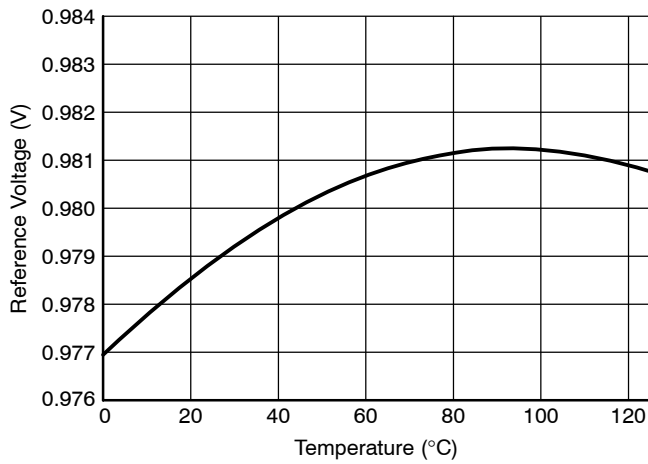


Figure 5. Reference Voltage vs. Temperature

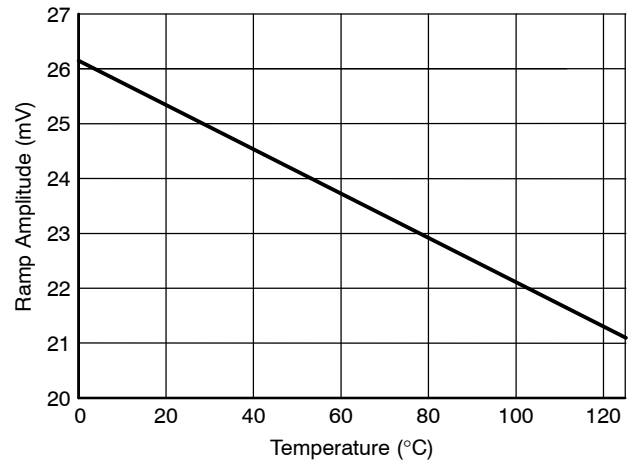


Figure 6. Artificial Ramp Amplitude vs. Temperature (50% Duty Cycle)

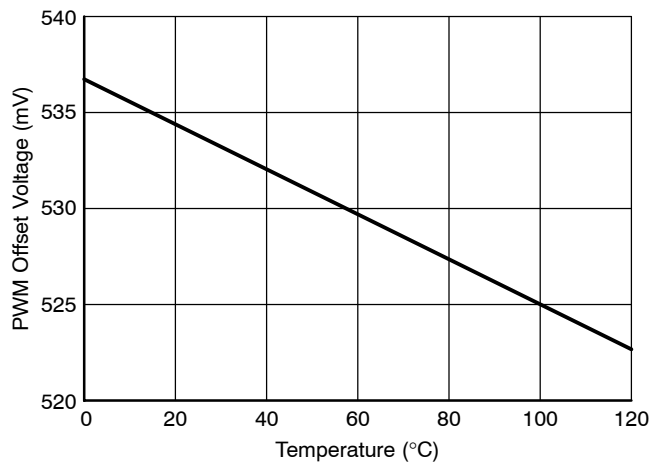


Figure 7. PWM Offset Voltage vs. Temperature

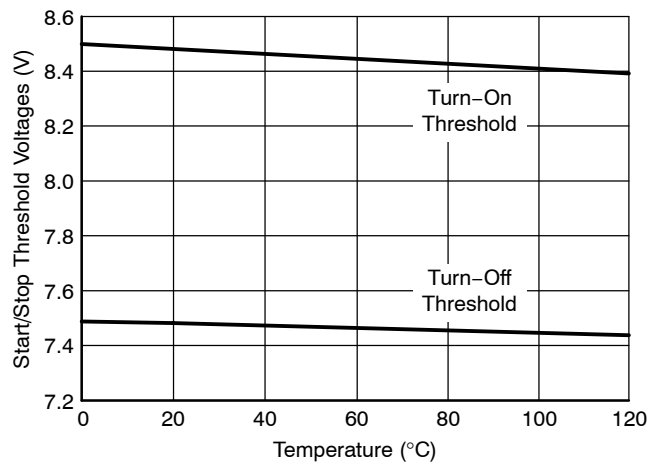


Figure 8. Undervoltage Lockout Thresholds vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

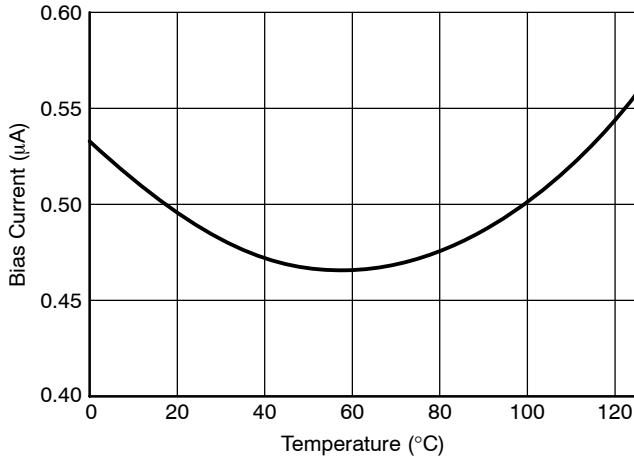


Figure 9. V_{FB} Bias Current vs. Temperature

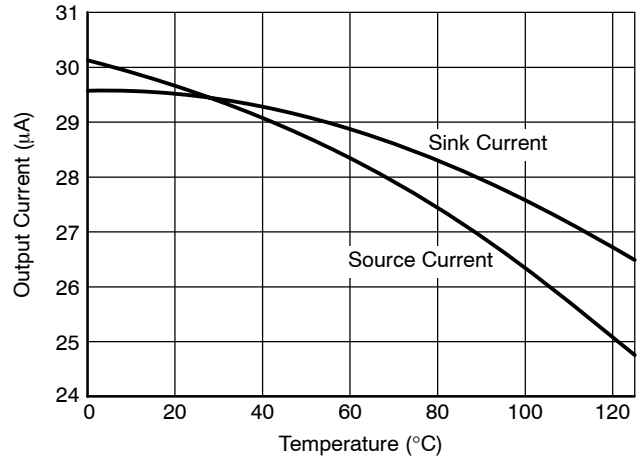


Figure 10. Error Amp Output Currents vs. Temperature

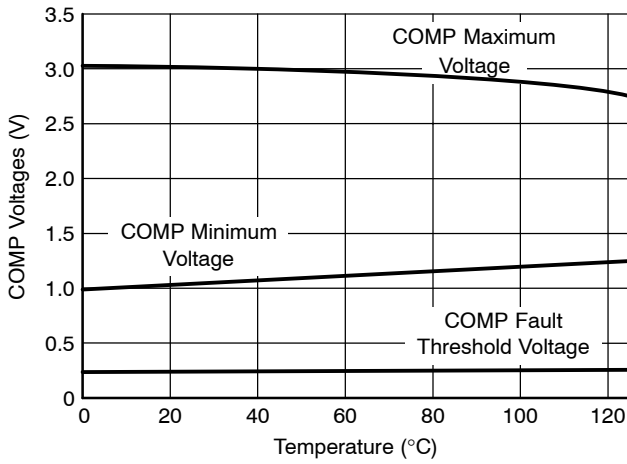


Figure 11. COMP Voltages vs. Temperature

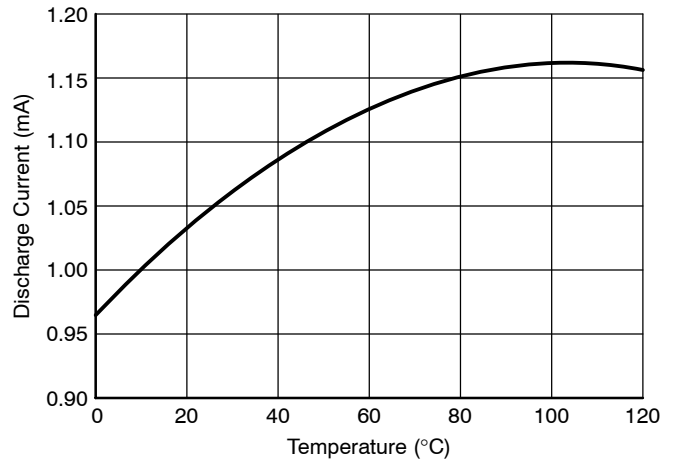


Figure 12. COMP Fault Mode Discharge Current vs. Temperature

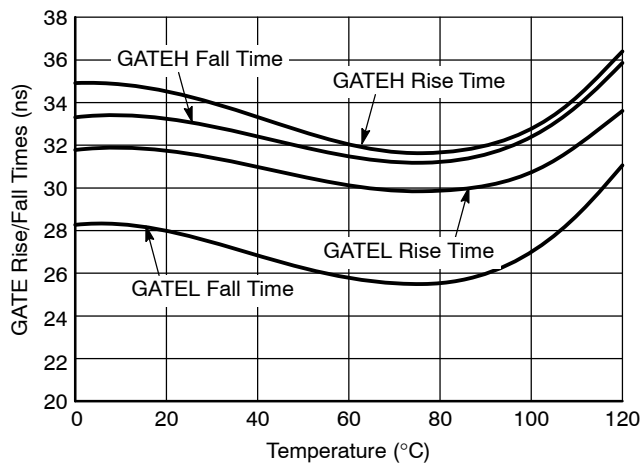


Figure 13. GATE Output Rise and Fall Times vs. Temperature

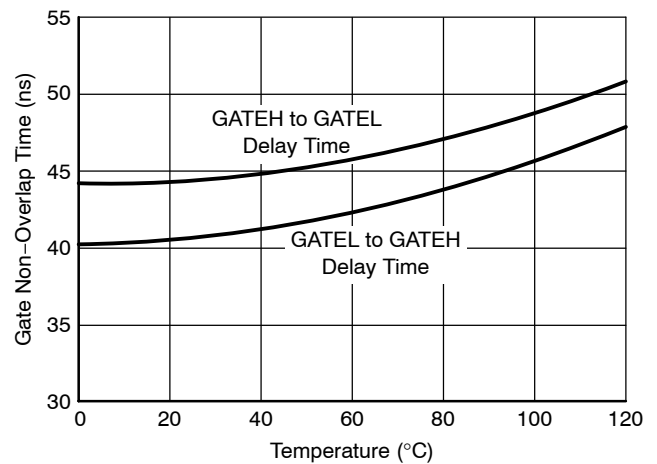


Figure 14. GATE Non-Overlap Times vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

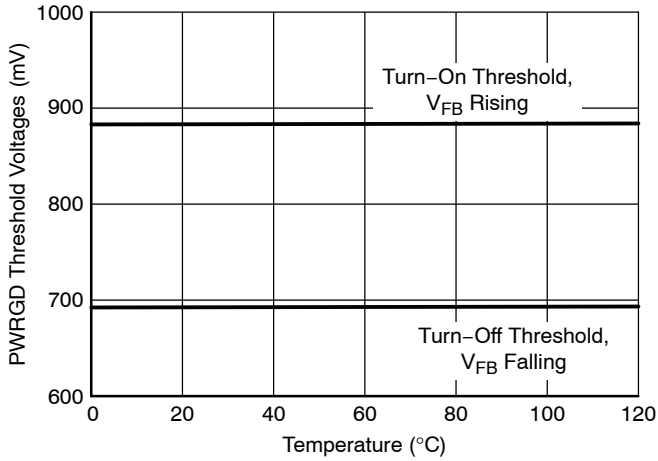


Figure 15. PWRGD Thresholds vs. Temperature

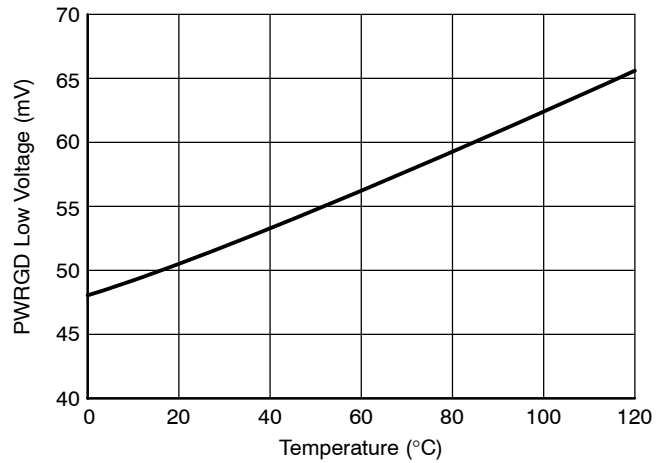


Figure 16. PWRGD Output Low Voltage vs. Temperature

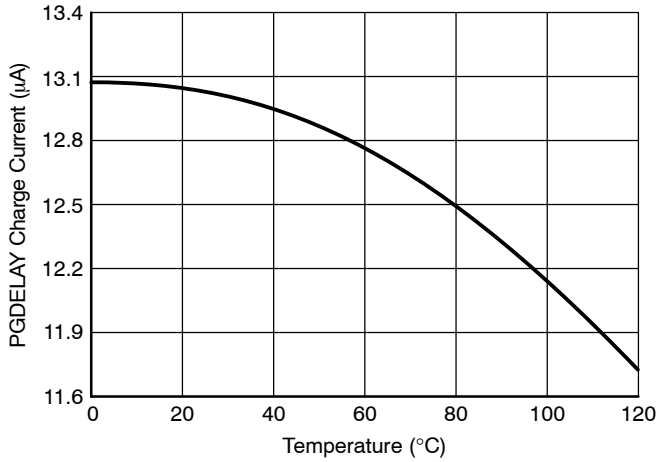


Figure 17. PGDELAY Charge Current vs. Temperature

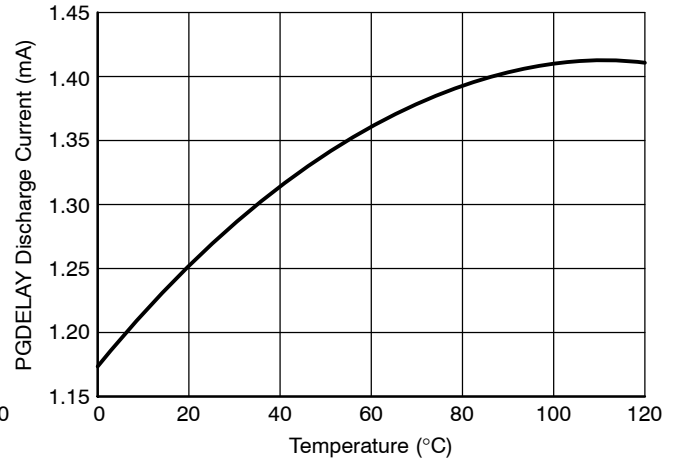


Figure 18. PGDELAY Discharge Current vs. Temperature

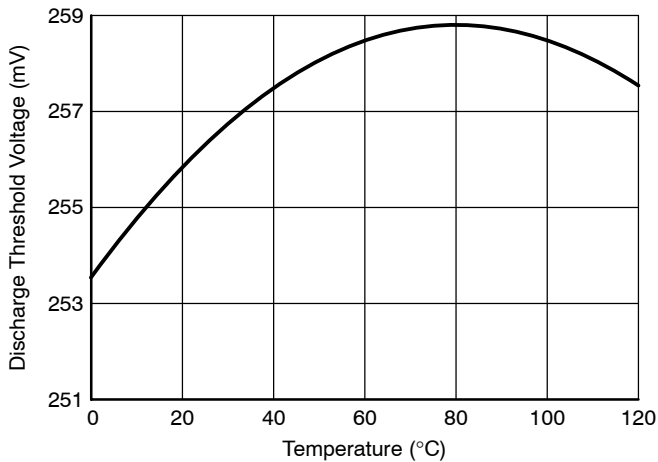


Figure 19. PGDELAY Discharge Threshold Voltage vs. Temperature

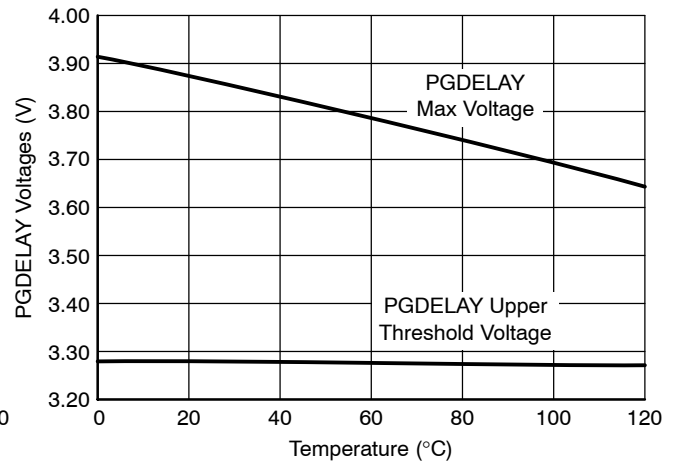


Figure 20. PGDELAY Voltages vs. Temperature

APPLICATION INFORMATION

THEORY OF OPERATION

The NCP1571 is a simple, synchronous, fixed-frequency, low-voltage buck controller using the V^2 control method. It provides a programmable-delay Power Good function to indicate when the output voltage is out of regulation.

 V^2 Control Method

The V^2 control method uses a ramp signal generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. The V^2 method differs from traditional techniques such as voltage mode control, which generates an artificial ramp, and current mode control, which generates a ramp using the inductor current.

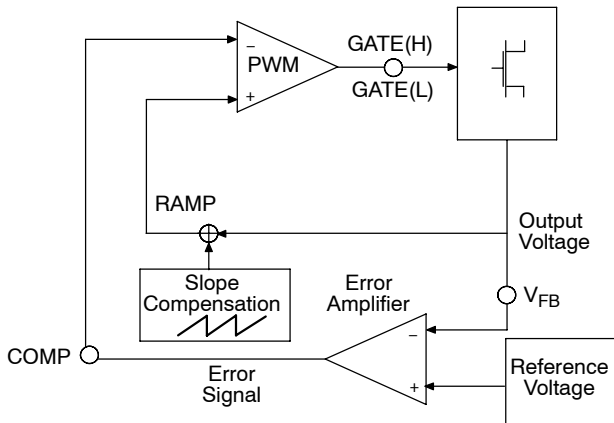


Figure 21. V^2 Control with Slope Compensation

The V^2 control method is illustrated in Figure 21. The output voltage generates both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output, regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, allowing the control circuit to drive the main switch from 0% to 100% duty cycle as required.

A variation in line voltage changes the current ramp in the inductor, which causes the V^2 control scheme to compensate the duty cycle. Since any variation in inductor current modifies the ramp signal, as in current mode control, the V^2 control scheme offers the same advantages in line transient response.

A variation in load current will affect the output voltage, modifying the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. The comparator response time and the transition speed of the main switch determine the load transient response. Unlike traditional control methods, the reaction

time to the output load step is not related to the crossover frequency of the error signal loop.

The error signal loop can have a low crossover frequency, since the transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent control loops. A voltage mode controller relies on the change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains a fixed error signal during line transients, since the slope of the ramp signal changes in this case. However, regulation of load transients still requires a change in the error signal. The V^2 method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

The stringent load transient requirements of modern microprocessors require the output capacitors to have very low ESR. The resulting shallow slope in the output ripple can lead to pulse width jitter and variation caused by both random and synchronous noise. A ramp waveform generated in the oscillator is added to the ramp signal from the output voltage to provide the proper voltage ramp at the beginning of each switching cycle. This slope compensation increases the noise immunity, particularly at duty cycles above 50%.

Startup

The NCP1571 features a programmable Soft-Start function, which is implemented through the error amplifier and the external compensation capacitor. This feature prevents stress to the power components and limits output voltage overshoot during startup. As power is applied to the regulator, the NCP1571 undervoltage lockout circuit (UVL) monitors the IC's supply voltage (V_{CC}). The UVL circuit holds both gate outputs low until V_{CC} exceeds the 8.5 V threshold. A hysteresis function of 1.0 V improves noise immunity. The compensation capacitor connected to the COMP pin is charged by a 30 μ A current source. When the capacitor voltage exceeds the 0.525 V offset of the PWM comparator, the PWM control loop will allow switching to occur. The upper gate driver GATE(H) is activated, turning on the upper MOSFET. The current ramps up through the main inductor and linearly powers the output capacitors and load. When the regulator output voltage exceeds the COMP pin voltage minus the 0.525 V PWM comparator offset threshold and the artificial ramp, the PWM comparator terminates the initial pulse.

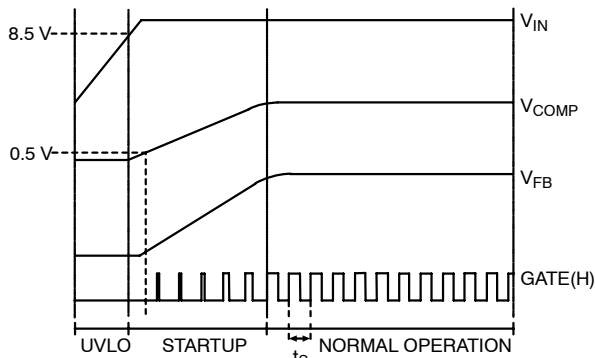


Figure 22. Idealized Waveforms

Normal Operation

During normal operation, the duty cycle of the gate drivers remains approximately constant as the V^2 control loop maintains the regulated output voltage under steady state conditions. Variations in supply line or output load conditions will result in changes in duty cycle to maintain regulation.

Input Supplies

The NCP1571 can be used in applications where a 12 V supply is available along with a lower voltage supply. Often the lower voltage supply is 5 V, but it can be any voltage less than the 12 V supply minus the required gate drive voltage of the top MOSFET. The greater the difference between the two voltages, the better the efficiency due to increasing V_{GS} available to turn on the upper MOSFET. In order to maintain power supply stability, the lower supply voltage should be at least 1.5 times the desired voltage.

A lower supply voltage between 2–7 V is recommended.

Gate Charge Effect on Switching Times

When using the onboard gate drivers, the gate charge has an important effect on the switching times of the FETs. A finite amount of time is required to charge the effective capacitor seen at the gate of the FET. Therefore, the rise and fall times rise linearly with increased capacitive loading.

Transient Response

The 200 ns reaction time of the control loop provides fast transient response to any variations in input voltage and output current. Pulse-by-pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitors during the time required to slew the inductor current. For better transient response, several high frequency and bulk output capacitors are usually used.

Overvoltage Protection

Overvoltage protection is provided as a result of the normal operation of the V^2 control method and requires no additional external components. The control loop responds to an overvoltage condition within 200 ns, turning off the upper MOSFET and disconnecting the regulator from its input voltage. This results in a crowbar action to clamp the

output voltage, preventing damage to the load. The regulator remains in this state until the overvoltage condition ceases.

Power Good

The PWRGD pin is asserted when the output voltage is within regulation limits. Sensing for the PWRGD pin is achieved through the V_{FB} pin. When the output voltage is rising, PWRGD goes high at 90% of the designed output voltage. When the output voltage is falling, PWRGD goes low at 70% of the designed output voltage. PWRGD is an open-collector output and should be externally pulled to logic high through a resistor to limit current to no more than 20 mA. Figure 23 shows the hysteric nature of the PWRGD pin's operation.

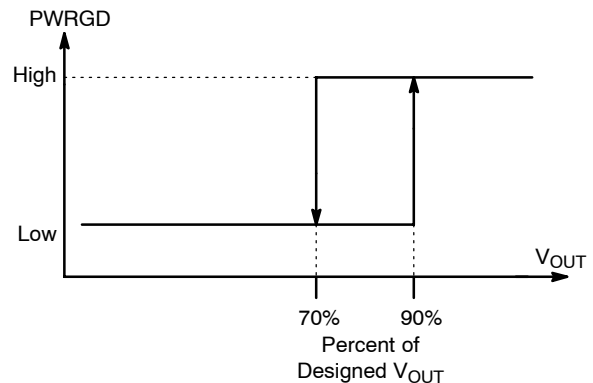


Figure 23. PWRGD Assertion

Shutdown

When the input voltage connected to V_{CC} falls through the lower threshold of the UVLO comparator, a fault latch is set. The fault latch provides a signal that forces both GATE(H) and GATE(L) into their logic low state, producing a high-impedance output at the converter switch node. At the same time, the latch also turns on two transistors which pull down on the COMP and PGDELAY pins, quickly discharging their external capacitors, and allowing PWRGD to fall.

CONVERTER DESIGN

Selection of the Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the regulator output voltage. Key specifications for output capacitors are their ESR (Equivalent Series Resistance) and ESL (Equivalent Series Inductance). For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

In order to determine the number of output capacitors the maximum voltage transient allowed during load transitions has to be specified. The output capacitors must hold the output voltage within these limits since the inductor current

can not change with the required slew rate. The output capacitors must therefore have a very low ESL and ESR.

The voltage change during the load current transient is:

$$\Delta V_{OUT} = \Delta I_{OUT} \times \left(\frac{ESL}{\Delta t} + ESR + \frac{t_{TR}}{C_{OUT}} \right)$$

where:

$\Delta I_{OUT} / \Delta t$ = load current slew rate;

ΔI_{OUT} = load transient;

Δt = load transient duration time;

ESL = Maximum allowable ESL including capacitors, circuit traces, and vias;

ESR = Maximum allowable ESR including capacitors and circuit traces;

t_{TR} = output voltage transient response time.

The designer has to independently assign values for the change in output voltage due to ESR, ESL, and output capacitor discharging or charging. Empirical data indicates that most of the output voltage change (droop or spike depending on the load current transition) results from the total output capacitor ESR.

The maximum allowable ESR can then be determined according to the formula:

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

where:

ΔV_{ESR} = change in output voltage due to ESR (assigned by the designer)

Once the maximum allowable ESR is determined, the number of output capacitors can be found by using the formula:

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

where:

ESR_{CAP} = maximum ESR per capacitor (specified in manufacturer's data sheet).

ESR_{MAX} = maximum allowable ESR.

The actual output voltage deviation due to ESR can then be verified and compared to the value assigned by the designer:

$$\Delta V_{ESR} = \Delta I_{OUT} \times ESR_{MAX}$$

Similarly, the maximum allowable ESL is calculated from the following formula:

$$ESL_{MAX} = \frac{\Delta V_{ESL} \times \Delta t}{\Delta I}$$

Selection of the Input Inductor

A common requirement is that the buck controller must not disturb the input voltage. One method of achieving this is by using an input inductor and a bypass capacitor. The input inductor isolates the supply from the noise generated in the switching portion of the buck regulator and also limits

the inrush current into the input capacitors upon power up. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients. The worst case is when the load changes from no load to full load (load step), a condition under which the highest voltage change across the input capacitors is also seen by the input inductor. The inductor successfully blocks the ripple current while placing the transient current requirements on the input bypass capacitor bank, which has to initially support the sudden load change.

The minimum inductance value for the input inductor is therefore:

$$L_{IN} = \frac{\Delta V}{(di/dt)_{MAX}}$$

where:

L_{IN} = input inductor value;

ΔV = voltage seen by the input inductor during a full load swing;

$(di/dt)_{MAX}$ = maximum allowable input current slew rate.

The designer must select the LC filter pole frequency so that at least 40 dB attenuation is obtained at the regulator switching frequency. The LC filter is a double-pole network with a slope of -2.0, a roll-off rate of -40 dB/dec, and a corner frequency:

$$f_C = \frac{1}{2\pi \times \sqrt{LC}}$$

where:

L = input inductor;

C = input capacitor(s).

Selection of the Output Inductor

There are many factors to consider when choosing the output inductor. Maximum load current, core and winding losses, ripple current, short circuit current, saturation characteristics, component height and cost are all variables that the designer should consider. However, the most important consideration may be the effect inductor value has on transient response.

The amount of overshoot or undershoot exhibited during a current transient is defined as the product of the current step and the output filter capacitor ESR. Choosing the inductor value appropriately can minimize the amount of energy that must be transferred from the inductor to the capacitor or vice-versa. In the subsequent paragraphs, we will determine the minimum value of inductance required for our system and consider the trade-off of ripple current vs. transient response.

In order to choose the minimum value of inductance, input voltage, output voltage and output current must be known. Most computer applications use reasonably well regulated bulk power supplies so that, while the equations below specify $V_{IN(MAX)}$ or $V_{IN(MIN)}$, it is possible to use the nominal value of V_{IN} in these calculations with little error.

Current in the inductor while operating in the continuous current mode is defined as the load current plus ripple current.

$$I_L = I_{LOAD} + I_{RIPPLE}$$

The ripple current waveform is triangular, and the current is a function of voltage across the inductor, switch FET on-time and the inductor value. FET on-time can be defined as the product of duty cycle and switch frequency, and duty cycle can be defined as a ratio of V_{OUT} to V_{IN} . Thus,

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{(f_{OSC})(L)(V_{IN})}$$

Peak inductor current is defined as the load current plus half of the peak current. Peak current must be less than the maximum rated FET switch current, and must also be less than the inductor saturation current. Thus, the maximum output current can be defined as:

$$I_{OUT(MAX)} = I_{SWITCH(MAX)} - \frac{(V_{IN(MAX)} - V_{OUT})V_{OUT}}{(2)(f_{OSC})(L)(V_{IN(MAX)})}$$

Since the maximum output current must be less than the maximum switch current, the minimum inductance required can be determined.

$$L_{(MIN)} = \frac{(V_{IN(MIN)} - V_{OUT})V_{OUT}}{(f_{OSC})(I_{SWITCH(MAX)})(V_{IN(MIN)})}$$

This equation identifies the value of inductor that will provide the full rated switch current as inductor ripple current, and will usually result in inefficient system operation. The system will sink current away from the load during some portion of the duty cycle unless load current is greater than half of the rated switch current. Some value larger than the minimum inductance must be used to ensure the converter does not sink current. Choosing larger values of inductor will reduce the ripple current, and inductor value can be designed to accommodate a particular value of ripple current by replacing $I_{SWITCH(MAX)}$ with a desired value of I_{RIPPLE} :

$$L_{(RIPPLE)} = \frac{(V_{IN(MIN)} - V_{OUT})V_{OUT}}{(f_{OSC})(I_{RIPPLE})(V_{IN(MIN)})}$$

However, reducing the ripple current will cause transient response times to increase. The response times for both increasing and decreasing current steps are shown below.

$$T_{RESPONSE(INCREASING)} = \frac{(L)(\Delta I_{OUT})}{(V_{IN} - V_{OUT})}$$

$$T_{RESPONSE(DECREASING)} = \frac{(L)(\Delta I_{OUT})}{(V_{OUT})}$$

Inductor value selection also depends on how much output ripple voltage the system can tolerate. Output ripple voltage is defined as the product of the output ripple current and the output filter capacitor ESR.

Thus, output ripple voltage can be calculated as:

$$V_{RIPPLE} = (ESRC)(I_{RIPPLE}) = \frac{(ESRC)(V_{IN} - V_{OUT})V_{OUT}}{(f_{OSC})(L)(V_{IN})}$$

Finally, we should consider power dissipation in the output inductors. Power dissipation is proportional to the square of inductor current:

$$P_D = (I_L^2)(ESR_L)$$

The temperature rise of the inductor relative to the air surrounding it is defined as the product of power dissipation and thermal resistance to ambient:

$$\Delta T(\text{inductor}) = (R_a)(P_D)$$

R_a for an inductor designed to conduct 20 A to 30 A is approximately 45°C/W. The inductor temperature is given as:

$$T(\text{inductor}) = \Delta T(\text{inductor}) + T_{\text{ambient}}$$

V_{CC} Bypass Filtering

A small RC filter should be added between module V_{CC} and the V_{CC} input to the IC. A 10 Ω resistor and a 0.47 μF capacitor should be sufficient to ensure the controller IC does not operate erratically due to injected noise, and will also supply reserve charge for the onboard gate drivers.

Input Filter Capacitors

The input filter capacitors provide a charge reservoir that minimizes supply voltage variations due to changes in current flowing through the switch FETs. These capacitors must be chosen primarily for ripple current rating.

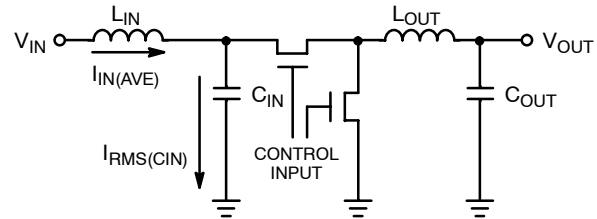


Figure 24.

Consider the schematic shown in Figure 24. The average current flowing in the input inductor L_{IN} for any given output current is:

$$I_{IN(AVE)} = I_{OUT} \times \frac{V_{OUT}}{V_{IN}}$$

Input capacitor current is positive into the capacitor when the switch FETs are off, and negative out of the capacitor when the switch FETs are on. When the switches are off, $I_{IN(AVE)}$ flows into the capacitor. When the switches are on, capacitor current is equal to the per-phase output current minus $I_{IN(AVE)}$. If we ignore the small current variation due to the output ripple current, we can approximate the input capacitor current waveform as a square wave. We can then calculate the RMS input capacitor ripple current:

$$I_{RMS(CIN)} = \sqrt{I_{IN(AVE)}^2 + \frac{V_{OUT}}{V_{IN}} \times [(I_{OUT \text{ per phase}} - I_{IN(AVE)})^2 - I_{IN(AVE)}^2]}$$

The input capacitance must be designed to conduct the worst case input ripple current. This will require several capacitors in parallel. In addition to the worst case current, attention must be paid to the capacitor manufacturer's derating for operation over temperature.

As an example, let us define the input capacitance for a 5 V to 3.3 V conversion at 10 A at an ambient temperature of 60°C. Efficiency of 80% is assumed. Average input current in the input filter inductor is:

$$I_{IN(AVE)} = (10 \text{ A})(3.3 \text{ V}/5 \text{ V}) = 6.6 \text{ A}$$

Input capacitor RMS ripple current is then

$$I_{IN(RMS)} = \sqrt{6.6^2 + \frac{3.3 \text{ V}}{5 \text{ V}} \times [(10 \text{ A} - 6.6 \text{ A})^2 - 6.6 \text{ A}^2]} \\ = 4.74 \text{ A}$$

If we consider a Rubycon MBZ series capacitor, the ripple current rating for a 6.3 V, 1800 nF capacitor is 2000 mA at 100 kHz and 105°C. We determine the number of input capacitors by dividing the ripple current by the percapacitor current rating:

$$\text{Number of capacitors} = 4.74 \text{ A}/2.0 \text{ A} = 2.3$$

A total of at least 3 capacitors in parallel must be used to meet the input capacitor ripple current requirements.

Output Switch FETs

Output switch FETs must be chosen carefully, since their properties vary widely from manufacturer to manufacturer. The NCP1571 system is designed assuming that N-Channel FETs will be used. The FET characteristics of most concern are the gate charge/gate-source threshold voltage, gate capacitance, on-resistance, current rating and the thermal capability of the package.

The onboard FET driver has a limited drive capability. If the switch FET has a high gate charge, the amount of time the FET stays in its ohmic region during the turn-on and turn-off transitions is larger than that of a low gate charge FET, with the result that the high gate charge FET will consume more power. Similarly, a low on-resistance FET will dissipate less power than will a higher on-resistance FET at a given current. Thus, low gate charge and low $R_{DS(ON)}$ will result in higher efficiency and will reduce generated heat.

It can be advantageous to use multiple switch FETs to reduce power consumption. By placing a number of FETs in parallel, the effective $R_{DS(ON)}$ is reduced, thus reducing the

ohmic power loss. However, placing FETs in parallel increases the gate capacitance so that switching losses increase. As long as adding another parallel FET reduces the ohmic power loss more than the switching losses increase, there is some advantage to doing so. However, at some point the law of diminishing returns will take hold, and a marginal increase in efficiency may not be worth the board area required to add the extra FET. Additionally, as more FETs are used, the limited drive capability of the FET driver will have to charge a larger gate capacitance, resulting in increased gate voltage rise and fall times. This will affect the amount of time the FET operates in its ohmic region and will increase power dissipation.

The following equations can be used to calculate power dissipation in the switch FETs.

For ohmic power losses due to $R_{DS(ON)}$:

$$P_{ON(TOP)} = \frac{(R_{DS(ON)}(TOP))(I_{RMS(TOP)})^2}{(\text{number of topside FETs})}$$

$$P_{ON(BOTTOM)} = \frac{(R_{DS(ON)}(BOTTOM))(I_{RMS(BOTTOM)})^2}{(\text{number of bottom-side FETs})}$$

where:

n = number of phases.

Note that $R_{DS(ON)}$ increases with temperature. It is good practice to use the value of $R_{DS(ON)}$ at the FET's maximum junction temperature in the calculations shown above.

$$I_{RMS(TOP)} = \sqrt{I_{PK}^2 - (I_{PK})(I_{RIPPLE}) + \frac{D}{3} I_{RIPPLE}^2}$$

$$I_{RMS(BOTTOM)} = \sqrt{I_{PK}^2 - (I_{PK})(I_{RIPPLE}) + \frac{(1-D)}{3} I_{RIPPLE}^2}$$

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_{OSC})(L)(V_{IN})}$$

$$I_{PEAK} = I_{LOAD} + \frac{I_{RIPPLE}}{2} = \frac{I_{OUT}}{3} + \frac{I_{RIPPLE}}{2}$$

where:

D = Duty cycle.

For switching power losses:

$$P_D = nCV^2(f_{OSC})$$

where:

n = number of switch FETs (either top or bottom),

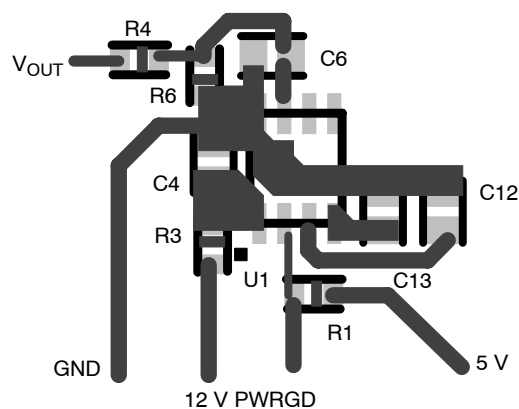
C = FET gate capacitance,

V = maximum gate drive voltage (usually V_{CC}),

f_{OSC} = switching frequency.

Layout Considerations

1. The fast response time of V^2 technology increases the IC's sensitivity to noise on the V_{FB} line. Fortunately, a simple RC filter, formed by the feedback network and a small capacitor (100 pF works well, shown below as C6) placed between V_{FB} and GND, filters out most noise and provides a system practically immune to jitter. This capacitor should be located as close as possible to the IC.
2. The COMP capacitor (shown below as C13) should be connected via its own path to the IC ground. The COMP capacitor is sensitive to the intermittent ground drops caused by switching currents. A separate ground path will reduce the potential for jitter.
3. The V_{CC} bypass capacitor (0.1 μ F or greater, shown below as C4) should be located as close as possible to the IC. This capacitor's connection to GND must be as short as possible. The 10 Ω resistor (shown below as R3) should be placed close to the V_{CC} pin.
4. The IC should not be placed in the path of switching currents. If a ground plane is used, care should be taken by the designer to ensure that the IC is not located over a ground or other current return path.

**Figure 25.**

NCP1573

Low Voltage Synchronous Buck Controller

The NCP1573 is a low voltage buck controller. It provides the control for a DC-DC power solution producing an output voltage as low as 0.980 V over a wide current range. The NCP1573-based solution is powered from 12 V with the output derived from a 2-7 V supply. It contains all required circuitry for a synchronous NFET buck regulator using the V²[™] control method to achieve the fastest possible transient response and best overall regulation. NCP1573 operates at a fixed internal 200 kHz frequency and is packaged in an SO-8.

This device provides Power Good with delay and built-in adaptive non-overlap.

Features

- 0.980 V $\pm$ 1.0% Reference Voltage
- V² Control Topology
- 200 ns Transient Response
- Power Good
- Programmable Power Good Delay
- 40 ns Gate Rise and Fall Times (3.3 nF Load)
- Adaptive FET Non-Overlap Time
- Fixed 200 kHz Oscillator Frequency
- On/Off Control Through Use of the COMP Pin
- Overvoltage Protection through Synchronous MOSFETs
- Synchronous N-Channel Buck Design
- Dual Supply, 12 V Control, 2-7 V Power Source



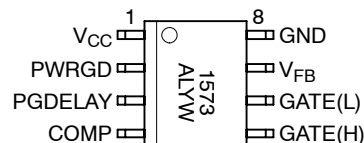
ON Semiconductor®

<http://onsemi.com>



**SO-8
D SUFFIX
CASE 751**

PIN CONNECTIONS AND MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NCP1573D	SO-8	98 Units/Rail
NCP1573DR2	SO-8	2500 Tape & Reel

NCP1573

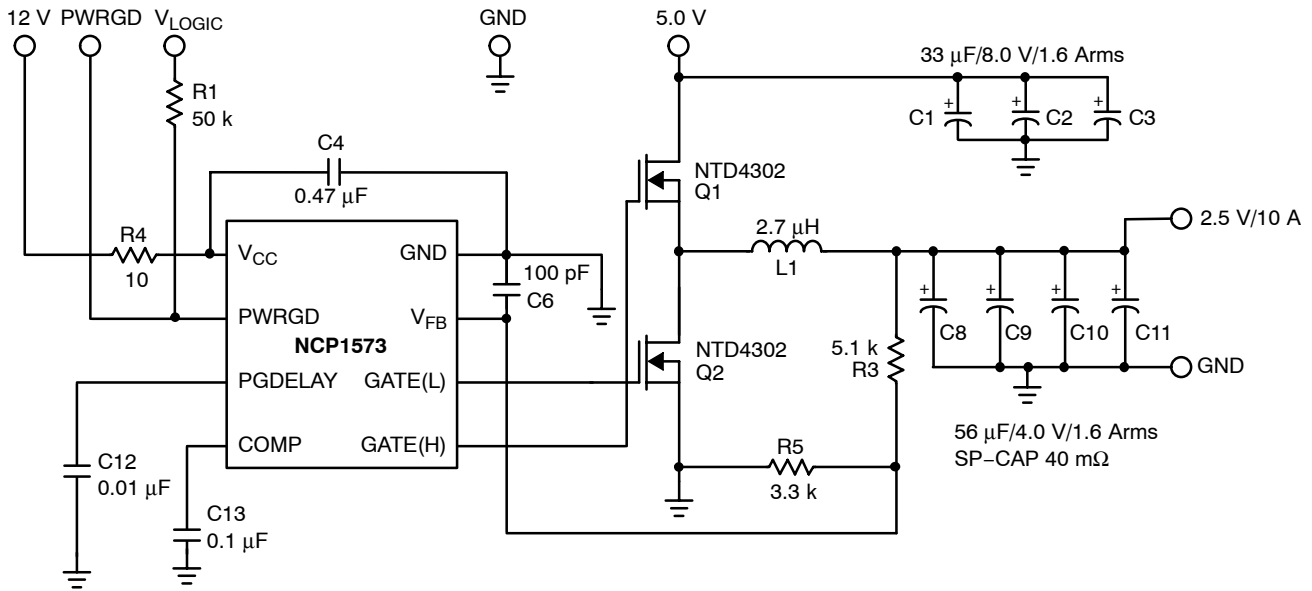


Figure 1. Applications Circuit

MAXIMUM RATINGS*

Rating	Value	Unit
Operating Junction Temperature	150	°C
Storage Temperature Range	-65 to 150	°C
ESD Susceptibility (Human Body Model)	2.0	kV
Lead Temperature Soldering: Reflow: (Note 1)	230 peak	°C
Moisture Sensitivity Level	2	–
Package Thermal Resistance, SO-8		
Junction-to-Case, $R_{\theta JC}$	48	°C/W
Junction-to-Ambient, $R_{\theta JA}$	165	°C/W

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

MAXIMUM RATINGS

Pin Name	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
IC Power Input	V_{CC}	15 V	-0.5 V	N/A	1.5 A Peak 450 mA DC
Compensation Capacitor	COMP	6.0 V	-0.5 V	10 mA	10 mA
Voltage Feedback Input	V_{FB}	6.0 V	-0.5 V	1.0 mA	1.0 mA
Power Good Output	PWRGD	15 V	-0.5 V	1.0 mA	20 mA
Power Good Delay	PGDELAY	6.0 V	-0.5 V	1.0 mA	10 mA
High-Side FET Driver	GATE(H)	15 V	-0.5 V -2.0 V for 50 ns	1.5 A Peak 200 mA DC	1.5 A Peak 200 mA DC
Low-Side FET Driver	GATE(L)	15 V	-0.5 V -2.0 V for 50 ns	1.5 A Peak 200 mA DC	1.5 A Peak 200 mA DC
Ground	GND	0.5 V	-0.5 V	1.5 A Peak 450 mA DC	N/A

NCP1573

ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $11.4\text{ V} < V_{CC} < 12.6\text{ V}$, $C_{\text{GATE(H)}} = C_{\text{GATE(L)}} = 3.3\text{ nF}$, $C_{\text{PGDELAY}} = 0.01\text{ }\mu\text{F}$, $C_{\text{COMP}} = 0.1\text{ }\mu\text{F}$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Error Amplifier					
V_{FB} Bias Current	$V_{\text{FB}} = 0\text{ V}$	–	0.2	2.0	μA
COMP Source Current	COMP = 1.5 V, $V_{\text{FB}} = 0.8\text{ V}$	15	30	60	μA
COMP Sink Current	COMP = 1.5 V, $V_{\text{FB}} = 1.2\text{ V}$	15	30	60	μA
Reference Voltage	COMP = V_{FB} $T_J < 25^{\circ}\text{C}$	0.970 0.965	0.980 0.980	0.990 0.995	V V
COMP Max Voltage	$V_{\text{FB}} = 0.8\text{ V}$	2.4	2.7	–	V
COMP Min Voltage	$V_{\text{FB}} = 1.2\text{ V}$	–	0.1	0.2	V
Open Loop Gain	–	–	98	–	dB
Unity Gain Bandwidth	–	–	20	–	kHz
PSRR @ 1.0 kHz	–	–	70	–	dB
Output Transconductance	–	–	32	–	mmho
Output Impedance	–	–	2.5	–	$\text{M}\Omega$

GATE(H) and GATE(L)

Rise Time	$1.0\text{ V} < \text{GATE(L)}, \text{GATE(H)} < V_{CC} - 2.0\text{ V}$	–	40	80	ns
Fall Time	$V_{CC} - 2.0\text{ V} < \text{GATE(L)}, \text{GATE(H)} < 1.0\text{ V}$	–	40	80	ns
GATE(H) to GATE(L) Delay	$\text{GATE(H)} < 2.0\text{ V}, \text{GATE(L)} > 2.0\text{ V}$	40	60	100	ns
GATE(L) to GATE(H) Delay	$\text{GATE(L)} < 2.0\text{ V}, \text{GATE(H)} > 2.0\text{ V}$	40	60	100	ns
Minimum Pulse Width	$\text{GATE(X)} = 4.0\text{ V}$	–	250	–	ns
High Voltage (AC)	Measure GATE(L) or GATE(H) $0.5\text{ nF} < C_{\text{GATE(H)}} = C_{\text{GATE(L)}} < 10\text{ nF}$ Note 2.	$V_{CC} - 0.5$	V_{CC}	–	V
Low Voltage (AC)	Measure GATE(L) or GATE(H) $0.5\text{ nF} < C_{\text{GATE(H)}} = C_{\text{GATE(L)}} < 10\text{ nF}$ Note 2.	–	0	0.5	V
GATE(H)/(L) Pull-Down	Resistance to GND. Note 2.	20	50	115	k Ω

Power Good

Lower Threshold, V_O Rising	$T_J < 25^{\circ}\text{C}$	0.852 0.847	0.882 0.882	0.912 0.917	V V
Lower Threshold, V_O Falling	$T_J < 25^{\circ}\text{C}$	0.663 0.658	0.685 0.685	0.709 0.714	V V
PWRGD Low Voltage	$I_{\text{SINK}} = 1.0\text{ mA}, V_{\text{FB}} = 0\text{ V}$	–	0.15	0.4	V
Delay Charge Current	$\text{PGDELAY} = 2.0\text{ V}$	7.0	12	18	μA
Delay Clamp Voltage	–	3.45	4.0	4.3	V
Delay Charge Threshold	Ramp PGDELAY , Monitor PWRGD	3.1	3.3	3.5	V
“Good” Signal Delay	With $0.01\text{ }\mu\text{F}$. Note 2.	1.0	3.0	5.0	ms

2. Guaranteed by design. Not tested in production.

NCP1573

ELECTRICAL CHARACTERISTICS (continued) ($0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $11.4\text{ V} < V_{CC} < 12.6\text{ V}$, $C_{\text{GATE(H)}} = C_{\text{GATE(L)}} = 3.3\text{ nF}$, $C_{\text{PGDELAY}} = 0.01\text{ }\mu\text{F}$, $C_{\text{COMP}} = 0.1\text{ }\mu\text{F}$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit

PWM Comparator

PWM Comparator Offset	$V_{\text{FB}} = 0\text{ V}$, Increase COMP Until GATE(H) Starts Switching	0.475	0.525	0.575	V
Ramp Max Duty Cycle	–	–	80	–	%
Artificial Ramp	Duty Cycle = 50%	15	25	35	mV
Transient Response	COMP = 1.5 V, V_{FB} 20 mV Overdrive. Note 3	–	200	300	ns
V_{FB} Input Range	Note 3	0	–	1.4	V

Oscillator

Switching Frequency	–	150	200	250	kHz

General Electrical Specifications

V_{CC} Supply Current	COMP = 0 V (No Switching)	–	10	15	mA

3. Guaranteed by design. Not tested in production.

PACKAGE PIN DESCRIPTION

PACKAGE PIN #	PIN SYMBOL	FUNCTION
1	V_{CC}	Power supply input.
2	PWRGD	Open collector output goes low when V_{FB} is out of regulation. User must externally limit current into this pin to less than 20 mA.
3	PGDELAY	External capacitor programs PWRGD low-to-high transition delay.
4	COMP	Error amp output. PWM comparator reference input. A capacitor to LGND provides error amp compensation. Pulling pin < 0.475 V locks gate outputs to a zero percent duty cycle state.
5	GATE(H)	High-side switch FET driver pin. Capable of delivering peak currents of 1.5 A.
6	GATE(L)	Low-side synchronous FET driver pin. Capable of delivering peak currents of 1.5 A.
7	V_{FB}	Error amplifier and PWM comparator input.
8	GND	Power supply return.

NCP1573

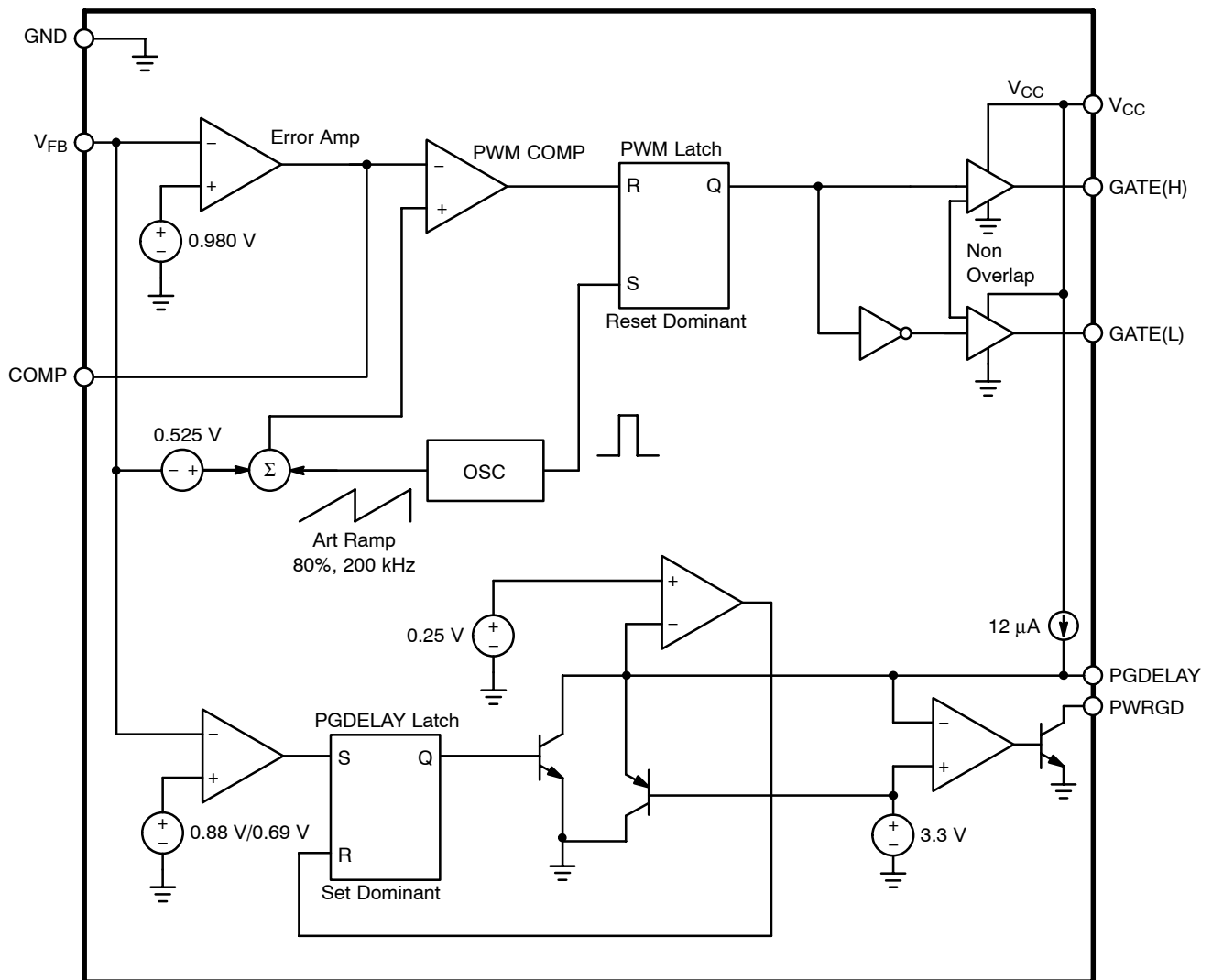


Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

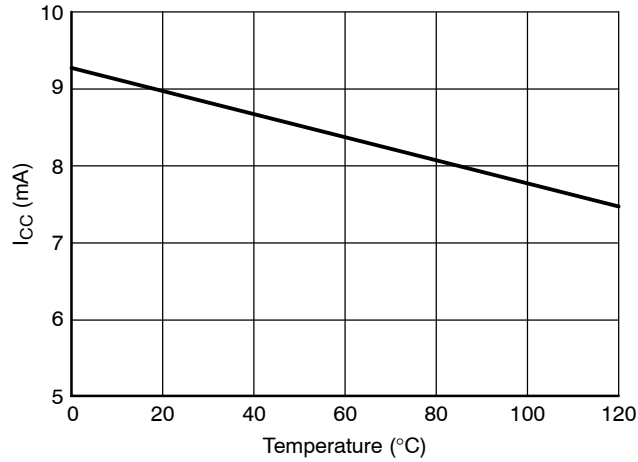


Figure 3. Supply Current vs. Temperature

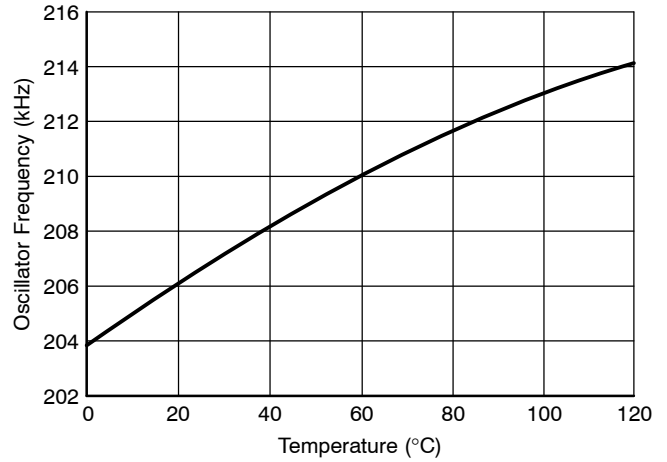


Figure 4. Oscillator Frequency vs. Temperature

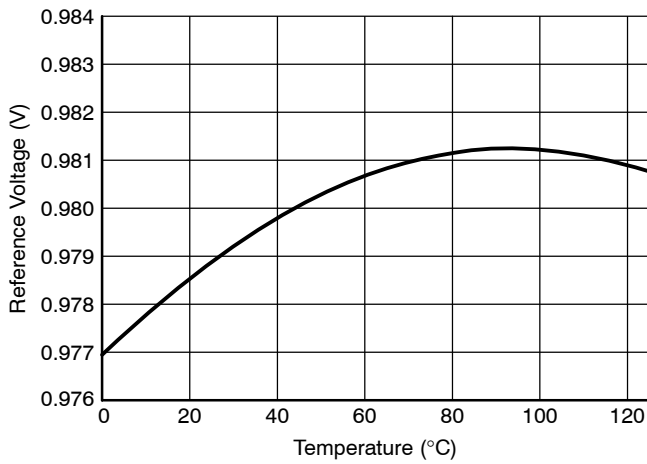


Figure 5. Reference Voltage vs. Temperature

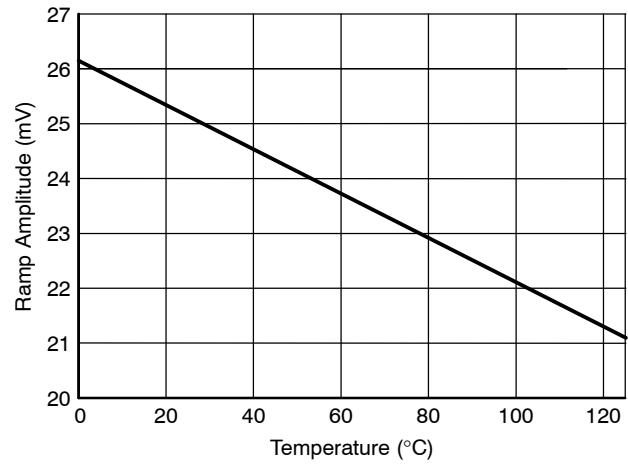


Figure 6. Artificial Ramp Amplitude vs. Temperature (50% Duty Cycle)

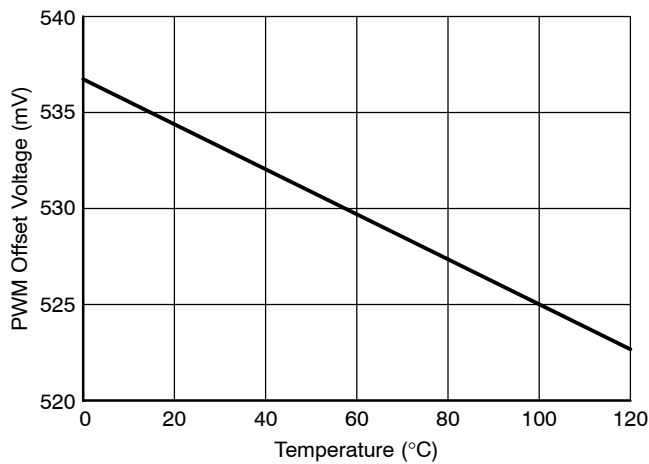


Figure 7. PWM Offset Voltage vs. Temperature

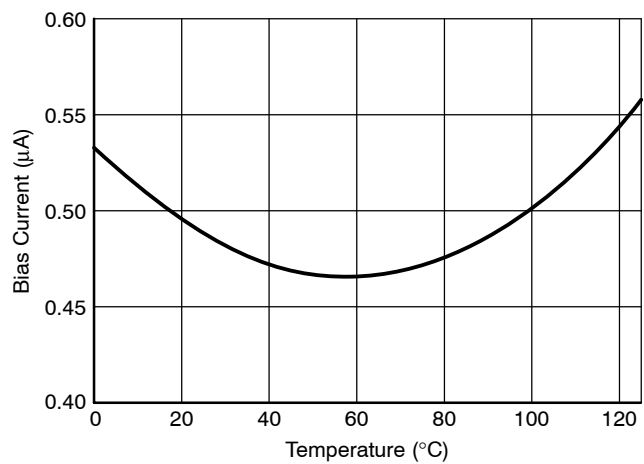


Figure 8. V_{FB} Bias Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

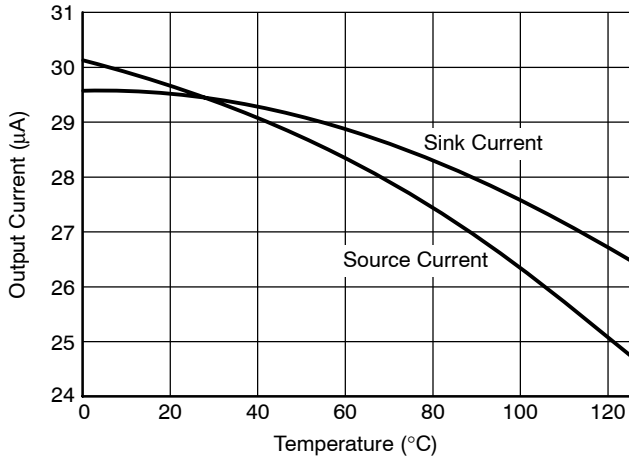


Figure 9. Error Amp Output Currents vs. Temperature

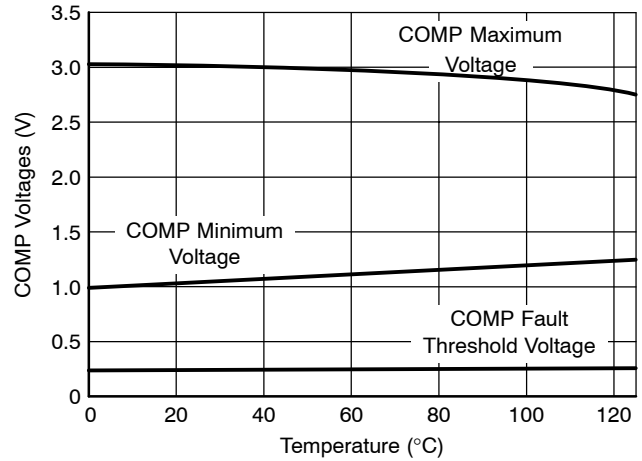


Figure 10. COMP Voltages vs. Temperature

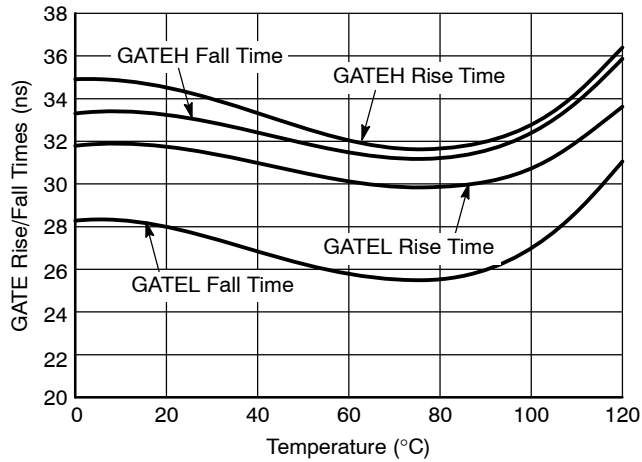


Figure 11. GATE Output Rise and Fall Times vs. Temperature

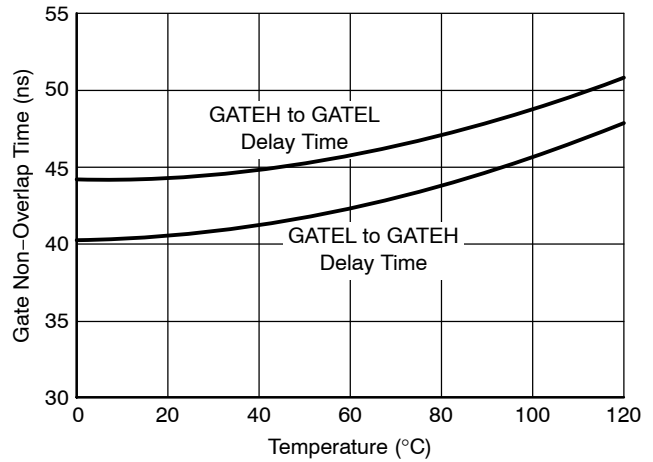


Figure 12. GATE Non-Overlap Times vs. Temperature

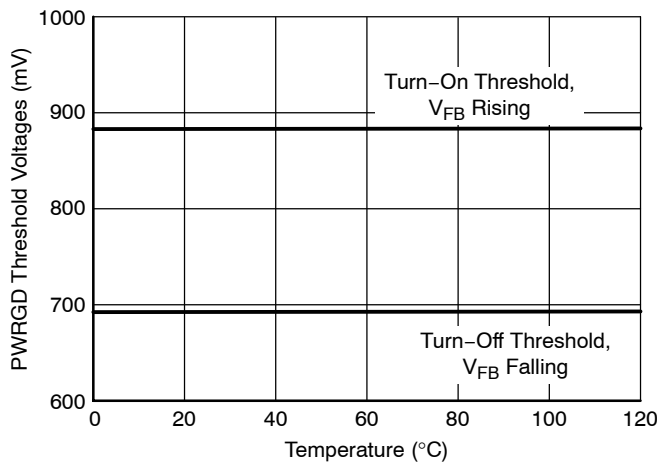


Figure 13. PWRGD Thresholds vs. Temperature

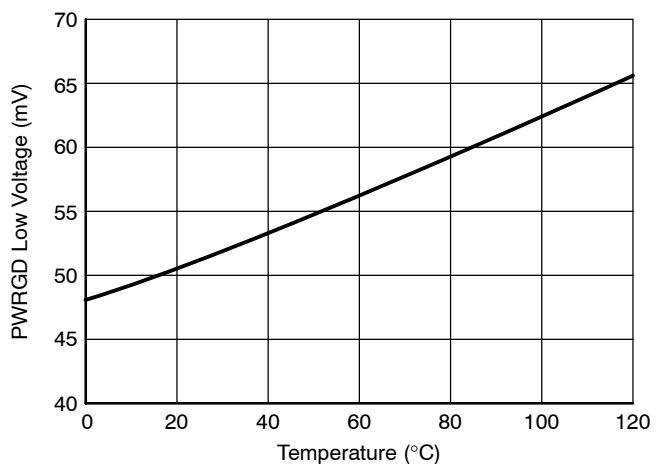


Figure 14. PWRGD Output Low Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

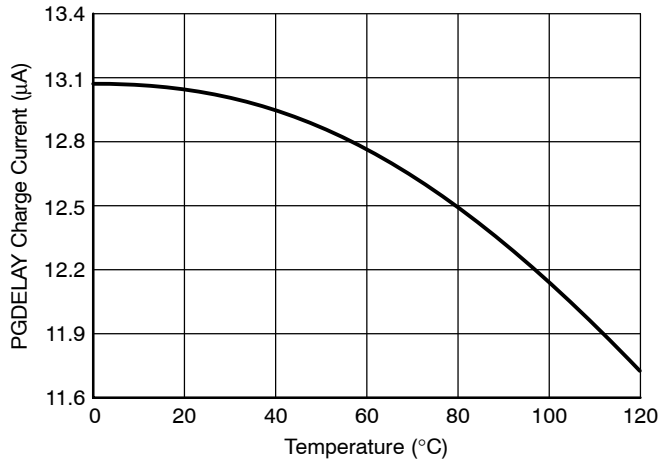


Figure 15. PGDELAY Charge Current vs. Temperature

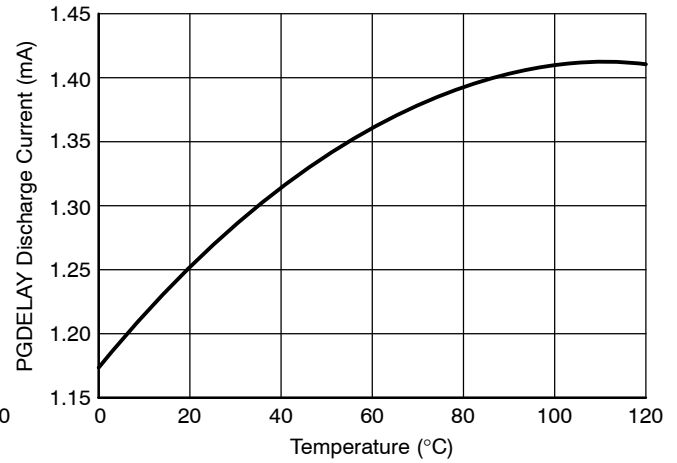


Figure 16. PGDELAY Discharge Current vs. Temperature

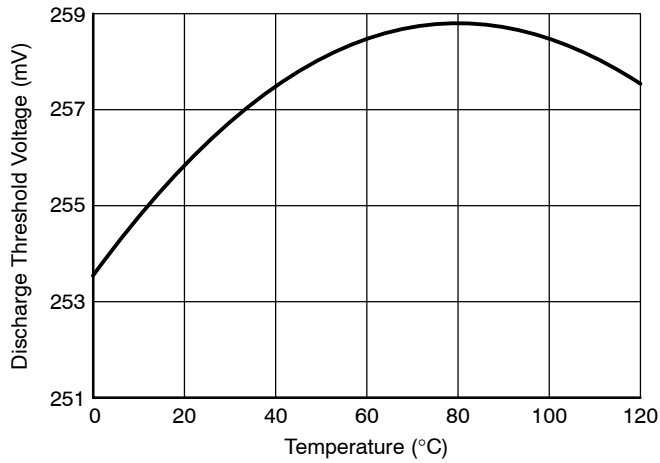


Figure 17. PGDELAY Discharge Threshold Voltage vs. Temperature

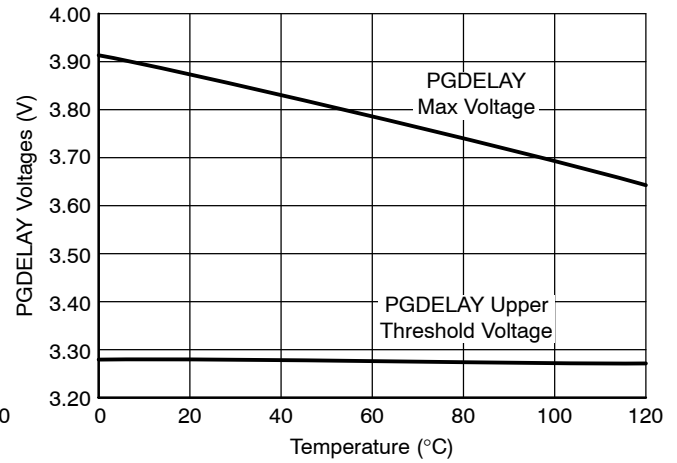


Figure 18. PGDELAY Voltages vs. Temperature

APPLICATION INFORMATION

THEORY OF OPERATION

The NCP1573 is a simple, synchronous, fixed-frequency, low-voltage buck controller using the V^2 control method. It provides a programmable-delay Power Good function to indicate when the output voltage is out of regulation.

 V^2 Control Method

The V^2 control method uses a ramp signal generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. The V^2 method differs from traditional techniques such as voltage mode control, which generates an artificial ramp, and current mode control, which generates a ramp using the inductor current.

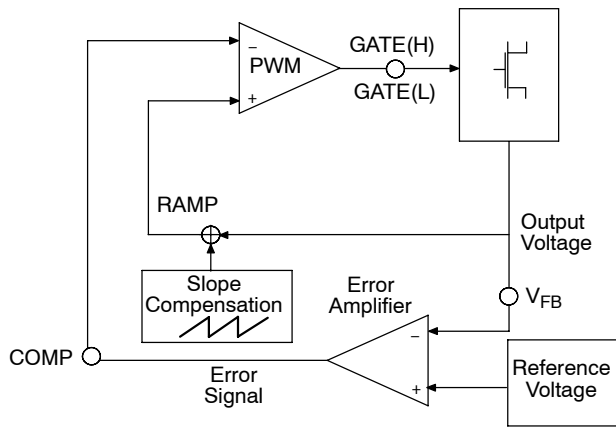


Figure 19. V^2 Control with Slope Compensation

The V^2 control method is illustrated in Figure 19. The output voltage generates both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output, regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, allowing the control circuit to drive the main switch from 0% to 100% duty cycle as required.

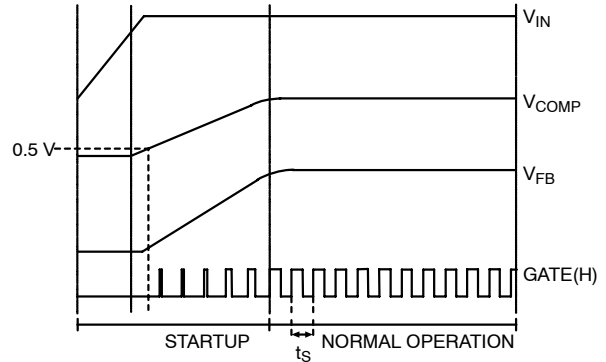


Figure 20. Idealized Waveforms

A variation in line voltage changes the current ramp in the inductor, which causes the V^2 control scheme to compensate the duty cycle. Since any variation in inductor current modifies the ramp signal, as in current mode control, the V^2 control scheme offers the same advantages in line transient response.

A variation in load current will affect the output voltage, modifying the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. The comparator response time and the transition speed of the main switch determine the load transient response. Unlike traditional control methods, the reaction time to the output load step is not related to the crossover frequency of the error signal loop.

The error signal loop can have a low crossover frequency, since the transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent control loops. A voltage mode controller relies on the change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains a fixed error signal during line transients, since the slope of the ramp signal changes in this case. However, regulation of load transients still requires a change in the error signal. The V^2 method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

The stringent load transient requirements of modern microprocessors require the output capacitors to have very low ESR. The resulting shallow slope in the output ripple can lead to pulse width jitter and variation caused by both random and synchronous noise. A ramp waveform generated in the oscillator is added to the ramp signal from the output voltage

to provide the proper voltage ramp at the beginning of each switching cycle. This slope compensation increases the noise immunity, particularly at duty cycles above 50%.

Start Up

The NCP1573 features a programmable Soft Start function, which is implemented through the error amplifier and the external compensation capacitor. This feature prevents stress to the power components and limits output voltage overshoot during start-up. As power is applied to the regulator, the compensation capacitor connected to the COMP pin is charged by a 30 μ A current source. When the capacitor voltage exceeds the 0.525 V offset of the PWM comparator, the PWM control loop will allow switching to occur. The upper gate driver GATE(H) is activated, turning on the upper MOSFET. The current ramps up through the main inductor and linearly powers the output capacitors and load. When the regulator output voltage exceeds the COMP pin voltage minus the 0.525 V PWM comparator offset threshold and the artificial ramp, the PWM comparator terminates the initial pulse.

Normal Operation

During normal operation, the duty cycle of the gate drivers remains approximately constant as the V^2 control loop maintains the regulated output voltage under steady state conditions. Variations in supply line or output load conditions will result in changes in duty cycle to maintain regulation.

Input Supplies

The NCP1573 can be used in applications where a 12 V supply is available along with a lower voltage supply. Often the lower voltage supply is 5 V, but it can be any voltage less than the 12 V supply minus the required gate drive voltage of the top MOSFET. The greater the difference between the two voltages, the better the efficiency due to increasing V_{GS} available to turn on the upper MOSFET. In order to maintain power supply stability, the lower supply voltage should be at least 1.5 times the desired voltage.

A lower supply voltage between 2–7 V is recommended.

Gate Charge Effect on Switching Times

When using the onboard gate drivers, the gate charge has an important effect on the switching times of the FETs. A finite amount of time is required to charge the effective capacitor seen at the gate of the FET. Therefore, the rise and fall times rise linearly with increased capacitive loading.

Transient Response

The 200 ns reaction time of the control loop provides fast transient response to any variations in input voltage and output current. Pulse-by-pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitors during the time required to slew the inductor current. For better transient response, several high frequency and bulk output capacitors are usually used.

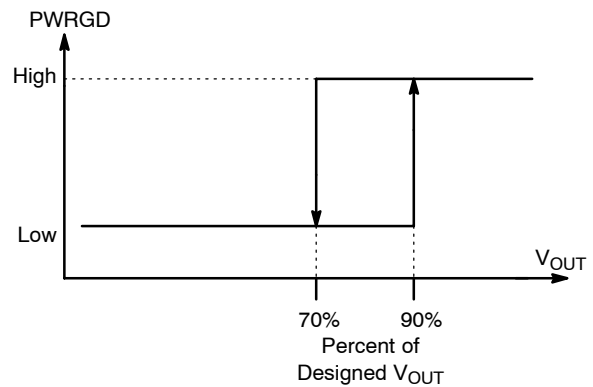


Figure 21. PWRGD Assertion

Overvoltage Protection

Overvoltage protection is provided as a result of the normal operation of the V^2 control method and requires no additional external components. The control loop responds to an overvoltage condition within 200 ns, turning off the upper MOSFET and disconnecting the regulator from its input voltage. This results in a crowbar action to clamp the output voltage, preventing damage to the load. The regulator remains in this state until the overvoltage condition ceases.

Power Good

The PWRGD pin is asserted when the output voltage is within regulation limits. Sensing for the PWRGD pin is achieved through the V_{FB} pin. When the output voltage is rising, PWRGD goes high at 90% of the designed output voltage. When the output voltage is falling, PWRGD goes low at 70% of the designed output voltage. PWRGD is an open-collector output and should be externally pulled to logic high through a resistor to limit current to no more than 20 mA. Figure 21 shows the hysteretic nature of the PWRGD pin's operation.

CONVERTER DESIGN

Selection of the Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the regulator output voltage. Key specifications for output capacitors are their ESR (Equivalent Series Resistance), and ESL (Equivalent Series Inductance). For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

In order to determine the number of output capacitors the maximum voltage transient allowed during load transitions has to be specified. The output capacitors must hold the output voltage within these limits since the inductor current can not change with the required slew rate. The output capacitors must therefore have a very low ESL and ESR.

The voltage change during the load current transient is:

$$\Delta V_{OUT} = \Delta I_{OUT} \times \left(\frac{ESL}{\Delta t} + ESR + \frac{t_{TR}}{C_{OUT}} \right)$$

where:

$\Delta I_{OUT} / \Delta t$ = load current slew rate;

ΔI_{OUT} = load transient;

Δt = load transient duration time;

ESL = Maximum allowable ESL including capacitors, circuit traces, and vias;

ESR = Maximum allowable ESR including capacitors and circuit traces;

t_{TR} = output voltage transient response time.

The designer has to independently assign values for the change in output voltage due to ESR, ESL, and output capacitor discharging or charging. Empirical data indicates that most of the output voltage change (droop or spike depending on the load current transition) results from the total output capacitor ESR.

The maximum allowable ESR can then be determined according to the formula:

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

where:

ΔV_{ESR} = change in output voltage due to ESR (assigned by the designer)

Once the maximum allowable ESR is determined, the number of output capacitors can be found by using the formula:

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

where:

ESR_{CAP} = maximum ESR per capacitor (specified in manufacturer's data sheet).

ESR_{MAX} = maximum allowable ESR.

The actual output voltage deviation due to ESR can then be verified and compared to the value assigned by the designer:

$$\Delta V_{ESR} = \Delta I_{OUT} \times ESR_{MAX}$$

Similarly, the maximum allowable ESL is calculated from the following formula:

$$ESL_{MAX} = \frac{\Delta V_{ESL} \times \Delta t}{\Delta I}$$

Selection of the Input Inductor

A common requirement is that the buck controller must not disturb the input voltage. One method of achieving this is by using an input inductor and a bypass capacitor. The input inductor isolates the supply from the noise generated in the switching portion of the buck regulator and also limits the inrush current into the input capacitors upon power up. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients. The worst case is when the load changes from no load to full load (load step), a condition under which the highest voltage change across the input capacitors is also seen by the input inductor. The inductor successfully blocks the ripple current while placing the transient current requirements on the input

bypass capacitor bank, which has to initially support the sudden load change.

The minimum inductance value for the input inductor is therefore:

$$L_{IN} = \frac{\Delta V}{(di/dt)_{MAX}}$$

where:

L_{IN} = input inductor value;

ΔV = voltage seen by the input inductor during a full load swing;

$(di/dt)_{MAX}$ = maximum allowable input current slew rate.

The designer must select the LC filter pole frequency so that at least 40 dB attenuation is obtained at the regulator switching frequency. The LC filter is a double-pole network with a slope of -2.0, a roll-off rate of -40 dB/dec, and a corner frequency:

$$f_C = \frac{1}{2\pi \times \sqrt{LC}}$$

where:

L = input inductor;

C = input capacitor(s).

Selection of the Output Inductor

There are many factors to consider when choosing the output inductor. Maximum load current, core and winding losses, ripple current, short circuit current, saturation characteristics, component height and cost are all variables that the designer should consider. However, the most important consideration may be the effect inductor value has on transient response.

The amount of overshoot or undershoot exhibited during a current transient is defined as the product of the current step and the output filter capacitor ESR. Choosing the inductor value appropriately can minimize the amount of energy that must be transferred from the inductor to the capacitor or vice-versa. In the subsequent paragraphs, we will determine the minimum value of inductance required for our system and consider the trade-off of ripple current vs. transient response.

In order to choose the minimum value of inductance, input voltage, output voltage and output current must be known. Most computer applications use reasonably well regulated bulk power supplies so that, while the equations below specify $V_{IN(MAX)}$ or $V_{IN(MIN)}$, it is possible to use the nominal value of V_{IN} in these calculations with little error.

Current in the inductor while operating in the continuous current mode is defined as the load current plus ripple current.

$$I_L = I_{LOAD} + I_{RIPPLE}$$

The ripple current waveform is triangular, and the current is a function of voltage across the inductor, switch FET on-time and the inductor value. FET on-time can be defined as the product of duty cycle and switch frequency, and duty cycle can be defined as a ratio of V_{OUT} to V_{IN} . Thus,

$$I_{\text{RIPPLE}} = \frac{(V_{\text{IN}} - V_{\text{OUT}})V_{\text{OUT}}}{(f_{\text{OSC}})(L)(V_{\text{IN}})}$$

Peak inductor current is defined as the load current plus half of the peak current. Peak current must be less than the maximum rated FET switch current, and must also be less than the inductor saturation current. Thus, the maximum output current can be defined as:

$$I_{\text{OUT(MAX)}} = I_{\text{SWITCH(MAX)}} - \frac{(V_{\text{IN(MAX)}} - V_{\text{OUT}})V_{\text{OUT}}}{(2)(f_{\text{OSC}})(L)(V_{\text{IN(MAX)}})}$$

Since the maximum output current must be less than the maximum switch current, the minimum inductance required can be determined.

$$L_{\text{(MIN)}} = \frac{(V_{\text{IN(MIN)}} - V_{\text{OUT}})V_{\text{OUT}}}{(f_{\text{OSC}})(I_{\text{SWITCH(MAX)}})(V_{\text{IN(MIN)}})}$$

This equation identifies the value of inductor that will provide the full rated switch current as inductor ripple current, and will usually result in inefficient system operation. The system will sink current away from the load during some portion of the duty cycle unless load current is greater than half of the rated switch current. Some value larger than the minimum inductance must be used to ensure the converter does not sink current. Choosing larger values of inductor will reduce the ripple current, and inductor value can be designed to accommodate a particular value of ripple current by replacing $I_{\text{SWITCH(MAX)}}$ with a desired value of I_{RIPPLE} :

$$L_{\text{(RIPPLE)}} = \frac{(V_{\text{IN(MIN)}} - V_{\text{OUT}})V_{\text{OUT}}}{(f_{\text{OSC}})(I_{\text{RIPPLE}})(V_{\text{IN(MIN)}})}$$

However, reducing the ripple current will cause transient response times to increase. The response times for both increasing and decreasing current steps are shown below.

$$T_{\text{RESPONSE(INCREASING)}} = \frac{(L)(\Delta I_{\text{OUT}})}{(V_{\text{IN}} - V_{\text{OUT}})}$$

$$T_{\text{RESPONSE(DECREASING)}} = \frac{(L)(\Delta I_{\text{OUT}})}{(V_{\text{OUT}})}$$

Inductor value selection also depends on how much output ripple voltage the system can tolerate. Output ripple voltage is defined as the product of the output ripple current and the output filter capacitor ESR.

Thus, output ripple voltage can be calculated as:

$$V_{\text{RIPPLE}} = (ESR_C)(I_{\text{RIPPLE}}) = \frac{(ESR_C)(V_{\text{IN}} - V_{\text{OUT}})V_{\text{OUT}}}{(f_{\text{OSC}})(L)(V_{\text{IN}})}$$

Finally, we should consider power dissipation in the output inductors. Power dissipation is proportional to the square of inductor current:

$$P_D = (I^2)(ESR_L)$$

The temperature rise of the inductor relative to the air surrounding it is defined as the product of power dissipation and thermal resistance to ambient:

$$\Delta T(\text{inductor}) = (R_a)(P_D)$$

R_a for an inductor designed to conduct 20 A to 30 A is approximately 45°C/W. The inductor temperature is given as:

$$T(\text{inductor}) = \Delta T(\text{inductor}) + T_{\text{ambient}}$$

V_{CC} Bypass Filtering

A small RC filter should be added between module V_{CC} and the V_{CC} input to the IC. A 10 Ω resistor and a 0.47 μF capacitor should be sufficient to ensure the controller IC does not operate erratically due to injected noise, and will also supply reserve charge for the onboard gate drivers.

Input Filter Capacitors

The input filter capacitors provide a charge reservoir that minimizes supply voltage variations due to changes in current flowing through the switch FETs. These capacitors must be chosen primarily for ripple current rating.

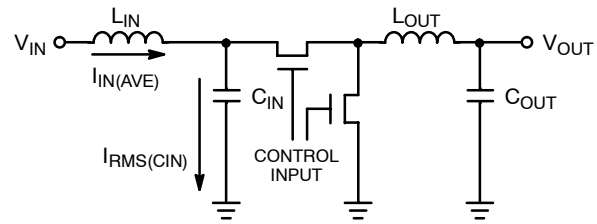


Figure 22.

Consider the schematic shown in Figure 22. The average current flowing in the input inductor L_{IN} for any given output current is:

$$I_{\text{IN(AVE)}} = I_{\text{OUT}} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

Input capacitor current is positive into the capacitor when the switch FETs are off, and negative out of the capacitor when the switch FETs are on. When the switches are off, $I_{\text{IN(AVE)}}$ flows into the capacitor. When the switches are on, capacitor current is equal to the per-phase output current minus $I_{\text{IN(AVE)}}$. If we ignore the small current variation due to the output ripple current, we can approximate the input capacitor current waveform as a square wave. We can then calculate the RMS input capacitor ripple current:

$$I_{\text{RMS(CIN)}} = \sqrt{I_{\text{IN(AVE)}}^2 + \frac{V_{\text{OUT}}}{V_{\text{IN}}} \times [(I_{\text{OUT per phase}} - I_{\text{IN(AVE)}})^2 - I_{\text{IN(AVE)}}^2]}$$

The input capacitance must be designed to conduct the worst case input ripple current. This will require several capacitors in parallel. In addition to the worst case current, attention must be paid to the capacitor manufacturer's derating for operation over temperature.

As an example, let us define the input capacitance for a 5 V to 3.3 V conversion at 10 A at an ambient temperature of 60°C. Efficiency of 80% is assumed. Average input current in the input filter inductor is:

$$I_{IN(AVE)} = (10 \text{ A})(3.3 \text{ V}/5 \text{ V}) = 6.6 \text{ A}$$

Input capacitor RMS ripple current is then

$$I_{IN(RMS)} = \sqrt{6.6^2 + \frac{3.3 \text{ V}}{5 \text{ V}} \times [(10 \text{ A} - 6.6 \text{ A})^2 - 6.6 \text{ A}^2]} \\ = 4.74 \text{ A}$$

If we consider a Rubycon MBZ series capacitor, the ripple current rating for a 6.3 V, 1800 nF capacitor is 2000 mA at 100 kHz and 105°C. We determine the number of input capacitors by dividing the ripple current by the per-capacitor current rating:

$$\text{Number of capacitors} = 4.74 \text{ A}/2.0 \text{ A} = 2.3$$

A total of at least 3 capacitors in parallel must be used to meet the input capacitor ripple current requirements.

Output Switch FETs

Output switch FETs must be chosen carefully, since their properties vary widely from manufacturer to manufacturer. The NCP1573 system is designed assuming that n-channel FETs will be used. The FET characteristics of most concern are the gate charge/gate-source threshold voltage, gate capacitance, on-resistance, current rating and the thermal capability of the package.

The onboard FET driver has a limited drive capability. If the switch FET has a high gate charge, the amount of time the FET stays in its ohmic region during the turn-on and turn-off transitions is larger than that of a low gate charge FET, with the result that the high gate charge FET will consume more power. Similarly, a low on-resistance FET will dissipate less power than will a higher on-resistance FET at a given current. Thus, low gate charge and low $R_{DS(ON)}$ will result in higher efficiency and will reduce generated heat.

It can be advantageous to use multiple switch FETs to reduce power consumption. By placing a number of FETs in parallel, the effective $R_{DS(ON)}$ is reduced, thus reducing the ohmic power loss. However, placing FETs in parallel increases the gate capacitance so that switching losses increase. As long as adding another parallel FET reduces the ohmic power loss more than the switching losses increase, there is some advantage to doing so. However, at some point the law of diminishing returns will take hold, and a marginal increase in efficiency may not be worth the board area required to add the extra FET. Additionally, as more FETs are used, the limited drive capability of the FET driver will have to charge a larger gate capacitance, resulting in increased gate voltage rise and fall times. This will affect the amount of time the FET operates in its ohmic region and will increase power dissipation.

The following equations can be used to calculate power dissipation in the switch FETs.

For ohmic power losses due to $R_{DS(ON)}$:

$$P_{ON(TOP)} = \frac{(R_{DS(ON)}(TOP))(I_{RMS(TOP)})^2}{(\text{number of topside FETs})}$$

$$P_{ON(BOTTOM)} = \frac{(R_{DS(ON)}(BOTTOM))(I_{RMS(BOTTOM)})^2}{(\text{number of bottom-side FETs})}$$

where:

n = number of phases.

Note that $R_{DS(ON)}$ increases with temperature. It is good practice to use the value of $R_{DS(ON)}$ at the FET's maximum junction temperature in the calculations shown above.

$$I_{RMS(TOP)} = \sqrt{I_{PK}^2 - (I_{PK})(I_{RIPPLE}) + \frac{D}{3} I_{RIPPLE}^2}$$

$$I_{RMS(BOTTOM)} = \sqrt{I_{PK}^2 - (I_{PK})(I_{RIPPLE}) + \frac{(1-D)}{3} I_{RIPPLE}^2}$$

$$I_{\text{RIPPLE}} = \frac{(V_{\text{IN}} - V_{\text{OUT}})(V_{\text{OUT}})}{(f_{\text{OSC}})(L)(V_{\text{IN}})}$$

$$I_{\text{PEAK}} = I_{\text{LOAD}} + \frac{I_{\text{RIPPLE}}}{2} = \frac{I_{\text{OUT}}}{3} + \frac{I_{\text{RIPPLE}}}{2}$$

where:

D = Duty cycle.

For switching power losses:

$$P_D = nCV^2(f_{\text{OSC}})$$

where:

n = number of switch FETs (either top or bottom),

C = FET gate capacitance,

V = maximum gate drive voltage (usually V_{CC}),

f_{OSC} = switching frequency.

System Considerations for the NCP1573

The NCP1573 controller is optimized for converter designs where the power supply for the controller IC has very short turn-on and turn-off times. Such systems can be found providing power to graphics cards or memory where standby power is also provided. The key features of the NCP1573 are that undervoltage lockout and soft start resetting are not included. These features must be absent to allow the NCP1573 to interface in a glitch-free manner with back-up power supplies.

A schematic showing a possible system implementation using the NCP1573 is included in Figure 23. Note that an

external p-channel FET gates the 12 V supply to the IC. The signal also controls an alternate supply that drives a linear regulator. The linear regulator provides back-up power for the load during low-power operation.

In this case, the 12 V supply turn-on and turn-off is so fast that the controller does not charge or discharge the output capacitance significantly during the transition intervals. This minimizes glitching during the transitions. Also, note that a resistor divider and a diode connect the logic signal to the COMP pin of the NCP1573. The divider and diode network serve to hold the COMP voltage up when the IC is powered down. When the power management state changes and the IC powers back up, having the COMP voltage at its correct level further reduces glitching. The correct COMP level is determined to be the IC reference voltage (0.98 V) plus the channel start-up offset of the controller (0.525 V), plus about 10 mV to account for artificial ramp amplitude (total of 1.615 V). The divider voltage must be about 100 mV higher to allow for the diode forward voltage. Note that very little current is assumed to flow through the diode since only capacitor leakage current should be present.

There will always be some small voltage adjustment during transitions due to manufacturing tolerances. Having the COMP voltage slightly low will result in a temporary sag in the output voltage as the linear regulator turns off and the switching supply turns on. Similarly, a positive change in V_{OUT} will occur if the COMP voltage is slightly too high.

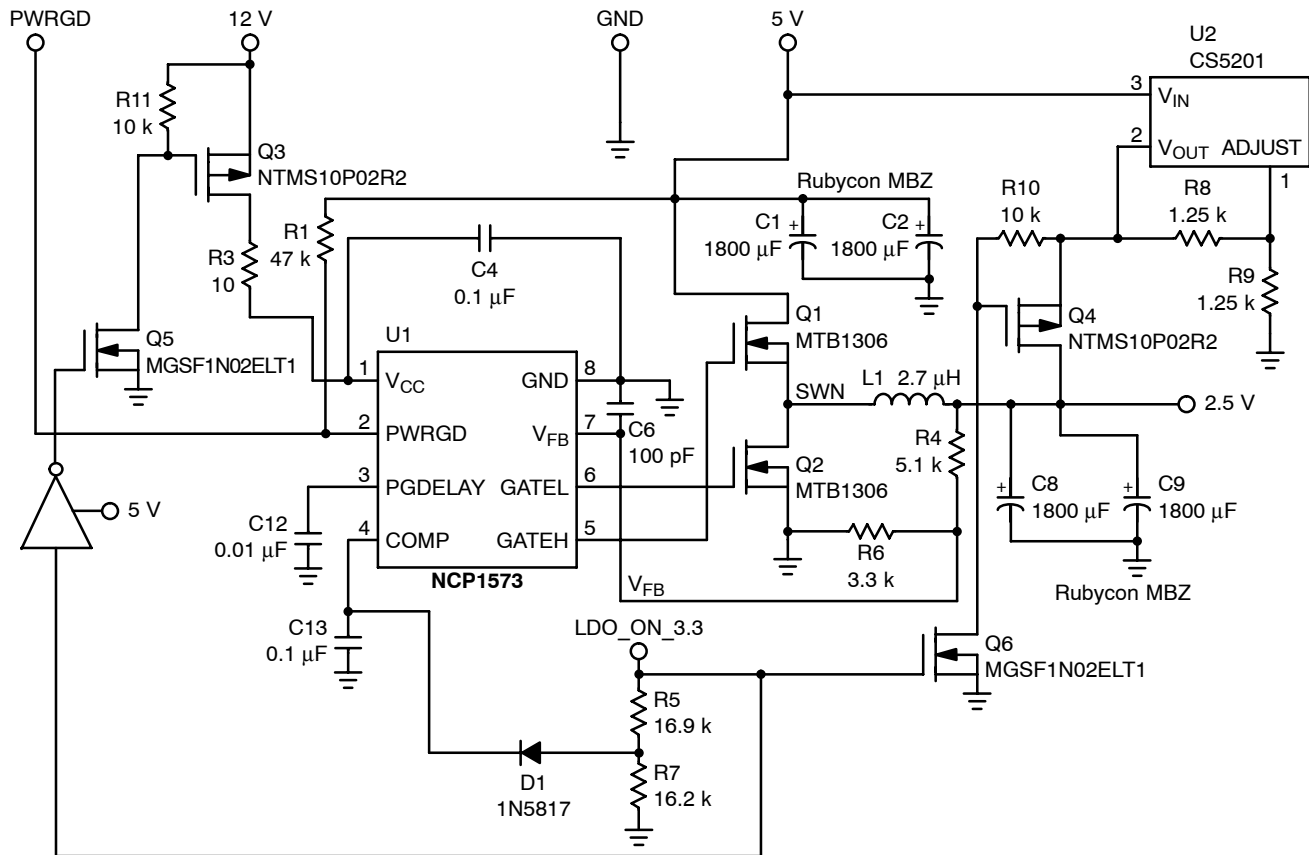


Figure 23.

Providing fast turn-on and turn-off edges to the IC power is very important in minimizing glitching because there is no undervoltage lockout circuitry. For example, if the switcher were powered up and regulating, and the supply began to decrease slowly, the GATE outputs of the IC would continue to switch until the driver circuitry ran out of headroom (when V_{CC} reaches approximately 5 V). When the drivers collapse, an on-chip resistor from the GATE pins to ground will bottom the external n-channel FETs and the switch

node becomes disconnected from the DC-DC converter. Until this happens, it is entirely possible that the bottom FET may have a large duty cycle and be trying to discharge the V_{OUT} capacitance. Additionally, as the bias circuitry in the IC collapses, the reference voltage to the error amplifier may change and result in false regulation. The circuit in Figure 23 will operate properly with turn-on and turn-off times on the order of 500 μ s or faster.

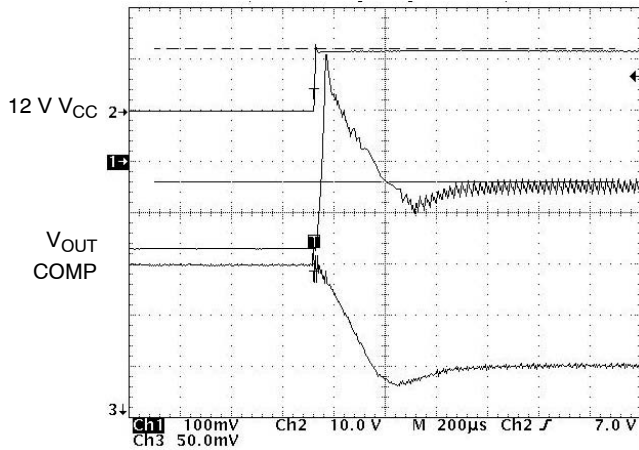


Figure 24. Output Transient with COMP Voltage Positioned 100 mV Too High

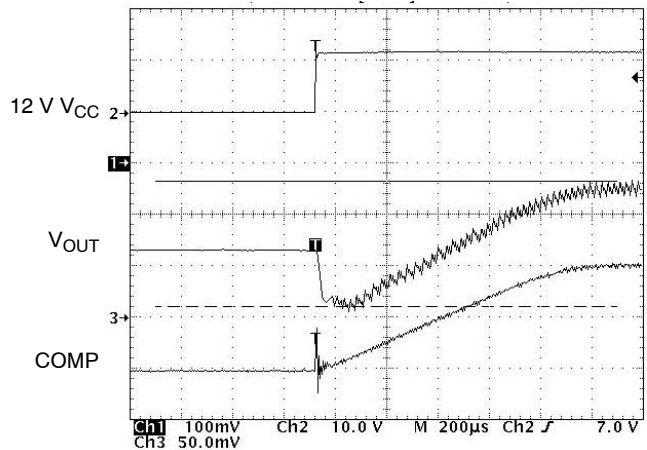
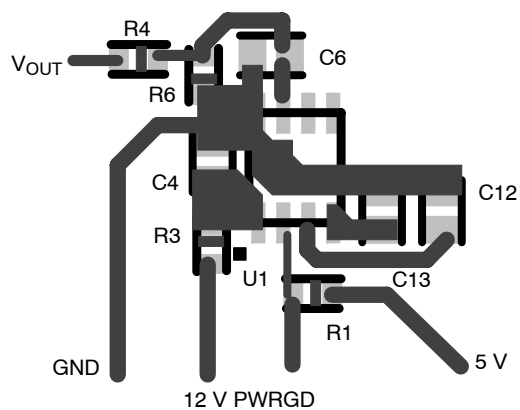


Figure 25. Output Transient with COMP Voltage Positioned 100 mV Too Low

Layout Considerations

1. The fast response time of V^2 technology increases the IC's sensitivity to noise on the V_{FB} line. Fortunately, a simple RC filter, formed by the feedback network and a small capacitor (100 pF works well, shown below as C6) placed between V_{FB} and GND, filters out most noise and provides a system practically immune to jitter. This capacitor should be located as close as possible to the IC.
2. The COMP capacitor (shown below as C13) should be connected via its own path to the IC ground. The COMP capacitor is sensitive to the intermittent ground drops caused by switching currents. A separate ground path will reduce the potential for jitter.
3. The V_{CC} bypass capacitor (0.1 μ F or greater, shown below as C4) should be located as close as possible to the IC. This capacitor's connection to GND must be as short as possible. The 10 Ω resistor (shown below as R3) should be placed close to the V_{CC} pin.

4. The IC should not be placed in the path of switching currents. If a ground plane is used, care should be taken by the designer to ensure that the IC is not located over a ground or other current return path.

**Figure 26.**

NCP1575

Low Voltage Synchronous Buck Controller with Adjustable Switching Frequency

The NCP1575 is a low voltage buck controller. It provides the control for a DC-DC power solution producing an output voltage as low as 0.980 V over a wide current range. It contains all required circuitry for a synchronous NFET buck regulator using the V^2 ™ control method to achieve the fastest possible transient response and best overall regulation. The NCP1575 operates at a default switching frequency of 200 kHz, but switching frequency is user-programmable with an additional resistor between R_{OSC} and ground. This device provides undervoltage lockout protection, soft-start, and built-in adaptive nonoverlap and is assembled in an SOIC-8 package.

The NCP1575-based solution requires a bias supply of 12 V, and it can convert from a bulk power supply ranging from 2 V to 12 V. Conversion from bulk supplies greater than 7 V is best accomplished by using an external doubler circuit to raise the enhancement voltage for the external NFET switches.

Features

- Pb-Free Packages are Available
- 0.980 V $\pm$ 1.0% Reference Voltage
- V^2 Control Topology
- 200 ns Transient Response
- Programmable Soft-Start
- 40 ns Gate Rise and Fall Times (3.3 nF Load)
- Adaptive FET Nonoverlap Time
- Default 200 kHz Oscillator Frequency (No External Resistor Required)
- User-Programmable Oscillator Frequency (One External Resistor Required)
- Undervoltage Lockout
- On/Off Control Through Use of the COMP Pin
- Overvoltage Protection through Synchronous MOSFETs
- Synchronous N-Channel Buck Design
- “12 V Only” or Dual Supply Operation



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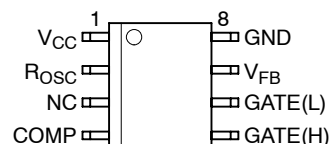
<http://onsemi.com>

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP1575D	SOIC-8	98 Units/Rail
NCP1575DG	SOIC-8 (Pb-Free)	98 Units/Rail
NCP1575DR2	SOIC-8	2500 Tape & Reel
NCP1575DR2G	SOIC-8 (Pb-Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP1575

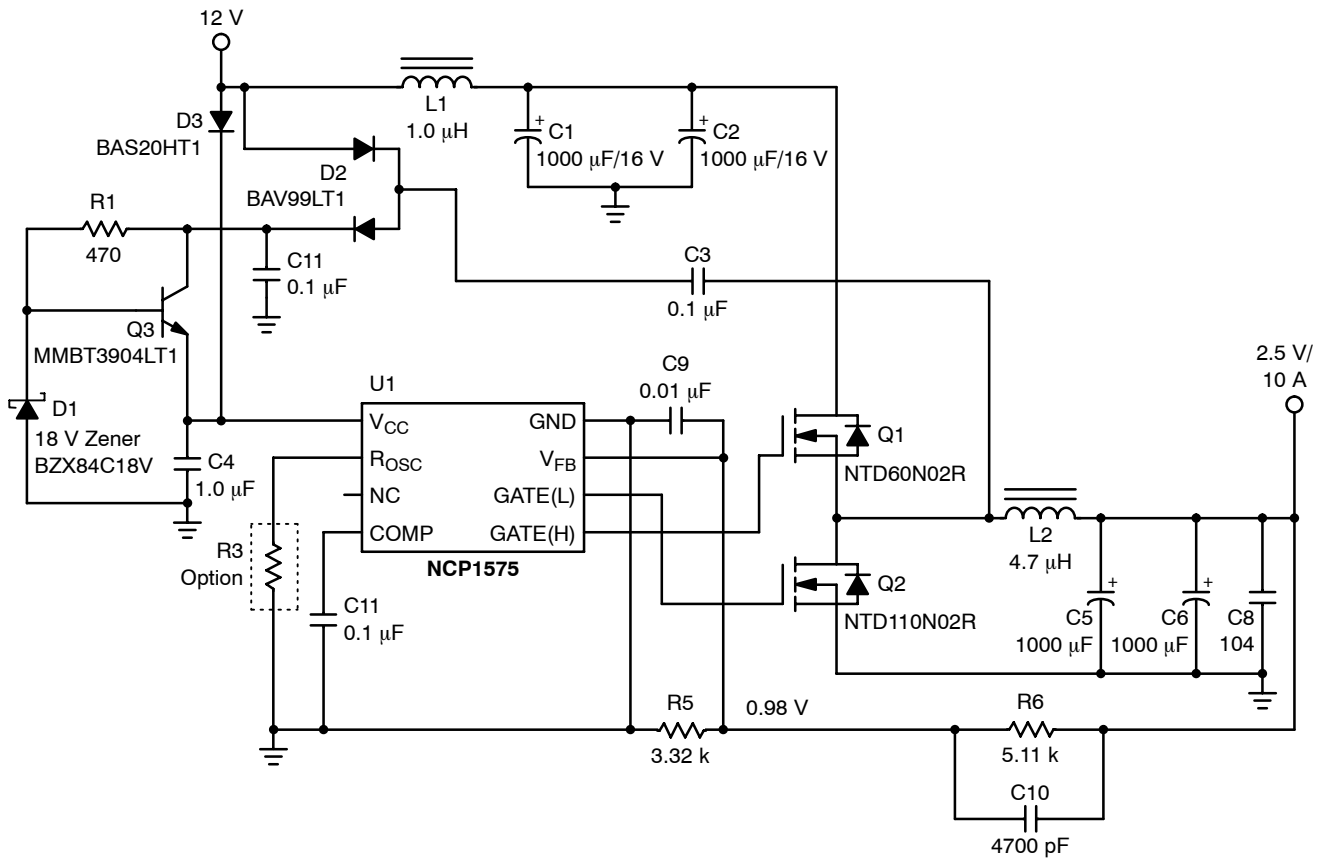


Figure 1. 12 V Only Applications Diagram, 12 V to 2.5 V Conversion at 10 A

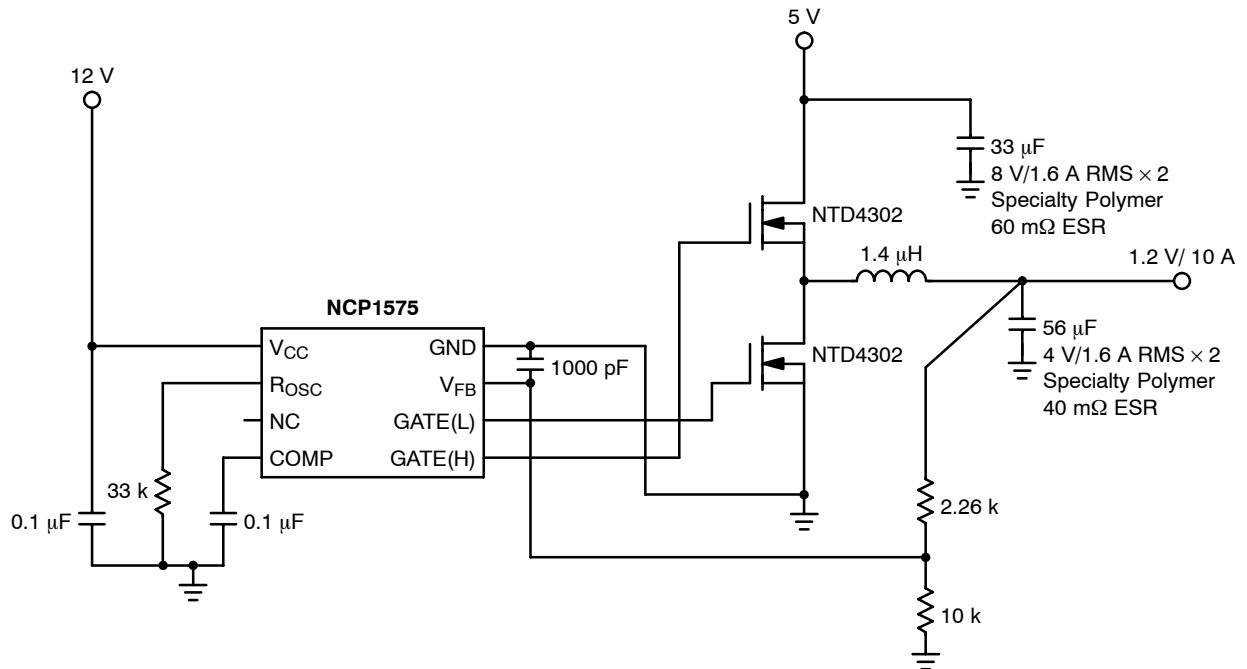


Figure 2. 12 V/5 V Applications Diagram, 350 kHz, 5 V to 1.2 V Conversion at 10 A

NCP1575

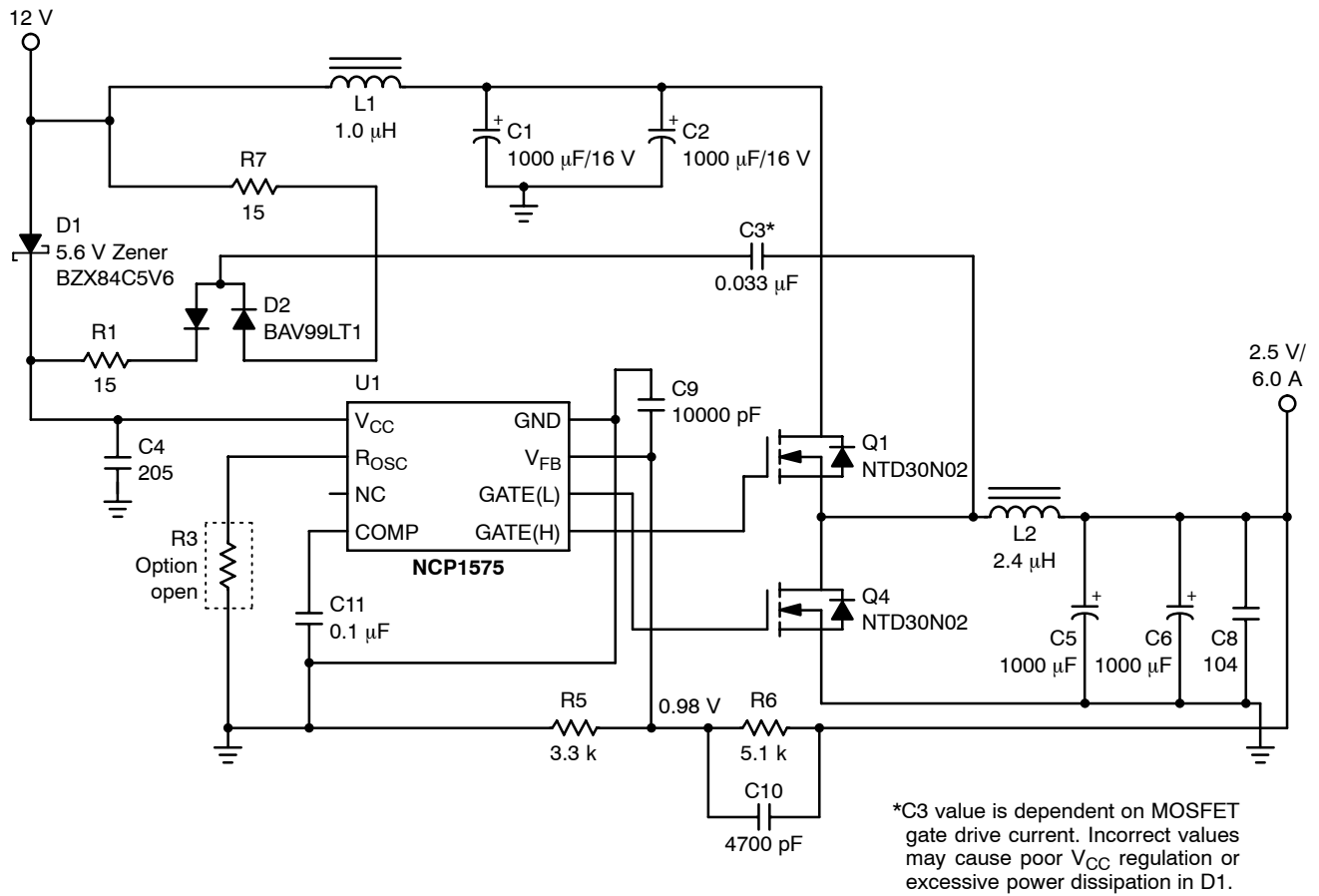


Figure 3. 12 V Only Applications Diagram, 12 V to 2.5 V Conversion at 6 A

MAXIMUM RATINGS

Rating	Value	Unit
Operating Junction Temperature	150	°C
Storage Temperature Range	–65 to 150	°C
ESD Susceptibility (Human Body Model)	2.0	kV
ESD Susceptibility (Charged Device Model)	200	V
Lead Temperature Soldering: Reflow: (Note 1)	230 peak	°C
Moisture Sensitivity Level	2	–
Package Thermal Resistance, SOIC–8: Junction–to–Case, $R_{\theta JC}$ Junction–to–Ambient, $R_{\theta JA}$	48 165	°C/W °C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. 60 second maximum above 183°C.

MAXIMUM RATINGS

Pin Name	Symbol	V _{MAX}	V _{MIN}	I _{SOURCE}	I _{SINK}
IC Power Input	V _{CC}	20 V	–0.5 V	N/A	1.5 A Peak, 450 mA DC
Compensation Capacitor	COMP	6.0 V	–0.5 V	10 mA	10 mA
Voltage Feedback Input	V _{FB}	6.0 V	–0.5 V	1.0 mA	1.0 mA
Frequency Adjust	R _{OSC}	6.0 V	–0.5 V	1.0 mA	1.0 mA
High–Side FET Driver	GATE(H)	20 V	–0.5 V, –2.0 V for 50 ns	1.5 A Peak, 200 mA DC	1.5 A Peak, 200 mA DC
Low–Side FET Driver	GATE(L)	20 V	–0.5 V, –2.0 V for 50 ns	1.5 A Peak, 200 mA DC	1.5 A Peak, 200 mA DC
Ground	GND	0.5 V	–0.5 V	1.5 A Peak, 450 mA DC	N/A

ELECTRICAL CHARACTERISTICS (0°C < T_J < 125°C, 9.0 V < V_{CC} < 20 V, C_{GATE(H)} = C_{GATE(L)} = 3.3 nF, C_{COMP} = 0.1 μF, R_{OSC} = 74 kΩ; unless otherwise specified.) Note 2

Characteristic	Test Conditions	Min	Typ	Max	Unit
Error Amplifier					
V _{FB} Bias Current	V _{FB} = 0 V	–	0.4	2.0	μA
COMP Source Current	COMP = 1.5 V, V _{FB} = 0.8 V	15	30	60	μA
COMP Sink Current	COMP = 1.5 V, V _{FB} = 1.2 V	15	30	60	μA
Reference Voltage	COMP = V _{FB} T _J < 25°C	0.970 0.965	0.980 0.980	0.990 0.995	V V
COMP Max Voltage	V _{FB} = 0.8 V	2.4	3.1	–	V
COMP Min Voltage	V _{FB} = 1.2 V	–	0.1	0.2	V
COMP Fault Discharge Current at UVLO	COMP = 1.2 V, V _{CC} = 6.9 V	0.5	1.2	–	mA
COMP Fault Discharge Threshold to Reset UVLO	–	0.1	0.25	0.3	V
Open Loop Gain	–	–	98	–	dB
Unity Gain Bandwidth	–	–	20	–	kHz
PSRR @ 1.0 kHz	–	–	70	–	dB
Output Transconductance	–	–	32	–	mmho
Output Impedance	–	–	2.5	–	MΩ

2. Characteristics at temperature extremes are guaranteed via correlation using quality statistical control methods.

NCP1575

ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $9.0\text{ V} < V_{CC} < 20\text{ V}$, $C_{\text{GATE(H)}} = C_{\text{GATE(L)}} = 3.3\text{ nF}$, $C_{\text{COMP}} = 0.1\text{ }\mu\text{F}$, $R_{\text{OSC}} = 74\text{ k}\Omega$; unless otherwise specified.) Note 3

Characteristic	Test Conditions	Min	Typ	Max	Unit

GATE(H) and GATE(L)

Rise Time	$1.0\text{ V} < \text{GATE(L)}, \text{GATE(H)} < V_{CC} - 2.0\text{ V}$, $V_{CC} = 12\text{ V}$	–	40	80	ns
Fall Time	$V_{CC} - 2.0\text{ V} < \text{GATE(L)}, \text{GATE(H)} < 1.0\text{ V}$, $V_{CC} = 12\text{ V}$	–	40	80	ns
GATE(H) to GATE(L) Delay	$\text{GATE(H)} < 2.0\text{ V}, \text{GATE(L)} > 2.0\text{ V}$	40	60	105	ns
GATE(L) to GATE(H) Delay	$\text{GATE(L)} < 2.0\text{ V}, \text{GATE(H)} > 2.0\text{ V}$	40	60	105	ns
Minimum Pulse Width	$\text{GATE(X)} = 4.0\text{ V}$	–	250	–	ns
High Voltage (AC)	Measure GATE(L) or GATE(H) $0.5\text{ nF} < C_{\text{GATE(H)}} = C_{\text{GATE(L)}} < 10\text{ nF}$, Note 4	$V_{CC} - 0.5$	V_{CC}	–	V
Low Voltage (AC)	Measure GATE(L) or GATE(H) $0.5\text{ nF} < C_{\text{GATE(H)}} = C_{\text{GATE(L)}} < 10\text{ nF}$, Note 4	–	0	0.5	V
GATE(H)/(L) Pull-Down	Resistance to GND. Note 4	20	50	115	k Ω

PWM Comparator

PWM Comparator Offset	$V_{FB} = 0\text{ V}$, Increase COMP Until GATE(H) Starts Switching	0.415	0.465	0.525	V
Ramp Max Duty Cycle	–	–	80	–	%
Artificial Ramp	Duty Cycle = 50%, $R_{\text{OSC}} = 74\text{ k}\Omega$	50	63	75	mV
Transient Response	COMP = 1.5 V, V_{FB} 20 mV Overdrive. Note 4	–	200	300	ns
V_{FB} Input Range	Note 4	0	–	1.4	V

Oscillator

Switching Frequency	R_{OSC} Not Used $R_{\text{OSC}} = 74\text{ k}\Omega$	170 240	200 280	230 320	kHz kHz

General Electrical Specifications

V_{CC} Supply Current	COMP = 0 V (No Switching)	–	9.0	12	mA
Start Threshold	GATE(H) Switching, COMP Charging	8.0	8.5	9.0	V
Stop Threshold	GATE(H) Not Switching, COMP Discharging	7.0	7.5	8.0	V
Hysteresis	Start – Stop	0.75	1.0	1.25	V

3. Characteristics at temperature extremes are guaranteed via correlation using quality statistical control methods.

4. Guaranteed by design. Not tested in production.

PACKAGE PIN DESCRIPTION

PIN #	PIN SYMBOL	FUNCTION
1	V _{CC}	Power supply input.
2	R _{OSC}	Frequency adjust pin. If not used, oscillator frequency is nominally 200 kHz. Connecting R _{OSC} to ground through a single resistor will increase oscillator frequency.
3	NC	No connect.
4	COMP	Error amp output. PWM comparator reference input. A capacitor to LGND provides error amp compensation and Soft-Start. Pulling pin < 0.415 V locks gate outputs to a zero percent duty cycle state.
5	GATE(H)	High-side switch FET driver pin. Capable of delivering peak currents of 1.5 A.
6	GATE(L)	Low-side synchronous FET driver pin. Capable of delivering peak currents of 1.5 A.
7	V _{FB}	Error amplifier and PWM comparator input.
8	GND	Power supply return.

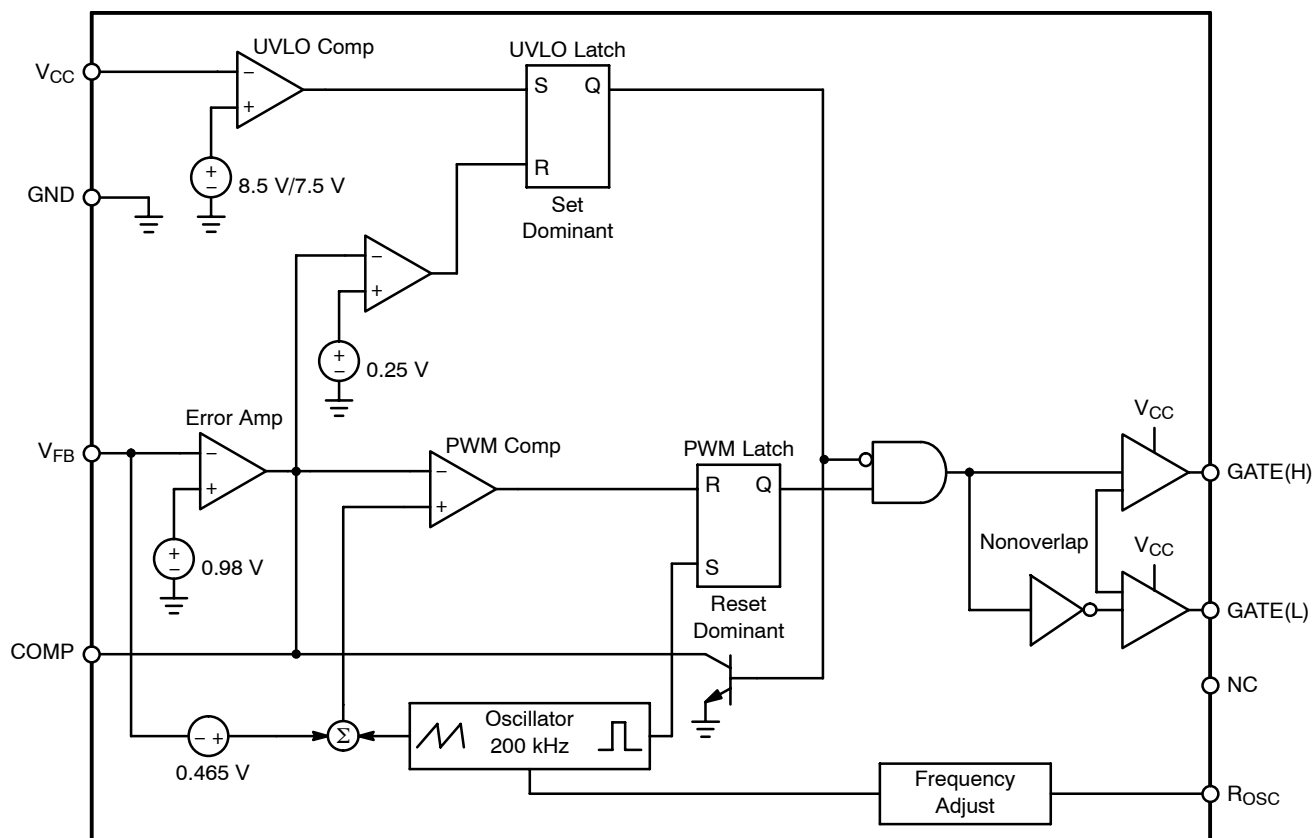


Figure 4. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

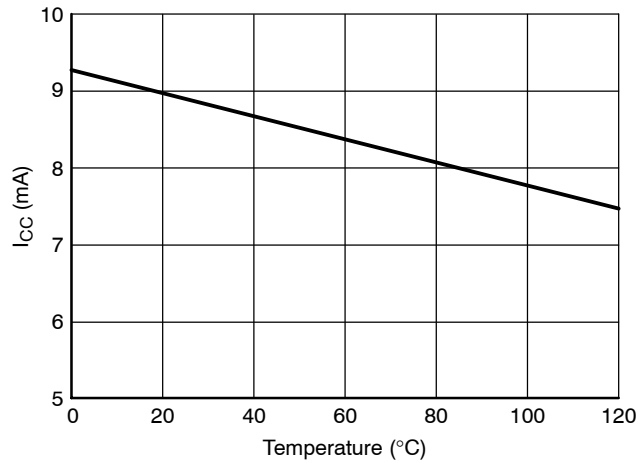


Figure 5. Supply Current vs. Temperature

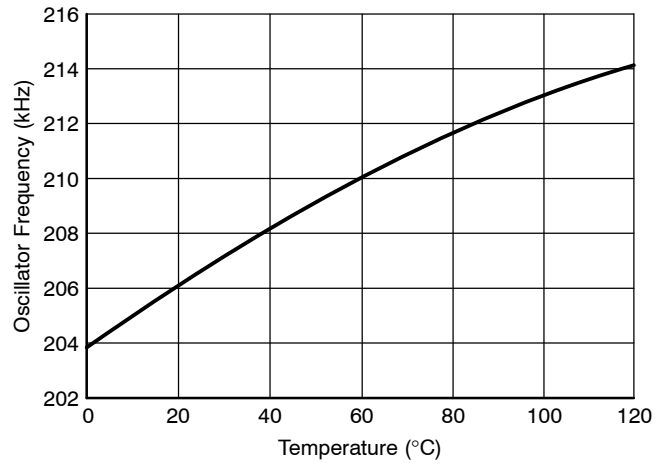


Figure 6. Oscillator Frequency vs. Temperature
(No R_{OSC})

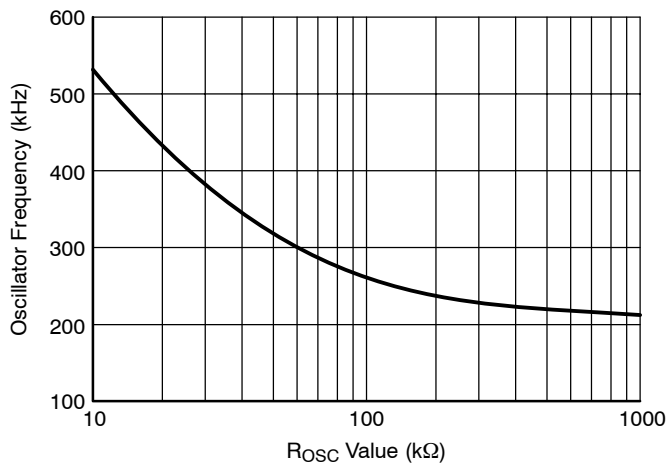


Figure 7. Oscillator Frequency vs. R_{OSC} Value

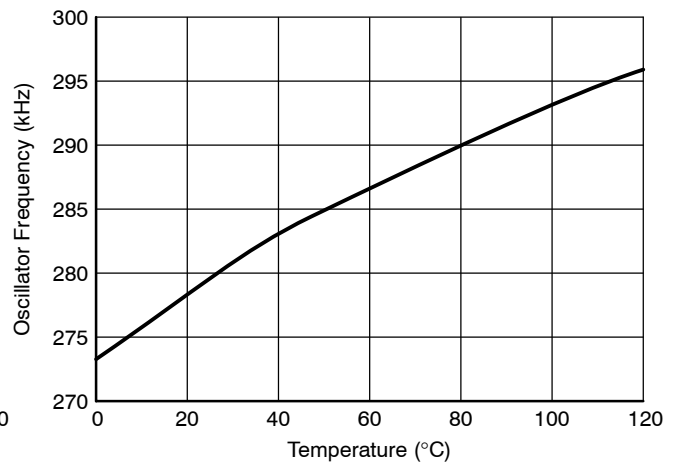


Figure 8. Oscillator Frequency (R_{OSC} = 74 kΩ)
vs. Temperature

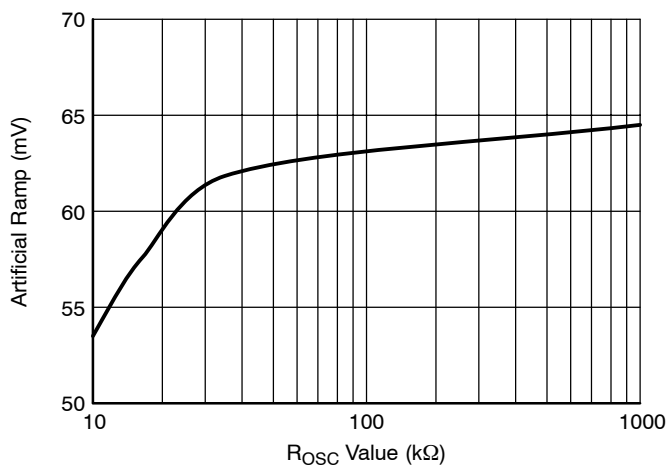


Figure 9. Artificial Ramp at 50% Duty Cycle
vs. R_{OSC} Value

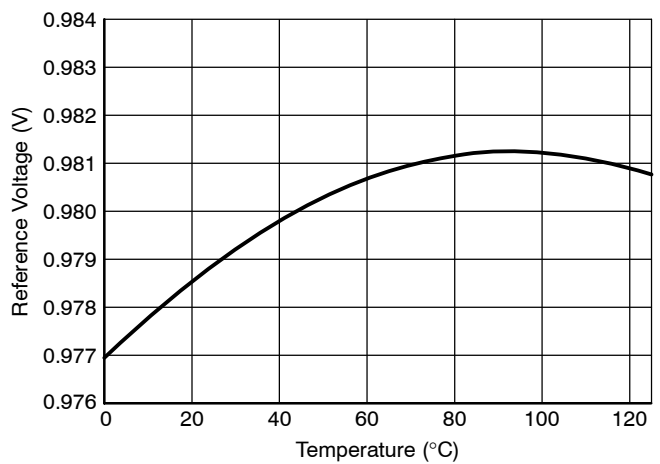


Figure 10. Reference Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

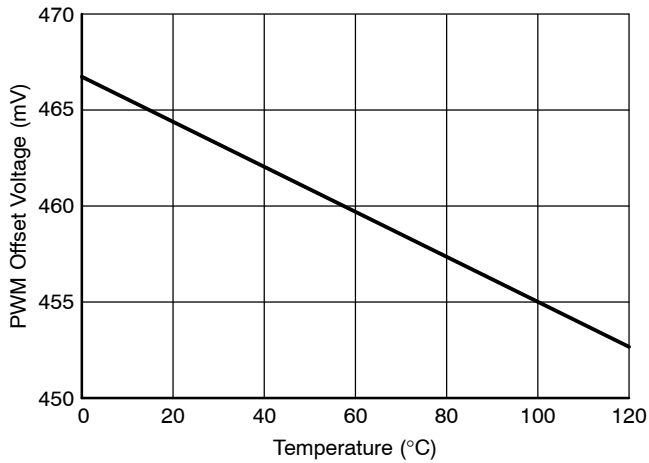


Figure 11. PWM Offset Voltage vs. Temperature

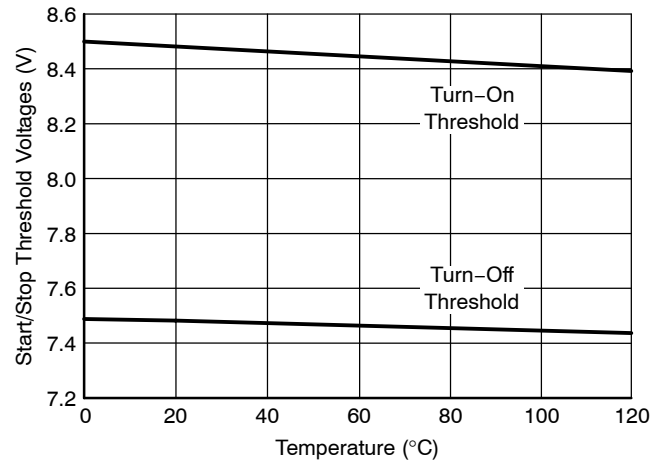


Figure 12. Undervoltage Lockout Thresholds vs. Temperature

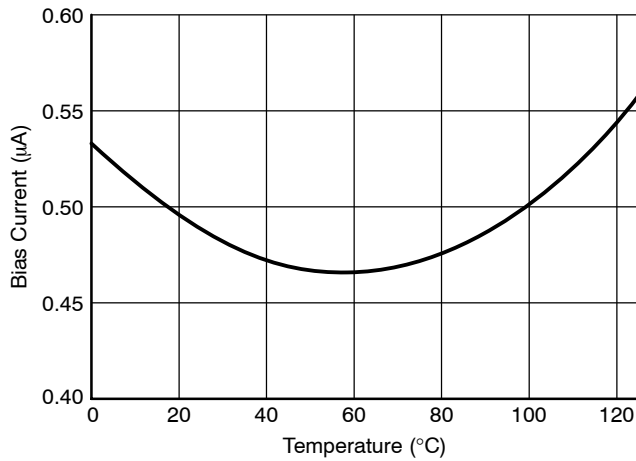


Figure 13. V_{FB} Bias Current vs. Temperature

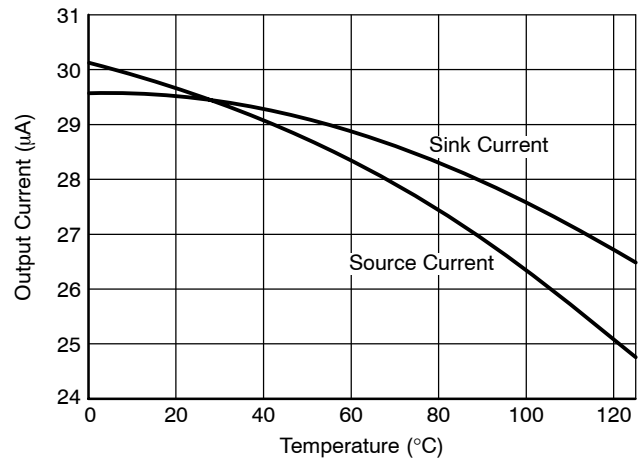


Figure 14. Error Amp Output Currents vs. Temperature

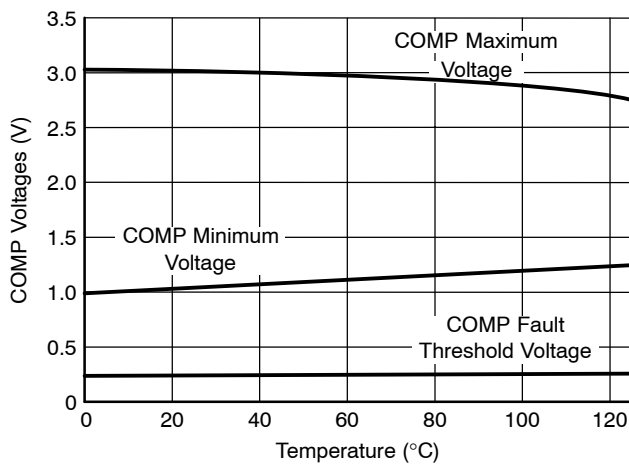


Figure 15. COMP Voltages vs. Temperature

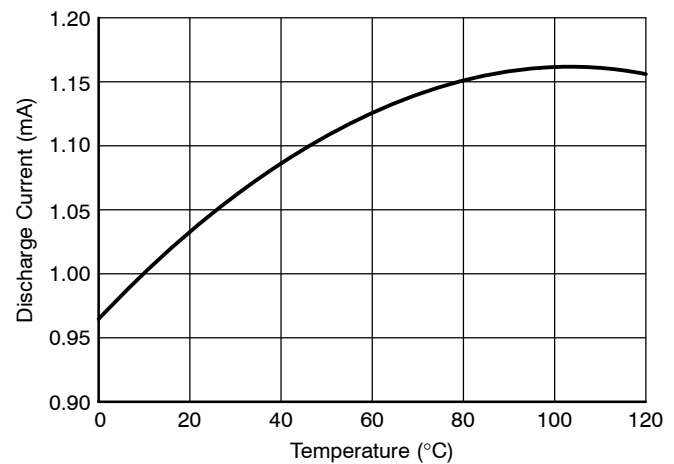


Figure 16. COMP Fault Mode Discharge Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

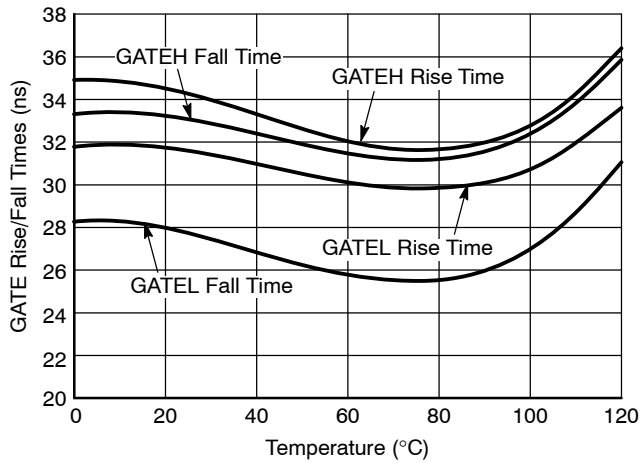


Figure 17. GATE Output Rise and Fall Times vs. Temperature ($V_{CC} = 12\text{ V}$)

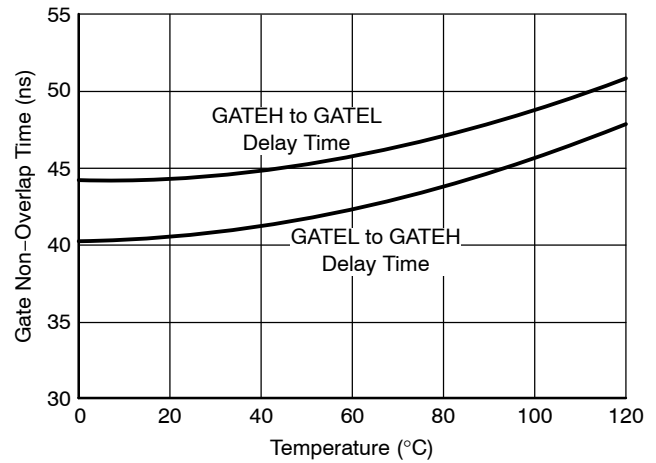


Figure 18. GATE Nonoverlap Times vs. Temperature

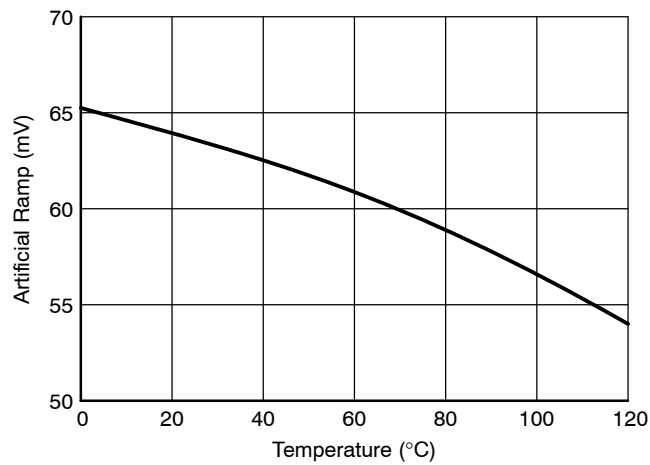


Figure 19. Artificial Ramp at 50% Duty Cycle (R_{OSC} Not Used)

APPLICATION INFORMATION

THEORY OF OPERATION

The NCP1575 is a simple, synchronous, fixed-frequency, low-voltage buck controller using the V^2 control method.

 V^2 Control Method

The V^2 control method uses a ramp signal generated by the ESR of the output capacitors. This ramp is proportional to the ac current through the main inductor and is offset by the dc output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. The V^2 method differs from traditional techniques such as voltage mode control, which generates an artificial ramp, and current mode control, which generates a ramp using the inductor current.

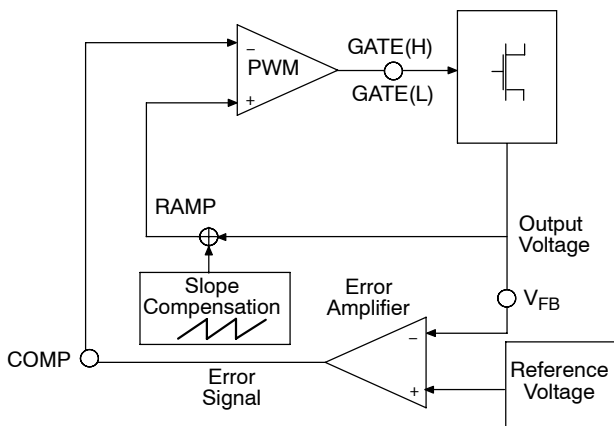


Figure 20. V^2 Control with Slope Compensation

The V^2 control method is illustrated in Figure 20. The output voltage generates both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output, regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, allowing the control circuit to drive the main switch from 0% to 100% duty cycle as required.

A variation in line voltage changes the current ramp in the inductor, which causes the V^2 control scheme to compensate the duty cycle. Since any variation in inductor current modifies the ramp signal, as in current mode control, the V^2 control scheme offers the same advantages in line transient response.

A variation in load current will affect the output voltage, modifying the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. The comparator response time and the transition speed of the main switch determine the load transient response. Unlike traditional control methods, the reaction time to the output load step is not related to the crossover frequency of the error signal loop.

The error signal loop can have a low crossover frequency, since the transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide dc accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent control loops. A voltage mode controller relies on the change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains a fixed error signal during line transients, since the slope of the ramp signal changes in this case. However, regulation of load transients still requires a change in the error signal. The V^2 method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

The stringent load transient requirements of modern microprocessors require the output capacitors to have very low ESR. The resulting shallow slope in the output ripple can lead to pulse width jitter and variation caused by both random and synchronous noise. A ramp waveform generated in the oscillator is added to the ramp signal from the output voltage to provide the proper voltage ramp at the beginning of each switching cycle. This slope compensation increases the noise immunity, particularly at duty cycles above 50%.

Startup

The NCP1575 features a programmable soft-start function, which is implemented through the error amplifier and the external compensation capacitor. This feature prevents stress to the power components and limits output voltage overshoot during startup. As power is applied to the regulator, the NCP1575 undervoltage lockout circuit (UVL) monitors the IC's supply voltage (V_{CC}). The UVL circuit holds the GATE(H) output low and the GATE(L) output high until V_{CC} exceeds the 8.5 V threshold. A hysteresis function of 1.0 V improves noise immunity. The compensation capacitor connected to the COMP pin is charged by a 30 μ A current source. When the capacitor voltage exceeds the 0.465 V offset of the PWM comparator, the PWM control loop will allow switching to occur. The upper gate driver GATE(H) is activated, turning on the upper MOSFET. The current ramps up through the main inductor and linearly powers the output capacitors and load. When the regulator output voltage exceeds the COMP pin voltage minus the 0.465 V PWM comparator offset threshold and the artificial ramp, the PWM comparator terminates the initial pulse.

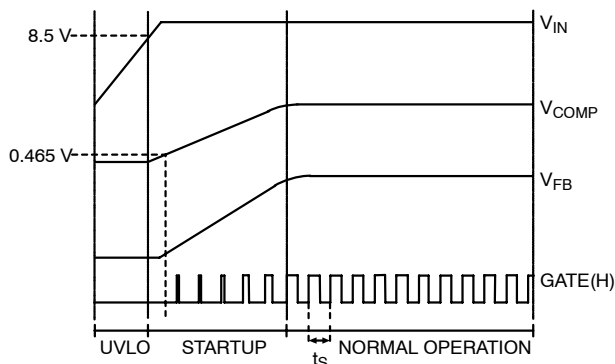


Figure 21. Idealized Waveforms

Normal Operation

During normal operation, the duty cycle of the gate drivers remains approximately constant as the V^2 control loop maintains the regulated output voltage under steady state conditions. Variations in supply line or output load conditions will result in changes in duty cycle to maintain regulation.

Input Supplies

The NCP1575 can be used in applications where a 12 V supply is available along with a lower voltage supply. Often the lower voltage supply is 5 V, but it can be any voltage less than the 12 V supply minus the required gate drive voltage of the top MOSFET. The greater the difference between the two voltages, the better the efficiency due to increasing V_{GS} available to turn on the upper MOSFET. In order to maintain power supply stability, the lower supply voltage should be at least 1.5 times the desired voltage.

Adding a few additional components allows the NCP1575 to convert power in a “12 V only” application. This circuit is illustrated in Figure 1. Note that in all cases, the maximum supply voltage specification of 20 V must not be exceeded.

Gate Charge Effect on Switching Times

When using the onboard gate drivers, the gate charge has an important effect on the switching times of the FETs. A finite amount of time is required to charge the effective capacitor seen at the gate of the FET. Therefore, the rise and fall times rise linearly with increased capacitive loading.

Transient Response

The 200 ns reaction time of the control loop provides fast transient response to any variations in input voltage and output current. Pulse-by-pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitors during the time required to slew the inductor current. For better transient response, several high frequency and bulk output capacitors are usually used.

Overvoltage Protection

Overvoltage protection is provided as a result of the normal operation of the V^2 control method and requires no additional external components. The control loop responds

to an overvoltage condition within 200 ns, turning off the upper MOSFET and disconnecting the regulator from its input voltage. This results in a crowbar action to clamp the output voltage, preventing damage to the load. The regulator remains in this state until the overvoltage condition ceases.

Shutdown

When the input voltage connected to V_{CC} falls through the lower threshold of the UVLO comparator, a fault latch is set. The fault latch provides a signal that forces both GATE(H) low and GATE(L) high, producing a low-impedance current sink to ground at the converter switch node. At the same time, the latch also turns on a transistor which pulls down on the COMP pin, quickly discharging the external capacitor, and allowing COMP to fall.

CONVERTER DESIGN

Choosing the V_{OUT} Resistor Divider Values

The NCP1575 has an internal 0.98 V reference. A resistor divider is used to set the output voltage.

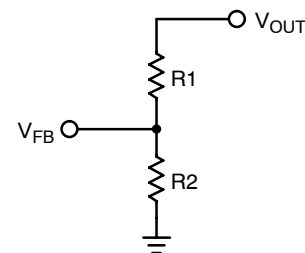


Figure 22.

The formula to set the output voltage is

$$V_{OUT} = (R1/R2 + 1) * (0.98 \text{ V})$$

Arbitrarily choose a value of $R2$ that is sufficiently low that the V_{FB} bias current (typically 50 nA) will have negligible effect on the output voltage. Solve the equation above for the value of $R1$.

Choosing the Oscillator Frequency

The NCP1575 has an oscillator that is trimmed to 200 kHz at the factory. The NCP1575 will operate at this frequency without the addition of any external components. However, the oscillator is user-programmable with a single resistor. This resistor is connected between the R_{OSC} pin and ground. Adding this resistor will raise the frequency above 200 kHz. A graph of oscillator frequency vs. R_{OSC} resistance is provided in the typical operating characteristics section of this data sheet.

Selection of the Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the regulator output voltage. Key specifications for output capacitors are their Equivalent

Series Resistance (ESR), and Equivalent Series Inductance (ESL). For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

In order to determine the number of output capacitors the maximum voltage transient allowed during load transitions has to be specified. The output capacitors must hold the output voltage within these limits since the inductor current can not change with the required slew rate. The output capacitors must therefore have a very low ESL and ESR.

The voltage change during the load current transient is:

$$\Delta V_{OUT} = \Delta I_{OUT} \times \left(\frac{ESL}{\Delta t} + ESR + \frac{t_{TR}}{C_{OUT}} \right)$$

where:

$\Delta I_{OUT} / \Delta t$ = load current slew rate;

ΔI_{OUT} = load transient;

Δt = load transient duration time;

ESL = Maximum allowable ESL including capacitors, circuit traces, and vias;

ESR = Maximum allowable ESR including capacitors and circuit traces;

t_{TR} = output voltage transient response time.

The designer has to independently assign values for the change in output voltage due to ESR, ESL, and output capacitor discharging or charging. Empirical data indicates that most of the output voltage change (droop or spike depending on the load current transition) results from the total output capacitor ESR.

The maximum allowable ESR can then be determined according to the formula:

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

where:

ΔV_{ESR} = change in output voltage due to ESR (assigned by the designer)

Once the maximum allowable ESR is determined, the number of output capacitors can be found by using the formula:

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

where:

ESR_{CAP} = maximum ESR per capacitor (specified in manufacturer's data sheet).

ESR_{MAX} = maximum allowable ESR.

The actual output voltage deviation due to ESR can then be verified and compared to the value assigned by the designer:

$$\Delta V_{ESR} = \Delta I_{OUT} \times ESR_{MAX}$$

Similarly, the maximum allowable ESL is calculated from the following formula:

$$ESL_{MAX} = \frac{\Delta V_{ESL} \times \Delta t}{\Delta I}$$

Selection of the Input Inductor

A common requirement is that the buck controller must not disturb the input voltage. One method of achieving this is by using an input inductor and a bypass capacitor. The input inductor isolates the supply from the noise generated in the switching portion of the buck regulator and also limits the inrush current into the input capacitors upon power up. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients. The worst case is when the load changes from no load to full load (load step), a condition under which the highest voltage change across the input capacitors is also seen by the input inductor. The inductor successfully blocks the ripple current while placing the transient current requirements on the input bypass capacitor bank, which has to initially support the sudden load change.

The minimum inductance value for the input inductor is therefore:

$$L_{IN} = \frac{\Delta V}{(dI/dt)_{MAX}}$$

where:

L_{IN} = input inductor value;

ΔV = voltage seen by the input inductor during a full load swing;

$(dI/dt)_{MAX}$ = maximum allowable input current slew rate.

The designer must select the LC filter pole frequency so that at least 40 dB attenuation is obtained at the regulator switching frequency. The LC filter is a double-pole network with a slope of -2.0, a roll-off rate of -40 dB/dec, and a corner frequency:

$$f_C = \frac{1}{2\pi \times \sqrt{LC}}$$

where:

L = input inductor;

C = input capacitor(s).

Selection of the Output Inductor

There are many factors to consider when choosing the output inductor. Maximum load current, core and winding losses, ripple current, short circuit current, saturation characteristics, component height and cost are all variables that the designer should consider. However, the most important consideration may be the effect inductor value has on transient response.

The amount of overshoot or undershoot exhibited during a current transient is defined as the product of the current step and the output filter capacitor ESR. Choosing the inductor value appropriately can minimize the amount of energy that must be transferred from the inductor to the capacitor or vice-versa. In the subsequent paragraphs, we will determine the minimum value of inductance required for our system and consider the trade-off of ripple current vs. transient response.

In order to choose the minimum value of inductance, input voltage, output voltage and output current must be known. Most computer applications use reasonably well regulated bulk power supplies so that, while the equations below specify $V_{IN(MAX)}$ or $V_{IN(MIN)}$, it is possible to use the nominal value of V_{IN} in these calculations with little error.

Current in the inductor while operating in the continuous current mode is defined as the load current plus ripple current.

$$I_L = I_{LOAD} + I_{RIPPLE}$$

The ripple current waveform is triangular, and the current is a function of voltage across the inductor, switch FET on-time and the inductor value. FET on-time can be defined as the product of duty cycle and switch frequency, and duty cycle can be defined as a ratio of V_{OUT} to V_{IN} . Thus,

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{(f_{OSC})(L)(V_{IN})}$$

Peak inductor current is defined as the load current plus half of the peak current. Peak current must be less than the maximum rated FET switch current, and must also be less than the inductor saturation current. Thus, the maximum output current can be defined as:

$$I_{OUT(MAX)} = I_{SWITCH(MAX)} - \frac{(V_{IN(MAX)} - V_{OUT})V_{OUT}}{(2)(f_{OSC})(L)(V_{IN(MAX)})}$$

Since the maximum output current must be less than the maximum switch current, the minimum inductance required can be determined.

$$L_{(MIN)} = \frac{(V_{IN(MIN)} - V_{OUT})V_{OUT}}{(f_{OSC})(I_{SWITCH(MAX)})(V_{IN(MIN)})}$$

This equation identifies the value of inductor that will provide the full rated switch current as inductor ripple current, and will usually result in inefficient system operation. The system will sink current away from the load during some portion of the duty cycle unless load current is greater than half of the rated switch current. Some value larger than the minimum inductance must be used to ensure the converter does not sink current. Choosing larger values of inductor will reduce the ripple current, and inductor value can be designed to accommodate a particular value of ripple current by replacing $I_{SWITCH(MAX)}$ with a desired value of I_{RIPPLE} :

$$L_{(RIPPLE)} = \frac{(V_{IN(MIN)} - V_{OUT})V_{OUT}}{(f_{OSC})(I_{RIPPLE})(V_{IN(MIN)})}$$

However, reducing the ripple current will cause transient response times to increase. The response times for both increasing and decreasing current steps are shown below.

$$T_{RESPONSE(INCREASING)} = \frac{(L)(\Delta I_{OUT})}{(V_{IN} - V_{OUT})}$$

$$T_{RESPONSE(DECREASING)} = \frac{(L)(\Delta I_{OUT})}{(V_{OUT})}$$

Inductor value selection also depends on how much output ripple voltage the system can tolerate. Output ripple voltage is defined as the product of the output ripple current and the output filter capacitor ESR.

Thus, output ripple voltage can be calculated as:

$$V_{RIPPLE} = (ESR_C)(I_{RIPPLE}) = \frac{(ESR_C)(V_{IN} - V_{OUT})V_{OUT}}{(f_{OSC})(L)(V_{IN})}$$

Finally, we should consider power dissipation in the output inductors. Power dissipation is proportional to the square of inductor current:

$$P_D = (I_L^2)(ESR_L)$$

The temperature rise of the inductor relative to the air surrounding it is defined as the product of power dissipation and thermal resistance to ambient:

$$\Delta T(\text{inductor}) = (R_a)(P_D)$$

R_a for an inductor designed to conduct 20 A to 30 A is approximately 45°C/W. The inductor temperature is given as:

$$T(\text{inductor}) = \Delta T(\text{inductor}) + T_{\text{ambient}}$$

V_{CC} Bypass Filtering

A small RC filter should be added between module V_{CC} and the V_{CC} input to the IC. A 10 Ω resistor and a 0.47 μF capacitor should be sufficient to ensure the controller IC does not operate erratically due to injected noise, and will also supply reserve charge for the onboard gate drivers.

Input Filter Capacitors

The input filter capacitors provide a charge reservoir that minimizes supply voltage variations due to changes in current flowing through the switch FETs. These capacitors must be chosen primarily for ripple current rating.

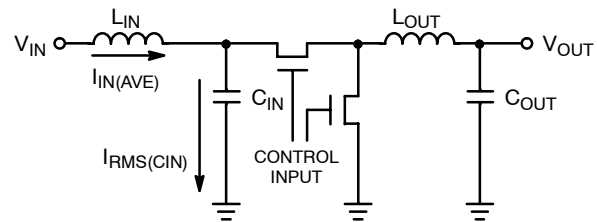


Figure 23.

Consider the schematic shown in Figure 23. The average current flowing in the input inductor L_{IN} for any given output current is:

$$I_{IN(AVE)} = I_{OUT} \times \frac{V_{OUT}}{V_{IN}}$$

Input capacitor current is positive into the capacitor when the switch FETs are off, and negative out of the capacitor when the switch FETs are on. When the switches are off, $I_{IN(AVE)}$ flows into the capacitor. When the switches are on, capacitor current is equal to the per-phase output current

minus $I_{IN(AVE)}$. If we ignore the small current variation due to the output ripple current, we can approximate the input capacitor current waveform as a square wave. We can then calculate the RMS input capacitor ripple current:

$$I_{RMS(CIN)} = \sqrt{I_{IN(AVE)}^2 + \frac{V_{OUT}}{V_{IN}} \times [(I_{OUT \text{ per phase}} - I_{IN(AVE)})^2 - I_{IN(AVE)}^2]}$$

The input capacitance must be designed to conduct the worst case input ripple current. This will require several capacitors in parallel. In addition to the worst case current, attention must be paid to the capacitor manufacturer's derating for operation over temperature.

As an example, let us define the input capacitance for a 5 V to 3.3 V conversion at 10 A at an ambient temperature of 60°C. Efficiency of 80% is assumed. Average input current in the input filter inductor is:

$$I_{IN(AVE)} = (10 \text{ A})(3.3 \text{ V}/5 \text{ V}) = 6.6 \text{ A}$$

Input capacitor RMS ripple current is then

$$I_{IN(RMS)} = \sqrt{6.6^2 + \frac{3.3 \text{ V}}{5 \text{ V}} \times [(10 \text{ A} - 6.6 \text{ A})^2 - 6.6 \text{ A}^2]} \\ = 4.74 \text{ A}$$

If we consider a Rubycon MBZ series capacitor, the ripple current rating for a 6.3 V, 1800 nF capacitor is 2000 mA at 100 kHz and 105°C. We determine the number of input capacitors by dividing the ripple current by the per-capacitor current rating:

$$\text{Number of capacitors} = 4.74 \text{ A}/2.0 \text{ A} = 2.3$$

A total of at least 3 capacitors in parallel must be used to meet the input capacitor ripple current requirements.

Output Switch FETs

Output switch FETs must be chosen carefully, since their properties vary widely from manufacturer to manufacturer. The NCP1575 system is designed assuming that n-channel FETs will be used. The FET characteristics of most concern are the gate charge/gate-source threshold voltage, gate capacitance, on-resistance, current rating and the thermal capability of the package.

The onboard FET driver has a limited drive capability. If the switch FET has a high gate charge, the amount of time the FET stays in its ohmic region during the turn-on and turn-off transitions is larger than that of a low gate charge FET, with the result that the high gate charge FET will consume more power. Similarly, a low on-resistance FET will dissipate less power than will a higher on-resistance

FET at a given current. Thus, low gate charge and low $R_{DS(ON)}$ will result in higher efficiency and will reduce generated heat.

It can be advantageous to use multiple switch FETs to reduce power consumption. By placing a number of FETs in parallel, the effective $R_{DS(ON)}$ is reduced, thus reducing the ohmic power loss. However, placing FETs in parallel increases the gate capacitance so that switching losses increase. As long as adding another parallel FET reduces the ohmic power loss more than the switching losses increase, there is some advantage to doing so. However, at some point the law of diminishing returns will take hold, and a marginal increase in efficiency may not be worth the board area required to add the extra FET. Additionally, as more FETs are used, the limited drive capability of the FET driver will have to charge a larger gate capacitance, resulting in increased gate voltage rise and fall times. This will affect the amount of time the FET operates in its ohmic region and will increase power dissipation.

The following equations can be used to calculate power dissipation in the switch FETs.

For ohmic power losses due to $R_{DS(ON)}$:

$$P_{ON(TOP)} = \frac{(R_{DS(ON)}(TOP))(I_{RMS(TOP)})^2}{(\text{number of topside FETs})}$$

$$P_{ON(BOTTOM)} = \frac{(R_{DS(ON)}(BOTTOM))(I_{RMS(BOTTOM)})^2}{(\text{number of bottom-side FETs})}$$

Note that $R_{DS(ON)}$ increases with temperature. It is good practice to use the value of $R_{DS(ON)}$ at the FET's maximum junction temperature in the calculations shown above.

$$I_{RMS(TOP)} = \sqrt{I_{PK}^2 - (I_{PK})(I_{RIPPLE}) + \frac{D}{3} I_{RIPPLE}^2}$$

$$I_{RMS(BOTTOM)} = \sqrt{I_{PK}^2 - (I_{PK})(I_{RIPPLE}) + \frac{(1-D)}{3} I_{RIPPLE}^2}$$

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_{OSC})(L)(V_{IN})}$$

$$I_{PEAK} = I_{LOAD} + \frac{I_{RIPPLE}}{2} = \frac{I_{OUT}}{3} + \frac{I_{RIPPLE}}{2}$$

where:

D = Duty cycle.

For switching power losses:

$$P_D = nCV^2(f_{OSC})$$

where:

n = number of switch FETs (either top or bottom),

C = FET gate capacitance,

V = maximum gate drive voltage (usually V_{CC}),

f_{OSC} = switching frequency.

Layout Considerations

1. The fast response time of V^2 technology increases the IC's sensitivity to noise on the V_{FB} line. Fortunately, a simple RC filter, formed by the feedback network and a small capacitor (100 pF works well) placed between V_{FB} and GND filters out most noise and provides a system practically immune to jitter. This capacitor should be located as close as possible to the IC.
2. The COMP capacitor should be connected via its own path to the IC ground. The COMP capacitor is sensitive to the intermittent ground drops caused

by switching currents. A separate ground path will reduce the potential for jitter.

3. The V_{CC} bypass capacitor (0.1 μ F or greater) should be located as close as possible to the IC. This capacitor's connection to GND must be as short as possible. A 10 Ω resistor should be placed close to the V_{CC} pin.
4. The IC should not be placed in the path of switching currents. If a ground plane is used, care should be taken by the designer to ensure that the IC is not located over a ground or other current return path.

NCP1580

Low Voltage Synchronous Buck Controller

The NCP1580 is a voltage mode PWM controller designed to operate from a 5.0 V or 12 V supply and produce an output voltage as low as 0.8 V. This 8-pin device provides an optimal level of integration to reduce size and cost of the power supply. The NCP1580 has a fixed 350 kHz oscillator and soft-start function. The NCP1580 provides a 1.5 A floating gate driver design to drive N-Channel MOSFETs in a synchronous configuration. Adaptive non-overlap circuitry reduces switching losses by preventing simultaneous conduction of both outputs. Protection features include thermal shutdown and undervoltage lockout (UVLO). The NCP1580 is available in an 8-pin SOIC package.

Features

- Input Voltage Range from 4.5 V to 13.2 V
- 350 kHz Internal Oscillator
- Boost Pin Operates to 26.5 V
- Voltage Mode PWM Control
- $0.8\text{ V} \pm 1.5\%$ Internal Reference Voltage
- Adjustable Output Voltage
- Internal Soft-Start
- Internal 1.5 A Gate Drivers
- Adaptive Non-Overlap Circuit
- 90% Max Duty Cycle
- Input UVLO
- Overtemperature Protection
- Fully Specified over -40°C to 85°C
- Pb-Free Package is Available

Applications

- Graphics Cards
- Desktop Computers
- Servers/Networking
- DSP and FPGA Power Supply
- DC-DC Regulator Modules



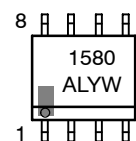
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM

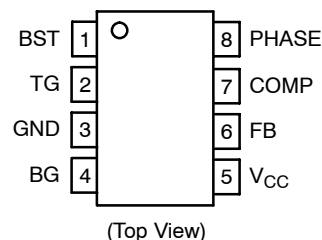


**SOIC-8
D SUFFIX
CASE 751**



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping [†]
NCP1580DR2	SOIC-8	2500/Tape & Reel
NCP1580DR2G	SOIC-8 (Pb-Free)	2500/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

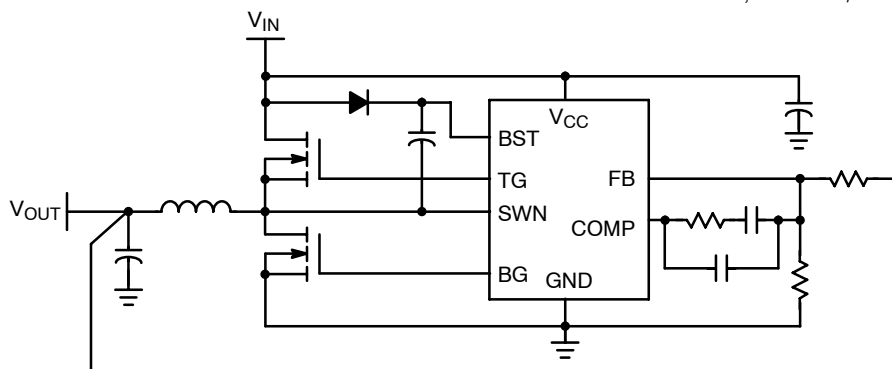


Figure 1. Typical Application Diagram

NCP1580

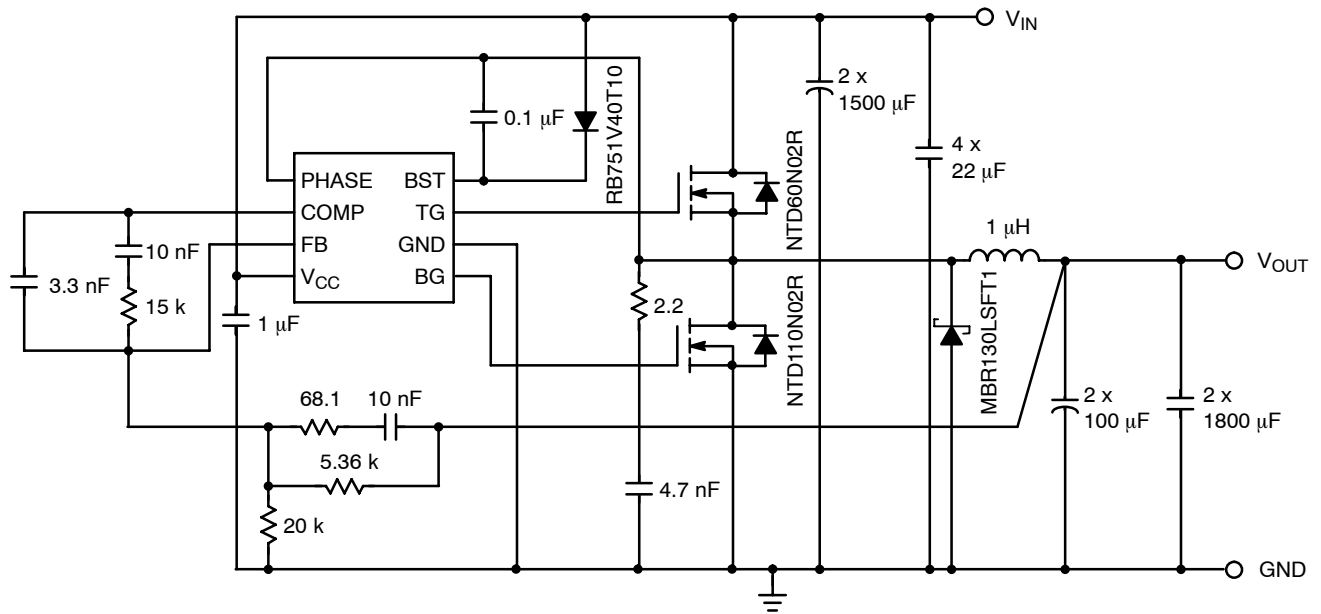


Figure 2. Application Diagram; 12 V Input, 1.0 V at 20 A Output

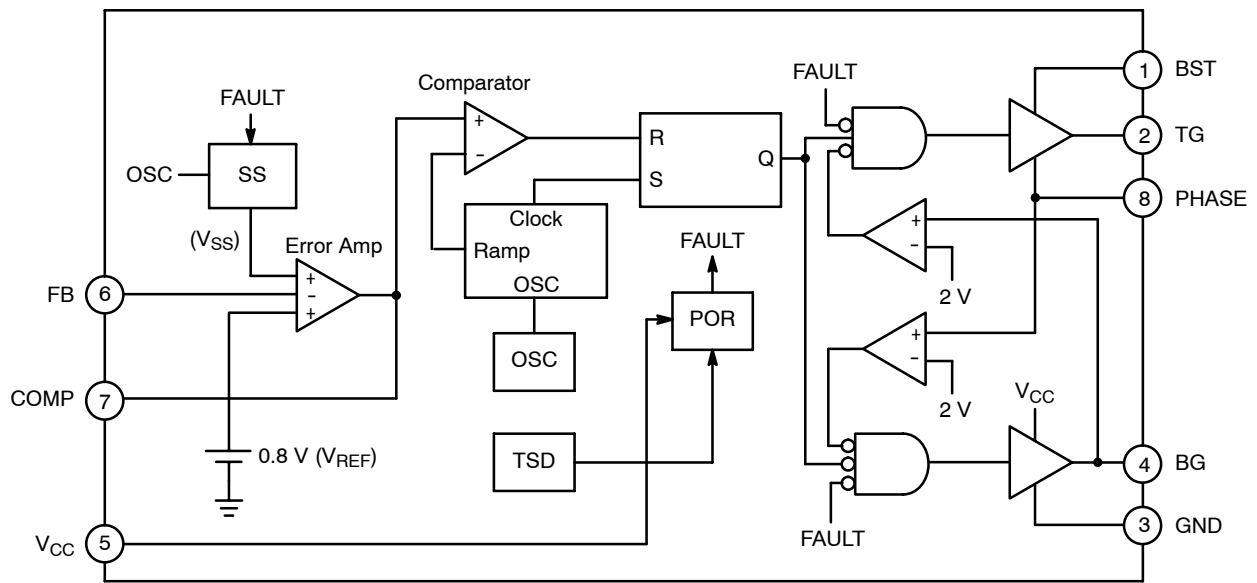


Figure 3. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	BST	Supply rail for the floating top gate driver. To form a boost circuit, use an external diode to bring the desired input voltage to this pin (cathode connected to BST pin). Connect a capacitor (C_{BST}) between this pin and the PHASE pin. Typical values for C_{BST} range from 0.1 μ F to 1 μ F. Ensure that C_{BST} is placed near the IC.
2	TG	Top gate MOSFET driver pin. Connect this pin to the gate of the top N-Channel MOSFET.
3	GND	IC ground reference. All control circuits are referenced to this pin.
4	BG	Bottom gate MOSFET driver pin. Connect this pin to the gate of the bottom N-Channel MOSFET.
5	V _{CC}	Supply rail for the internal circuitry. Operating supply range is 4.5 V to 13.2 V. Decouple with a 1 μ F capacitor to GND. Ensure that this decoupling capacitor is placed near the IC.
6	FB	This pin is the inverting input to the error amplifier. Use this pin in conjunction with the COMP pin to compensate the voltage-control feedback loop. Connect this pin to the output resistor divider (if used) or directly to Vout.
7	COMP	Compensation Pin. This is the output of the error amplifier (EA) and the non-inverting input of the PWM comparator. Use this pin in conjunction with the FB pin to compensate the voltage-control feedback loop. This pin should not be shorted to ground to disable switching.
8	PHASE	Switch node pin. This is the reference for the floating top gate driver. Connect this pin to the source of the top MOSFET. A Schottky diode between this pin and ground is recommended to reduce negative transient voltages which is common in a power supply system.

ABSOLUTE MAXIMUM RATINGS

Pin Name	Symbol	V _{MAX}	V _{MIN}
Main Supply Voltage Input	V _{CC}	15 V	-0.3 V
Bootstrap Supply Voltage Input	BST	30 V wrt/GND 15 V wrt/PHASE	-0.3 V
Switching Node (Bootstrap Supply Return)	PHASE	30 V	-0.7 V, t > 50 ns -2.0 V, t < 50 ns
High-Side Driver Output (Top Gate)	TG	30 V wrt/GND 15 V wrt/PHASE	-0.3 V wrt/PHASE
Low-Side Driver Output (Bottom Gate)	BG	15 V	-0.3 V
Feedback	FB	5.5 V	-0.3 V
COMP	COMP	5.5 V	-0.3 V

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	R _{θJC}	45	°C/W
Operating Junction Temperature Range	T _J	-40 to 150	°C
Operating Ambient Temperature Range	T _A	-40 to 85	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
ESD Susceptibility	Human Body Model Charge Device Model	2.0 200	kV V
Moisture Sensitivity Level	MSL	1	-

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

NCP1580

ELECTRICAL CHARACTERISTICS ($-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$, $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$ (Note 1), $4.5\text{ V} < V_{CC} < 13.2\text{ V}$, $4.5\text{ V} < \text{BST} < 26.5\text{ V}$, $C_{TG} = C_{BG} = 1.0\text{ nF}$, for min/max values unless otherwise noted.)

Characteristic	Conditions	Min	Typ	Max	Unit
Input Voltage Range	–	4.5	–	13.2	V
Boost Voltage Range	–	4.5	–	26.5	V

Supply Current

Quiescent Supply Current	$V_{FB} = 1.0\text{ V}$, No Switching $V_{CC} = 13.2\text{ V}$	–	1.0	1.75	mA
Boost Quiescent Current	$V_{FB} = 1.0\text{ V}$, No Switching	–	140	–	μA

Undervoltage Lockout

UVLO Threshold	V_{CC} Rising Edge	3.85	4.2	–	V
UVLO Hysteresis	–	–	0.5	–	V

Switching Regulator

VFB Feedback Voltage, Control Loop in Regulation	$T_A = 0\text{ to }70^{\circ}\text{C}$ $T_A = -40\text{ to }85^{\circ}\text{C}$	0.788 0.784	0.800 –	0.812 0.816	V
Oscillator Frequency	–	288	350	412	kHz
Ramp–Amplitude Voltage	–	–	1.1	–	V
Minimum Duty Cycle	–	–	0	–	%
Maximum Duty Cycle	–	85	90	95	%
Minimum Pulse Width	Static Operating (Note 2)	50	100	150	nsec

Error Amplifier

DC Gain	(Note 2)	70	80	–	dB
Gain–Bandwidth Product	(Note 2)	8.0	10	–	MHz
Slew Rate	COMP_GND = 100 pF (Note 2)	2.0	4.0	–	V/ μS
FB Bias Current	$V_{FB} = 1\text{ V}$ (Note 2)	–	0.1	1.0	μA

Gate Drivers

TG Rise Time	Load = 1.0 nF $V_{CC} = 8.0\text{ V}$	–	6.0	15	ns
TG Fall Time		–	15	30	ns
BG Rise Time		–	6.0	15	ns
BG Fall Time		–	6.0	15	ns
TG Sink Current	$V_{CC} = 12\text{ V}$ $V_{TG} = V_{BG} = 2.0\text{ V}$ (Note 2)	–	1.0	–	A
TG Source Current		–	1.5	–	A
BG Sink Current		–	1.5	–	A
BG Source Current		–	1.5	–	A
PHASE falling to BG rising delay	$V_{CC} = 12\text{ V}$ PHASE < 2.0 V BG > 2.0 V	–	30	90	ns
BG falling to TG rising delay	$V_{CC} = 12\text{ V}$ BG < 2.0 V TG > 2.0 V	–	30	40	ns

Internal Soft–Start

Time	–	1.0	2.0	3.0	ms

Thermal Shutdown

Overtemperature Trip Point	(Note 2)	–	160	–	$^{\circ}\text{C}$

- Specifications to -40°C are guaranteed via correlation using standard statistical quality control (SQC), not tested in production.
- Guaranteed by design, not tested in production.

TYPICAL CHARACTERISTIC CURVES

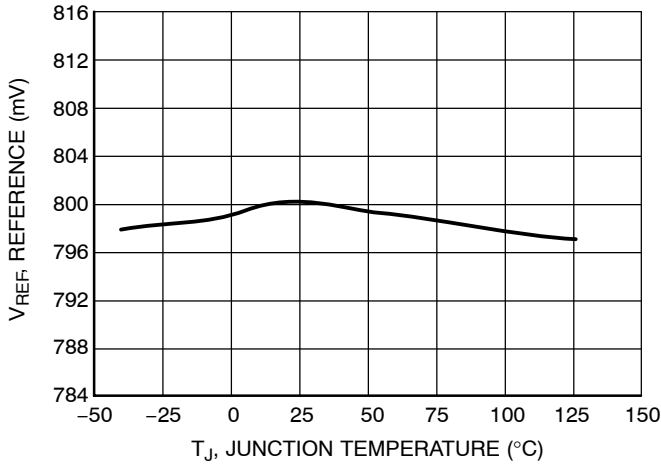


Figure 4. Reference Voltage (V_{REF}) vs. Temperature

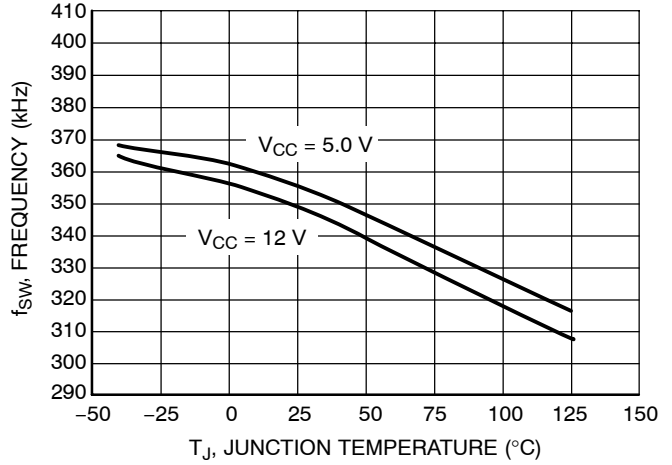


Figure 5. Oscillator Frequency (f_{SW}) vs. Temperature

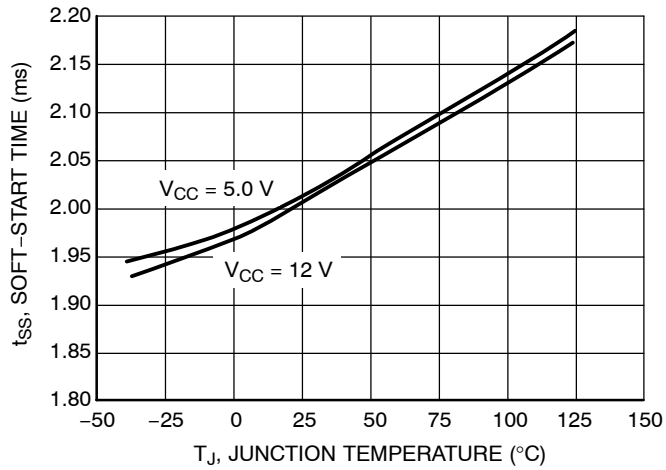


Figure 6. Soft-Start Time (t_{SS}) vs. Temperature

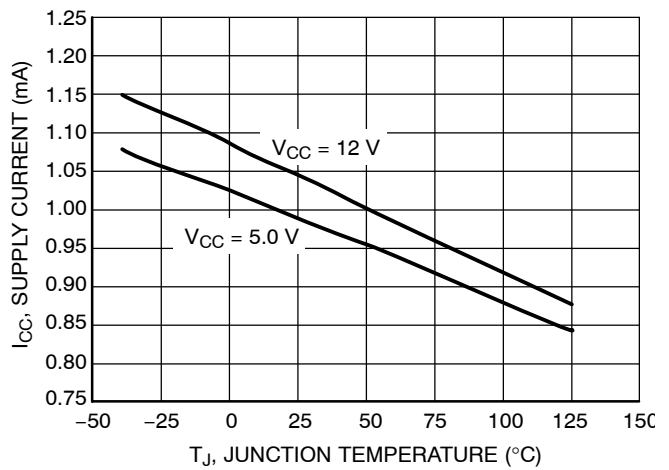


Figure 7. Quiescent Current (I_{CC}) vs. Temperature (No Switching)

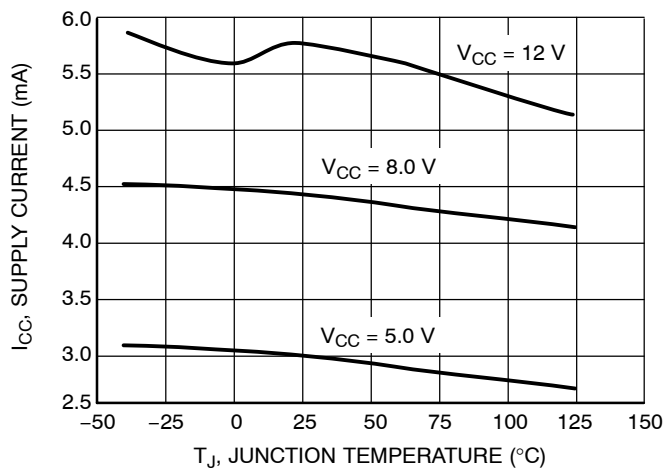


Figure 8. Quiescent Current (I_{CC}) vs. Temperature (Switching)

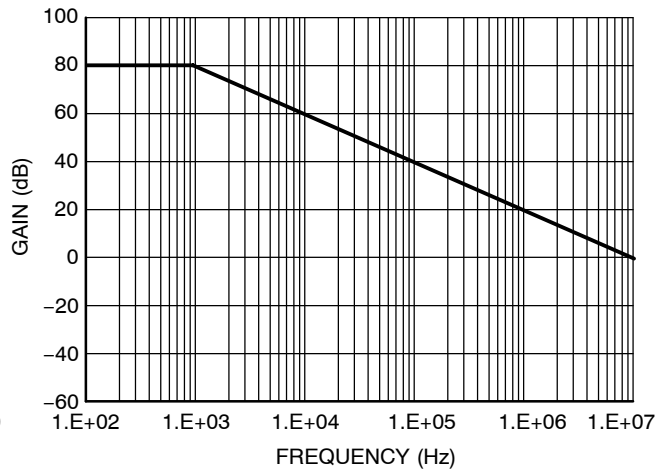


Figure 9. Error Amplifier

DETAILED OPERATING DESCRIPTION

General

The NCP1580 is an 8-pin PWM controller intended for DC-DC conversion from 5.0 V and 12 V buses. The NCP1580 has a 1.5 A internal floating gate driver circuit designed to drive N-Channel MOSFETs in a synchronous-rectifier buck topology. The internal floating gate driver simplifies design, improves performance, and minimizes board area. The output voltage of the converter can be precisely regulated down to 800 mV $\pm$ 1.5% when the V_{FB} pin is tied to V_{OUT} . The switching frequency, which is internally set to 350 kHz, and soft-start are completely integrated. The voltage error amplifier features a 10 MHz unity gain bandwidth and 4 V/ μ sec slew rate for fast transient response.

Duty Cycle and Maximum Pulse Width Limits

In steady state DC operation, the duty cycle will stabilize at an operating point defined by the ratio of the input to the output voltage. The NCP1580 can achieve a 90% duty cycle. There is a built in off-time which ensures that the bootstrap supply is charged every cycle. The NCP1580, which is capable of a 100 nsec minimum pulse width (typ), can allow a 12 V to 1.0 V conversion at 350 kHz.

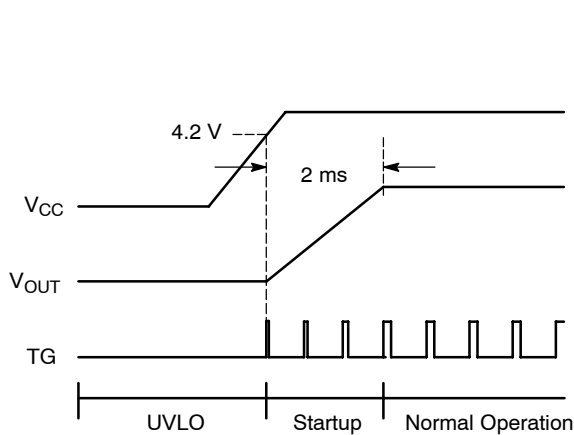


Figure 10. Normal Startup

Input Voltage Range (V_{CC} and BST)

The input voltage range for both V_{CC} and BST is 4.5 V to 13.2 V with respect to GND and PHASE, respectively. Although BST is rated at 13.2 V with respect to PHASE, it can also tolerate 26.5 V with respect to GND.

Normal Shutdown Behavior

Normal shutdown occurs when the IC stops switching because the input supply reaches UVLO threshold. In this case, switching stops, the internal SS is discharged, and all GATE pins go low. The switch node enters a high impedance state and the output capacitors discharge through the load with no ringing on the output voltage.

Internal Soft-Start

The NCP1580 features an internal soft-start function, which reduces inrush current and overshoot of the output voltage. Figure 10 shows a typical soft-start sequence. Soft-start is achieved by ramping up the internal soft-start voltage (V_{SS}) which is applied to the input of the error amplifier. This ramp is generated by applying 0.5 μ A to a 100 pf capacitor for 1 μ sec on every fourth clock pulse. This sequence begins once V_{CC} surpasses its UVLO threshold (see Figure 11). The typical soft-start time is 2 msec. The internal soft-start voltage is held low when the part is in UVLO.

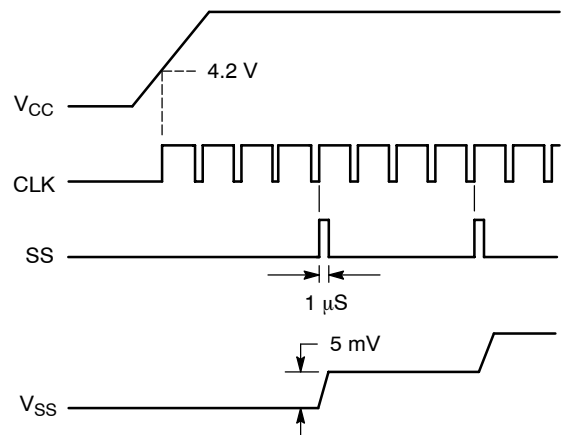


Figure 11. Achieving Internal Soft-Start

UVLO

Undervoltage Lockout (UVLO) is provided to ensure that unexpected behavior does not occur when V_{CC} is too low to support the internal rails and power the converter. For the NCP1580, the UVLO is set to ensure that the IC will start up when V_{CC} reaches 4.2 V and shutdown when V_{CC} drops below 3.7 V. This permits operation when converting from a 5.0 V input voltage.

Thermal Shutdown

The NCP1580 also provides Thermal Shutdown (TSD) for added protection. The TSD circuit monitors the die temperature and turns off the top and bottom gate drivers if an over temperature condition is detected. The internal soft-start capacitor is also discharged. This is a latched state and requires a power cycle to reset.

Drivers

The NCP1580 includes 1.5 A gate drivers to switch external N-Channel MOSFETs. This allows the NCP1580 to address high-power as well as low-power conversion requirements. The gate drivers also include adaptive non-overlap circuitry. The non-overlap circuitry increases efficiency, which minimizes power dissipation, by minimizing the body diode conduction time.

A detailed block diagram of the non-overlap and gate drive circuitry used in the chip is shown in Figure 12.

Careful selection and layout of external components is required, to realize the full benefit of the onboard drivers. The capacitors between V_{CC} and GND and between BST and SWN must be placed as close as possible to the IC. The current paths for the TG and BG connections must be optimized. A ground plane should be placed on the closest layer for return currents to GND in order to reduce loop area and inductance in the gate drive circuit.

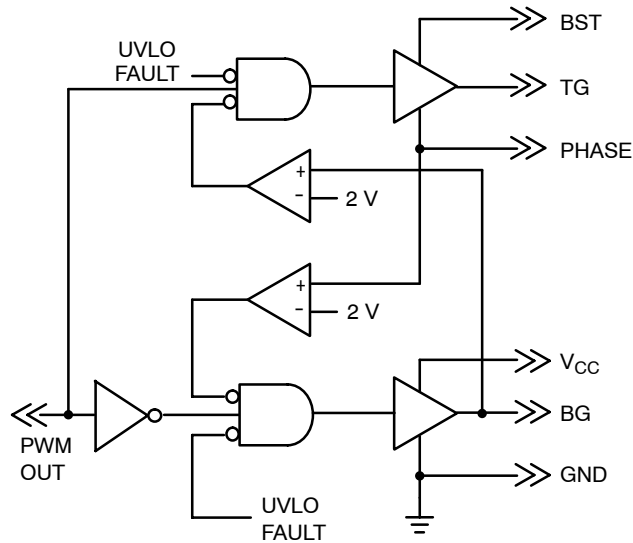


Figure 12. Block Diagram

APPLICATION SECTION

Input Capacitor Selection

The input capacitor has to sustain the ripple current produced during the on time of the upper MOSFET, so it must have a low ESR to minimize the losses. The RMS value of this ripple is:

$$I_{inRMS} = I_{OUT} \sqrt{D \times (1 - D)},$$

where D is the duty cycle, I_{inRMS} is the input RMS current, and I_{OUT} is the load current. The equation reaches its maximum value with $D = 0.5$. Losses in the input capacitors can be calculated with the following equation:

$$P_{CIN} = ESR_{CIN} \times I_{inRMS}^2,$$

where P_{CIN} is the power loss in the input capacitors and ESR_{CIN} is the effective series resistance of the input capacitance. Due to large dI/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used, it must be surge protected. Otherwise, capacitor failure could occur.

Calculating Input Startup Current

To calculate the input startup current, the following equation can be used.

$$I_{inrush} = \frac{C_{OUT} \times V_{OUT}}{t_{SS}},$$

where I_{inrush} is the input current during startup, C_{OUT} is the total output capacitance, V_{OUT} is the desired output voltage, and t_{SS} is the internal soft-start interval.

If the inrush current is higher than the steady state input current during max load, then the input fuse should be rated accordingly, if one is used.

Output Capacitor Selection

The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, for the first few microseconds it supplies the current to the load. The controller immediately recognizes the load transient and sets the duty cycle to maximum, but the current slope is limited by the inductor value.

During a load step transient the output voltage initially drops due to the current variation inside the capacitor and the ESR. (neglecting the effect of the effective series inductance (ESL)):

$$\Delta V_{OUT-ESR} = \Delta I_{OUT} \times ESR_{COUT},$$

where $V_{OUT-ESR}$ is the voltage deviation of V_{OUT} due to the effects of ESR and the ESR_{COUT} is the total effective series resistance of the output capacitors.

A minimum capacitor value is required to sustain the current during the load transient without discharging it. The voltage drop due to output capacitor discharge is given by the following equation:

$$\Delta V_{OUT-DISCHARGE} = \frac{\Delta I_{OUT}^2 \times L_{OUT}}{2 \times C_{OUT} \times (V_{IN} \times D - V_{OUT})},$$

where $V_{OUT-DISCHARGE}$ is the voltage deviation of V_{OUT} due to the effects of discharge, L_{OUT} is the output inductor value and V_{IN} is the input voltage.

It should be noted that $\Delta V_{OUT-DISCHARGE}$ and $\Delta V_{OUT-ESR}$ are out of phase with each other, and the larger of these two voltages will determine the maximum deviation of the output voltage (neglecting the effect of the ESL).

Inductor Selection

Both mechanical and electrical considerations influence the selection of an output inductor. From a mechanical perspective, smaller inductor values generally correspond to smaller physical size. Since the inductor is often one of the largest components in the regulation system, a minimum inductor value is particularly important in space-constrained applications. From an electrical perspective, the maximum current slew rate through the output inductor for a buck regulator is given by:

$$SlewRate_{L_{OUT}} = \frac{V_{IN} - V_{OUT}}{L_{OUT}}$$

This equation implies that larger inductor values limit the regulator's ability to slew current through the output inductor in response to output load transients. Consequently, output capacitors must supply the load current until the inductor current reaches the output load current level. This results in larger values of output capacitance to maintain tight output voltage regulation. In contrast, smaller values of inductance increase the regulator's maximum achievable slew rate and decrease the necessary capacitance, at the expense of higher ripple current. The peak-to-peak ripple current is given by the following equation:

$$I_{pk-pkL_{OUT}} = \frac{V_{OUT}(1 - D)}{L_{OUT} \times 350 \text{ KHZ}},$$

where $I_{pk-pkL_{OUT}}$ is the peak to peak current of the output. From this equation it is clear that the ripple current increases as L_{OUT} decreases, emphasizing the trade-off between dynamic response and ripple current.

Feedback and Compensation

The NCP1580 allows the output of the DC-DC converter to be adjusted from 0.8 V to 5.0 V via an external resistor divider network. The controller will try to maintain 0.8 V at the feedback pin. Thus, if a resistor divider circuit was placed across the feedback pin to V_{OUT} , the controller will regulate the output voltage proportional to the resistor divider network in order to maintain 0.8 V at the FB pin.

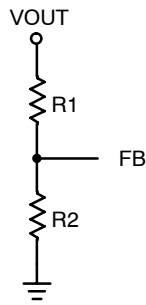


Figure 13.

The relationship between the resistor divider network in Figure 13 and the output voltage is shown in the following equation:

$$R_2 = R_1 \times \left(\frac{V_{REF}}{V_{OUT} - V_{REF}} \right).$$

Resistor R1 is selected based on a design trade off between efficiency and output voltage accuracy. For high values of R1 there is less current consumption in the feedback network. However the trade off is output voltage accuracy due to the bias current in the error amplifier. The output voltage error of this bias current can be estimated using the following equation (neglecting resistor tolerance):

$$\text{Error}\% = \frac{0.1 \mu\text{A} \times R_1}{V_{REF}} \times 100\%$$

Once R1 has been determined, R2 can be calculated.

The NCP1580 utilizes voltage mode control. This is to say, the control loop regulates V_{OUT} by monitoring V_{OUT} and controlling the output current. However, since the control loop is controlling the output current to regulate the output voltage, there are some stability concerns since the inductor current is 90 degrees out of phase with the voltage. It is inherent with all voltage-mode control loops to have a compensation network.

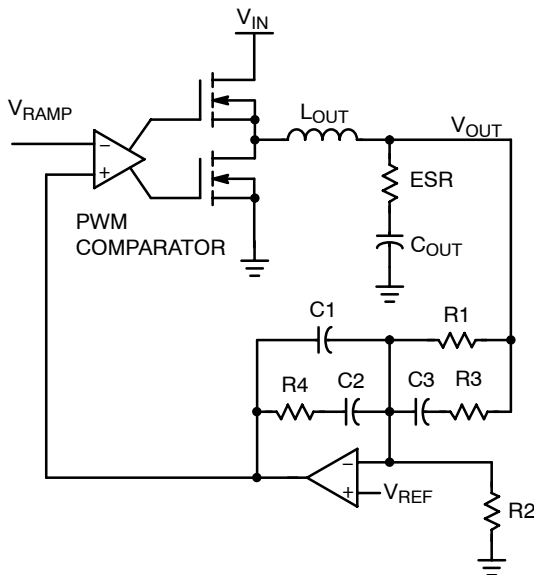


Figure 14. Simplified Diagram of Control Loop

The compensation network consists of the internal error amplifier and the impedance networks Z_{IN} (R1, R3 and C3) and Z_{FB} (R4, C1 and C2). The compensation network has to provide a closed loop transfer function with the highest 0 dB crossing frequency to have fast response (but always lower than $f_{SW}/8$) and the highest gain in DC conditions to minimize the load regulation. A stable control loop has a gain crossing with -20 dB/decade slope and a phase margin greater than 45° . Include worst-case component variations when determining phase margin. To place the poles and zeroes of the compensation networks, the following equations may be used:

Modulator frequencies:

$$\omega_{LC} = \frac{1}{\sqrt{L_{OUT} \times C_{OUT}}} \quad \omega_{ESR} = \frac{1}{\sqrt{ESR \times C_{OUT}}}$$

Compensation network frequency:

$$\omega_{P1} = \frac{1}{R_4 \times \left(\frac{C_1 \times C_2}{C_1 + C_2} \right)} \quad \omega_{P2} = \frac{1}{R_3 \times C_3}$$

$$\omega_{Z1} = \frac{1}{R_4 \times C_2} \quad \omega_{Z2} = \frac{1}{(R_1 + R_3) \times C_3}$$

Place ω_{Z1} and ω_{Z2} around the output filter resonance ω_{LC} ; Place ω_{P1} at the output capacitor ESR zero ω_{ESR} ; Place ω_{P2} at one half of the switching frequency;

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP} . This function has a double pole at frequency ω_{LC} and a zero at ω_{ESR} . The DC Gain of the modulator is simply the input voltage V_{IN} divided by the peak-to-peak oscillator voltage ΔV_{OSC} .

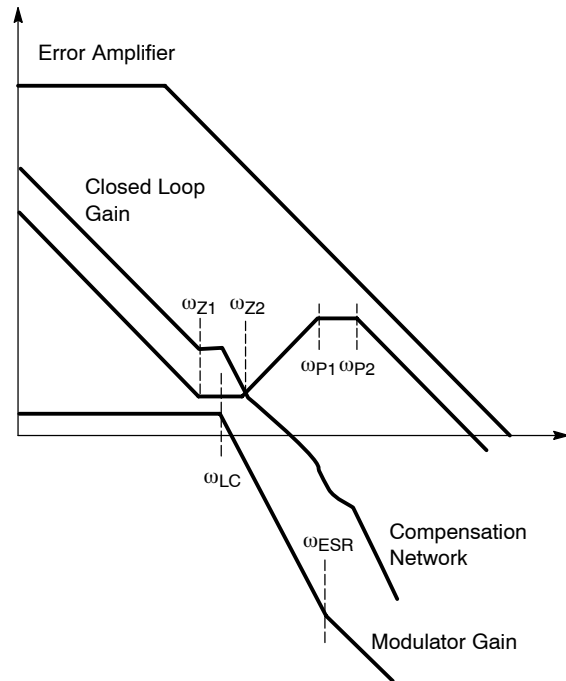


Figure 15.

Visit <http://www.onsemi.com/pub/Collateral/COMPCALC> for self extracting compensation program for design assistance.

Thermal Considerations

The power dissipation of the NCP1580 varies with the MOSFETs used, V_{CC} , and the boost voltage (V_{BST}). The average MOSFET gate current typically dominates the control IC power dissipation. The IC power dissipation is determined by the formula:

$$P_{IC} = (I_{CC} \times V_{CC}) + P_{TG} + P_{BG}.$$

Where:

P_{IC} = Control IC power dissipation,
 I_{CC} = IC measured supply current,
 V_{CC} = IC supply voltage,
 P_{TG} = Top gate driver losses,
 P_{BG} = Bottom gate driver losses.

The upper (switching) MOSFET gate driver losses are:

$$P_{TG} = Q_{TG} \times f_{SW} \times V_{BST}.$$

Where:

Q_{TG} = Total upper MOSFET gate charge at V_{BST} ,
 f_{SW} = The switching frequency,
 V_{BST} = The BST pin voltage.

The lower (synchronous) MOSFET gate driver losses are:

$$P_{BG} = Q_{BG} \times f_{SW} \times V_{CC}.$$

Where:

Q_{BG} = total lower MOSFET gate charge at V_{CC} .

The junction temperature of the control IC can then be calculated as:

$$T_J = T_A + P_{IC} \times \theta_{JA}.$$

Where:

T_J = The junction temperature of the IC,
 T_A = The ambient temperature,
 θ_{JA} = The junction-to-ambient thermal resistance of the IC package.

The package thermal resistance ($R_{\theta JC}$) can be obtained from the specifications section of this data sheet and a calculation can be made to determine the IC junction temperature. In addition, a thermal resistance (Junction-to-Ambient/Safe Operating Area) curve has been included below to further aid design. However, it should be noted that the physical layout of the board, the proximity of other heat sources such as MOSFETs and inductors, and the amount of metal connected to the IC, impact the temperature of the device. Use these calculations as a guide, but measurements should be taken in the actual application.

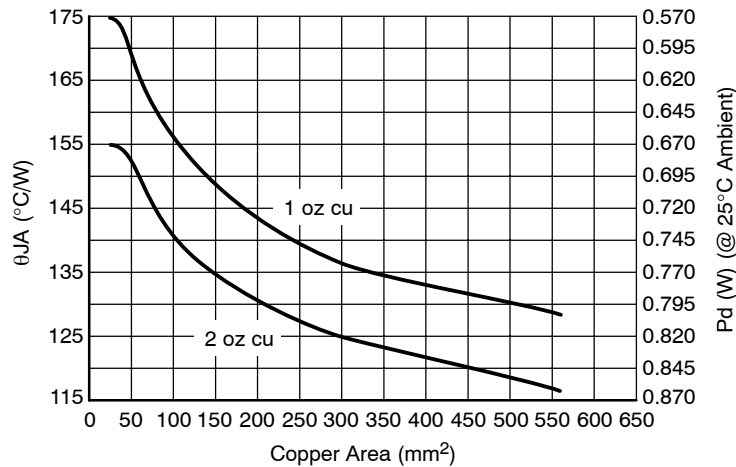


**Figure 16. Thermal Resistance
(Junction-to-Ambient/Safe Operating Area)**

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding. Figure 17 shows the critical power components of the converter. To minimize the voltage overshoot the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board. The components shown in Figure 17 should be located as close together as possible. Please note that the capacitors C_{IN} and C_{OUT} each represent numerous physical capacitors. It is desirable to locate the NCP1580 within 1 inch of the MOSFETs, Q1 and Q2. The circuit traces for the MOSFETs' gate and source connections from the NCP1580 must be sized to handle up to 2.0 A peak current.

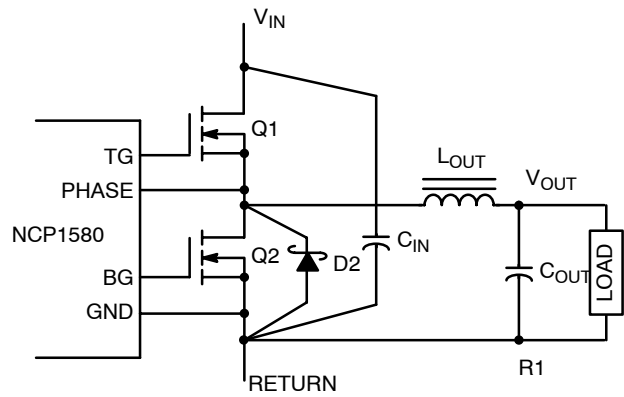


Figure 17.

NCP5422A

Dual Out-of-Phase Synchronous Buck Controller with Current Limit

The NCP5422A is a dual N-channel synchronous buck regulator controller. It contains all the circuitry required for two independent buck regulators and utilizes the V^2 ™ control method to achieve the fastest possible transient response and best overall regulation, while using the least number of external components. The NCP5422A features out-of-phase synchronization between the channels, reducing the input filter requirement. The NCP5422A also provides undervoltage lockout, Soft Start, built in adaptive non-overlap time and hiccup mode overcurrent protection.

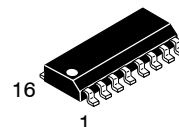
Features

- V^2 Control Topology
- Hiccup Mode Overcurrent Protection
- 150 ns Transient Response
- Programmable Soft Start
- 100% Duty Cycle for Enhanced Transient Response
- 150 kHz to 600 kHz Programmable Frequency Operation
- Switching Frequency Set by Single Resistor
- Out-Of-Phase Synchronization Between Channels
- Undervoltage Lockout
- Both Gate Drive Outputs Held Low During Fault Condition



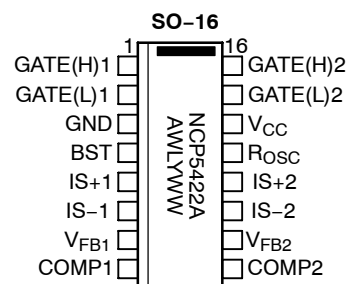
ON Semiconductor®

<http://onsemi.com>



SO-16
AD SUFFIX
CASE 751B

PIN CONNECTIONS AND MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NCP5422ADR2	SO-16	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NCP5422A

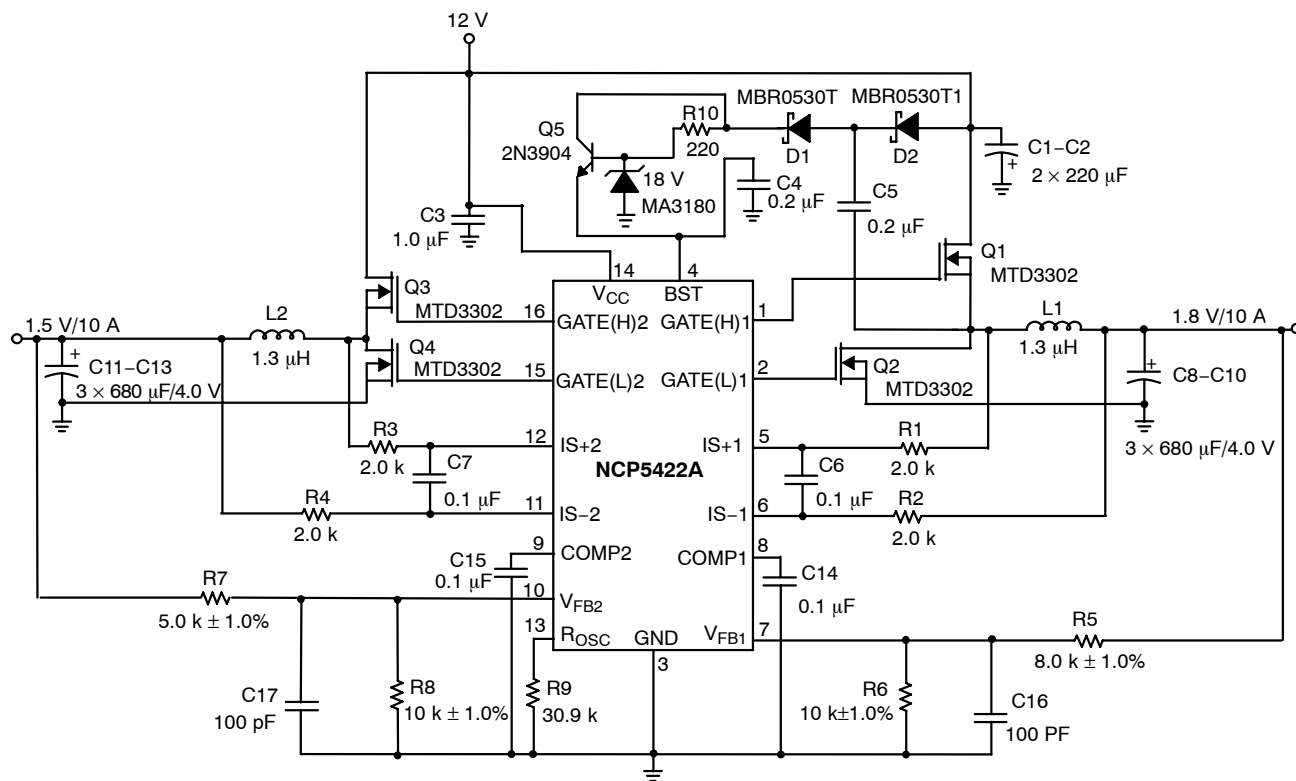


Figure 1. Application Diagram, 12 V to 1.5 V/10 A and 1.8 V/10 A Converter

ABSOLUTE MAXIMUM RATINGS*

Rating	Value	Unit
Operating Junction Temperature, T_J	150	°C
Storage Temperature Range, T_S	-65 to +150	°C
ESD Susceptibility (Human Body Model)	2.0	kV
Package Thermal Resistance, SO-16: Junction-to-Case, $R_{\theta JC}$ Junction-to-Ambient, $R_{\theta JA}$	28 115	°C/W °C/W
Lead Temperature Soldering: Reflow: (Note 1)	230 peak	°C

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ABSOLUTE MAXIMUM RATINGS

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
V_{CC}	IC Power Input	16 V	-0.3 V	N/A	1.5 A peak 200 mA DC
COMP1, COMP2	Compensation Capacitor for Channel 1 or 2	4.0 V	-0.3 V	1.0 mA	1.0 mA
V_{FB1} , V_{FB2}	Voltage Feedback Input for Channel 1 or 2	5.0 V	-0.3 V	1.0 mA	1.0 mA
BST	Power Input for GATE(H)1, 2	20 V	-0.3 V	N/A	1.5 A peak 200 mA DC
R_{OSC}	Oscillator Resistor	4.0 V	-0.3 V	1.0 mA	1.0 mA
GATE(H)1, GATE(H)2	High-Side FET Driver for Channel 1 or 2	20 V	-2.0 V for 100 ns -0.3 V DC	1.5 A peak 200 mA DC	1.5 A peak 200 mA DC
GATE(L)1, GATE(L)2	Low-Side FET Driver for Channel 1 or 2	16 V	-2.0 V for 100 ns -0.3 V DC	1.5 A peak 200 mA DC	1.5 A peak 200 mA DC
GND	Ground	0 V	0 V	1.5 A peak 200 mA DC	N/A
IS+1, IS+2	Positive Current Sense for Channel 1 or 2	6.0 V	-0.3 V	1.0 mA	1.0 mA
IS-1, IS-2	Negative Current Sense for Channel 1 or 2	6.0 V	-0.3 V	1.0 mA	1.0 mA

NCP5422A

ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$; $0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$; $R_{OSC} = 30.9\text{ k}$, $C_{COMP1,2} = 0.1\text{ }\mu\text{F}$, $10.8\text{ V} < V_{CC} < 13.2\text{ V}$; $10.8\text{ V} < BST < 20\text{ V}$, $C_{GATE(H)1,2} = C_{GATE(L)1,2} = 1.0\text{ nF}$, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit

Error Amplifier

$V_{FB1(2)}$ Bias Current	$V_{FB1(2)} = 0\text{ V}$	–	0.5	1.6	μA
$V_{FB1(2)}$ Input Range	–	0	–	1.1	V
COMP1,2 Source Current	COMP1,2 = 1.2 V to 2.5 V; $V_{FB1(2)} = 0.8\text{ V}$	15	30	60	μA
COMP1,2 Sink Current	COMP1,2 = 1.2 V; $V_{FB1(2)} = 1.2\text{ V}$	15	30	60	μA
Reference Voltage 1(2)	COMP1 = V_{FB1} ; COMP2 = V_{FB2}	0.980	1.000	1.020	V
COMP1,2 Max Voltage	$V_{FB1(2)} = 0.8\text{ V}$	3.0	3.3	–	V
COMP1,2 Min Voltage	$V_{FB1(2)} = 1.2\text{ V}$	–	0.25	0.35	V
Open Loop Gain	–	–	95	–	dB
Unity Gain Band Width	–	–	40	–	kHz
PSRR @ 1.0 kHz	–	–	70	–	dB
Transconductance	–	–	32	–	mmho
Output Impedance	–	–	2.5	–	$\text{M}\Omega$

GATE(H) and GATE(L)

High Voltage (AC)	Measure: $V_{CC} - \text{GATE(L)1,2}$; BST – GATE(H)1,2; Note 2	–	0	0.5	V
Low Voltage (AC)	Measure: GATE(L)1,2 or GATE(H)1,2; Note 2	–	0	0.5	V
Rise Time	$1.0\text{ V} < \text{GATE(L)1,2} < V_{CC} - 1.0\text{ V}$ $1.0\text{ V} < \text{GATE(H)1,2} < \text{BST} - 1.0\text{ V}$, $\text{BST} \leq 14\text{ V}$	–	20	50	ns
Fall Time	$V_{CC} - 1.0 > \text{GATE(L)1,2} > 1.0\text{ V}$ $\text{BST} - 1.0 > \text{GATE(H)1,2} > 1.0\text{ V}$, $\text{BST} \leq 14\text{ V}$	–	15	50	ns
GATE(H) to GATE(L) Delay	$\text{GATE(H)1,2} < 2.0\text{ V}$, $\text{GATE(L)1,2} > 2.0\text{ V}$ $\text{BST} \leq 14\text{ V}$	20	40	70	ns
GATE(L) to GATE(H) Delay	$\text{GATE(L)1,2} < 2.0\text{ V}$, $\text{GATE(H)1,2} > 2.0\text{ V}$; $\text{BST} \leq 14\text{ V}$	20	40	70	ns
GATE(H)1(2) and GATE(L)1(2) pull-down.	Resistance to GND Note 2	50	125	280	$\text{k}\Omega$

PWM Comparator

PWM Comparator Offset	$V_{FFB1(2)} = 0\text{ V}$; Increase COMP1,2 until GATE(H)1,2 starts switching	0.30	0.425	0.55	V
Artificial Ramp	Duty cycle = 50%, Note 2	40	70	100	mV
Minimum Pulse Width	Note 2	–	–	300	ns

Oscillator

Switching Frequency	$R_{OSC} = 61.9\text{ k}$; Measure GATE(H)1; Note 2	112	150	188	kHz
Switching Frequency	$R_{OSC} = 30.9\text{ k}$; Measure GATE(H)1	250	300	350	kHz
Switching Frequency	$R_{OSC} = 15.1\text{ k}$; Measure GATE(H)1; Note 2	450	600	750	kHz
R_{OSC} Voltage	$R_{OSC} = 30.9\text{ k}$, Note 2	0.970	1.000	1.030	V
Phase Difference	–	–	180	–	$^{\circ}$

NCP5422A

ELECTRICAL CHARACTERISTICS (continued) ($0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$; $0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$; $R_{\text{OSC}} = 30.9 \text{ k}$, $C_{\text{COMP1,2}} = 0.1 \mu\text{F}$, $10.8 \text{ V} < V_{\text{CC}} < 13.2 \text{ V}$; $10.8 \text{ V} < \text{BST} < 20 \text{ V}$, $C_{\text{GATE(H)1,2}} = C_{\text{GATE(L)1,2}} = 1.0 \text{ nF}$, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit

Supply Currents

V_{CC} Current	COMP1,2 = 0 V (No Switching)	–	13	17	mA
BST Current	COMP1,2 = 0 V (No Switching)	–	3.5	6.0	mA

Undervoltage Lockout

Start Threshold	GATE(H) Switching; COMP1,2 charging	7.8	8.6	9.4	V
Stop Threshold	GATE(H) not switching; COMP1,2 discharging	7.0	7.8	8.6	V
Hysteresis	Start–Stop	0.5	0.8	1.5	V

Hiccup Mode Overcurrent Protection

OVC Comparator Offset Voltage	$0 \text{ V} < \text{IS}^+ 1(2) < 5.5 \text{ V}$, $0 \text{ V} < \text{IS}^- 1(2) < 5.5 \text{ V}$	55	70	85	mV
Discharge Threshold	–	0.20	0.25	0.30	V
$\text{IS}^+ 1(2)$ Bias Current	$0 \text{ V} < \text{IS}^+ 1(2) < 5.5 \text{ V}$	–1.0	0.1	1.0	μA
$\text{IS}^- 1(2)$ Bias Current	$0 \text{ V} < \text{IS}^- 1(2) < 5.5 \text{ V}$	–1.0	0.1	1.0	μA
OVC Common Mode Range	Note 2	0	–	5.5	V
OVC Latch COMP1 Discharge Current	COMP1 = 1.0 V	2.0	5.0	8.0	μA
OVC Latch COMP2 Discharge Current	COMP2 = 1.0 V	0.3	1.2	3.5	mA
COMP1 Charge/Discharge Ratio in OVC	–	5.0	6.0	7.0	–

2. Guaranteed by design, not 100% tested in production.

NCP5422A

PACKAGE PIN DESCRIPTION

PIN NO.	PIN SYMBOL	FUNCTION
1	GATE(H)1	High Side Switch FET driver pin for channel 1.
2	GATE(L)1	Low Side Synchronous FET driver pin for channel 1.
3	GND	Ground pin for all circuitry contained in the IC. This pin is internally bonded to the substrate of the IC.
4	BST	Power input for GATE(H)1 and GATE(H)2 pins.
5	IS+1	Positive input for channel 1 overcurrent comparator.
6	IS-1	Negative input for channel 1 overcurrent comparator.
7	V _{FB1}	Error amplifier inverting input for channel 1.
8	COMP1	Channel 1 Error Amp output. PWM Comparator reference input. A capacitor to LGND provides Error Amp compensation. The same capacitor provides Soft Start timing for channel 1. This pin also disables the channel 1 output when pulled below 0.3 V.
9	COMP2	Channel 2 Error Amp output. PWM Comparator reference input. A capacitor to LGND provides Error Amp compensation and Soft Start timing for channel 2. Channel 2 output is disabled when this pin is pulled below 0.3 V.
10	V _{FB2}	Error amplifier inverting input for channel 2.
11	IS-2	Negative input for channel 2 overcurrent comparator.
12	IS+2	Positive input for channel 2 overcurrent comparator.
13	R _{OSC}	Oscillator frequency pin. A resistor from this pin to ground sets the oscillator frequency.
14	V _{CC}	Input Power supply pin.
15	GATE(L)2	Low Side Synchronous FET driver pin for channel 2.
16	GATE(H)2	High Side Switch FET driver pin for channel 2.

NCP5422A

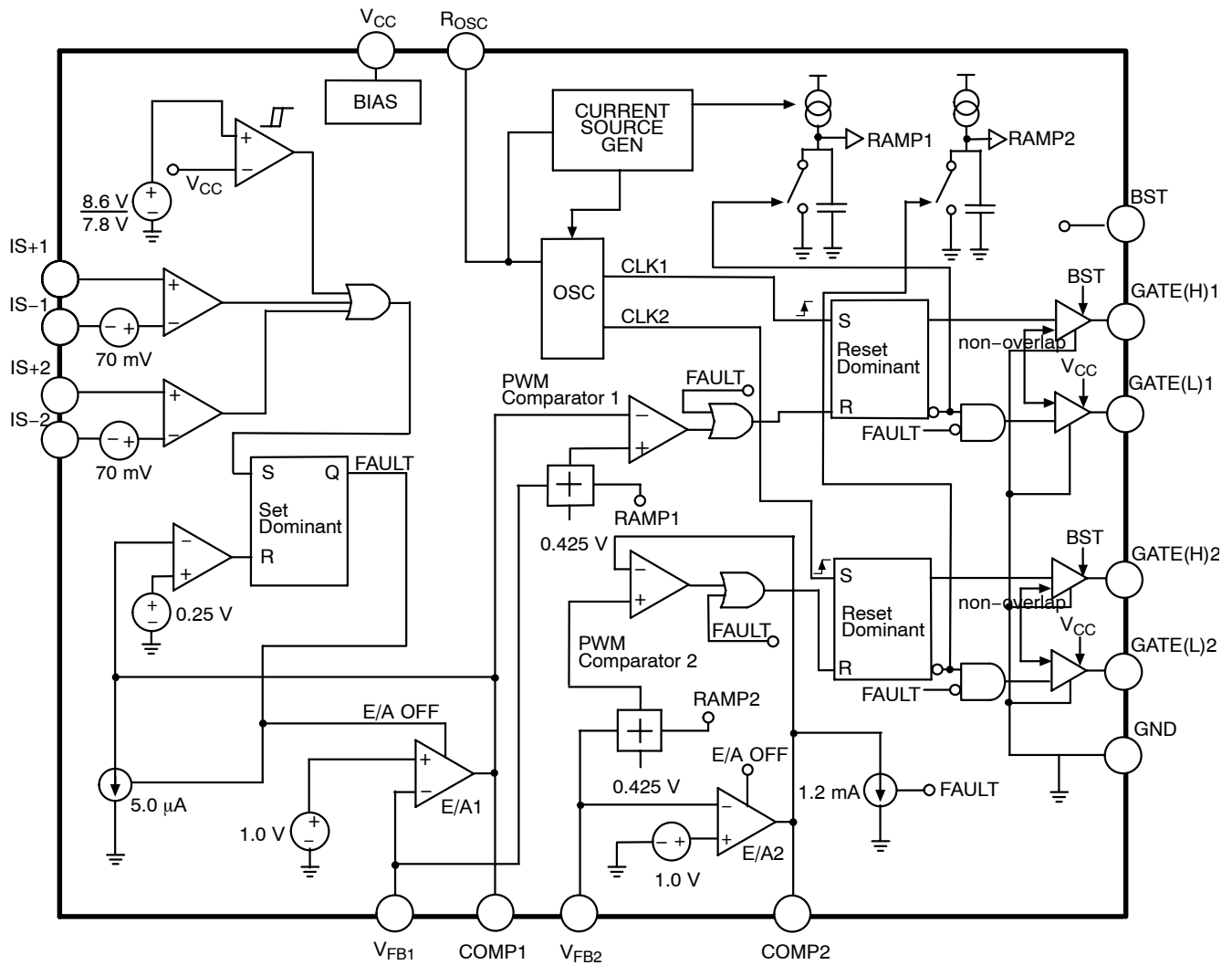


Figure 2. Block Diagram

APPLICATIONS INFORMATION

THEORY OF OPERATION

The NCP5422A is a dual power supply controller that utilizes the V^2 control method. Two synchronous V^2 buck regulators can be built using a single controller. The fixed-frequency architecture, driven from a common oscillator, ensures a 180° phase differential between channels.

 V^2 Control Method

The V^2 method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. The V^2 method differs from traditional techniques such as voltage mode control, which generates an artificial ramp, and current mode control, which generates a ramp using the inductor current.

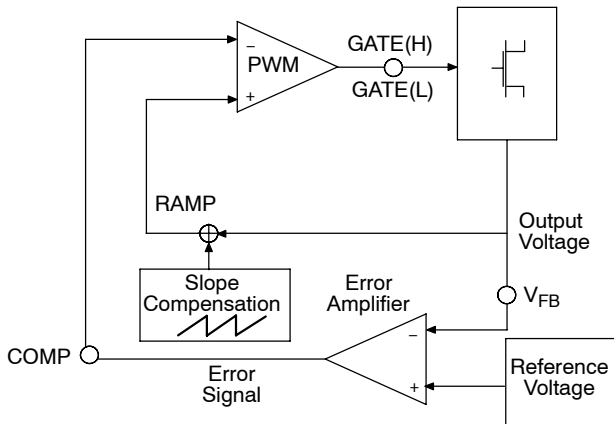


Figure 3. V^2 Control with Slope Compensation

The V^2 control method is illustrated in Figure 3. The output voltage generates both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output, regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, allowing the control circuit to drive the main switch to 0% or 100% duty cycle as required.

A variation in line voltage changes the current ramp in the inductor, which causes the V^2 control scheme to compensate the duty cycle. Since any variation in inductor current modifies the ramp signal, as in current mode control, the V^2 control scheme offers the same advantages in line transient response.

A variation in load current will affect the output voltage, modifying the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. The comparator response time and the transition speed of the main switch determine the load transient response. Unlike traditional control methods, the reaction

time to the output load step is not related to the crossover frequency of the error signal loop.

The error signal loop can have a low crossover frequency, since the transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation is drastically improved because there are two independent control loops. A voltage mode controller relies on the change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulations. A current mode controller maintains a fixed error signal during line transients, since the slope of the ramp signal changes in this case. However, regulation of load transients still requires a change in the error signal. The V^2 method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

The stringent load transient requirements of modern microprocessors require the output capacitors to have very low ESR. The resulting shallow slope in the output ripple can lead to pulse width jitter and variation caused by both random and synchronous noise. A ramp waveform generated in the oscillator is added to the ramp signal from the output voltage to provide the proper voltage ramp at the beginning of each switching cycle. This slope compensation increases the noise immunity particularly at higher duty cycle (above 50%).

Start Up

The NCP5422A features a programmable Soft Start function, which is implemented through the Error Amplifier and the external Compensation Capacitor. This feature prevents stress to the power components and overshoot of the output voltage during start-up. As power is applied to the regulator, the NCP5422A Undervoltage Lockout circuit (UVL) monitors the IC's supply voltage (V_{CC}). The UVL circuit prevents the MOSFET gates from switching until V_{CC} exceeds the 8.6 V threshold. A hysteresis function of 800 mV improves noise immunity. The Compensation Capacitor connected to the COMP pin is charged by a 30 μ A current source. When the capacitor voltage exceeds the 0.425 V offset of the PWM comparator, the PWM control loop will allow switching to occur. The upper gate driver GATE(H) is activated turning on the upper MOSFET. The current then ramps up through the main inductor and linearly powers the output capacitors and load. When the regulator output voltage exceeds the COMP pin voltage minus the

0.40 V PWM comparator offset threshold and the artificial ramp, the PWM comparator terminates the initial pulse.

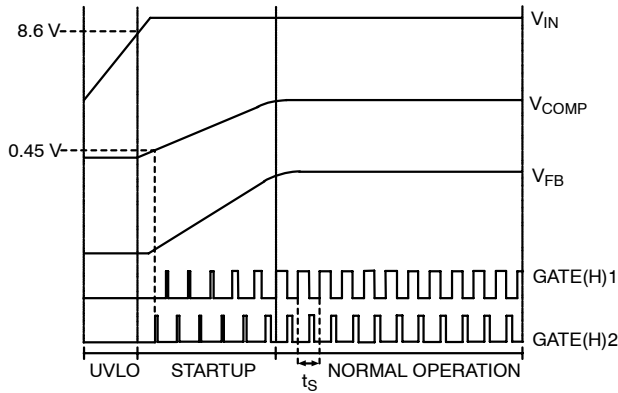


Figure 4. Idealized Waveforms

Normal Operation

During normal operation, the duty cycle of the gate drivers remains approximately constant as the V^2 control loop maintains the regulated output voltage under steady state conditions. Variations in supply line or output load conditions will result in changes in duty cycle to maintain regulation.

Gate Charge Effect on Switching Times

When using the onboard gate drivers, the gate charge has an important effect on the switching times of the FETs. A finite amount of time is required to charge the effective capacitor seen at the gate of the FET. Therefore, the rise and fall times rise linearly with increased capacitive loading, according to the following graphs.

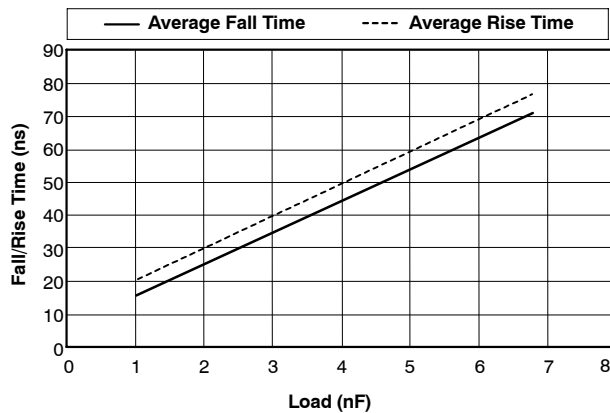


Figure 5. Average Rise and Fall Times

Transient Response

The 150 ns reaction time of the control loop provides fast transient response to any variations in input voltage and output current. Pulse-by-pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed

instantaneously, regulation is maintained by the output capacitors during the time required to slew the inductor current. For better transient response, several high frequency and bulk output capacitors are usually used.

Out-of-Phase Synchronization

In out-of-phase synchronization, the turn-on of the second channel is delayed by half the switching cycle. This delay is supervised by the oscillator, which supplies a clock signal to the second channel which is 180° out of phase with the clock signal of the first channel.

The advantages of out-of-phase synchronization are many. Since the input current pulses are interleaved with one another, the overlap time is reduced. The effect of this overlap reduction is to reduce the input filter requirement, allowing the use of smaller components. In addition, since peak current occurs during a shorter time period, emitted EMI is also reduced, thereby reducing shielding requirements.

Overvoltage Protection

Overvoltage Protection (OVP) is provided as a result of the normal operation of the V^2 control method and requires no additional external components. The control loop responds to an overvoltage condition within 150 ns, turning off the upper MOSFET and disconnecting the regulator from its input voltage. This results in a crowbar action to clamp the output voltage preventing damage to the load. The regulator remains in this state until the overvoltage condition ceases.

Hiccup Overcurrent Protection

A lossless hiccup mode short circuit protection feature is provided on the chip. The only external component required is the COMP1 capacitor. Any overcurrent condition results in the immediate shutdown of both output phases. Both the upper and lower gate drives are driven low, turning off both MOSFETs.

A comparator between the IS+ and IS- on each output phase detects a short circuit when the voltage difference between the two pins exceeds 70 mV and sets the fault latch. The fault latch immediately turns off the error amplifier and discharges both COMP capacitors. The capacitor connected to COMP1 is discharged through a $5.0 \mu\text{A}$ current sink in order to provide timing for the reset cycle. When COMP1 has fallen below 0.25 V, a comparator resets the fault latch and error amplifier 1 begins to charge COMP1 with a $30 \mu\text{A}$ source current. When COMP1 exceeds the feedback voltage plus the PWM Comparator offset voltage, the normal switching cycle will resume.

If the short circuit condition persists through the restart cycle, the overcurrent reset cycle will repeat itself until the short circuit is removed, resulting in small hiccup output pulses while the COMP capacitor charges, as shown in Figure 6.

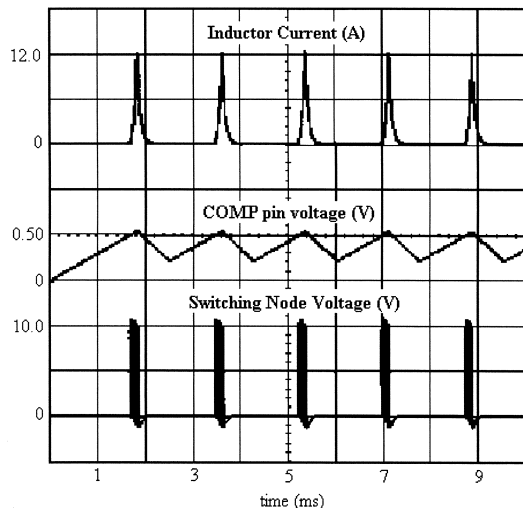


Figure 6. Hiccup Overcurrent Protection

Output Enable

On/Off control of the regulator outputs can be implemented by pulling the COMP pins low. The COMP pins must be driven below the 0.425 V PWM comparator offset voltage in order to disable the switching of the GATE drivers.

DESIGN GUIDELINES

Definition of the design specifications

The output voltage tolerance can be affected by any or all of the following reasons:

1. buck regulator output voltage setpoint accuracy;
2. output voltage change due to discharging or charging of the bulk decoupling capacitors during a load current transient;
3. output voltage change due to the ESR and ESL of the bulk and high frequency decoupling capacitors, circuit traces, and vias;
4. output voltage ripple and noise.

Budgeting the tolerance is left up to the designer who must take into account all of the above effects and provide an output voltage that will meet the specified tolerance at the load.

The designer must also ensure that the regulator component temperatures are kept within the manufacturer's specified ratings at full load and maximum ambient temperature.

Selecting Feedback Divider Resistors

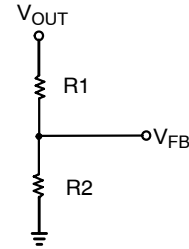


Figure 7. Selecting Feedback Divider Resistors

Selection of Feedback Divider Resistors

Feedback divider resistors R1 and R2 are selected based on a design trade-off between efficiency and output voltage accuracy. Both error amplifiers are referenced to 1.0 V, and resistors R1 and R2 are connected from each channel's output voltage to the inverting pin ($V_{FB1(2)}$) of each error amplifier. To set the channel output voltage, first choose a value for R1, and then R2 can be sized as follows:

$$R2 = \frac{R1}{\frac{V_{out}}{1.0} - 1}$$

The output voltage error due to the bias current of the error amplifier and the parallel combination of R1 and R2 can now be estimated:

$$\text{Error} = 1.6 \cdot 10^{-6} \cdot \frac{R1 \cdot R2}{R1 + R2}$$

Reducing the size of R1 and R2 will reduce the output voltage error, but increase the power dissipation.

Calculating Duty Cycle

The duty cycle of a buck converter (including parasitic losses) is given by the formula:

$$\text{Duty Cycle} = D = \frac{V_{OUT} + V_{LFET} + V_L}{V_{IN} + V_{LFET} - V_{HFET}}$$

where:

V_{OUT} = buck regulator output voltage;

V_{HFET} = high side FET voltage drop due to $R_{DS(ON)}$;

V_L = output inductor voltage drop due to inductor wire DC resistance;

V_{IN} = buck regulator input voltage;

V_{LFET} = low side FET voltage drop due to $R_{DS(ON)}$.

Selecting the Switching Frequency

Selecting the switching frequency is a trade-off between component size and power losses. Operation at higher switching frequencies allows the use of smaller inductor and capacitor values. Nevertheless, it is common to select lower frequency operation because a higher frequency results in lower efficiency due to MOSFET gate charge losses. Additionally, the use of smaller inductors at higher frequencies results in higher ripple current, higher output voltage ripple, and lower efficiency at light load currents.

The value of the oscillator resistor is designed to be linearly related to the switching period. If the designer prefers not to use Figure 8 to select the necessary resistor, the following equation quite accurately predicts the proper resistance for room temperature conditions.

$$R_{OSC} = \frac{21700 - f_{SW}}{2.31 \times f_{SW}}$$

where:

R_{OSC} = oscillator resistor in k Ω ;
 f_{SW} = switching frequency in kHz.

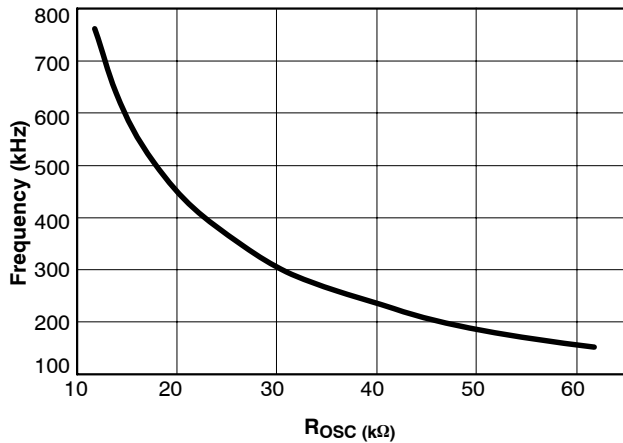


Figure 8. Switching Frequency

Selection of the Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. There are many factors to consider in selecting the inductor including cost, efficiency, EMI and ease of manufacture. The inductor must be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss.

There are a variety of materials and types of magnetic cores that could be used for this application. Among them are ferrites, molypermalloy cores (MPP), amorphous and powdered iron cores. Powdered iron cores are very commonly used. Powdered iron cores are very suitable due to its high saturation flux density and have low loss at high frequencies, a distributed gap and exhibit very low EMI.

The minimum value of inductance which prevents inductor saturation or exceeding the rated FET current can be calculated as follows:

$$L_{MIN} = \frac{(V_{IN(MIN)} - V_{OUT}) \times V_{OUT}}{f_{SW} \times V_{IN(MIN)} \times I_{SW(MAX)}}$$

where:

L_{MIN} = minimum inductance value;
 $V_{IN(MIN)}$ = minimum design input voltage;
 V_{OUT} = output voltage;
 f_{SW} = switching frequency;
 $I_{SW(MAX)}$ = maximum design switch current.

The inductor ripple current can then be determined:

$$\Delta I_L = \frac{V_{OUT} \times (1 - D)}{L \times f_{SW}}$$

where:

ΔI_L = inductor ripple current;
 V_{OUT} = output voltage;
 L = inductor value;
 D = duty cycle.
 f_{SW} = switching frequency

The designer can now verify if the number of output capacitors will provide an acceptable output voltage ripple (1.0% of output voltage is common). The formula below is used:

$$\Delta I_L = \frac{\Delta V_{OUT}}{ESR_{MAX}}$$

Rearranging we have:

$$ESR_{MAX} = \frac{\Delta V_{OUT}}{\Delta I_L}$$

where:

ESR_{MAX} = maximum allowable ESR;
 $\Delta V_{OUT} = 1.0\% \times V_{OUT}$ = maximum allowable output voltage ripple (budgeted by the designer);
 ΔI_L = inductor ripple current;
 V_{OUT} = output voltage.

The number of output capacitors is determined by:

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

where:

ESR_{CAP} = maximum ESR per capacitor (specified in manufacturer's data sheet).

The designer must also verify that the inductor value yields reasonable inductor peak and valley currents (the inductor current is a triangular waveform):

$$I_{L(PEAK)} = I_{OUT} + \frac{\Delta I_L}{2}$$

where:

$I_{L(PEAK)}$ = inductor peak current;
 I_{OUT} = load current;
 ΔI_L = inductor ripple current.

$$I_{L(VALLEY)} = I_{OUT} - \frac{\Delta I_L}{2}$$

where:

$I_{L(\text{VALLEY})}$ = inductor valley current.

Input Capacitor Selection

The choice and number of input capacitors is determined by their voltage and ripple current ratings. The designer must choose capacitors that will support the worst case input voltage with an adequate margin. To calculate the number of input capacitors one must first determine the RMS ripple current through the capacitors. To this end, first calculate the average input current to the converter:

$$I_{in(\text{Avg})} = \frac{V_1 \cdot I_1 + V_2 \cdot I_2}{\eta \cdot V_{in}} \quad \text{where } \eta \text{ is the expected efficiency (typical } \sim 85\%)$$

With the average input current determined, the RMS ripple current through the input capacitor will be:

$$I_{rms} = \sqrt{\left(I_{O1}^2 + \frac{I_{P1}^2}{3}\right) \cdot D_1 + \left(I_{O2}^2 + \frac{I_{P2}^2}{3}\right) \cdot D_2 - I_{in}^2}$$

where:

$I_{O1,2}$ is the maximum DC output current for channel 1 and 2 respectively.

$I_{P1,2}$ is the peak inductor current ($1/2 \Delta I_L$) for channel's 1 and 2 respectively. If the channel peak inductor current is less than 50% of the channel output current it may be neglected.

$D_{1,2}$ is the channel duty cycle. Here it is assumed that each channel's duty cycle is less than 50% so that each phase does not overlap.

Once the RMS ripple current has been determined, the required number of input capacitor's needed is based on the rated RMS ripple current rating of the chosen capacitor.

Selection of the Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the regulator output voltage. Key specifications for output capacitors are their ESR (Equivalent Series Resistance), and ESL (Equivalent Series Inductance). For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

In order to determine the number of output capacitors the maximum voltage transient allowed during load transitions has to be specified. The output capacitors must hold the output voltage within these limits since the inductor current can not change with the required slew rate. The output capacitors must therefore have a very low ESL and ESR.

The voltage change during the load current transient is:

$$\Delta V_{OUT} = \Delta I_{OUT} \times \left(\frac{ESL}{\Delta t} + ESR + \frac{t_{TR}}{C_{OUT}} \right)$$

where:

$\Delta I_{OUT} / \Delta t$ = load current slew rate;

ΔI_{OUT} = load transient;

Δt = load transient duration time;

ESL = Maximum allowable ESL including capacitors, circuit traces, and vias;

ESR = Maximum allowable ESR including capacitors and circuit traces;

t_{TR} = output voltage transient response time.

The designer has to independently assign values for the change in output voltage due to ESR, ESL, and output capacitor discharging or charging. Empirical data indicates that most of the output voltage change (droop or spike depending on the load current transition) results from the total output capacitor ESR.

The maximum allowable ESR can then be determined according to the formula:

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

where:

ΔV_{ESR} = change in output voltage due to ESR (assigned by the designer)

Once the maximum allowable ESR is determined, the number of output capacitors can be found by using the formula:

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

where:

ESR_{CAP} = maximum ESR per capacitor (specified in manufacturer's data sheet).

ESR_{MAX} = maximum allowable ESR.

The actual output voltage deviation due to ESR can then be verified and compared to the value assigned by the designer:

$$\Delta V_{ESR} = \Delta I_{OUT} \times ESR_{MAX}$$

Similarly, the maximum allowable ESL is calculated from the following formula:

$$ESL_{MAX} = \frac{\Delta V_{ESL} \times \Delta t}{\Delta I}$$

Selection of the Input Inductor

A common requirement is that the buck controller must not disturb the input voltage. One method of achieving this is by using an input inductor and a bypass capacitor. The input inductor isolates the supply from the noise generated in the switching portion of the buck regulator and also limits the inrush current into the input capacitors upon power up. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients. The worst case is when the load changes from no load to full load (load step), a condition under which the highest voltage change across the input capacitors is also seen by the input inductor. The inductor successfully blocks the ripple current while placing the transient current requirements on the input bypass capacitor bank, which has to initially support the sudden load change.

The minimum inductance value for the input inductor is therefore:

$$L_{IN} = \frac{\Delta V}{(di/dt)_{MAX}}$$

where:

L_{IN} = input inductor value;

ΔV = voltage seen by the input inductor during a full load swing;

$(di/dt)_{MAX}$ = maximum allowable input current slew rate.

The designer must select the LC filter pole frequency so that at least 40 dB attenuation is obtained at the regulator switching frequency. The LC filter is a double-pole network with a slope of -2.0, a roll-off rate of -40 dB/dec, and a corner frequency:

$$f_C = \frac{1}{2\pi \times \sqrt{LC}}$$

where:

L = input inductor;

C = input capacitor(s).

SELECTION OF THE POWER FETS

FET Basics

The use of the MOSFET as a power switch is propelled by two reasons: 1) *Its very high input impedance*; and 2) *Its very fast switching times*. The electrical characteristics of a MOSFET are considered to be those of a perfect switch. Control and drive circuitry power is therefore reduced. Because the input impedance is so high, it is voltage driven. The input of the MOSFET acts as if it were a small capacitor, which the driving circuit must charge at turn on. The lower the drive impedance, the higher the rate of rise of V_{GS} , and the faster the turn-on time. Power dissipation in the switching MOSFET consists of 1) conduction losses, 2) leakage losses, 3) turn-on switching losses, 4) turn-off switching losses, and 5) gate-transitions losses. The latter three losses are proportional to frequency.

The most important aspect of FET performance is the Static Drain-To-Source On-Resistance ($R_{DS(ON)}$), which affects regulator efficiency and FET thermal management requirements. The On-Resistance determines the amount of current a FET can handle without excessive power dissipation that may cause overheating and potentially catastrophic failure. As the drain current rises, especially above the continuous rating, the On-Resistance also increases. Its positive temperature coefficient is between +0.6%/°C and +0.85%/°C. The higher the On-Resistance the larger the conduction loss is. Additionally, the FET gate charge should be low in order to minimize switching losses and reduce power dissipation.

Both logic level and standard FETs can be used.

Voltage applied to the FET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the FET gates

will be driven rail-to-rail due to overshoot caused by the capacitive load they present to the controller IC.

Selection of the Switching (Upper) FET

The designer must ensure that the total power dissipation in the FET switch does not cause the power component to exceed its maximum rating.

The maximum RMS current through the switch can be determined by the following formula:

$$I_{RMS(H)} = \sqrt{\frac{I_L(PEAK)^2 + (I_L(PEAK) \times I_L(VALLEY)) + I_L(VALLEY)^2 \times D}{3}}$$

where:

$I_{RMS(H)}$ = maximum switching MOSFET RMS current;

$I_L(PEAK)$ = inductor peak current;

$I_L(VALLEY)$ = inductor valley current;

D = duty cycle.

Once the RMS current through the switch is known, the switching MOSFET conduction losses can be calculated:

$$P_{RMS(H)} = I_{RMS(H)}^2 \times R_{DS(ON)}$$

where:

$P_{RMS(H)}$ = switching MOSFET conduction losses;

$I_{RMS(H)}$ = maximum switching MOSFET RMS current;

$R_{DS(ON)}$ = FET drain-to-source on-resistance

The upper MOSFET switching losses are caused during MOSFET switch-on and switch-off and can be determined by using the following formula:

$$P_{SWH} = P_{SWH(ON)} + P_{SWH(OFF)} \\ = \frac{V_{IN} \times I_{OUT} \times (t_{RISE} + t_{FALL})}{6T}$$

where:

$P_{SWH(ON)}$ = upper MOSFET switch-on losses;

$P_{SWH(OFF)}$ = upper MOSFET switch-off losses;

V_{IN} = input voltage;

I_{OUT} = load current;

t_{RISE} = MOSFET rise time (from FET manufacturer's switching characteristics performance curve);

t_{FALL} = MOSFET fall time (from FET manufacturer's switching characteristics performance curve);

$T = 1/f_{SW}$ = period.

The total power dissipation in the switching MOSFET can then be calculated as:

$$P_{HFET(TOTAL)} = P_{RMS(H)} + P_{SWH(ON)} + P_{SWH(OFF)}$$

where:

$P_{HFET(TOTAL)}$ = total switching (upper) MOSFET losses;

$P_{RMS(H)}$ = upper MOSFET switch conduction Losses;

$P_{SWH(ON)}$ = upper MOSFET switch-on losses;

$P_{SWH(OFF)}$ = upper MOSFET switch-off losses;

Once the total power dissipation in the switching FET is known, the maximum FET switch junction temperature can be calculated:

$$T_J = T_A + [P_{HFET(TOTAL)} \times R_{\theta JA}]$$

where:

T_J = FET junction temperature;
 T_A = ambient temperature;
 $P_{HFET(TOTAL)}$ = total switching (upper) FET losses;
 $R_{\theta JA}$ = upper FET junction-to-ambient thermal resistance.

Selection of the Synchronous (Lower) FET

The switch conduction losses for the lower FET can be calculated as follows:

$$P_{RMS(L)} = I_{RMS}^2 \times R_{DS(ON)} \\ = [I_{OUT} \times \sqrt{(1 - D)}]^2 \times R_{DS(ON)}$$

where:

$P_{RMS(L)}$ = lower MOSFET conduction losses;
 I_{OUT} = load current;
 D = Duty Cycle;
 $R_{DS(ON)}$ = lower FET drain-to-source on-resistance.

The synchronous MOSFET has no switching losses, except for losses in the internal body diode, because it turns on into near zero voltage conditions. The MOSFET body diode will conduct during the non-overlap time and the resulting power dissipation (neglecting reverse recovery losses) can be calculated as follows:

$$P_{SWL} = V_{SD} \times I_{LOAD} \times \text{non-overlap time} \times f_{SW}$$

where:

P_{SWL} = lower FET switching losses;
 V_{SD} = lower FET source-to-drain voltage;
 I_{LOAD} = load current;
Non-overlap time = GATE(L)-to-GATE(H) or GATE(H)-to-GATE(L) delay (from NCP5422A data sheet Electrical Characteristics section);
 f_{SW} = switching frequency.

The total power dissipation in the synchronous (lower) MOSFET can then be calculated as:

$$P_{LFET(TOTAL)} = P_{RMS(L)} + P_{SWL}$$

where:

$P_{LFET(TOTAL)}$ = Synchronous (lower) FET total losses;
 $P_{RMS(L)}$ = Switch Conduction Losses;
 P_{SWL} = Switching losses.

Once the total power dissipation in the synchronous FET is known the maximum FET switch junction temperature can be calculated:

$$T_J = T_A + [P_{LFET(TOTAL)} \times R_{\theta JA}]$$

where:

T_J = MOSFET junction temperature;
 T_A = ambient temperature;
 $P_{LFET(TOTAL)}$ = total synchronous (lower) FET losses;
 $R_{\theta JA}$ = lower FET junction-to-ambient thermal resistance.

Control IC Power Dissipation

The power dissipation of the IC varies with the MOSFETs used, V_{CC} , and the NCP5422A operating frequency. The average MOSFET gate charge current typically dominates the control IC power dissipation.

The IC power dissipation is determined by the formula:

$$P_{CONTROL(IC)} = I_{CC1}V_{CC1} + I_{BST}V_{BST} + P_{GATE(H)1} \\ + P_{GATE(L)1} + P_{GATE(H)2} + P_{GATE(L)2}$$

where:

$P_{CONTROL(IC)}$ = control IC power dissipation;
 I_{CC1} = IC quiescent supply current;
 V_{CC1} = IC supply voltage;
 $P_{GATE(H)}$ = upper MOSFET gate driver (IC) losses;
 $P_{GATE(L)}$ = lower MOSFET gate driver (IC) losses.
The upper (switching) MOSFET gate driver (IC) losses are:

$$P_{GATE(H)} = Q_{GATE(H)} \times f_{SW} \times V_{BST}$$

where:

$P_{GATE(H)}$ = upper MOSFET gate driver (IC) losses;
 $Q_{GATE(H)}$ = total upper MOSFET gate charge at V_{CC} ;
 f_{SW} = switching frequency;
The lower (synchronous) MOSFET gate driver (IC) losses are:

$$P_{GATE(L)} = Q_{GATE(L)} \times f_{SW} \times V_{CC}$$

where:

$P_{GATE(L)}$ = lower MOSFET gate driver (IC) losses;
 $Q_{GATE(L)}$ = total lower MOSFET gate charge at V_{CC} ;
 f_{SW} = switching frequency;

The junction temperature of the control IC is primarily a function of the PCB layout, since most of the heat is removed through the traces connected to the pins of the IC.

Current Sensing

The current supplied to the load can be sensed easily using the IS+ and IS- pins for the output. These pins sense a voltage, proportional to the output current, and compare it to a fixed internal voltage threshold. When the differential voltage exceeds 70 mV, the internal overcurrent protection system goes into hiccup mode. Two methods for sensing the current are available.

Sense Resistor. A sense resistor can be added in series with the inductor. When the voltage drop across the sense resistor exceeds the internal voltage threshold of 70 mV, a fault condition is set.

The sense resistor is selected according to:

$$R_{SENSE} = \frac{0.070 \text{ V}}{I_{LIMIT}}$$

In a high current supply, the sense resistor will be a very low value, typically less than 10 mΩ. Such a resistor can be either a discrete component or a PCB trace. The resistance value of a discrete component can be more precise than a PCB trace, but the cost is also greater.

Setting the current limit using an external sense resistor is very precise because all the values can be designed to specific tolerances. However, the disadvantage of using a sense resistor is its additional constant power loss and heat generation.

Inductor ESR. Another means of sensing current is to use the intrinsic resistance of the inductor. A model of an inductor (Figure 9) reveals that the windings of an inductor have an effective series resistance (ESR).

The voltage drop across the inductor ESR can be measured with a simple parallel circuit: an RC integrator. If the value of R_{S1} and C are chosen such that:

$$\frac{L}{ESR} = R_{S1}C$$

then the voltage measured across the capacitor C will be:

$$V_C = ESR \times I_{LIM}$$

Selecting Components. Select the capacitor C first. A value of $0.1 \mu F$ is recommended. The value of R_{S1} can be selected according to:

$$R_{S1} = \frac{1}{ESR \times C}$$

Typical values for inductor ESR range in the low $m\Omega$. Consult manufacturer's datasheet for specific details.

Selection of components at these values will result in a current limit of:

$$I_{LIM} = \frac{0.070 V}{ESR}$$

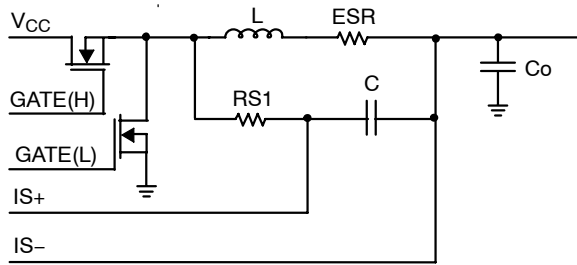


Figure 9. Inductor ESR Current Sensing

Given an ESR value of $3.5 m\Omega$, the current limit becomes $20 A$. If an increased current limit is required, a resistor divider can be added.

The advantages of setting the current limit by using the winding resistance of the inductor are that efficiency is maximized and heat generation is minimized. The tolerance of the inductor ESR must be factored into the design of the current limit. Finally, one or two more components are required for this approach than with resistor sensing. Note that, in the example of Figure 9, the $IS+$ input bias current flowing through $RS1$ will introduce a small offset error. If $RS1 = 4 k\Omega$, at the maximum bias current limit of $1 \mu A$, the error will be $4 mV$. This error can be avoided by using two separate resistors, each half the calculated value, as shown ($R1$ through $R4$) in the typical application circuit of Figure 1.

Adding External Slope Compensation

Today's voltage regulators are expected to meet very stringent load transient requirements. One of the key factors in achieving tight dynamic voltage regulation is low ESR. Low ESR at the regulator output results in low output

voltage ripple. The consequence is, however, that very little voltage ramp exists at the control IC feedback pin (V_{FB}), resulting in increased regulator sensitivity to noise and the potential for loop instability. In applications where the internal slope compensation is insufficient, the performance of the NCP5422A-based regulator can be improved through the addition of a fixed amount of external slope compensation at the output of the PWM Error Amplifier (the COMP pin) during the regulator off-time. Referring to Figure 10, the amount of voltage ramp at the COMP pin is dependent on the gate voltage of the lower (synchronous) FET and the value of resistor divider formed by $R1$ and $R2$.

$$V_{SLOPECOMP} = V_{GATE(L)} \times \left(\frac{R2}{R1 + R2} \right) \times \left(1 - e^{-\frac{t}{\tau}} \right)$$

where:

$V_{SLOPECOMP}$ = amount of slope added;

$V_{GATE(L)}$ = lower MOSFET gate voltage;

$R1, R2$ = voltage divider resistors;

$t = t_{ON}$ or t_{OFF} (switch off-time);

τ = RC constant determined by $C1$ and the parallel combination of $R1, R2$ neglecting the low driver output impedance.

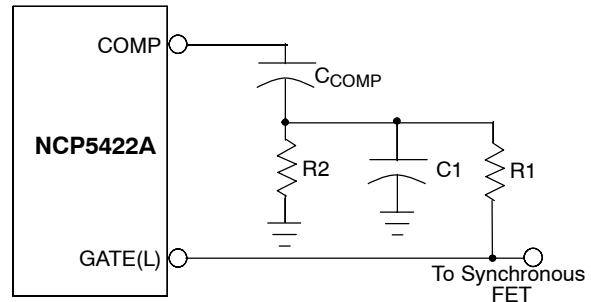


Figure 10. Small RC Filter Provides the Proper Voltage Ramp at the Beginning of Each On-Time Cycle

The artificial voltage ramp created by the slope compensation scheme results in improved control loop stability provided that the RC filter time constant is smaller than the off-time cycle duration (time during which the lower MOSFET is conducting). It is important that the series combination of $R1$ and $R2$ is high enough in resistance to avoid loading the $GATE(L)$ pin. Also, $C1$ should be very small (less than a few nF) to avoid heating the part.

EMI MANAGEMENT

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the

board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.

LAYOUT GUIDELINES

When laying out the CPU buck regulator on a printed circuit board, the following checklist should be used to ensure proper operation of the NCP5422A.

1. Rapid changes in voltage across parasitic capacitors and abrupt changes in current in parasitic inductors are major concerns for a good layout.
2. Keep high currents out of sensitive ground connections.
3. Avoid ground loops as they pick up noise. Use star or single point grounding.
4. For high power buck regulators on double-sided PCB's a single ground plane (usually the bottom) is recommended.
5. Even though double sided PCB's are usually sufficient for a good layout, four-layer PCB's are the optimum approach to reducing susceptibility to noise. Use the two internal layers as the power and GND planes, the top layer for power connections and component vias, and the bottom layers for the noise sensitive traces.
6. Keep the inductor switching node small by placing the output inductor, switching and synchronous FETs close together.
7. The MOSFET gate traces to the IC must be short, straight, and wide as possible.
8. Use fewer, but larger output capacitors, keep the capacitors clustered, and use multiple layer traces with heavy copper to keep the parasitic resistance low.
9. Place the switching MOSFET as close to the input capacitors as possible.
10. Place the output capacitors as close to the load as possible.
11. Place the COMP capacitor as close as possible to the COMP pin.
12. Connect the filter components of the following pins: R_{OSC}, V_{FB}, V_{OUT}, and COMP to the GND pin with a single trace, and connect this local GND trace to the output capacitor GND.
13. Place the V_{CC} bypass capacitors as close as possible to the IC.
14. Place the R_{OSC} resistor as close as possible to the R_{OSC} pin.
15. Include provisions for 100–100pF capacitor across each resistor of the feedback network to improve noise immunity and add COMP.
16. Assign the output with lower duty cycle to channel 2, which has better noise immunity.

NCP5425

Dual Synchronous Buck Controller

The NCP5425 is a highly flexible dual buck controller with internal gate drivers that can be used with two input power supplies and one or two outputs in multiple configurations. The part contains all the circuitry required for two independent synchronous dual NFET buck regulators utilizing a feed forward voltage mode control method. The NCP5425 can run from a single supply ranging from 4.6 to 12 volts and support a single two phase or dual single phase outputs. When used as a dual output controller, the second output tracks voltage transients from the first. Power blanking for low noise applications is supported as well as independent cycle-by-cycle current limiting. The part is available in a 20 pin TSSOP package allowing the designer to minimize PCB area.

Features

- Operation Over 4.6 to 13.2 Volts
- Dual Synchronous Buck Design
- Configurable as a Single Two Phase Output or Two Single Phase Outputs
- Programmable Power Sharing and Budgeting from Two Independent Supplies
- 0.8 Volt $\pm 1\%$ Reference for Low Voltage Outputs
- 1.5 A Peak Power Drive
- Switch Blanking for Noise Sensitive Applications through use of ROSC Pin
- Programmable Frequency, 150 kHz to 750 kHz Operation
- Programmable Soft Start
- Cycle-by-Cycle Overcurrent Protection
- Independent Programmable Current Limits
- 100% Duty Cycle for Fast Transient Response
- Internal Slope Compensation
- Out-of-Phase Synchronization between the Controllers
- Input Undervoltage Lockout
- On/Off Enable through use of the COMP Pins
- Power Supply Sequencing

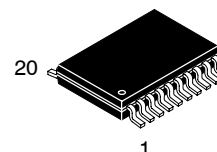
Applications

- DDR Memory Power
- Graphics Cards



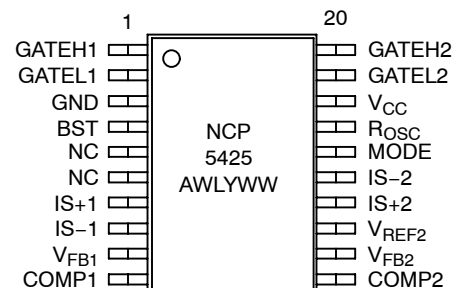
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**TSSOP-20
DB SUFFIX
CASE 948E**

PIN CONNECTIONS AND MARKING DIAGRAM



A = Assembly Location

WL = Wafer Lot

Y = Year

WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping [†]
NCP5425DB	TSSOP-20	61 Units/Rail
NCP5425DBR2	TSSOP-20	2500 Units/Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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MAXIMUM RATINGS

Rating	Value	Unit
Operating Junction Temperature, T_J	150	°C
Storage Temperature Range, T_J	–65 to 150	°C
ESD Susceptibility (Human Body Model)	2.0	kV
ESD Susceptibility (Machine Model)	200	V
Moisture Sensitivity Level (MSL)	1	
Lead Temperature Soldering: Reflow: (Note 1)	260 peak	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. 60 to 150 seconds maximum above 183°C, 260°C peak.

MAXIMUM RATINGS

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
V_{CC}	IC Power Input	16 V	–0.3 V	N/A	2.0 A Peak 200 mA DC
COMP1, COMP2	Compensation Capacitor for Channel 1 or 2	4.0 V	–0.3 V	1.0 mA	1.0 mA
V_{FB1} , V_{FB2} , V_{REF2}	Voltage Feedback Input for Channel 1 or 2	6.0 V	–0.3 V	1.0 mA	1.0 mA
R_{OSC}	Oscillator Resistor	5.0 V	–0.3 V	1.0 mA	1.0 mA
GATE(H)1, GATE(H)2	High-Side FET Driver for Channel 1 or 2	20 V	–0.3 V	2.0 A Peak 200 mA DC	2.0 A Peak 200 mA DC
GATE(L)1, GATE(L)2	Low-Side FET Driver for Channel 1 or 2	16 V	–0.3 V	2.0 A Peak 200 mA DC	2.0 A Peak 200 mA DC
IS+1, IS+2	Positive Current Sense for Channel 1 or 2	6.0 V	–0.3 V	1.0 mA	1.0 mA
IS–1, IS–2	Negative Current Sense for Channel 1 or 2	6.0 V	–0.3 V	1.0 mA	1.0 mA
GND	Ground	100 mV	0 V	2.0 A Peak 200 mA DC	N/A
BST	Power Input for GATE(H)1 GATE(H)2	20 V	–0.3 V	N/A	2.0 A Peak 200 mA DC
MODE	Dual or Single Output Select	3.5 V	–0.3 V	N/A	N/A

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ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$; $R_{\text{OSC}} = 30.9 \text{ k}$, $C_{\text{COMP1,2}} = 0.1 \mu\text{F}$, $4.75 \text{ V} < V_{\text{CC}} < 13.2 \text{ V}$; $10.8 \text{ V} < \text{BST} < 20 \text{ V}$, $C_{\text{GATE(H)1,2}} = C_{\text{GATE(L)1,2}} = 1.0 \text{ nF}$; unless otherwise specified.)

Characteristic	Test Condition	Min	Typ	Max	Unit
Error Amplifier					
V_{FB1} Input Bias Current	$V_{\text{FB1}} = 0 \text{ V}$	–	0.1	1.0	μA
V_{FB2} , V_{REF2} Input Bias Current	V_{FB2} , $V_{\text{REF2}} = 0.8 \text{ V}$	–	0.1	1.0	μA
Input Voltage Range	–	0.3	–	1.9	V
COMP1(2) Source Current	COMP1(2) = 1.2 V to 2.5 V; $V_{\text{FB1(2)}} = 0.6 \text{ V}$	15	30	60	μA
COMP1(2) Sink Current	COMP1(2) = 1.2 V; $V_{\text{FB1(2)}} = 1.0 \text{ V}$	15	30	60	μA
Reference Voltage	COMP1 = V_{FB1}	0.792	0.800	0.808	V
COMP1 Max Voltage	$V_{\text{FB1(2)}} = 0.6 \text{ V}$	–	2.0	2.1	V
COMP2 Max Voltage, Mode Floating	$V_{\text{FB1(2)}} = 0.6 \text{ V}$	3.0	3.1	–	
COMP2 Max Voltage, Mode = 0	$V_{\text{FB1(2)}} = 0.6 \text{ V}$	–	2.0	2.1	
COMP1(2) Min Voltage	$V_{\text{FB1(2)}} = 1.2 \text{ V}$	–	0.10	0.20	V
Open Loop Gain		–	95	–	dB
Unity Gain Bandwidth		–	40	–	kHz
PSRR @ 1.0 kHz		–	70	–	dB
Transconductance	–	–	32	–	mmho
Output Impedance	–	–	2.5	–	$\text{M}\Omega$

GATE(H) and GATE(L)

High Voltage (AC)	$V_{\text{CC}} - \text{GATE(L)1,2}$ BST – GATE(H)1,2 (Note 2)	–	0	0.5	V
Low Voltage (AC)	GATE(L)1,2 or GATE(H)1,2 (Note 2)	–	0	0.5	V
Rise Time	$1.0 \text{ V} < \text{GATE(L)1,2} < V_{\text{CC}} - 1.0 \text{ V}$ $1.0 \text{ V} < \text{GATE(H)1,2} < \text{BST} - 1.0 \text{ V}$	–	25	80	ns
Fall Time	$V_{\text{CC}} - 1.0 > \text{GATE(L)1,2} > 1.0 \text{ V}$ BST – $1.0 > \text{GATE(H)1,2} > 1.0 \text{ V}$	–	25	80	ns
GATE(H) to GATE(L) Delay	GATE(H)1,2 < 2.0 V GATE(L)1,2 > 2.0 V	20	40	80	ns
GATE(L) to GATE(H) Delay	GATE(L)1,2 < 2.0 V GATE(H)1,2 > 2.0 V	20	40	80	ns
GATE(H)1(2) and GATE(L)1(2) Pull-Down	Resistance to GND (Note 2)	50	125	280	$\text{k}\Omega$

PWM Comparator

Propagation Delay	COMP1(2) = 1.0 V $V_{\text{FB1(2)}} = 0$ to 1.2 V Note 2	–	200	300	ns
PWM Comparator Offset	$V_{\text{FB1(2)}} = 0 \text{ V}$; Increase COMP1(2) until GATE(H)1(2) starts switching	0.20	0.30	0.45	V
Artificial Ramp	Duty Cycle = 50%	55	95	150	mV
Minimum Pulse Width	(Note 2)	–	80	130	ns

2. Guaranteed by design, not 100% tested in production.

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ELECTRICAL CHARACTERISTICS (continued) ($0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$; $R_{\text{OSC}} = 30.9 \text{ k}$, $C_{\text{COMP1,2}} = 0.1 \mu\text{F}$, $4.75 \text{ V} < V_{\text{CC}} < 13.2 \text{ V}$; $10.8 \text{ V} < \text{BST} < 20 \text{ V}$, $C_{\text{GATE(H)1,2}} = C_{\text{GATE(L)1,2}} = 1.0 \text{ nF}$; unless otherwise specified.)

Characteristic	Test Condition	Min	Typ	Max	Unit

Oscillator

Switching Frequency	$R_{\text{OSC}} = 61.9 \text{ k}$; Measure GATE(H)1	112	150	188	kHz
Switching Frequency	$R_{\text{OSC}} = 30.9 \text{ k}$; Measure GATE(H)1	224	300	376	kHz
Switching Frequency	$R_{\text{OSC}} = 11.8 \text{ k}$; Measure GATE(H)1	562	750	938	kHz
R_{OSC} Voltage	$R_{\text{OSC}} = 30.9 \text{ k}$	0.970	1.000	1.030	V
Phase Difference	–	–	180	–	°
Low Noise Disable	Guaranteed By Design	–	3.1	3.5	V

Overcurrent Protection

OVC Comparator Offset Voltage	$0 \text{ V} < \text{IS}+1(2) < 5.5 \text{ V}$ $0 \text{ V} < \text{IS}-1(2) < 5.5 \text{ V}$	55	70	85	mV
IS+1(2) Bias Current	$0 \text{ V} < \text{IS}+1(2) < 5.5 \text{ V}$	–1.0	0.1	1.0	μA
IS–1(2) Bias Current	$0 \text{ V} < \text{IS}-1(2) < 5.5 \text{ V}$	–1.0	0.1	1.0	μA
OVC Common Mode Range	–	0	–	5.5	V

Supply Currents

V_{CC} Current	COMP = 0 V (No Switching)	–	16	22	mA
BST Current	COMP = 0 V (No Switching)	–	3.5	6.0	mA

Undervoltage Lockout

Start Threshold	GATE(H) Switching; COMP1(2) Charging	3.8	4.2	4.6	V
Stop Threshold	GATE(H) Not Switching; COMP1(2) Discharging	3.6	4.0	4.4	V
Hysteresis	Start–Stop	0.1	0.2	0.25	V

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PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	GATE(H)1	High Side Switch FET driver pin for the channel 1 FET.
2	GATE(L)1	Low Side Synchronous FET driver pin for the channel 1 FET.
3	GND	Ground. All circuits are referenced to this pin. IC substrate connection.
4	BST	Power input for GATE(H)1 and GATE(H)2 pins.
5	NC	No connection.
6	NC	No connection.
7	IS+1	Positive input for channel 1 overcurrent comparator.
8	IS-1	Negative input for channel 1 overcurrent comparator.
9	V _{FB1}	Error amplifier inverting input for channel 1.
10	COMP1	Channel 1 Error Amp output. PWM comparator reference input. A capacitor to GND provides Error Amp compensation. The same capacitor provides soft-start timing for channel 1. This pin also disables the channel 1 output when pulled below 0.2 V.
11	COMP2	Channel 2 Error Amp output. PWM comparator reference input. A capacitor to GND provides Error Amp compensation and soft-start timing for channel 2. Channel 2 output is disabled when this pin is pulled below 0.2 V.
12	V _{FB2}	Error amplifier inverting input for channel 2.
13	V _{REF2}	Error amplifier noninverting input for channel 2.
14	IS+2	Positive input for channel 2 overcurrent comparator.
15	IS-2	Negative input for channel 2 overcurrent comparator.
16	MODE	Input pin used to inform internal circuitry of dual output or single output operation. Ground this pin for dual output operation, leave open for single output operation.
17	R _{OSC}	A resistor from this pin to ground sets switching frequency.
18	V _{CC}	Input Power supply pin. Power input for GATE(L)1 and GATE(L)2 pins.
19	GATE(L)2	Low Side Synchronous FET driver pin for the channel 2 FET.
20	GATE(H)2	High Side Switch FET driver pin for the channel 2 FET.

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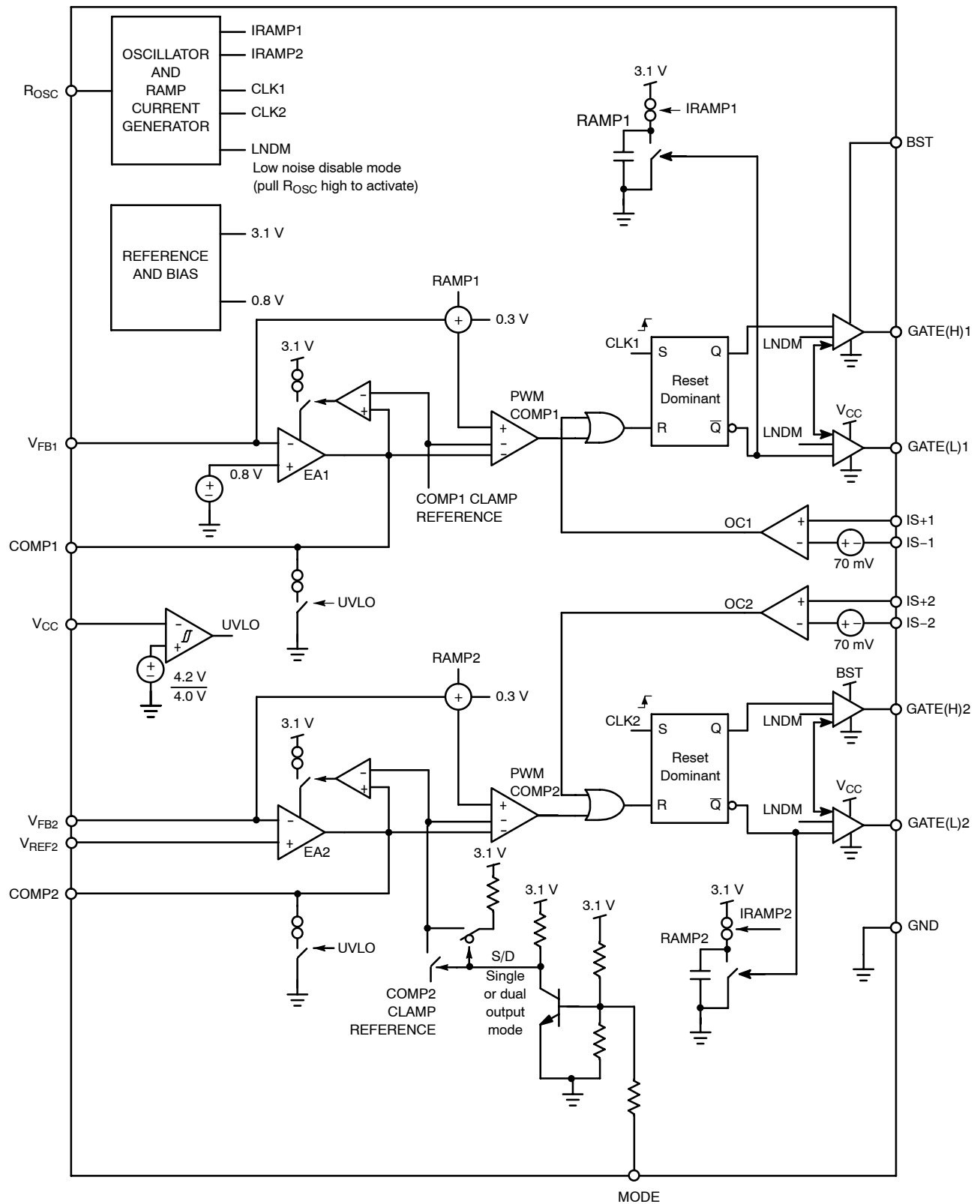


Figure 12. Block Diagram

APPLICATIONS INFORMATION

Theory of Operation

The NCP5425 is a very versatile buck controller using V^2 ™ control method. It can be configured as:

- Dual output Buck Controller.
- Two phase Buck Controller with current limit.
- Two phase Buck Controller with input power ratio and current limit.

The fixed-frequency architecture, driven from a common oscillator, ensures a 180° phase differential between channels.

 V^2 Control Method

The V^2 method of control uses a ramp signal generated by the ESR (Effective Series Resistance) of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. The V^2 method differs from traditional techniques such as voltage mode control, which generates an artificial ramp, and current mode control, which generates a ramp using the inductor current.

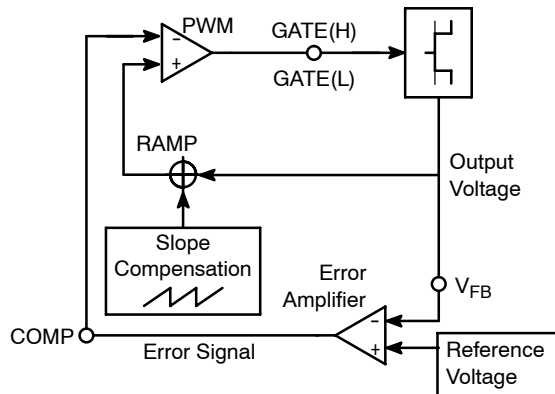


Figure 13. V^2 Control with Slope Compensation

The V^2 control method is illustrated in Figure 13. The output voltage generates both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output, regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, allowing the control circuit to drive the main switch to 0% or 100% duty cycle as required. A variation in line voltage changes the current ramp in the inductor, which causes the V^2 control scheme to compensate the duty cycle. Since any variation in inductor current modifies the ramp signal, as in current mode control, the V^2 control scheme offers the same advantages in line transient response. A variation in load current will affect the output voltage, modifying the ramp signal. A load step immediately changes the state of the comparator output, which controls

the main switch. The comparator response time and the transition speed of the main switch determine the load transient response. Unlike traditional control methods, the reaction time to the output load step is not related to the crossover frequency of the error signal loop. The error signal loop can have a low crossover frequency, since the transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered. Line and load regulation are drastically improved because there are two independent control loops. A voltage mode controller relies on the change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, the consequence of which is normally specified as line or load regulation. A current mode controller maintains a fixed error signal during line transients, since the slope of the ramp signal changes in this case. However, regulation of load transients still requires a change in the error signal. The V^2 method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

The stringent load transient requirements of modern power supplies require the output capacitors to have very low ESR. The resulting shallow slope in the output ripple can lead to pulse width jitter and variation caused by both random and synchronous noise. A ramp waveform generated in the oscillator is added to the ramp signal from the output voltage to provide the proper voltage ramp at the beginning of each switching cycle. This slope compensation increases the noise immunity, particularly at higher duty cycle (above 50%).

Start Up

The NCP5425 features a programmable soft start function, which is implemented through the error amplifier and external compensation capacitor. This feature reduces stress to the power components and limits overshoot of the output voltage, during startup. As power is applied to the regulator, the NCP5425 Undervoltage Lockout circuit (UVLO) monitors the IC's supply voltage (V_{CC}). The UVLO circuit prevents the MOSFET gates from switching until V_{CC} exceeds 4.2 V. Internal UVLO threshold hysteresis of 200 mV improves noise immunity. During start up, the external Compensation Capacitor connected to the COMP pin is charged by an internal 30 μ A current source. When the capacitor voltage exceeds the 0.3 V offset of the PWM comparator, the PWM control loop will allow switching to occur. The upper gate driver GATE(H) is now activated, turning on the upper MOSFET. The output current then ramps up through the main inductor and linearly powers the output capacitors and load. When the regulator

output voltage exceeds the COMP pin voltage, minus the 0.3 V PWM comparator offset threshold and the artificial ramp, the PWM comparator terminates the initial pulse.

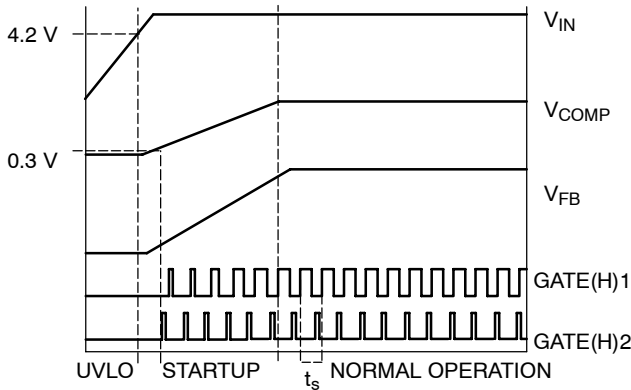


Figure 14. Idealized Start Up Waveforms

Normal Operation

During normal operation, the duty cycle remains approximately constant as the V^2 control loop maintains regulated output voltage under steady state conditions. Variations in supply line or output load conditions will result in changes in duty cycle to maintain regulation.

Gate Charge Effect on Switching Times

When using the on board gate drivers, the gate charge has an important effect on the switching times of the FETs. A finite amount of time is required to charge the effective capacitor seen at the gate of the FET. Therefore, the rise and fall times rise linearly with increased capacitive loading, according to the following graphs.

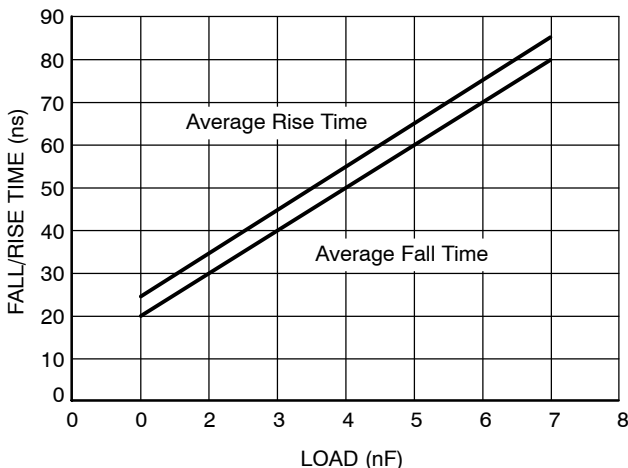


Figure 15. Average Rise and Fall Times

Transient Response

The 200 ns reaction time of the control loop provides fast transient response to any variations in input voltage or output current. Pulse-by-pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitors during the time required to slew the inductor current. For better transient response, a combination of several high frequency and bulk output capacitors are typically used.

Out-of-Phase Synchronization

The turn-on of the second channel is delayed by half the switching cycle. This delay is supervised by the oscillator, which supplies a clock signal to the second channel that is 180° out of phase with the clock signal of the first channel. Advantages of out-of-phase synchronization are many. Since the input current pulses are interleaved with one another, the overlap time is reduced. Overlap reduction reduces the input filter requirement, allowing the use of smaller components. In addition, since peak current occurs during a shorter time period, emitted EMI is also reduced, potentially reducing shielding requirements. Interleaving the phases in a two phase application reduces ripple voltage and allows supplies with tighter tolerances to be built.

Overvoltage Protection

Overvoltage Protection (OVP) is provided as a consequence of the normal operation of the V^2 control method, and requires no additional external components to implement. The control loop responds to an overvoltage condition within 200 ns, turning off the upper MOSFET and disconnecting the regulator from its input voltage. This results in a crowbar action to clamp the output voltage, preventing damage to the load. The regulator remains in this state until the overvoltage condition clears.

Low Noise Disable Mode

A PWM converter operating at a constant frequency concentrates its noise output over a small frequency band. In noise-sensitive applications, this frequency can be chosen to prevent interference with other system functions. Some applications may have even more stringent requirements, where absolutely no noise may be emitted for a short period of time.

The user may disable the clock during noise sensitive periods to temporarily inhibit switching noise by disconnecting or pulling the R_{OSC} pin to 3.3 V. This disables both gate drivers, leaving the switch node floating, and discharges the internal ramp.

The control circuitry remains enabled while the clock and drivers are disabled, so the COMP pins will charge up to a higher voltage. The COMP pins are clamped to prevent excessive overshoot when switching is resumed.

Current Sharing

When used in a two separate input to a single output mode, the NCP5425 dual controller can provide input power sharing in either of two ways:

- A preset ratio. For example, Channel 1 could provide 70% of the load current, and Channel 2, the remaining 30%. Practical ratios for Channel 1/Channel 2 contribution to total load current range from 50%–50% to 80%–20%.
- A preset ratio up to a specific current contribution from Channel 2. In excess of that limit, all of the additional load current would be supplied by Channel 1. Figure 17 depicts the actual performance of a NCP5425 configured in a 70%–30% share ratio, with Channel 2 output current limited to 5.0 Amps.

The availability both Channel 2 error amplifier inputs (signal and reference) at device pins is key to programmable current ratio sharing. Current sense information from

Channel 1 is connected to the reference input of the Channel 2 error amplifier. Current information from Channel 2 is fed back to the error amplifier's inverting input. Channel 2 will therefore act to adjust its current to match the current information fed to its reference input from Channel 1. If this information is one-half the voltage developed across the Channel 1 output inductor, Channel 2 will run at half the current and supply a approximately 33% of the total load current. This application is illustrated in Figure 17.

In some applications the power supply designer may not only wish to draw a known percentage of power from one source, but also limit the power drawn from that source. The current limit amplifier on Channel 2 can be programmed to budget the maximum input power into Channel 2 and all power in excess of that limit will be supplied solely by Channel 1. This is accomplished by setting the Channel 2 cycle-by-cycle current limit in conjunction with programming the current ratio as described above.

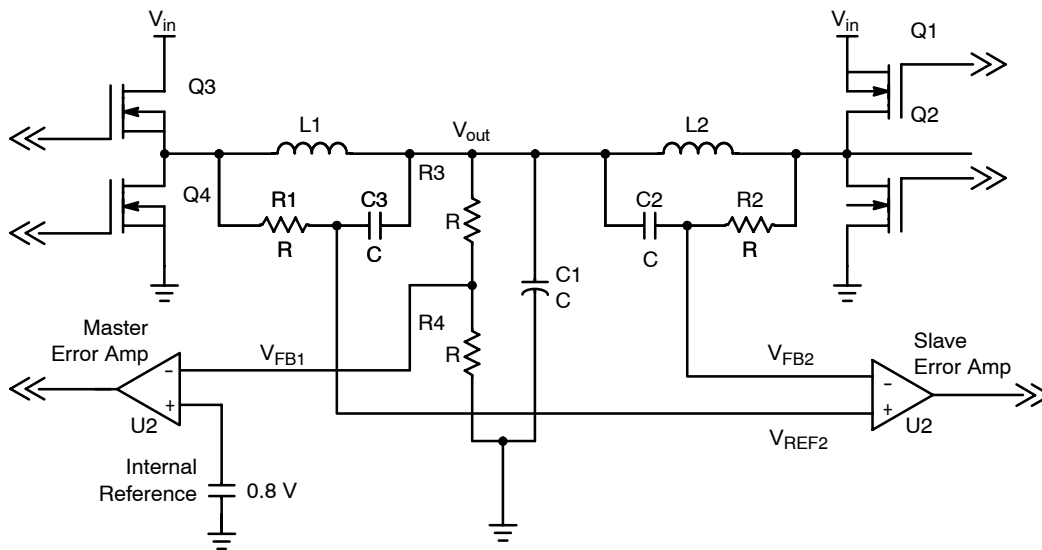


Figure 16. Two Phase Current Sharing Circuit

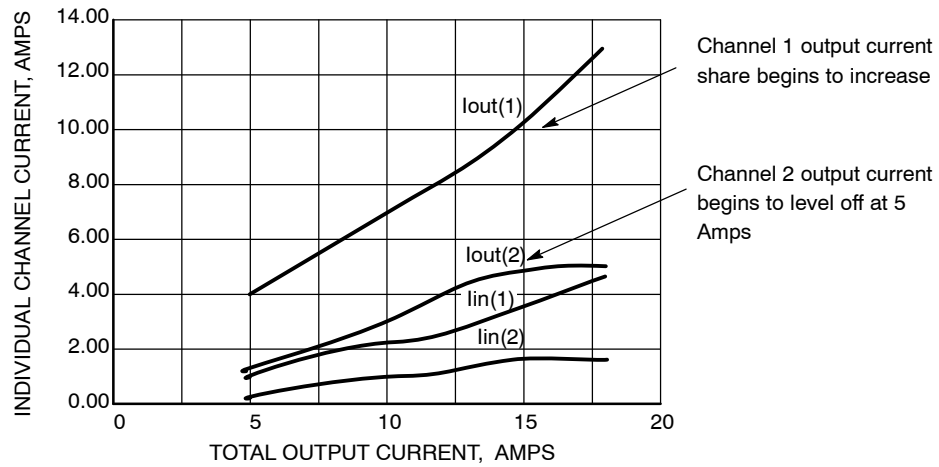


Figure 17. 70%/30% Current Sharing with Channel 2 Current Limiting

NOTE: Channel 1 input voltage = Channel 2 input voltage = 5.0 V
Output voltage = 1.5 V

Inductor Current Sensing

Examples of lossless current sensing across an output inductor are shown in Figure 18. L_x is the output inductance and R_x represents its equivalent series resistance. To compensate the current sense signal, the values of R_1 and C_1 are chosen so that $L_x/R_x = R_1 \times C_1$. With these values, the

current sense signal will have the same wave shape as the inductor current and the voltage signal on C_1 will represent the instantaneous value of inductor current. The voltage across C_1 can be used as though it were a sense resistor with the same value as the inductor's ESR, thus avoiding a sense resistor's power loss.

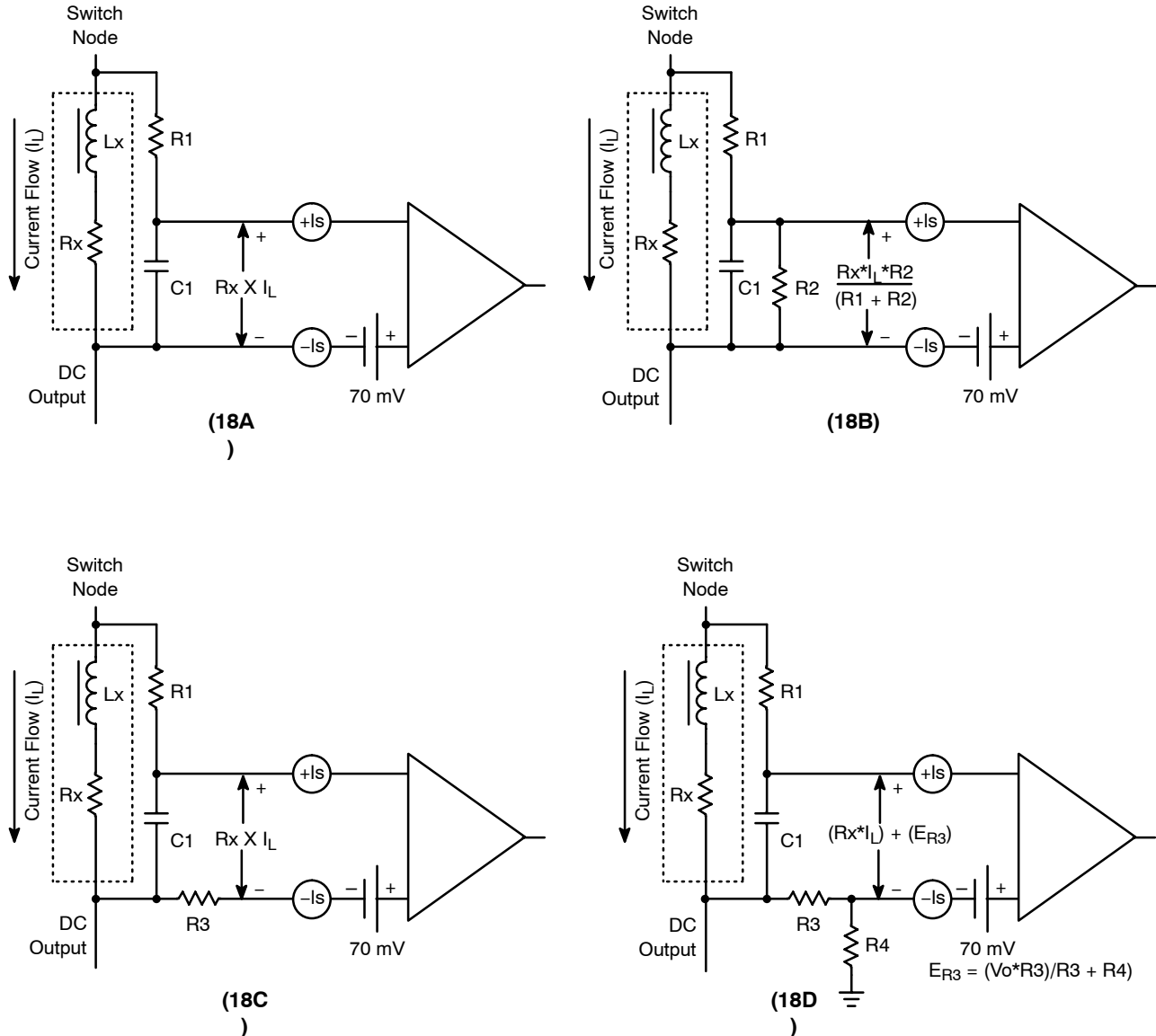


Figure 18. Inductor Current Sensing – Circuit Configurations

Figure 18A – Basic Current Sensing

Represents a basic inductor sensing configuration. When the voltage at pin +Is exceeds the voltage at pin –Is by 70 mV (nominal), the internal current sense comparator offset will be overcome. For this case, the current limit threshold is equal to $(70 \text{ mV}/R_x)$ amps. An obvious disadvantage of the basic configuration is the power supply designer has no control over the 70 mV offset, and limited control over the value of R_x . Therefore, he or she has little flexibility to set a specific current limit. Configurations (18B) and (18D) depict techniques to increase and decrease, respectively, the threshold current.

Figure 18B – Increasing the Current Threshold

Addition of resistor R_2 forms a voltage divider such that only a portion of the voltage across R_x appears across $C1$. If, for example, $R_1 = R_2$, it will require a 140 mV drop across R_x to overcome the internal 70 mV current sense comparator offset. For optimum compensation with this configuration, R_1 and R_2 should be selected such that R_x is equal to their equivalent parallel resistance.

Figure 18C – Bias Current Compensation

Configurations 18A, 18B and 18D all introduce a potential error, since the bias currents of the current sense comparator inputs flow through unbalanced resistance paths. The addition of R_3 in configuration 18C, where $R_3 = R_1$, restores a balanced input resistance, such that any voltage drops introduced by bias currents will cancel (assuming the +Is and –Is bias currents are equal). In the case of configuration 18B, R_3 would be made equal to the equivalent resistance of R_1 and R_2 in parallel.

Figure 18D – Decreasing the Current Threshold

A voltage divider comprised of R_3 and R_4 is introduced to develop, by scaling the output voltage, a small voltage drop across R_3 that opposes the internal current sense comparator offset. For example, if $V_{out} = 1.2 \text{ V}$, $R_3 = 200 \Omega$, and $R_4 = 11.8 \text{ K}$, a DC voltage drop of 20 mV will be established across R_3 . The polarity of that voltage is such that it opposes the internal 70 mV offset, effectively reducing it to 50 mV. The current threshold is now given by $(50 \text{ mV}/R_x)$ instead of $(70 \text{ mV}/R_x)$.

Current Limiting

Both channels of the NCP5425 employ identical Cycle-by-Cycle current limiting. Comparators with internal 70 mV offsets provide the references for setting current limit. Once a voltage greater than 70 mV is applied to the current limiting comparator, it resets that channel's output RS flip flop. This terminates the PWM pulse for the cycle and limits the energy delivered to the load. One advantage of this current limiting scheme is that the NCP5425 will limit large transient currents yet resume normal operation on the following cycle. A second benefit of limiting the PWM pulse width is, in an input power sharing application, one controller can be current limiting while the other supplies the remaining load current.

Output Enable

On/Off control of the regulator outputs can be implemented by pulling the COMP pins low. Driving the COMP pins below the 0.20 V PWM comparator offset voltage disables switching of the GATE drivers.

DESIGN GUIDELINES

General

The output voltage tolerance can be affected by any or all of the following:

5. Buck regulator output voltage set point accuracy.
6. Output voltage change due to discharging or charging of the bulk decoupling capacitors during a load current transient.
7. Output voltage change due to the ESR and ESL of the bulk and high frequency decoupling capacitors, circuit traces, and vias.
8. Output voltage ripple and noise.

Budgeting the tolerance is left to the designer who must consider all of the above effects and provide an output voltage that will meet the specified tolerance at the load. The designer must also ensure that the regulator component temperatures are kept within the manufacturer's specified ratings at full load and maximum ambient temperature.

Selecting Feedback Divider Resistors

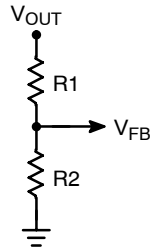


Figure 19. Feedback Divider Resistors

The feedback pins (VFB1(2)) are connected to external resistor dividers to set the output voltages. The error amplifier is referenced to 0.8 V and the output voltage is determined by selecting resistor divider values. Resistor R1 is selected based on a design trade-off between efficiency and output voltage accuracy. The output voltage error resulting from the bias current of the error amplifier can be estimated, neglecting resistor tolerance, from the following equation:

$$\%Error = (100)(1 \times 10^{-6})(R1)/0.8$$

$$\text{Rearranging, } R1 = (\%Error)(0.8)/(1 \times 10^{-4})$$

After R1 has been chosen, R2 can be calculated from:

$$R2 = (R1)/((V_{OUT}/0.8 \text{ V}) - 1)$$

Example:

Assume the desired $V_{OUT} = 1.2 \text{ V}$, and the tolerable error due to input bias current is 0.2%.

$$R1 = (0.2)(0.8)/(1 \times 10^{-4}) = 1.6 \text{ K}$$

$$R2 = 1.6 \text{ K}/((1.2/0.8) - 1) = 1.6 \text{ K}/0.5 = 3.2 \text{ K}$$

Calculating Duty Cycle

The duty cycle of a buck converter (including parasitic losses) is given by the formula:

$$\text{Duty Cycle} = D = \frac{V_{OUT} + (V_{HFET} + V_L)}{V_{IN} + V_{LFET} + V_{HFET} + V_L}$$

where:

V_{OUT} = buck regulator output voltage;

V_{HFET} = high side FET voltage drop due to $R_{DS(ON)}$;

V_L = output inductor voltage drop due to inductor wire DC resistance;

V_{IN} = buck regulator input voltage;

V_{LFET} = low side FET voltage drop due to $R_{DS(ON)}$.

Switching Frequency Select and Set

Selecting the switching frequency is a trade-off between component size and power losses. Operation at higher switching frequencies allows the use of smaller inductor and capacitor values. Nevertheless, it is common to select lower frequency operation because a higher frequency also diminishes efficiency due to MOSFET gate charge losses. Additionally, low value inductors at higher frequencies result in higher ripple current, higher output voltage ripple, and lower efficiency at light load currents. The value of the oscillator resistor is designed to be linearly related to the switching period. If the designer prefers not to use Figure 20 to select the appropriate resistance, the following equation is a suitable alternative:

$$R_{OSC} = \frac{21700 - f_{SW}}{2.31 f_{SW}}$$

where:

R_{OSC} = oscillator resistor in $k\Omega$;

f_{SW} = switching frequency in kHz.

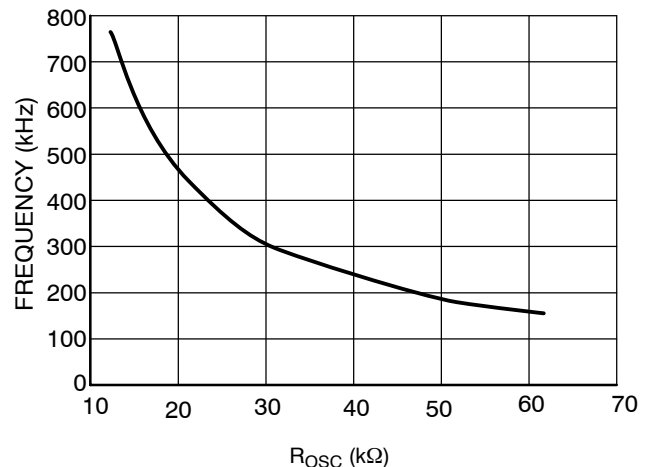


Figure 20. Switching Frequency vs. R_{osc}

Output Inductor Selection

The inductor should be selected based on the criteria of inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. There are many factors to consider in selecting inductors including cost, efficiency, EMI and ease of manufacture. The inductor must be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss.

There are a variety of materials and types of magnetic cores that could be used, such as ferrites, molypermalloy cores (MPP), and amorphous and powdered iron cores. Powdered iron cores are particularly suitable due to high saturation flux density and low loss at high frequencies, a distributed gap, and they produce very low EMI. The minimum value of inductance to prevent inductor saturation, or exceeding the rated FET current, can be calculated as follows:

$$L_{MIN} = \frac{(V_{IN(MIN)} - V_{OUT})V_{OUT}}{f_{SW} \times V_{IN(MIN)} \times I_{SW(MAX)}}$$

where:

L_{MIN} = minimum inductance value;
 $V_{IN(MIN)}$ = minimum design input voltage;
 V_{OUT} = output voltage;
 f_{SW} = switching frequency;
 $I_{SW(MAX)}$ = maximum design switch current.

The inductor ripple current can then be determined by:

$$\Delta I_L = \frac{V_{OUT} \times (1 - D)}{L \times f_{SW}}$$

where:

ΔI_L = inductor ripple current;
 V_{OUT} = output voltage;
 L = inductor value;
 D = duty cycle;
 f_{SW} = switching frequency.

After inductor selection, the designer can verify if the number of output capacitors will provide an acceptable output voltage ripple (1.0% of output voltage is common). The formula below is used;

$$\Delta I_L = \frac{\Delta V_{OUT}}{ESR_{MAX}}$$

where:

ESR_{MAX} = maximum allowable ESR;
 $\Delta V_{OUT} = 1.0\% \cdot V_{OUT}$ = maximum allowable output voltage ripple (budgeted by the designer);
 ΔI_L = inductor ripple current;
 V_{OUT} = output voltage.

Rearranging, we have:

$$ESR_{MAX} = \frac{\Delta V_{OUT}}{\Delta I_L}$$

The number of output capacitors is determined by:

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

where:

ESR_{CAP} = maximum ESR per capacitor
 (specified in manufacturer's data sheet).

The designer must also verify that the inductor value yields reasonable inductor peak and valley currents (the inductor current is a triangular waveform):

$$I_{L(PEAK)} = I_{OUT} + \frac{\Delta I_L}{2} \quad I_{L(VALLEY)} = I_{OUT} - \frac{\Delta I_L}{2}$$

where:

$I_{L(PEAK)}$ = inductor peak current;
 $I_{L(VALLEY)}$ = inductor valley current;
 I_{OUT} = load current;
 ΔI_L = inductor ripple current.

Output Capacitor Selection

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the regulator output voltage. Key specifications for output capacitors are ESR (Equivalent Series Resistance) and ESL (Equivalent Series Inductance). For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required. To determine the number of output capacitors the maximum voltage transient allowed during load transitions has to be specified. The output capacitors must hold the output voltage within these limits since the inductor current can not change at the required slew rate. The output capacitors must therefore have a very low ESL and ESR.

The voltage change during the load current transient is given by:

$$\Delta V_{OUT} = \Delta I_{OUT} \times \left(\frac{ESL}{\Delta t} + ESR + \frac{t_{TR}}{C_{OUT}} \right)$$

where:

$\Delta I_{OUT}/\Delta t$ = load current slew rate;
 ΔI_{OUT} = load transient;
 Δt = load transient duration time;
 ESL = Maximum allowable ESL including capacitors, circuit traces, and vias;
 ESR = Maximum allowable ESR including capacitors and circuit traces;
 t_{TR} = output voltage transient response time;
 C_{OUT} = output capacitance.

The designer must independently assign values for the change in output voltage due to ESR, ESL, and output capacitor discharging or charging. Empirical data indicates that most of the output voltage change (droop or spike, depending on the load current transition) results from the total output capacitor ESR.

Maximum allowable ESR can then be determined according to the formula:

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

where:

ΔV_{ESR} = change in output voltage due to ESR
(assigned by the designer)

Once the maximum allowable ESR is determined, the number of output capacitors can be calculated:

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

where:

ESR_{CAP} = maximum ESR per capacitor
(specified in manufacturer's data sheet);

ESR_{MAX} = maximum allowable ESR.

The actual output voltage deviation due to ESR can then be verified and compared to the value assigned by the designer:

$$\Delta V_{ESR} = \Delta I_{OUT} \times ESR_{MAX}$$

Similarly, the maximum allowable ESL is calculated from the following formula:

$$ESL_{MAX} = \frac{\Delta V_{ESL} \times \Delta t}{\Delta I}$$

Input Inductor Selection

A common requirement is that the buck controller must not disturb the input voltage. One method of achieving this is by using an input inductor and a bypass capacitor. The input inductor isolates the supply from the noise generated in the switching portion of the buck regulator and also limits the inrush current into the input capacitors during power up. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients. The worst case is when the load changes from no load to full load (load step), a condition under which the highest voltage change across the input capacitors is also seen by the input inductor. An input inductor successfully blocks the ripple current while placing the transient current requirements on the input bypass capacitor bank, which has to initially support the sudden load change. The minimum value for the input inductor is:

$$L_{IN} = \frac{\Delta V}{(di/dt)_{MAX}}$$

where:

L_{IN} = input inductor value;

ΔV = voltage seen by the input inductor during a full load swing;

$(di/dt)_{MAX}$ = maximum allowable input current slew rate.

The designer must select the LC filter pole frequency such that a minimum of 40 dB attenuation is obtained at the regulator switching frequency. The LC filter is a

double-pole network with a slope of -2.0, a roll-off rate of -40 dB/decade, and a corner frequency given by:

$$f_C = \frac{1}{2\pi \times \sqrt{LC}}$$

where:

L = input inductor;

C = input capacitor(s).

POWER FET SELECTION

FET Basics

The use of a MOSFET as a power switch is compelled by two reasons: 1) *high input impedance*; and 2) *fast switching times*. The electrical characteristics of a MOSFET are considered to be nearly those of a perfect switch. Control and drive circuitry power is therefore reduced. Because the input impedance is so high, it is voltage driven. The input of the MOSFET acts as if it were a small capacitor, which the driving circuit must charge at turn on. The lower the drive impedance, the higher the rate of rise of V_{GS} , and the faster the turn-on time. Power dissipation in the switching MOSFET consists of: (1) conduction losses, (2) leakage losses, (3) turn-on switching losses, (4) turn-off switching losses, and (5) gate-transitions losses. The latter three losses are all proportional to frequency. The most important aspect of FET performance is the Static Drain-to-Source On-Resistance ($R_{DS(ON)}$), which affects regulator efficiency and FET thermal management requirements. The On-Resistance determines the amount of current a FET can handle without excessive power dissipation that may cause overheating and potentially catastrophic failure. As the drain current rises, especially above the continuous rating, the On-Resistance also increases. Its positive temperature coefficient is between +0.6%/°C and +0.85%/°C. The higher the On-Resistance, the larger the conduction loss is. Additionally, the FET gate charge should be low in order to minimize switching losses and reduce power dissipation. Both logic level and standard FETs can be used. Voltage applied to the FET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the FET gates will be driven rail-to-rail due to overshoot caused by the capacitive load they present to the controller IC.

Switching (Upper) FET Selection

The designer must ensure that the total power dissipation in the FET switch does not cause the power component's junction temperature to exceed 150°C. The maximum RMS current through the switch can be determined by the following formula:

$$I_{RMS(H)} = \sqrt{\frac{I_L(PEAK)^2 + (I_L(PEAK) \times I_L(VALLEY)) + I_L(VALLEY)^2 \times D}{3}}$$

where:

$I_{RMS(H)}$ = maximum switching MOSFET RMS current;
 $I_{L(PEAK)}$ = inductor peak current;
 $I_{L(VALLEY)}$ = inductor valley current;
 D = duty cycle.

Once the RMS current through the switch is known, the switching MOSFET conduction losses can be calculated by:

$$P_{RMS(H)} = I_{RMS(H)}^2 \times R_{DS(ON)}$$

where:

$P_{RMS(H)}$ = switching MOSFET conduction losses;
 $I_{RMS(H)}$ = maximum switching MOSFET RMS current;
 $R_{DS(ON)}$ = FET drain-to-source on-resistance.

Upper MOSFET switching losses occur during MOSFET switch-on and switch-off, and can be calculated by:

$$P_{SWH} = P_{SWH(ON)} + P_{SWH(OFF)} \\ = \frac{V_{IN} \times I_{OUT} \times (t_{RISE} + t_{FALL})}{6T}$$

where:

$P_{SWH(ON)}$ = upper MOSFET switch-on losses;
 $P_{SWH(OFF)}$ = upper MOSFET switch-off losses;
 V_{IN} = input voltage;
 I_{OUT} = load current;
 T_{RISE} = MOSFET rise time (from FET manufacturer's switching characteristics performance curve);
 T_{FALL} = MOSFET fall time (from FET manufacturer's switching characteristics performance curve);
 $T = 1/f_{SW}$ = period.

The total power dissipation in the switching MOSFET can then be calculated as:

$$P_{HFET(TOTAL)} = P_{RMS(H)} + P_{SWH(ON)} + P_{SWH(OFF)}$$

where:

$P_{HFET(TOTAL)}$ = total switching (upper) MOSFET losses;
 $P_{RMS(H)}$ = upper MOSFET switch conduction Losses;
 $P_{SWH(ON)}$ = upper MOSFET switch-on losses;
 $P_{SWH(OFF)}$ = upper MOSFET switch-off losses.

Once the total power dissipation in the switching FET is known, the maximum FET switch junction temperature can be calculated:

$$T_J = T_A + [P_{HFET(TOTAL)} \times R_{\theta JA}]$$

where:

T_J = FET junction temperature;
 T_A = ambient temperature;
 $P_{HFET(TOTAL)}$ = total switching (upper) FET losses;
 $R_{\theta JA}$ = upper FET junction-to-ambient thermal resistance.

Synchronous (Lower) FET Selection

The switch conduction losses for the lower FET are calculated as follows:

$$P_{RMS(L)} = I_{RMS}^2 \times R_{DS(ON)} \\ = [I_{OUT} \times \sqrt{(1 - D)}]^2 \times R_{DS(ON)}$$

where:

$P_{RMS(L)}$ = lower MOSFET conduction losses;
 I_{OUT} = load current;
 D = Duty Cycle;
 $R_{DS(ON)}$ = lower FET drain-to-source on-resistance.

The synchronous MOSFET has no switching losses, except for losses in the internal body diode, because it turns on into near zero voltage conditions. The MOSFET body diode will conduct during the non-overlap time and the resulting power dissipation (neglecting reverse recovery losses) can be calculated as follows:

$$P_{SWL} = V_{SD} \times I_{LOAD} \times \text{non-overlap time} \times f_{SW}$$

where:

P_{SWL} = lower FET switching losses;
 V_{SD} = lower FET source-to-drain voltage;
 I_{LOAD} = load current;
Non-overlap time = GATE(L)-to-GATE(H) or GATE(H)-to-GATE(L) delay (from NCP5425 data sheet Electrical Characteristics section);
 f_{SW} = switching frequency.

The total power dissipation in the synchronous (lower) MOSFET can then be calculated as:

$$P_{LFET(TOTAL)} = P_{RMS(L)} + P_{SWL}$$

where:

$P_{LFET(TOTAL)}$ = Synchronous (lower) FET total losses;
 $P_{RMS(L)}$ = Switch Conduction Losses;
 P_{SWL} = Switching losses.

Once the total power dissipation in the synchronous FET is known the maximum FET switch junction temperature can be calculated:

$$T_J = T_A + [P_{LFET(TOTAL)} \times R_{\theta JA}]$$

where:

T_J = MOSFET junction temperature;
 T_A = ambient temperature;
 $P_{LFET(TOTAL)}$ = total synchronous (lower) FET losses;
 $R_{\theta JA}$ = lower FET junction-to-ambient thermal resistance.

Control IC Power Dissipation

The power dissipation of the IC varies with the MOSFETs used, VCC, and the NCP5425 operating frequency. The average MOSFET gate charge current typically dominates the control IC power dissipation, and is given by:

$$P_{\text{CONTROL(IC)}} = I_{\text{CC1}}V_{\text{CC1}} + I_{\text{BST}}V_{\text{BST}} \\ + P_{\text{GATE(H)1}} + P_{\text{GATE(L)1}} \\ + P_{\text{GATE(H)2}} + P_{\text{GATE(L)2}}$$

where:

$P_{\text{CONTROL(IC)}}$ = control IC power dissipation;
 I_{CC1} = IC quiescent supply current;
 V_{CC1} = IC supply voltage;
 $P_{\text{GATE(H)}}$ = upper MOSFET gate driver (IC) losses;
 $P_{\text{GATE(L)}}$ = lower MOSFET gate driver (IC) losses.

The upper (switching) MOSFET gate driver (IC) losses are given by:

$$P_{\text{GATE(H)}} = Q_{\text{GATE(H)}} \times f_{\text{SW}} \times V_{\text{BST}}$$

where:

$P_{\text{GATE(H)}}$ = upper MOSFET gate driver (IC) losses;
 $Q_{\text{GATE(H)}}$ = total upper MOSFET gate charge at VCC;
 f_{SW} = switching frequency.

The lower (synchronous) MOSFET gate driver (IC) losses are:

$$P_{\text{GATE(L)}} = Q_{\text{GATE(L)}} \times f_{\text{SW}} \times V_{\text{CC}}$$

where:

$P_{\text{GATE(L)}}$ = lower MOSFET gate driver (IC) losses;
 $Q_{\text{GATE(L)}}$ = total lower MOSFET gate charge at VCC;
 f_{SW} = switching frequency.

The junction temperature of the control IC is primarily a function of the PCB layout, since most of the heat is removed through the traces connected to the pins of the IC.

CURRENT SENSING AND CURRENT SHARING

Current Sharing Errors

The three main errors in current are from board layout imbalances, inductor mismatch, and input offsets in the error amplifiers. The first two sources of error can be controlled through careful component selection and good layout practice. With a 4.0 mΩ (parasitic winding resistance) inductor, for example, one mV of input offset error will represent 0.25 A of measurement error. One way to diminish this effect is to use higher resistance inductors, but the penalty is higher power losses in the inductors.

Current Limiting Options

The current supplied to the load can be sensed using the IS+ and IS− pins. These pins sense a voltage, proportional to the output current, and compare it to a fixed internal voltage threshold. When the differential voltage exceeds 70 mV, the internal overcurrent protection system goes into a cycle-by-cycle limiting mode. Two methods for sensing the current are available.

Sense Resistor

A sense resistor can be added in series with the inductor. When the voltage drop across the sense resistor exceeds the internal voltage threshold of 70 mV, a limit condition is set. The sense resistor value is calculated by:

$$R_{\text{SENSE}} = \frac{0.070 \text{ V}}{I_{\text{LIMIT}}}$$

In a high current supply, the sense resistor will be a very low value, typically less than 10 mΩ. Such a resistor can be either a discrete component or a PCB trace. The resistance of a discrete component can be more precise than a PCB trace, but the cost is also greater. Setting the current limit using an external sense resistor is very precise because all the values can be designed to specific tolerances. However, the disadvantage of using a sense resistor is its additional constant power loss and heat generation. Trace resistance can vary as much as ±10% due to copper plating variations.

Inductor ESR

Another means of sensing current is to use the intrinsic resistance of the inductor. A model of an inductor reveals that the windings have an effective series resistance (ESR). The voltage drop across the inductor ESR can be measured with a simple parallel circuit: an RC integrator. If the value of RS1 and C are chosen such that:

$$\frac{L}{\text{ESR}} = R_{\text{S1}}C$$

then the voltage measured across the capacitor C will be:

$$V_C = \text{ESR} \times I_{\text{LIM}}$$

Inductor Sensing Component Selection

Select the capacitor C first. A value of 0.1 μF is recommended. The value of RS1 can be calculated by:

$$R_{\text{S1}} = \frac{L}{\text{ESR} \times C}$$

Typical values for inductor ESR range in the low milliohms; consult manufacturer's data sheets for specific values. Selection of components at these values will result in a current limit of:

$$I_{\text{LIM}} = \frac{0.070 \text{ V}}{\text{ESR}}$$

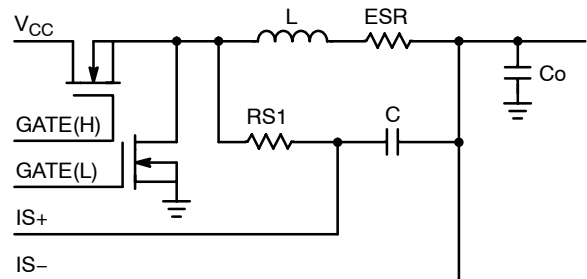


Figure 21. Inductor ESR Current Sensing

Given an ESR value of $3.5\text{ m}\Omega$, the current limit becomes 20 A. If an increased current limit is required, a resistor divider can be added (see Figure 18). Advantages of setting the current limit by using the winding resistance of the inductor (relative to a sense resistor) are higher efficiency and lower heat generation. The tolerance of the inductor ESR must be factored into the design of the current limit. Finally, one or two more components are required for this approach than with resistor sensing.

Selecting and Configuring Current Sharing for a 2 Phase Single Output Application

When the two controllers are connected as a single output two phase Buck Converter, they are in a Master–Slave configuration. The Slave controller on the right side of Figure 16 tries to follow information provided by the Master controller, on the left. This circuit uses inductor current sensing, in which the parasitic resistances (LSR) of the controllers' output chokes are used as current sensing elements. On the Slave side (Controller Two), both Error Amplifier inputs are brought to external pins so the reference is available. The RC network in parallel with the output inductor on the Master side (Controller One) generates the reference for the Slave. Current information from the Slave is fed back to the error amplifier's inverting input. In this configuration, the Slave tries to adjust its current to match the current information fed to its reference input from the Master Controller. If 50–50 current sharing is needed, then Figure 8a is used for both sides to generate the reference and the inverting signals. The values for both sides should be calculated with the following equation:

$$R1 = \frac{L_x}{C1 \cdot R_x}, \text{ where,}$$

L_x = Inductor value, both controllers should use the same inductor.

R_x = Internal resistance of L_x from the inductor data sheet.

$C1$ = Select a value such that $R1$ is less than $15\text{ K}\Omega$.

With the RC time constant selected to equal the L_x/R_x time constant, the voltage across the capacitor will be equal to the voltage drop across the internal resistance of the inductor. For proper sharing, the inductors on both Master and Slave side should be the identical.

If a current share ratio other than 50–50 is desired, inductor sense resistor network selection is a three step process:

1. Decide how the total load current will be budgeted between the two controllers.
2. Calculate the value of $R1$ for the controller with the lesser current share.
3. Calculate the current sense resistor network (2 resistors) for the controller with the greater current share.

In the two examples that follow, the inductor sense resistors are designated $R1$, $R2$, and $R3$, as depicted in Figures 22 and 23.

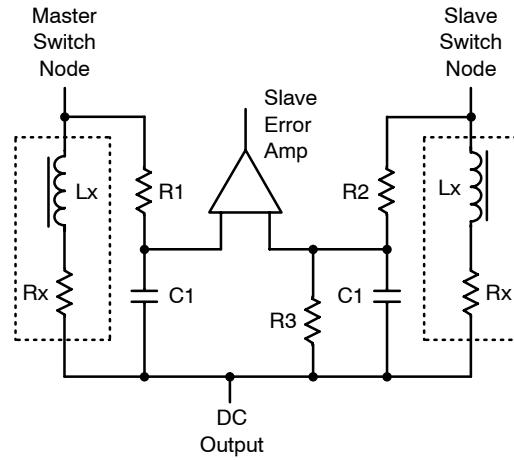


Figure 22. 40%/60% Current Sharing

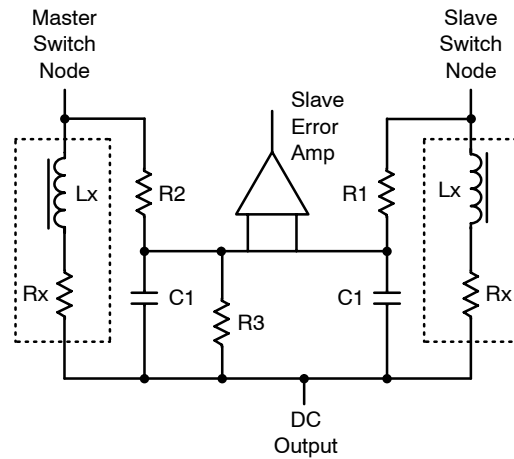


Figure 23. 66.7%/33.3% Current Sharing

Example 1

Assume we have elected to source 40% of the output current from the master controller, and 60% from the Slave. Figure 22 shows the configuration of the inductor sense networks and Slave error amplifier. The ratio of Slave-to-Master load current is 60%/40%, or 1.5:1. $R2$ and $R3$ must be chosen to satisfy two conditions:

A parallel equivalent resistance equal to $R1$, and,

A ratio such that the drop across the parasitic resistance of the Slave inductor is 1.5 times the drop across the parasitic resistance of the Master inductor when the inputs to the Slave error amplifier are equal (assumes the inductors are identical). The optimum value of $R1$ is described by the equation:

$$R1 = L_x / (C1 \cdot R_x)$$

The values of R2 and R3 can be found by solving two simultaneous equations:

$$R2 = R3/2$$

$$R1 = (R2 * R3)/(R2 + R3)$$

Solving for R2 and R3 yields:

$$R2 = 1.5R1$$

$$R3 = 3R1$$

Example 2

Assume we have elected to source 66.7% output current from the Master controller, and 33.3% from the Slave. Figure 23 shows the configuration of the inductor sense networks and Slave error amplifier for this case. The ratio of Master-to-Slave load current is equal to 66.7%/33.3%, or 2:1. Therefore R2 and R3 must be chosen to satisfy two conditions:

A parallel equivalent resistance equal to R1, and,

A ratio such that the drop across the parasitic resistance of the Master inductor is 2 times the drop across the parasitic resistance of the Slave inductor when the inputs to the Slave error amplifier are equal (assumes the inductors are identical). The optimum value of R1 is described by the equation:

$$R1 = Lx/(C1 * Rx)$$

The values of R2 and R3 can be found by solving two simultaneous equations:

$$R2 = R3$$

$$R1 = (R2 * R3)/(R2 + R3)$$

Solving for R2 and R3 yields:

$$R2 = 2R1$$

$$R3 = 2R1$$

Note that the Mode pin must be floating for a two-phase, single output design. This disables the internal Error Amplifier Reference clamp, and increases its common mode range.

No Load Zero Balance

To improve current matching, a low pass filter can be inserted between the Master controller inductor sensing RC network and the Slave controller Vref2 input pin (see Figure 24). This will attenuate the amplitude of the out-of-phase ripple current signal superimposed on the DC current signal, providing a smoother Slave Error Amplifier reference input.

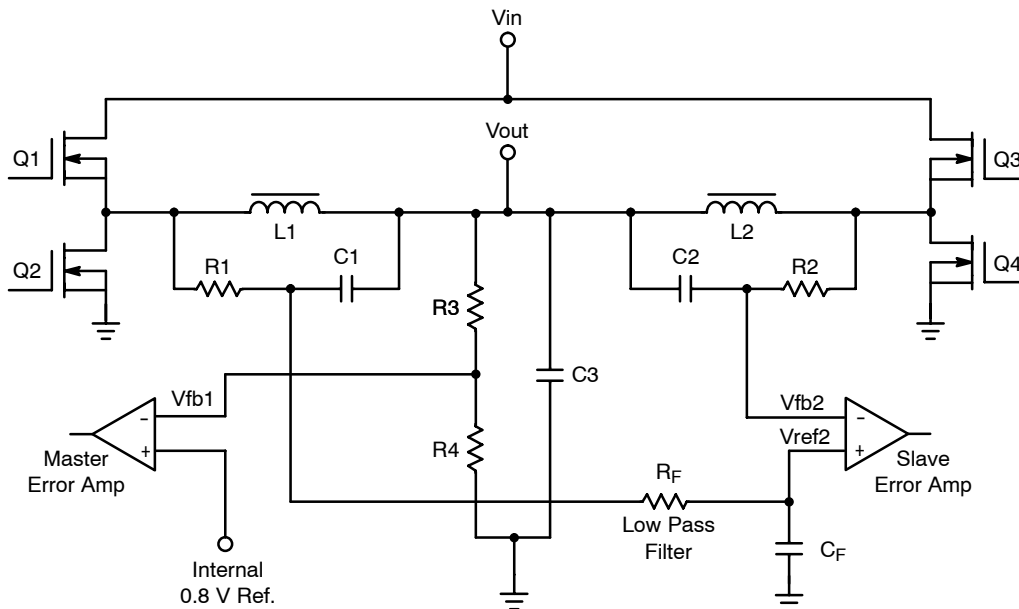


Figure 24. Addition of a Low Pass Filter to the Current Sense Reference Input

With the value of Rf set to approximately two times the value of R1, Cf can be calculated as follows:

$$Cf = 1/(2\pi \cdot f \cdot Rf), \text{ where :}$$

f = operating frequency of the controller

When a filter is added, the response delay introduced by the RC time constant must be considered.

Configuring a Dual Output Application

To configure the NCP5425 for a dual output application:

- The Mode pin must be grounded
- An external voltage reference must be provided for Controller 2, via the Vref2 pin

Grounding the Mode pin enables an internal clamp to limit the Comp 2 voltage excursions during overcurrent faults. Without this clamp, the output voltage (Vout1 and Vout2) can overshoot the regulated output voltages when the fault is removed. For a single output two-phase application the Mode pin must be floating, which disables the clamp and permits a larger current-sharing reference voltage range. The Comp1 pin is always clamped, because it is regulated to a fixed internal voltage (0.8 V).

The simplest way to provide a Controller 2 reference is by using the Controller 1 feedback voltage. This will provide a 0.8 V reference for regulation, and also causes the Controller 2 output to track the Controller 1 output during transients. With a voltage reference established and the Mode pin floating, Controller 2 can function as an independent Buck regulator.

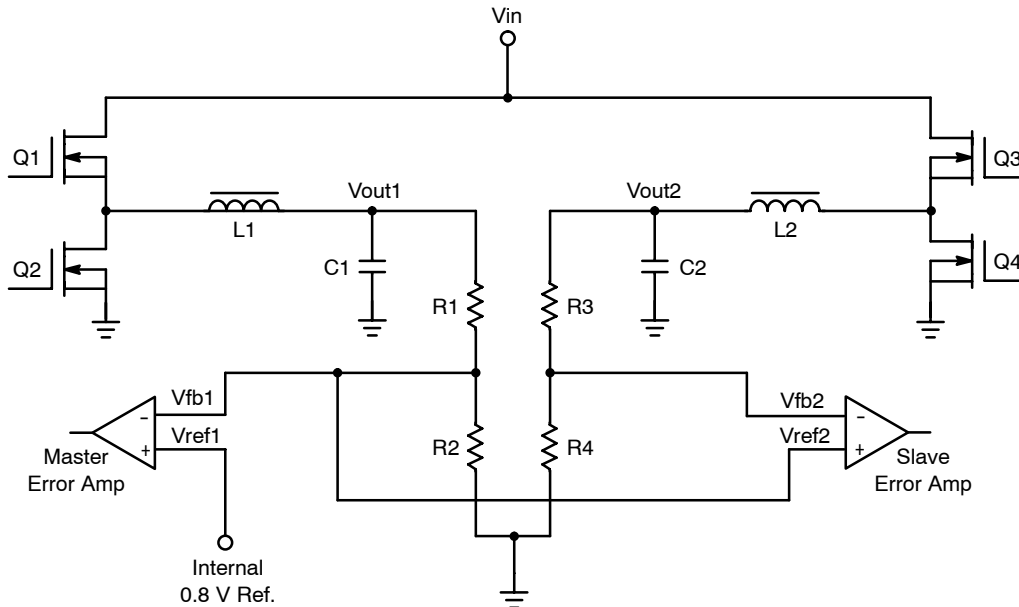


Figure 25. Dual Output Configuration

Adding External Slope Compensation

Today's voltage regulators are expected to meet very stringent load transient requirements. One of the key factors in achieving tight dynamic voltage regulation is low ESR. Low ESR at the regulator output results in low output voltage ripple. The consequence is, however, that very little voltage ramp exists at the control IC feedback pin (VFB), resulting in increased regulator sensitivity to noise and the potential for loop instability. In applications where the internal slope compensation is insufficient, the performance of the NCP5425-based regulator can be improved through the addition of a fixed amount of external slope compensation at the output of the PWM Error Amplifier (the COMP pin) during the regulator off-time. Referring to Figure 18, the amount of voltage ramp at the COMP pin is dependent on the gate voltage of the lower (synchronous) FET and the value of resistor divider formed by R1 and R2.

$$V_{SLOPECOMP} = V_{GATE(L)} \times \left(\frac{R_2}{R_1 + R_2} \right) \times (1 - e^{-\frac{t}{\tau}})$$

where:

- $V_{SLOPECOMP}$ = amount of slope added;
- $V_{GATE(L)}$ = lower MOSFET gate voltage;
- R1, R2 = voltage divider resistors;
- $t = t_{ON}$ or t_{OFF} (switch off-time);

$\tau = RC$ constant determined by C1 and the parallel combination of R1, R2 neglecting the low driver output impedance.

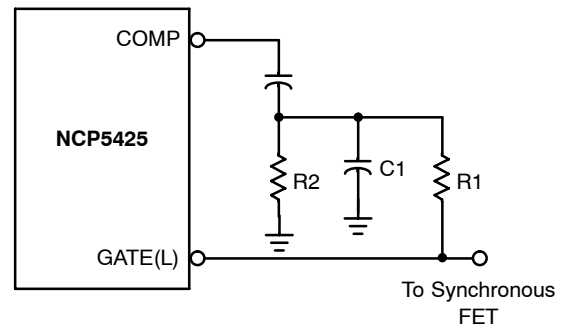


Figure 26. RC Filter Provides the Proper Voltage Ramp at the Beginning of each On-Time Cycle

The artificial voltage ramp created by the slope compensation scheme results in improved control loop stability provided that the RC filter time constant is smaller than the off-time cycle duration (time during which the lower MOSFET is conducting). It is important that the series combination of R1 and R2 is high enough in resistance to avoid loading the GATE(L) pin. Also, C1 should be very small (less than a few nF) to avoid heating the part.

EMI MANAGEMENT

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise during normal operation. When designing for compliance with EMI/EMC regulations, additional components may be necessary to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power components to minimize routing distance will also help to reduce emissions.

LAYOUT GUIDELINES

When laying out a buck regulator on a printed circuit board, the following checklist should be used to ensure proper operation of the NCP5425.

1. Rapid changes in voltage across parasitic capacitors and abrupt changes in current in parasitic inductors are major concerns.
2. Keep high currents out of sensitive ground connections.
3. Avoid ground loops as they pick up noise. Use star or single point grounding.
4. For high power buck regulators on double-sided PCB's a single ground plane (usually the bottom) is recommended.
5. Even though double sided PCB's are usually sufficient for a good layout, four-layer PCB's are the optimum approach to reducing susceptibility to noise. Use the two internal layers as the power and GND planes, the top layer for power connections and component vias, and the bottom layers for the noise sensitive traces.
6. Keep the inductor switching node small by placing the output inductor, switching and synchronous FETs close together.
7. The MOSFET gate traces to the IC must be short, straight, and wide as possible.
8. Use fewer, but larger output capacitors, keep the capacitors clustered, and use multiple layer traces with wide, thick copper to keep the parasitic resistance low.
9. Place the switching MOSFET as close to the input capacitors as possible.
10. Place the output capacitors as close to the load as possible.
11. Place the COMP capacitor as close as possible to the COMP pin.
12. Connect the filter components of pins ROSC, VFB, VOUT, and COMP, to the GND pin with a single trace, and connect this local GND trace to the output capacitor GND.
13. Place the VCC bypass capacitors as close as possible to the IC.
14. Place the ROSC resistor as close as possible to the ROSC pin.
15. Assign the output with lower duty cycle to channel 2, which has inherently better noise immunity.

NCV33163

2.5 A, Step-Up/Down/ Inverting Switching Regulators

The NCV33163 series are monolithic power switching regulators that contain the primary functions required for dc-to-dc converters. This series is specifically designed to be incorporated in step-up, step-down, and voltage-inverting applications with a minimum number of external components.

These devices consist of two high gain voltage feedback comparators, temperature compensated reference, controlled duty cycle oscillator, driver with bootstrap capability for increased efficiency, and a high current output switch. Protective features consist of cycle-by-cycle current limiting, and internal thermal shutdown. Also included is a low voltage indicator output designed to interface with microprocessor based systems.

These devices are contained in a 16 pin dual-in-line heat tab plastic package for improved thermal conduction.

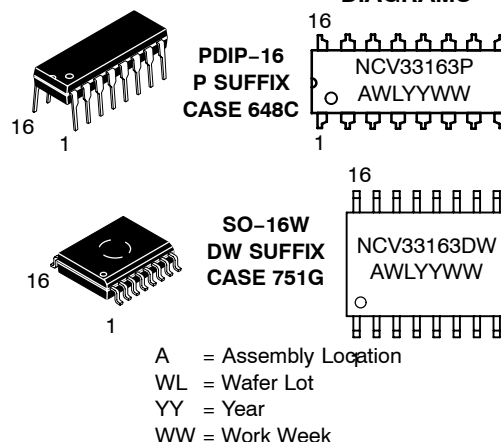
- Output Switch Current in Excess of 2.0 A
- Operation from 2.5 V to 60 V_{OC} Input
- Low Standby Current
- Precision 2% Reference
- Controlled Duty Cycle Oscillator
- Driver with Bootstrap Capability for Increased Efficiency
- Cycle-by-Cycle Current Limiting
- Internal Thermal Shutdown Protection
- Low Voltage Indicator Output for Direct Microprocessor Interface
- Heat Tab Power Package
- Moisture Sensitivity Level (MSL) Equals 1
- NCV Prefix, for Automotive and Other Applications Requiring Site and Change Control



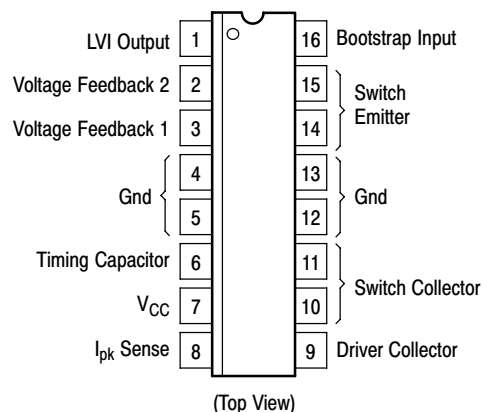
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MARKING DIAGRAMS



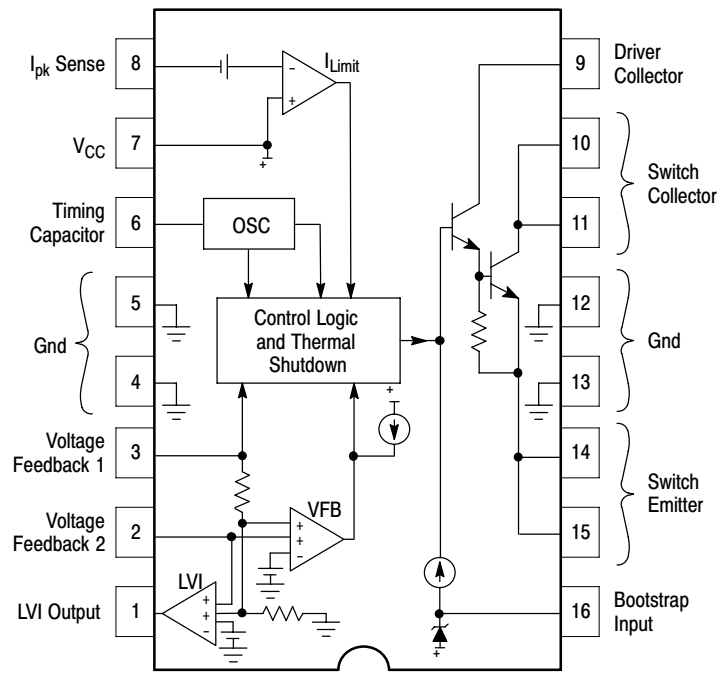
PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping
NCV33163DW	SO-16W	47 Units/Rail
NCV33163DWR2	SO-16W	1000 Tape & Reel
NCV33163P	PDIP-16	25 Units/Rail

NCV33163



(Bottom View)

This device contains 114 active transistors.

Figure 1. Representative Block Diagram

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	60	V
Switch Collector Voltage Range	$V_{C(switch)}$	-1.0 to +60	V
Switch Emitter Voltage Range	$V_{E(switch)}$	-2.0 to $V_{C(switch)}$	V
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	60	V
Switch Current (Note 2)	I_{SW}	2.5	A
Driver Collector Voltage	$V_{C(driver)}$	-1.0 to +60	V
Driver Collector Current	$I_{C(driver)}$	150	mA
Bootstrap Input Current Range (Note 2)	I_{BS}	-100 to +100	mA
Current Sense Input Voltage Range	$V_{Ipk (Sense)}$	$(V_{CC}-7.0)$ to $(V_{CC}+1.0)$	V
Feedback and Timing Capacitor Input Voltage Range	V_{in}	-1.0 to +7.0	V
Low Voltage Indicator Output Voltage Range	$V_{C(LVI)}$	-1.0 to +60	V
Low Voltage Indicator Output Sink Current	$I_{C(LVI)}$	10	mA
Thermal Characteristics			°C/W
P Suffix, Dual-In-Line Case 648C			
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	80	
Thermal Resistance, Junction-to-Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	15	
DW Suffix, Surface Mount Case 751G			
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	94	
Thermal Resistance, Junction-to-Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	18	
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	-40 to +115	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NCV33163

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, Pin 16 = V_{CC} , $C_T = 620\text{ pF}$, for typical values $T_A = 25^\circ\text{C}$, for min/max values $T_A = -40^\circ\text{C}$ to $+115^\circ\text{C}$.)

Characteristic	Symbol	Min	Typ	Max	Unit

OSCILLATOR

Frequency $T_A = 25^\circ\text{C}$ Total Variation over $V_{CC} = 2.5\text{ V}$ to 60 V , and Temperature	f_{OSC}	46 45	50 –	54 55	kHz
Charge Current	I_{chg}	–	225	–	μA
Discharge Current	I_{dischg}	–	25	–	μA
Charge to Discharge Current Ratio	$I_{\text{chg}}/I_{\text{dischg}}$	8.0	9.0	10	–
Sawtooth Peak Voltage	$V_{\text{OSC(P)}}$	–	1.25	–	V
Sawtooth Valley Voltage	$V_{\text{OSC(V)}}$	–	0.55	–	V

FEEDBACK COMPARATOR 1

Threshold Voltage $T_A = 25^\circ\text{C}$ Line Regulation ($V_{CC} = 2.5\text{ V}$ to 60 V , $T_A = 25^\circ\text{C}$) Total Variation over Line, and Temperature	$V_{\text{th(FB1)}}$	4.9 – 4.85	5.05 0.008 –	5.2 0.03 5.25	V %/V V
Input Bias Current ($V_{\text{FB1}} = 5.05\text{ V}$)	$I_{\text{IB(FB1)}}$	–	100	200	μA

FEEDBACK COMPARATOR 2

Threshold Voltage $T_A = 25^\circ\text{C}$ Line Regulation ($V_{CC} = 2.5\text{ V}$ to 60 V , $T_A = 25^\circ\text{C}$) Total Variation over Line, and Temperature	$V_{\text{th(FB2)}}$	1.225 – 1.213	1.25 0.008 –	1.275 0.03 1.287	V %/V V
Input Bias Current ($V_{\text{FB2}} = 1.25\text{ V}$)	$I_{\text{IB(FB2)}}$	– 0.4	0	0.4	μA

CURRENT LIMIT COMPARATOR

Threshold Voltage $T_A = 25^\circ\text{C}$ Total Variation over $V_{CC} = 2.5\text{ V}$ to 60 V , and Temperature	$V_{\text{th(Ipk Sense)}}$	– 230	250 –	– 270	mV
Input Bias Current ($V_{\text{Ipk (Sense)}} = 15\text{ V}$)	$I_{\text{IB(sense)}}$	–	1.0	20	μA

DRIVER AND OUTPUT SWITCH (Note 3)

Sink Saturation Voltage ($I_{\text{SW}} = 2.5\text{ A}$, Pins 14, 15 grounded) Non-Darlington Connection ($R_{\text{Pin 9}} = 110\ \Omega$ to V_{CC} , $I_{\text{SW}}/I_{\text{DRV}} \approx 20$) Darlington Connection (Pins 9, 10, 11 connected)	$V_{\text{CE(sat)}}$	– –	0.6 1.0	1.0 1.4	V
Collector Off-State Leakage Current ($V_{\text{CE}} = 60\text{ V}$)	$I_{\text{C(off)}}$	–	0.02	100	μA
Bootstrap Input Current Source ($V_{\text{BS}} = V_{CC} + 5.0\text{ V}$)	$I_{\text{source(DRV)}}$	0.5	2.0	4.0	mA
Bootstrap Input Zener Clamp Voltage ($I_Z = 25\text{ mA}$)	V_Z	$V_{CC} + 6.0$	$V_{CC} + 7.0$	$V_{CC} + 9.0$	V

LOW VOLTAGE INDICATOR

Input Threshold (V_{FB2} Increasing)	V_{th}	1.07	1.125	1.18	V
Input Hysteresis (V_{FB2} Decreasing)	V_{H}	–	15	–	mV
Output Sink Saturation Voltage ($I_{\text{sink}} = 2.0\text{ mA}$)	$V_{\text{OL(LVI)}}$	–	0.15	0.4	V
Output Off-State Leakage Current ($V_{\text{OH}} = 15\text{ V}$)	I_{OH}	–	0.01	5.0	μA

TOTAL DEVICE

Standby Supply Current ($V_{CC} = 2.5\text{ V}$ to 60 V , Pin 8 = V_{CC} , Pins 6, 14, 15 = Gnd, remaining pins open)	I_{CC}	–	6.0	10	mA

- This device series contains ESD protection and exceeds the following tests:
Human Body Model 1500 V per MIL-STD-883, Method 3015.
Machine Model Method 150 V.
- Maximum package power dissipation limits must be observed.
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

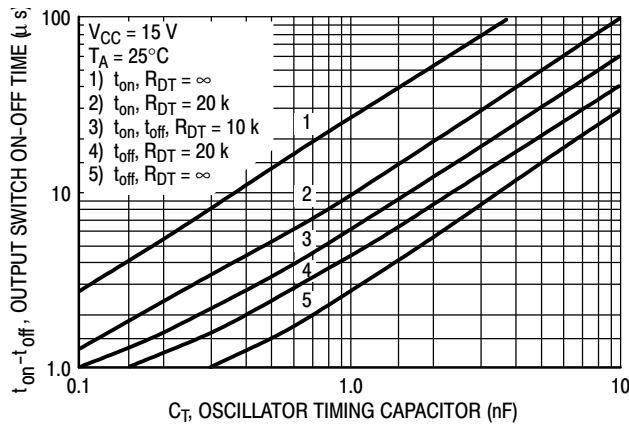


Figure 2. Output Switch On-Off Time versus Oscillator Timing Capacitor

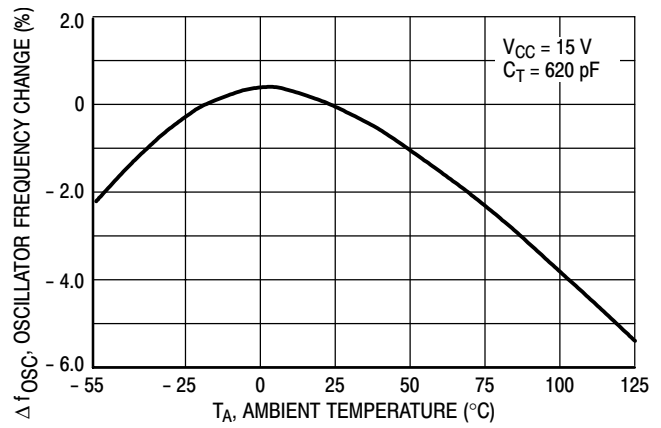


Figure 3. Oscillator Frequency Change versus Temperature

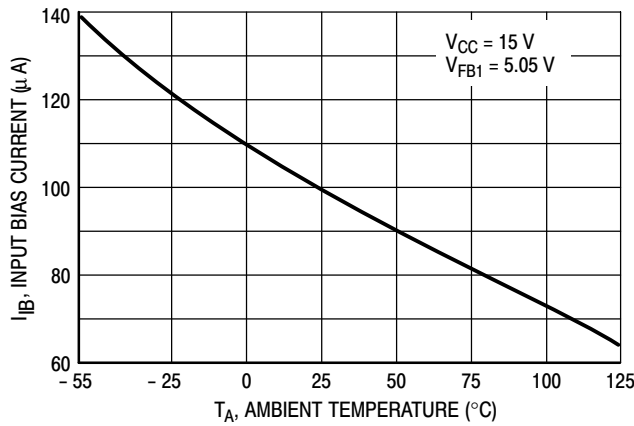


Figure 4. Feedback Comparator 1 Input Bias Current versus Temperature

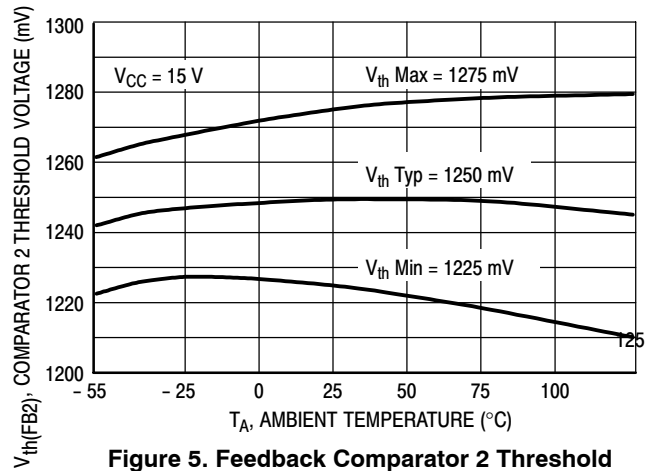


Figure 5. Feedback Comparator 2 Threshold Voltage versus Temperature

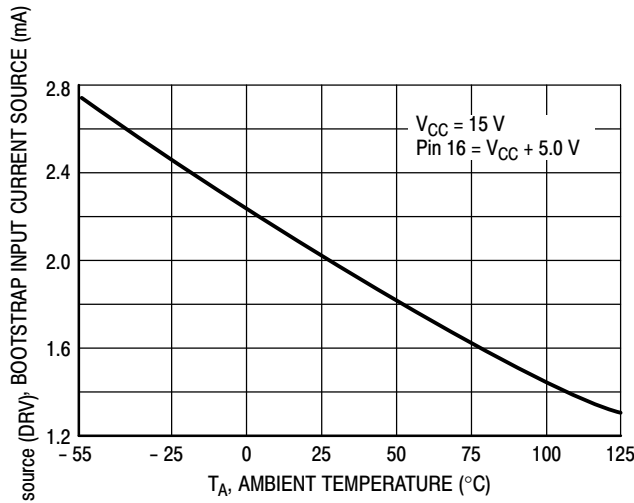


Figure 6. Bootstrap Input Current Source versus Temperature

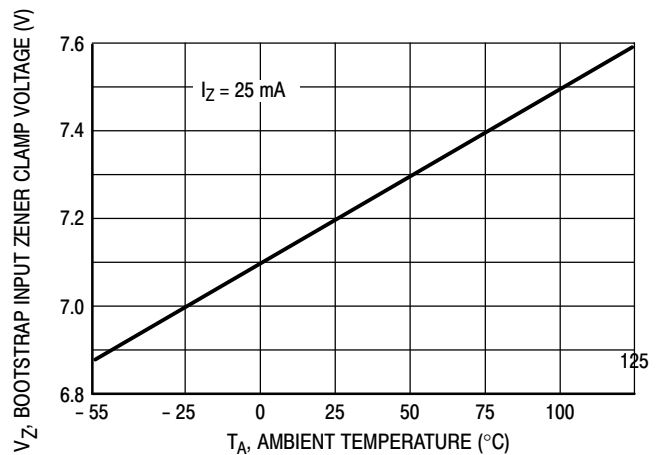


Figure 7. Bootstrap Input Zener Clamp Voltage versus Temperature

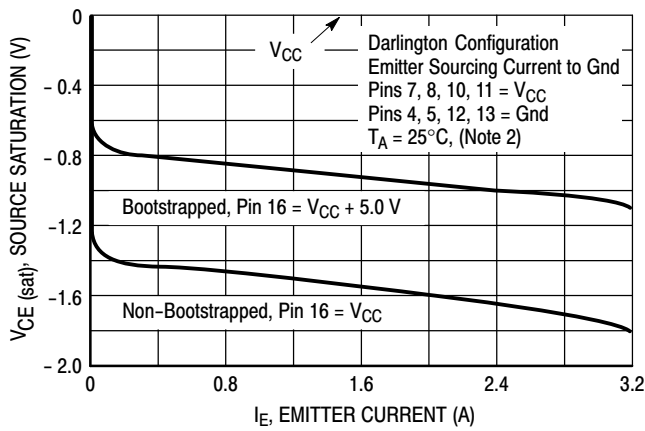


Figure 8. Output Switch Source Saturation versus Emitter Current

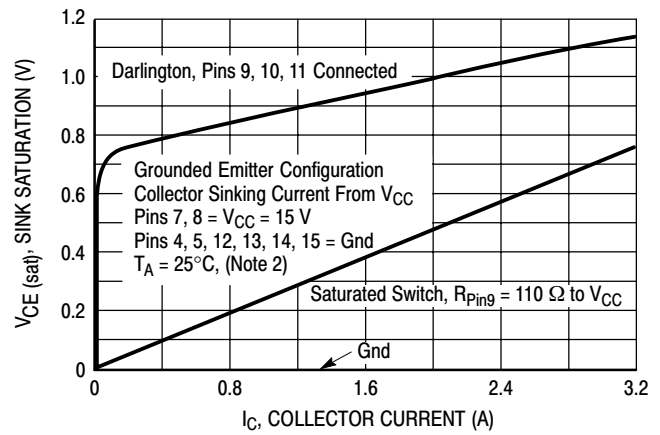


Figure 9. Output Switch Sink Saturation versus Collector Current

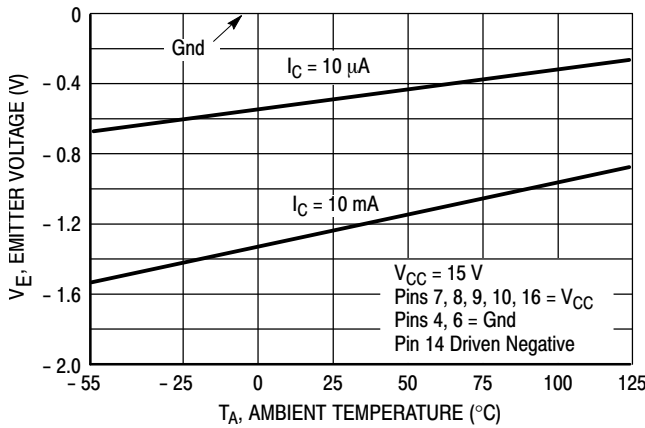


Figure 10. Output Switch Negative Emitter Voltage versus Temperature

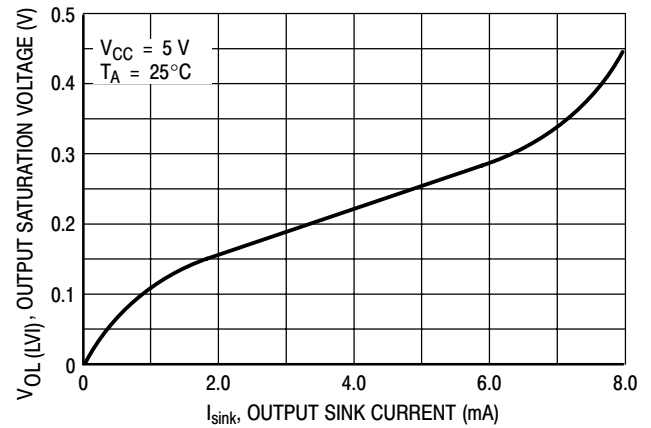


Figure 11. Low Voltage Indicator Output Sink Saturation Voltage versus Sink Current

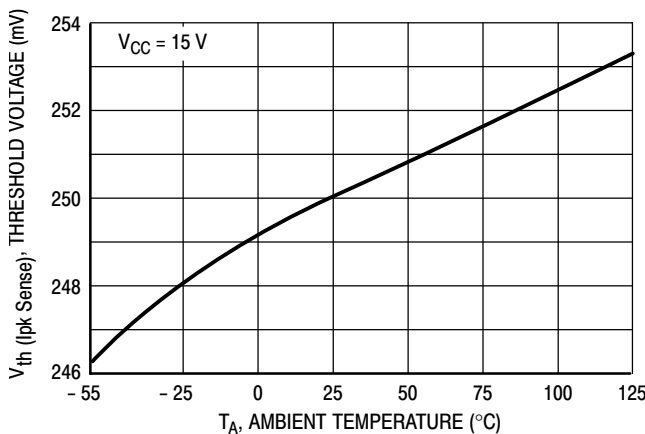


Figure 12. Current Limit Comparator Threshold Voltage versus Temperature

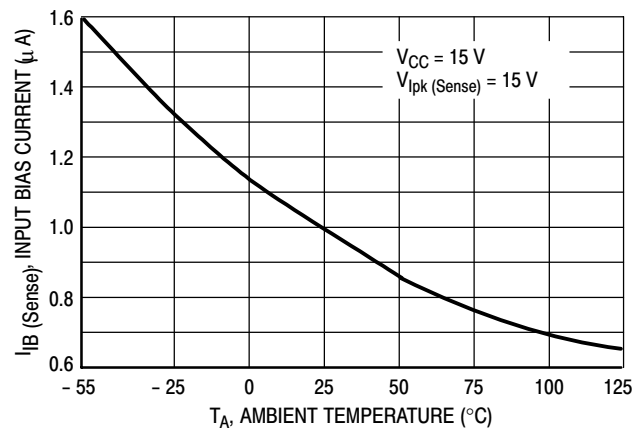


Figure 13. Current Limit Comparator Input Bias Current versus Temperature

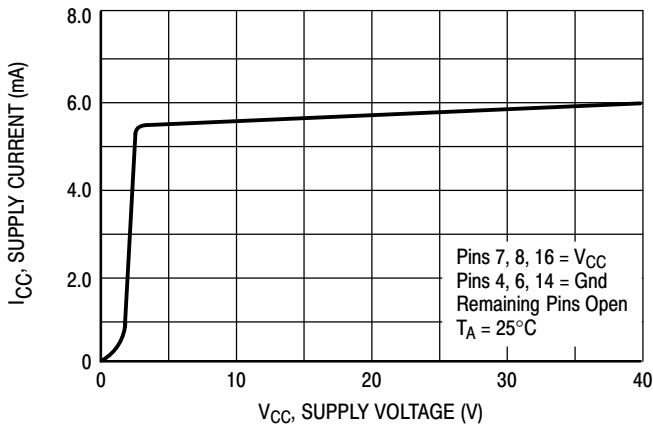


Figure 14. Standby Supply Current versus Supply Voltage

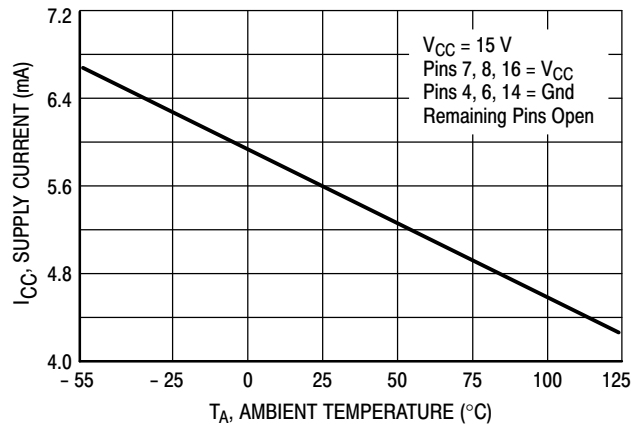


Figure 15. Standby Supply Current versus Temperature

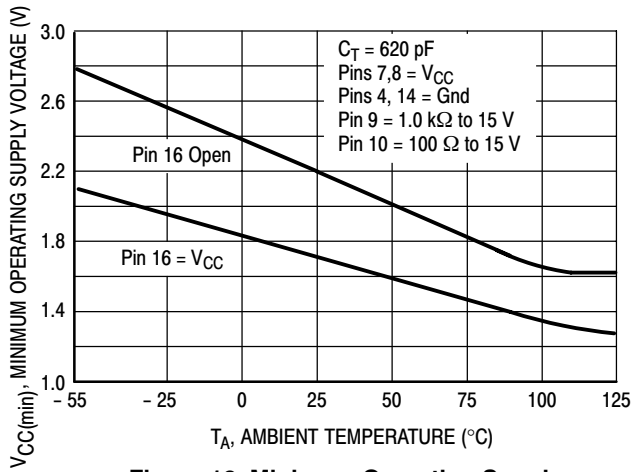


Figure 16. Minimum Operating Supply Voltage versus Temperature

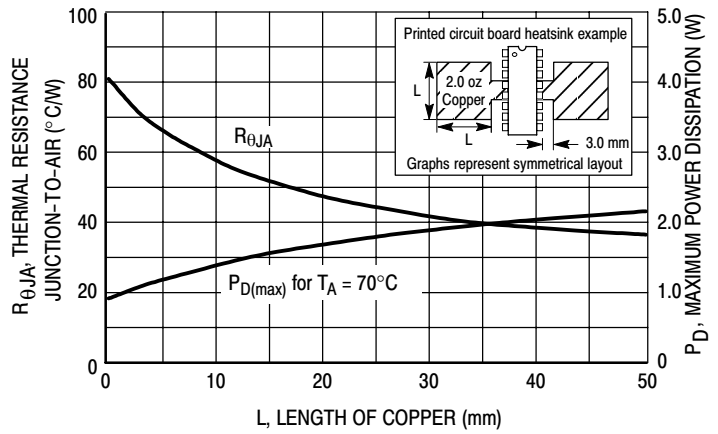


Figure 17. P Suffix (DIP-16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

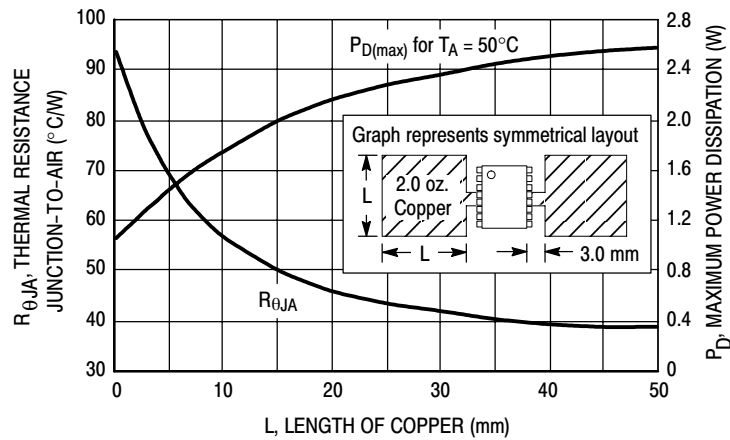


Figure 18. DW Suffix (SOP-16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

NCV33163

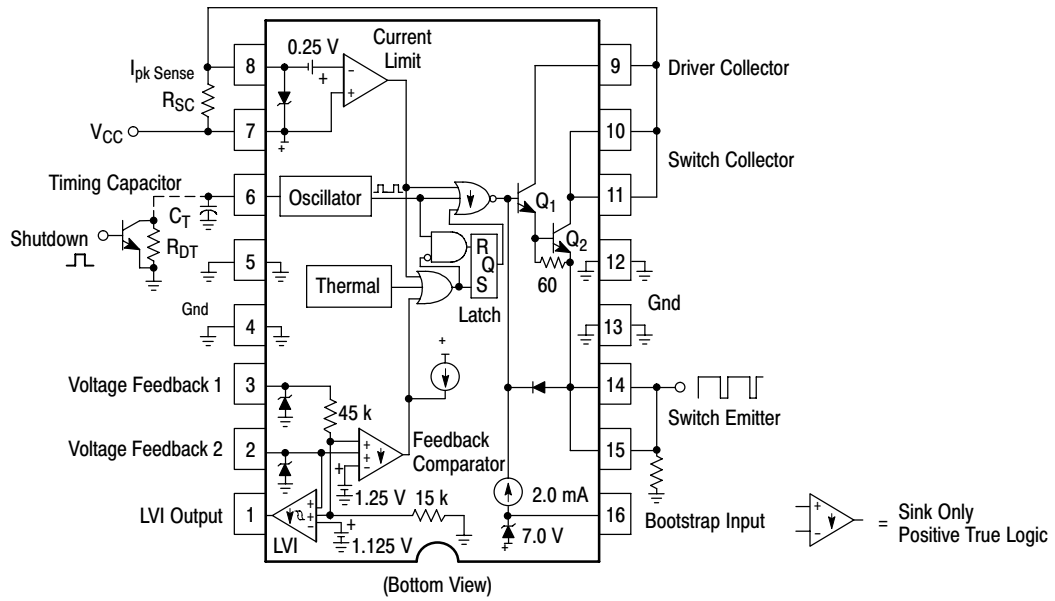


Figure 19. Representative Block Diagram

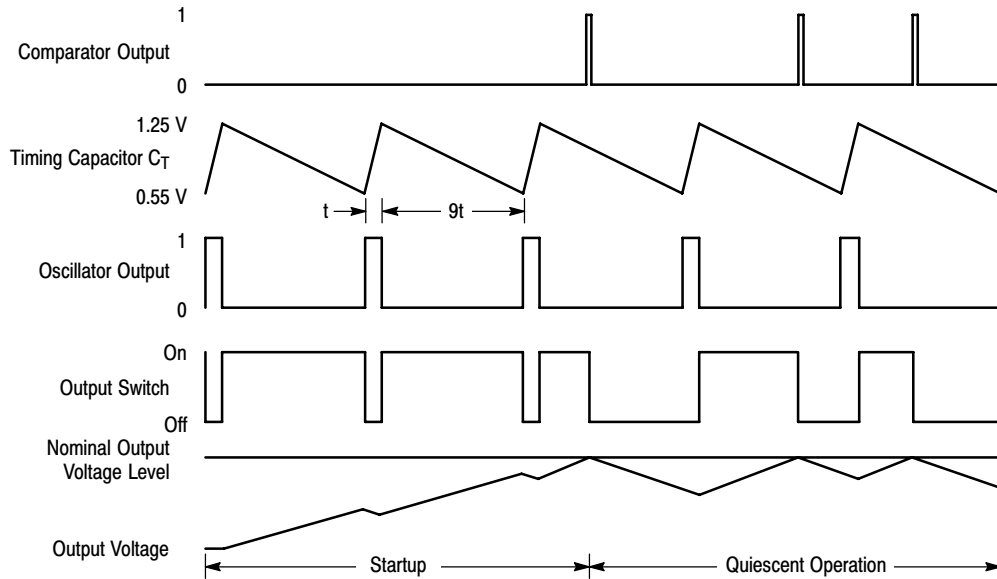


Figure 20. Typical Operating Waveforms

INTRODUCTION

The NCV33163 series are monolithic power switching regulators optimized for dc-to-dc converter applications. The combination of features in this series enables the system designer to directly implement step-up, step-down, and voltage-inverting converters with a minimum number of external components. Potential applications include cost sensitive consumer products as well as equipment for the automotive, computer, and industrial markets. A Representative Block Diagram is shown in Figure 19.

OPERATING DESCRIPTION

The NCV33163 operates as a fixed on-time, variable off-time voltage mode ripple regulator. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The Typical Operating Waveforms are shown in Figure 20. The output voltage waveform shown is for a step-down converter with the ripple and phasing exaggerated for clarity. During initial converter startup, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal, the feedback comparator sets the latch, immediately terminating switch conduction. The feedback comparator will inhibit the switch until the load current causes the output voltage to fall below nominal. Under these conditions, output switch conduction can be inhibited for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles.

Oscillator

The oscillator frequency and on-time of the output switch are programmed by the value selected for timing capacitor C_T . Capacitor C_T is charged and discharged by a 9 to 1 ratio internal current source and sink, generating a negative going sawtooth waveform at Pin 6. As C_T charges, an internal pulse is generated at the oscillator output. This pulse is connected to the NOR gate center input, preventing output switch conduction, and to the AND gate upper input, allowing the latch to be reset if the comparator output is low. Thus, the output switch is always disabled during ramp-up and can be enabled by the comparator output only at the start of ramp-down. The oscillator peak and valley thresholds are 1.25 V and 0.55 V, respectively, with a charge current of 225 μ A and a discharge current of 25 μ A, yielding a maximum on-time duty cycle of 90%. A reduction of the maximum duty cycle may be required for specific converter configurations. This can be accomplished with the addition of an external deadtime resistor (R_{DT}) placed across C_T . The

resistor increases the discharge current which reduces the on-time of the output switch. A graph of the Output Switch On-Off Time versus Oscillator Timing Capacitance for various values of R_{DT} is shown in Figure 2. Note that the maximum output duty cycle, $t_{on}/t_{on} + t_{off}$, remains constant for values of C_T greater than 0.2 nF. The converter output can be inhibited by clamping C_T to ground with an external NPN small-signal transistor.

Feedback and Low Voltage Indicator Comparators

Output voltage control is established by the Feedback comparator. The inverting input is internally biased at 1.25 V and is not pinned out. The converter output voltage is typically divided down with two external resistors and monitored by the high impedance noninverting input at Pin 2. The maximum input bias current is $\pm 0.4 \mu$ A, which can cause an output voltage error that is equal to the product of the input bias current and the upper divider resistance value. For applications that require 5.0 V, the converter output can be directly connected to the noninverting input at Pin 3. The high impedance input, Pin 2, must be grounded to prevent noise pickup. The internal resistor divider is set for a nominal voltage of 5.05 V. The additional 50 mV compensates for a 1.0% voltage drop in the cable and connector from the converter output to the load. The Feedback comparator's output state is controlled by the highest voltage applied to either of the two noninverting inputs.

The Low Voltage Indicator (LVI) comparator is designed for use as a reset controller in microprocessor-based systems. The inverting input is internally biased at 1.125 V, which sets the noninverting input thresholds to 90% of nominal. The LVI comparator has 15 mV of hysteresis to prevent erratic reset operation. The Open Collector output is capable of sinking in excess of 6.0 mA (see Figure 11). An external resistor (R_{LVI}) and capacitor (C_{DLY}) can be used to program a reset delay time (t_{DLY}) by the formula shown below, where $V_{th(MPU)}$ is the microprocessor reset input threshold. Refer to Figure 21.

$$t_{DLY} = R_{LVI} C_{DLY} \ln \left(\frac{1}{1 - \frac{V_{th(MPU)}}{V_{out}}} \right)$$

Current Limit Comparator, Latch and Thermal Shutdown

With a voltage mode ripple converter operating under normal conditions, output switch conduction is initiated by the oscillator and terminated by the Voltage Feedback comparator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the Current Limit comparator will protect the Output Switch.

The switch current is converted to a voltage by inserting a fractional ohm resistor, R_{SC} , in series with V_{CC} and output switch transistor Q_2 . The voltage drop across R_{SC} is monitored by the Current Sense comparator. If the voltage drop exceeds 250 mV with respect to V_{CC} , the comparator will set the latch and terminate output switch conduction on a cycle-by-cycle basis. This Comparator/Latch configuration ensures that the Output Switch has only a single on-time during a given oscillator cycle. The calculation for a value of R_{SC} is:

$$R_{SC} = \frac{0.25 \text{ V}}{I_{pk} (\text{Switch})}$$

Figures 12 and 13 show that the Current Sense comparator threshold is tightly controlled over temperature and has a typical input bias current of 1.0 μA . The propagation delay from the comparator input to the Output Switch is typically 200 ns. The parasitic inductance associated with R_{SC} and the circuit layout should be minimized. This will prevent unwanted voltage spikes that may falsely trip the Current Limit comparator.

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the Latch is forced into the “Set” state, disabling the Output Switch. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.

Driver and Output Switch

To aid in system design flexibility and conversion efficiency, the driver current source and collector, and output switch collector and emitter are pinned out separately. This allows the designer the option of driving the output switch into saturation with a selected force gain or driving it near saturation when connected as a Darlington. The output switch is designed to switch a maximum of 60 V collector to emitter, with up to 2.5 A peak collector current. The minimum value for R_{SC} is:

$$R_{SC}(\text{min}) = \frac{0.25 \text{ V}}{2.5 \text{ A}} = 0.100 \Omega$$

When configured for step-down or voltage-inverting applications, as in Figures 21 and 25, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn-on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing

additional device heating and reduced conversion efficiency.

Figure 10 shows that by clamping the emitter to 0.5 V, the collector current will be in the range 10 μA over temperature. A 1N5822 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

A bootstrap input is provided to reduce the output switch saturation voltage in step-down and voltage-inverting converter applications. This input is connected through a series resistor and capacitor to the switch emitter and is used to raise the internal 2.0 mA bias current source above V_{CC} . An internal zener limits the bootstrap input voltage to $V_{CC} + 7.0 \text{ V}$. The capacitor's equivalent series resistance must limit the zener current to less than 100 mA. An additional series resistor may be required when using tantalum or other low ESR capacitors. The equation below is used to calculate a minimum value bootstrap capacitor based on a minimum zener voltage and an upper limit current source.

$$C_{B(\text{min})} = I \frac{\Delta t}{\Delta V} = 4.0 \text{ mA} \frac{t_{on}}{4.0 \text{ V}} = 0.001 t_{on}$$

Parametric operation of the NCV33163 is guaranteed over a supply voltage range of 2.5 V to 60 V. When operating below 3.0 V, the Bootstrap Input should be connected to V_{CC} . Figure 16 shows that functional operation down to 1.7 V at room temperature is possible.

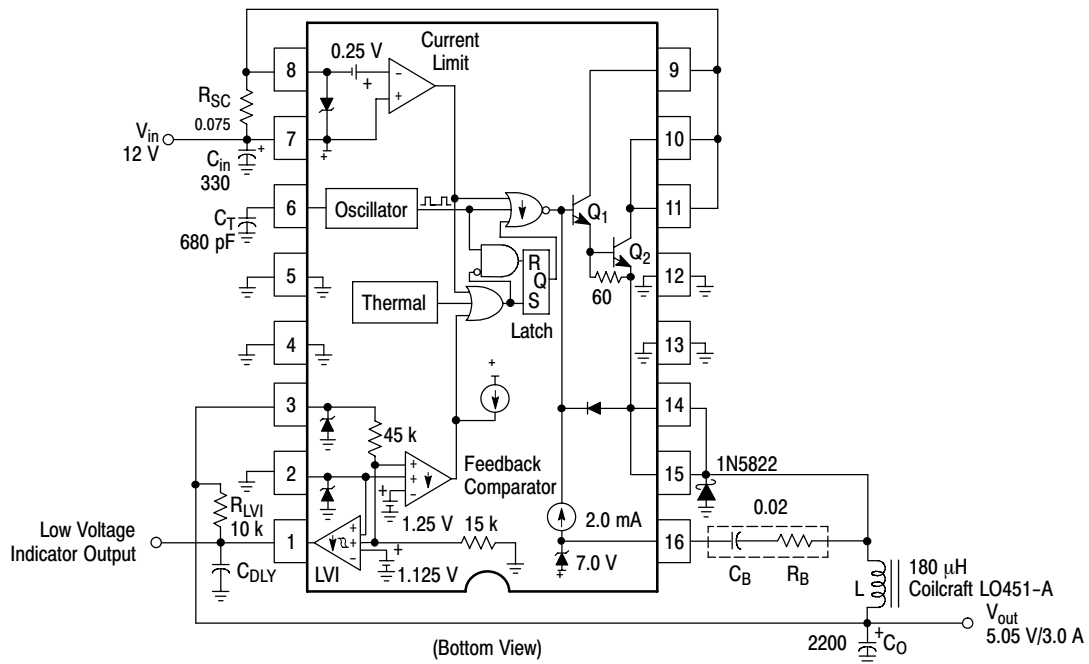
Package

The NCV33163 is contained in a heat-sinkable 16-lead plastic dual-in-line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 17 and 18 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction-to-air thermal resistance. These examples are for a symmetrical layout on a single-sided board with two ounce per square foot of copper.

APPLICATIONS

The following converter applications show the simplicity and flexibility of this circuit architecture. Three main converter topologies are demonstrated with actual test data shown below each of the circuit diagrams.

NCV33163



Test	Condition	Results
Line Regulation	$V_{in} = 8.0 \text{ V to } 24 \text{ V}$, $I_O = 3.0 \text{ A}$	$6.0 \text{ mV} = \pm 0.06\%$
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 0.6 \text{ A to } 3.0 \text{ A}$	$2.0 \text{ mV} = \pm 0.02\%$
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 3.0 \text{ A}$	36 mVpp
Short Circuit Current	$V_{in} = 12 \text{ V}$, $R_L = 0.1 \Omega$	3.3 A
Efficiency, Without Bootstrap	$V_{in} = 12 \text{ V}$, $I_O = 3.0 \text{ A}$	76.7%
Efficiency, With Bootstrap	$V_{in} = 12 \text{ V}$, $I_O = 3.0 \text{ A}$	81.2%

Figure 21. Step-Down Converter

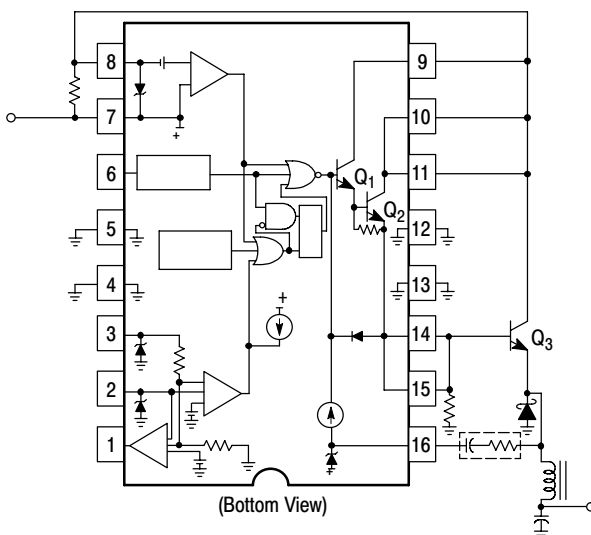


Figure 22A. External NPN Switch

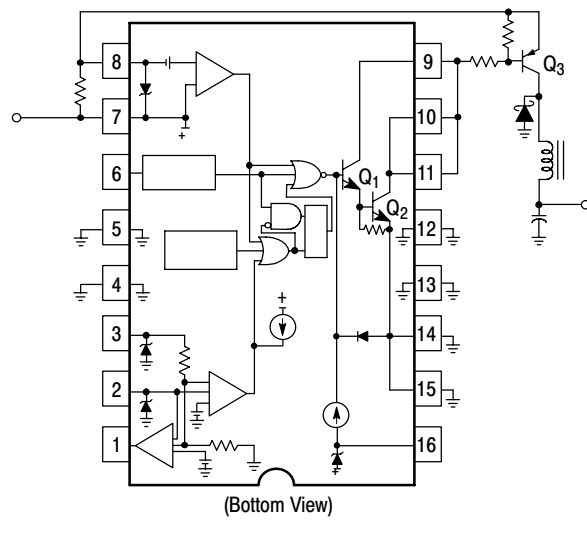
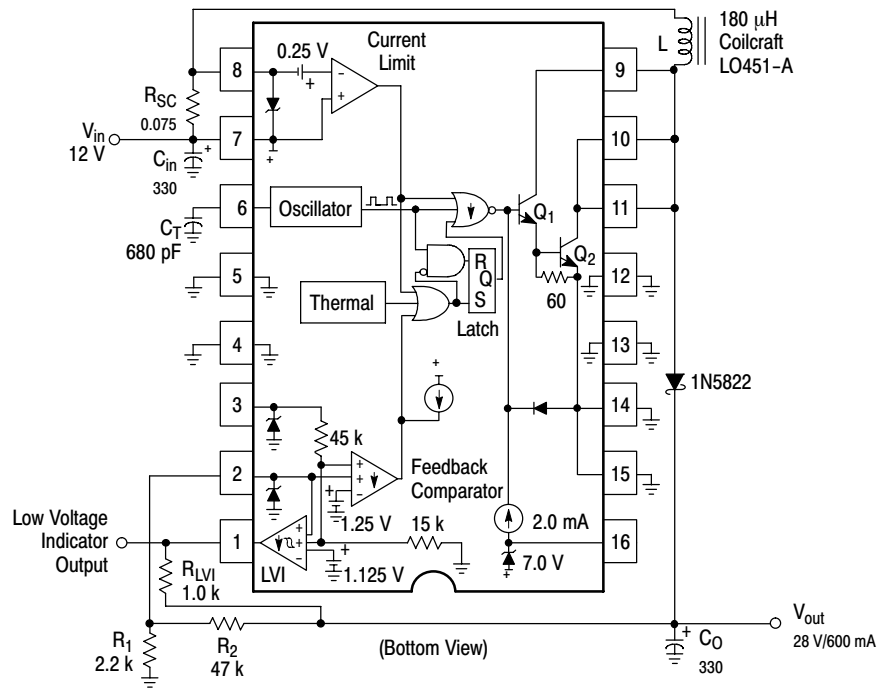


Figure 22B. External PNP Saturated Switch

Figure 22. External Current Boost Connections for $I_{pk} \text{ (Switch) Greater Than } 2.5 \text{ A}$

NCV33163



Test	Condition	Results
Line Regulation	$V_{in} = 9.0 \text{ V to } 16 \text{ V}$, $I_O = 0.6 \text{ A}$	$30 \text{ mV} = \pm 0.05\%$
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 0.1 \text{ A to } 0.6 \text{ A}$	$50 \text{ mV} = \pm 0.09\%$
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 0.6 \text{ A}$	140 mVpp
Efficiency	$V_{in} = 12 \text{ V}$, $I_O = 0.6 \text{ A}$	88.1%

Figure 23. Step-Up Converter

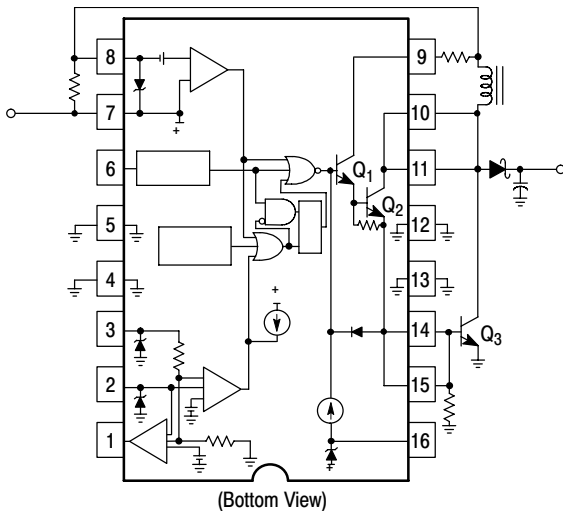


Figure 24A. External NPN Switch

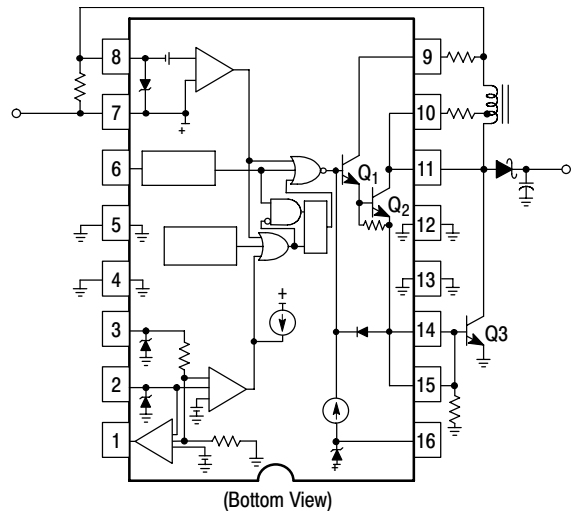
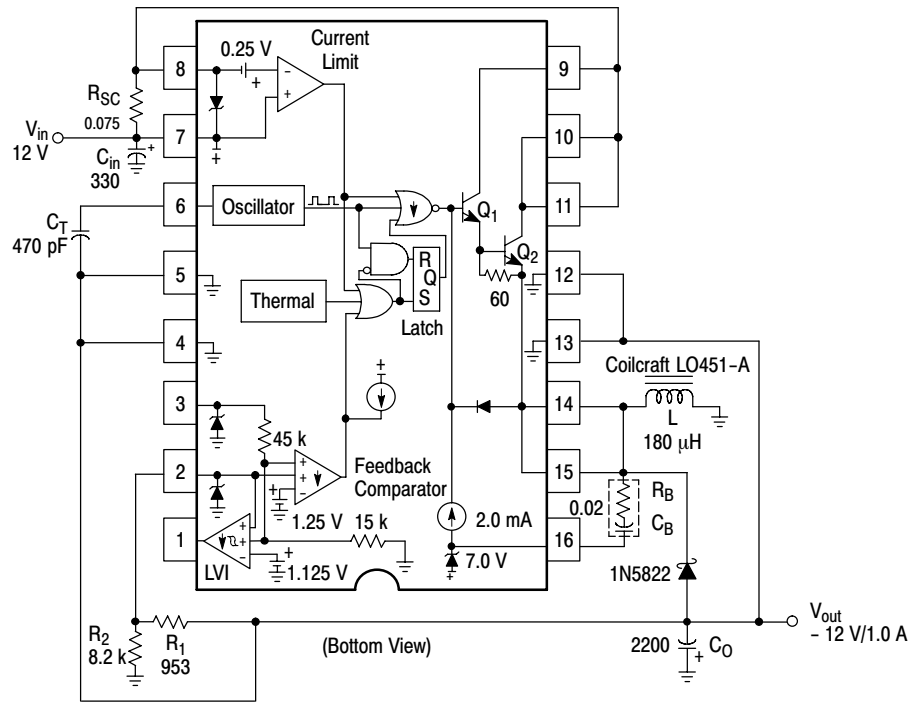


Figure 24B. External PNP Saturated Switch

Figure 24. External Current Boost Connections for $I_{pk} \text{ (Switch) Greater Than } 2.5 \text{ A}$



Test	Condition	Results
Line Regulation	$V_{in} = 9.0 \text{ V to } 16 \text{ V}$, $I_O = 1.0 \text{ A}$	$5.0 \text{ mV} \pm 0.02\%$
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 0.6 \text{ A to } 1.0 \text{ A}$	$2.0 \text{ mV} \pm 0.01\%$
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ A}$	130 mVpp
Short Circuit Current	$V_{in} = 12 \text{ V}$, $R_L = 0.1 \Omega$	3.2 A
Efficiency, Without Bootstrap	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ A}$	73.1%
Efficiency, With Bootstrap	$V_{in} = 12 \text{ V}$, $I_O = 1.0 \text{ A}$	77.5%

Figure 25. Voltage-Inverting Converter

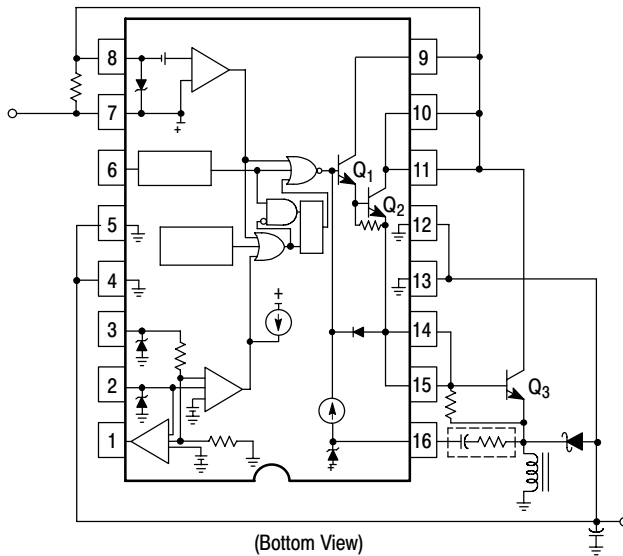


Figure 26A. External NPN Switch

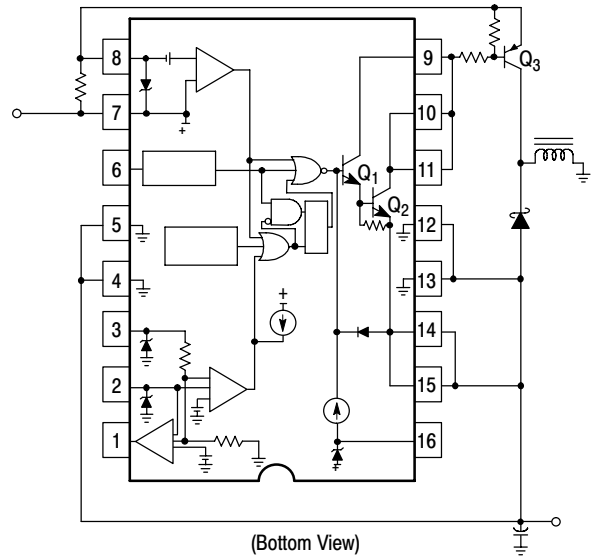


Figure 26B. External PNP Saturated Switch

Figure 26. External Current Boost Connections for $I_{pk} \text{ (Switch)}$ Greater Than 2.5 A

Calculation	Step-Down	Step-Up	Voltage-Inverting
$\frac{t_{on}}{t_{off}}$ (Notes 1, 2, 3)	$\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in}}{V_{in} - V_{sat}}$	$\frac{ V_{out} + V_F}{V_{in} - V_{sat}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f \left(\frac{t_{on}}{t_{off}} + 1 \right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f \left(\frac{t_{on}}{t_{off}} + 1 \right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f \left(\frac{t_{on}}{t_{off}} + 1 \right)}$
C_T	$\frac{32.143 \cdot 10^{-6}}{f}$	$\frac{32.143 \cdot 10^{-6}}{f}$	$\frac{32.143 \cdot 10^{-6}}{f}$
$I_{L(avg)}$	I_{out}	$I_{out} \left(\frac{t_{on}}{t_{off}} + 1 \right)$	$I_{out} \left(\frac{t_{on}}{t_{off}} + 1 \right)$
$I_{pk} \text{ (Switch)}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$
R_{SC}	$\frac{0.25}{I_{pk} \text{ (Switch)}}$	$\frac{0.25}{I_{pk} \text{ (Switch)}}$	$\frac{0.25}{I_{pk} \text{ (Switch)}}$
L	$\left(\frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L} \right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L} \right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L} \right) t_{on}$
$V_{ripple(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8 \cdot C_O} \right)^2 + (ESR)^2}$	$\approx \frac{t_{on} I_{out}}{C_O}$	$\approx \frac{t_{on} I_{out}}{C_O}$
V_{out}	$V_{ref} \left(\frac{R_2}{R_1} + 1 \right)$	$V_{ref} \left(\frac{R_2}{R_1} + 1 \right)$	$V_{ref} \left(\frac{R_2}{R_1} + 1 \right)$

The following Converter Characteristics must be chosen:

- V_{in} – Nominal operating input voltage.
- V_{out} – Desired output voltage.
- I_{out} – Desired output current.
- ΔI_L – Desired peak-to-peak inductor ripple current. For maximum output current it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L(avg)}$. This will help prevent $I_{pk} \text{ (Switch)}$ from reaching the current limit threshold set by R_{SC} . If the design goal is to use a minimum inductance value, let $\Delta I_L = 2(I_{L(avg)})$. This will proportionally reduce converter output current capability.
- f – Maximum output switch frequency.
- $V_{ripple(pp)}$ – Desired peak-to-peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

- NOTES:**
- V_{sat} – Saturation voltage of the output switch, refer to Figures 8 and 9.
 - V_F – Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.5 V.
 - The calculated t_{on}/t_{off} must not exceed the minimum guaranteed oscillator charge to discharge ratio of 8, at the minimum operating input voltage.

Figure 27. Design Equations

NCV8800 Series

Synchronous Buck Regulator with 1.0 Amp Switch

The NCV8800 is an automotive synchronous step-down buck regulator. This part provides an efficient step-down voltage compared to linear regulators. The NCV8800 uses very few external components allowing for maximum use of printed circuit board space.

Features

- Output Voltage Options: 2.6 V, 3.3 V, 5.0 V, 7.5 V
- $\pm 3.0\%$ Output
- 3.5 V Operation
- AUXILIARY Hold Up Pin (for Cranking Conditions)
- On-Chip Switching Power Devices ($0.4 \Omega R_{DS(ON)}$)
- Constant Frequency
- Synchronous Operation
- On-Chip Charge Pump Control Circuitry
- Nonoverlap Logic
- Power Up Sequencing Control Option (2.6 V and 3.3 V Only)
- ENABLE Battery Voltage Capable Option
- Selectable Reset Delay
- Dual Pin Feedback Connection
- V^2 ™ Control Topology
- Internally Fused Leads in SO-16L Package
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control

Typical Applications

- Telecommunications
- Mobile Multimedia
- Instrumentation
- Automotive Entertainment Systems

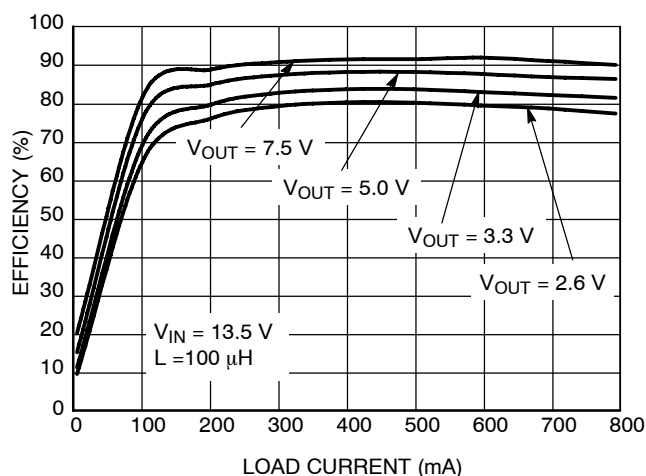
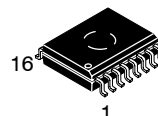


Figure 1. Efficiency vs. Load Current



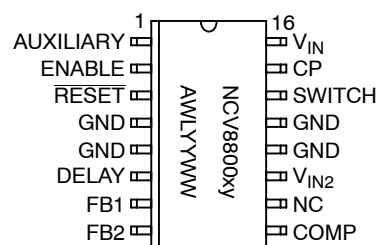
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SO-16L
DW SUFFIX
CASE 751G

PIN CONNECTIONS AND MARKING DIAGRAM

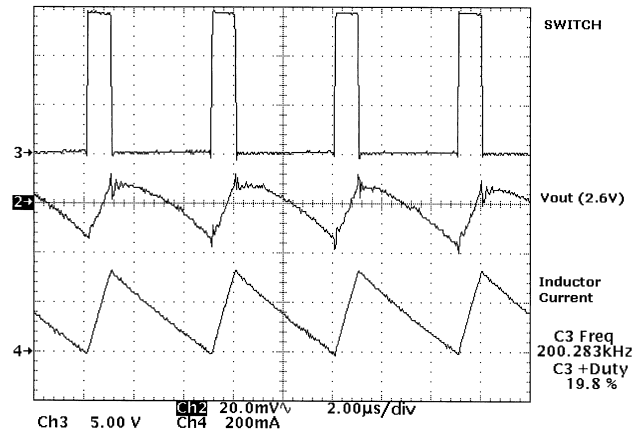
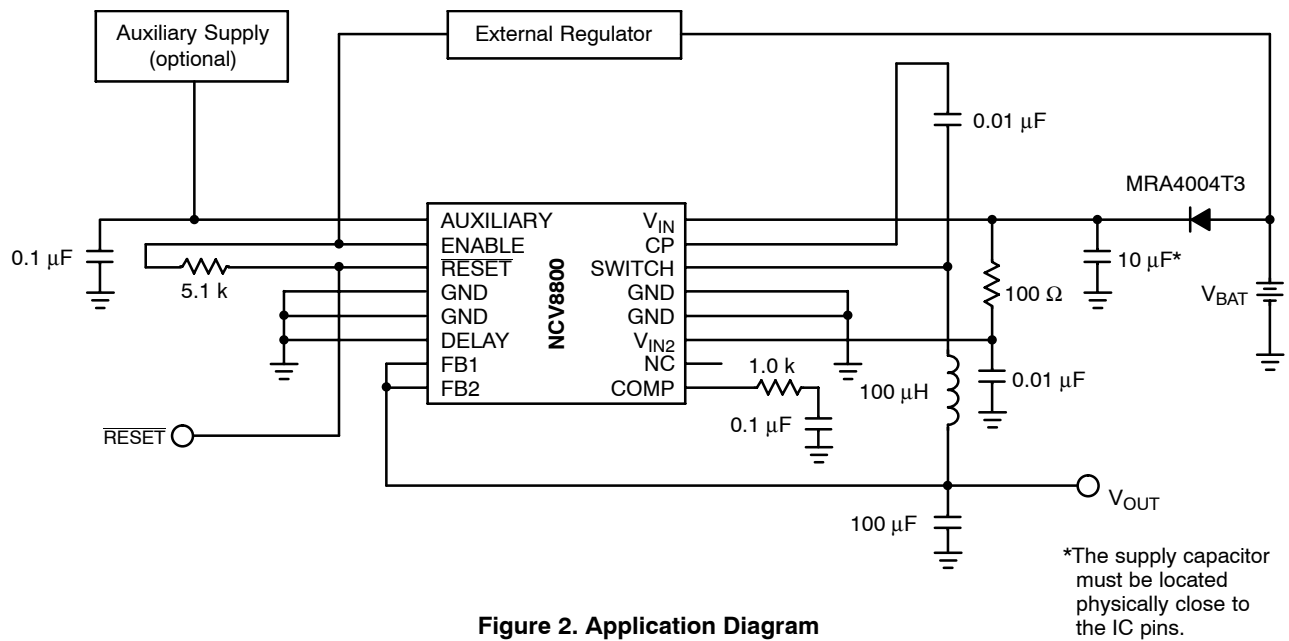


- x = Voltage Ratings as Indicated Below:
2 = 2.6 V
3 = 3.3 V
5 = 5.0 V
7 = 7.5 V
- y = ENABLE Option as Indicated Below:
S = Sequenced
H = High Voltage
- A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 600 of this data sheet.

NCV8800 Series



NCV8800 Series

MAXIMUM RATINGS*

Rating	Value	Unit
Supply Voltages, V_{IN} , V_{IN2}	-0.3 to 45	V
AUXILIARY	-0.3 to 8.0	V
ENABLE (Sequenced Option)	-0.3 to 7.0	V
ENABLE (High Voltage Option)	-0.3 to 8.0	V
RESET	-0.3 to 30	V
DELAY	-0.3 to 7.0	V
SWITCH ($V_{5VSENSE} = 0$ V)	-1.0 to 45	V
Operating Junction Temperature	-40 to 150	°C
Storage Temperature Range	-55 to 150	°C
ESD – Human Body Model (AUXILIARY, ENABLE, RESET, DELAY, FB1, FB2, CP, SWITCH, COMP)	2.0	kV
Human Body Model (V_{IN} , V_{IN2})	1.3	kV
Machine Model (All Pins)	200	V
Package Thermal Resistance, SO-16L		°C/W
Junction-to-Case, $R_{\theta JC}$	18	
Junction-to-Ambient, $R_{\theta JA}$	80	
Lead Temperature Soldering: Reflow (SMD Style Only) (Note 4)	240 Peak (Note 5)	°C

4. 60 second maximum above 183°C.

5. -5°C/+0°C allowable condition.

*The maximum package power dissipation must be observed.

NCV8800 Series

ELECTRICAL CHARACTERISTICS ($-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$; Sequenced ENABLE Option: $3.5\text{ V} \leq V_{\text{IN}} \leq 16\text{ V}$, $3.5\text{ V} \leq V_{\text{IN2}} \leq 16\text{ V}$, AUXILIARY = 6.0 V, ENABLE = 5.0 V; High Voltage ENABLE Option: $6.0\text{ V} \leq V_{\text{IN}} \leq 16\text{ V}$, $6.0\text{ V} \leq V_{\text{IN2}} \leq 16\text{ V}$; unless otherwise stated.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
General					
Quiescent Current (V_{IN2}) Sleep Mode Operating	ENABLE = 0 V, $V_{\text{IN}} = 12.6\text{ V}$, $T_J = -40^{\circ}\text{C}$	–	–	40	μA
	ENABLE = 0 V, $V_{\text{IN}} = 12.6\text{ V}$, $T_J = 25^{\circ}\text{C}$, 125°C	–	–	30	μA
	ENABLE = 5.0 V, $V_{\text{IN}} = 13.5\text{ V}$, $I_{\text{OUT}} = 0$	–	–	15	mA
Switching Frequency	–	180	200	230	kHz
Switching Duty Cycle	–	85	90	95	%
Thermal Shutdown	Note 6	150	165	200	$^{\circ}\text{C}$

Feedback

Feedback Voltage Threshold, 2.6 V Option (V_{FB})	–	2.522	2.6	2.678	V
Feedback Voltage Threshold, 3.3 V Option (V_{FB})	–	3.201	3.3	3.399	V
Feedback Voltage Threshold, 5.0 V Option (V_{FB})	–	4.850	5.0	5.150	V
Feedback Voltage Threshold, 7.5 V Option (V_{FB})	–	7.275	7.5	7.725	V

RESET

Undervoltage $\overline{\text{RESET}}$ Threshold, 2.6 V Option	V_{OUT} Increasing	2.44	–	V_{FB}	V
	V_{OUT} Decreasing	2.40	–	$V_{\text{FB}} - 0.04$	V
Undervoltage $\overline{\text{RESET}}$ Hysteresis, 2.6 V Option	–	40	–	–	mV
Overvoltage $\overline{\text{RESET}}$ Threshold, 2.6 V Option	V_{OUT} Increasing	$V_{\text{FB}} + 0.04$	–	2.80	V
	V_{OUT} Decreasing	V_{FB}	–	2.76	V
Overvoltage $\overline{\text{RESET}}$ Hysteresis, 2.6 V Option	–	40	–	–	mV
Undervoltage $\overline{\text{RESET}}$ Threshold, 3.3 V Option	V_{OUT} Increasing	3.10	–	V_{FB}	V
	V_{OUT} Decreasing	3.04	–	$V_{\text{FB}} - 0.05$	V
Undervoltage $\overline{\text{RESET}}$ Hysteresis, 3.3 V Option	–	50	–	–	mV
Overvoltage $\overline{\text{RESET}}$ Threshold, 3.3 V Option	V_{OUT} Increasing	$V_{\text{FB}} + 0.05$	–	3.56	V
	V_{OUT} Decreasing	V_{FB}	–	3.51	V
Overvoltage $\overline{\text{RESET}}$ Hysteresis, 3.3 V Option	–	50	–	–	mV
Undervoltage $\overline{\text{RESET}}$ Threshold, 5.0 V Option	V_{OUT} Increasing	4.70	–	V_{FB}	V
	V_{OUT} Decreasing	4.61	–	$V_{\text{FB}} - 0.075$	V
Undervoltage $\overline{\text{RESET}}$ Hysteresis, 5.0 V Option	–	75	–	–	mV
Overvoltage $\overline{\text{RESET}}$ Threshold, 5.0 V Option	V_{OUT} Increasing	$V_{\text{FB}} + 0.075$	–	5.39	V
	V_{OUT} Decreasing	V_{FB}	–	5.31	V
Overvoltage $\overline{\text{RESET}}$ Hysteresis, 5.0 V Option	–	75	–	–	mV
Undervoltage $\overline{\text{RESET}}$ Threshold, 7.5 V Option	V_{OUT} Increasing	7.05	–	V_{FB}	V
	V_{OUT} Decreasing	6.92	–	$V_{\text{FB}} - 0.115$	V
Undervoltage $\overline{\text{RESET}}$ Hysteresis, 7.5 V Option	–	115	–	–	mV
Overvoltage $\overline{\text{RESET}}$ Threshold, 7.5 V Option	V_{OUT} Increasing	$V_{\text{FB}} + 0.115$	–	8.08	V
	V_{OUT} Decreasing	V_{FB}	–	7.96	V
Overvoltage $\overline{\text{RESET}}$ Hysteresis, 7.5 V Option	–	115	–	–	mV

6. Guaranteed By Design.

NCV8800 Series

ELECTRICAL CHARACTERISTICS (continued) ($-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$; Sequenced ENABLE Option: $3.5\text{ V} \leq V_{\text{IN}} \leq 16\text{ V}$, $3.5\text{ V} \leq V_{\text{IN2}} \leq 16\text{ V}$, AUXILIARY = 6.0 V, ENABLE = 5.0 V; High Voltage ENABLE Option: $6.0\text{ V} \leq V_{\text{IN}} \leq 16\text{ V}$, $6.0\text{ V} \leq V_{\text{IN2}} \leq 16\text{ V}$; unless otherwise stated.)

Characteristic	Test Conditions	Min	Typ	Max	Unit

RESET

RESET Leakage Current	RESET = 5.25 V	–	–	25	μA
RESET Output Low Voltage	I _{OUT} = 1.6 mA	–	–	0.4	V
RESET Delay	DELAY Connected to FB1, FB2 DELAY = 0 V	28.70 14.35	32.60 16.30	36.66 18.33	ms ms

ENABLE

ENABLE Threshold	Increasing Decreasing	1.1 1.0	1.9 1.6	2.3 2.2	V V
ENABLE Hysteresis	–	100	250	550	mV
ENABLE Input Resistance	ENABLE = 5.25 V, V _{IN2} = 13.5 V	50	100	200	k Ω

DELAY

DELAY Input Current	DELAY = 5.15 V	4.0	10	16	μA

SWITCH

SWITCH ON Resistance	I _{SWITCH} = 0.5 A, T _J = -40°C , 25°C I _{SWITCH} = 0.5 A, T _J = 125°C	– –	0.40 0.55	0.60 0.75	Ω Ω
Current Limit	–	1.0	1.6	2.5	A

Error Amplifier

Error Amplifier Transconductance	2.6 V Option	2.58 V ≤ FB1 ≤ 2.62 V 2.58 V ≤ FB2 ≤ 2.62 V	0.55	–	2.10	1/m Ω
	3.3 V Option	3.275 V ≤ FB1 ≤ 3.325 V 3.275 V ≤ FB2 ≤ 3.325 V	0.43	–	1.65	
		5.0 V Option	4.962 V ≤ FB1 ≤ 5.038 V 4.962 V ≤ FB2 ≤ 5.038 V	0.28	–	
	7.5 V Option		7.442 V ≤ FB1 ≤ 7.558 V 7.442 V ≤ FB2 ≤ 7.558 V	0.19	–	
		Error Amplifier Bandwidth		Note 7	1.0	

Output Tracking (Sequencing)

Feedback to ENABLE Tracking Voltage, 2.6 V Option	–	60	67	75	%
Feedback to ENABLE Tracking Voltage, 3.3 V Option	–	80	85	90	%

7. Guaranteed By Design.

NCV8800 Series

PACKAGE PIN DESCRIPTION

PACKAGE LEAD #	LEAD SYMBOL	FUNCTION
1	AUXILIARY	Alternate path for voltage input to the IC.
2	ENABLE	Sense for powerup. This pin must be high before SWITCH turns on.
3	$\overline{\text{RESET}}$	CMOS compatible open drain output lead. $\overline{\text{RESET}}$ goes low whenever FB1 or FB2 is below the $\overline{\text{RESET}}$ low threshold, or above the $\overline{\text{RESET}}$ high threshold.
4, 5, 12, 13	GND	Ground.
6	DELAY	$\overline{\text{RESET}}$ delay control. Time is doubled when pin moved to FB1 or FB2 from 0 V.
7	FB1	Voltage feedback to error amplifier. Shorted with FB2.
8	FB2	Voltage feedback to error amplifier. Shorted with FB1.
9	COMP	Loop compensation node for error amplifier. (1.0 k Ω and 0.1 μ F to ground).
10	NC	No connection.
11	V _{IN2}	Supply input voltage for internal bias circuitry.
14	SWITCH	Drive for external inductor.
15	CP	Node for charge pump bootstrap capacitor.
16	V _{IN}	Supply input voltage for output drivers.

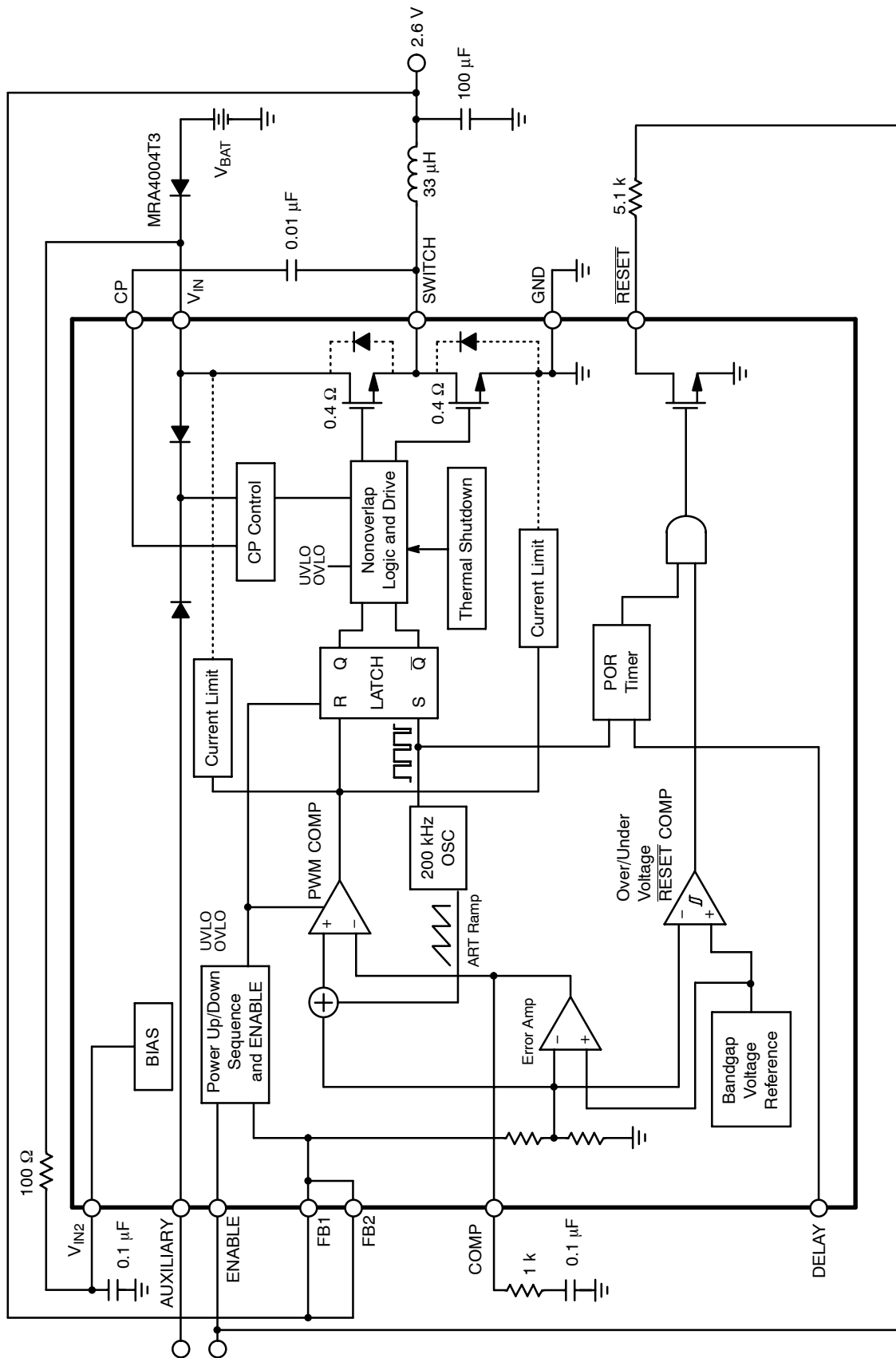


Figure 4. Block Diagram

CIRCUIT DESCRIPTION

ENABLE

The NCV8800 remains in sleep mode drawing less than 25 μ A of quiescent current until the ENABLE pin is brought high powering up the device. There are two options available for the ENABLE feature.

- Option 1 (Sequenced). The output voltage tracks the ENABLE pin with a maximum delta voltage between them (reference the Output Tracking specs in the Electrical Characteristics). This allows the device to be used with microprocessors requiring dual supply voltages. One voltage is typically needed to power the core of the microprocessor, and another high voltage is needed to power the microprocessor I/O.
- Option 2 (High Voltage). This option removes the sequencing feature above, and allows the device to be controlled up to the battery voltage on the ENABLE pin with an external resistor (10 k). See Figure 5.

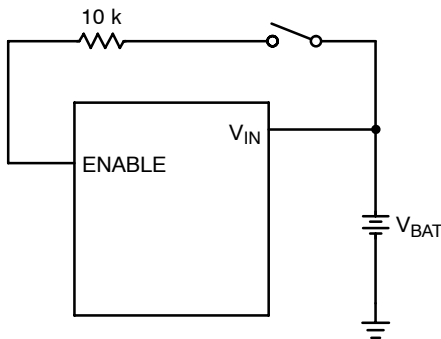


Figure 5. Switched Battery Application

AUXILIARY

The AUXILIARY pin provides an alternate path for the IC to maintain operation. The AUXILIARY pin is diode OR'd with the V_{IN} pin to the control circuitry (the DMOS output drivers are not included). If the voltage (V_{IN}) from the battery dips as low as 3.5 V during a crank condition, the NCV8800 will maintain operation through a 6.0 V(min) connection on the AUXILIARY pin. Using this feature is optional. This pin should be grounded when not in use.

V_{IN}

Normal supply voltage input. An external diode must be provided to afford reverse battery protection.

SWITCH

DMOS output drivers with 0.75 Ω max push/pull capability. Non-overlap logic is provided to guarantee shoot through current is minimized.

RESET

The $\overline{\text{RESET}}$ is an open drain output which goes low when the feedback voltage on FB1 and FB2 goes below the undervoltage $\overline{\text{RESET}}$ threshold. The output also goes low when the voltage on FB1 and FB2 exceeds the overvoltage $\overline{\text{RESET}}$ threshold. The $\overline{\text{RESET}}$ output is an open drain output capable of sinking 1.6 mA.

FB1 and FB2

FB1 and FB2 are the feedback pins to the error amplifier, which control the output SWITCH as needed to the regulated output. They are internally wire bonded to the same electrical connection providing double protection for an open circuit which would cause the buck regulator to rise above its desired output reaching the voltage on V_{IN} . These pins also provide the feedback path for the $\overline{\text{RESET}}$ function.

DELAY

There are two options for the delay time for the $\overline{\text{RESET}}$ to go low. Connecting the pin to GND will provide a minimum of 14 ms. Connecting the pin to FB1 and FB2 will provide a minimum of 28 ms. Absolute max voltage on the DELAY pin is 7.0 V. Use a resistor divider to run off higher voltages. The 7.5 V option will require this divider (see Figure 6).

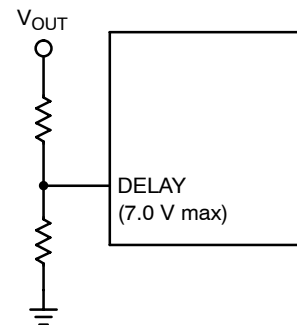


Figure 6.

COMP

The COMP pin provides access to the error amplifiers output. Switching power supplies work as feedback control systems, and require compensation for stability. A 1.0 k resistor and 0.1 μ F capacitor work well in the application in Figure 2.

CP

The on-chip DMOS drivers require the gates of the devices to be pulled above their drain voltage. An external capacitor located between the SWITCH output, and the CP pin provides the charge pump action to drive the gate of the high-side driver high enough to turn the device on.

APPLICATIONS INFORMATION

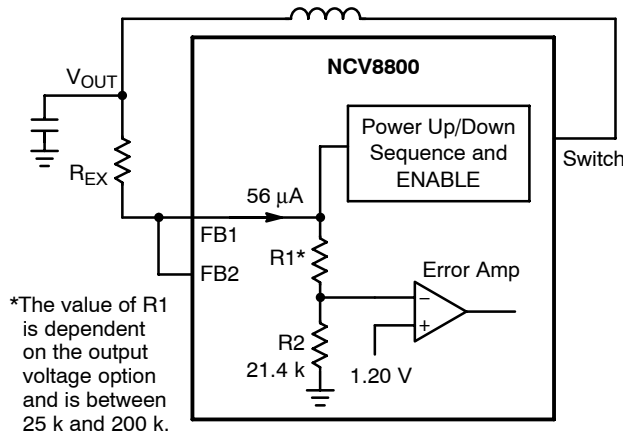


Figure 7.

Increasing the Output Voltage

Adjustments to the output voltage can be made with an external resistor (R_{EX}). The increase in output voltage will typically be $56 \mu A \times R_{EX}$. Caution and consideration must be given to the tracking feature and temperature coefficient and matching of internal and external resistors. Output tracking always follows the Feedback pins (FB1 and FB2). The typical temperature coefficient for R1 and R2 is +4600 ppm/°C.

THEORY OF OPERATION

V² Control Method

The V² method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variations in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.

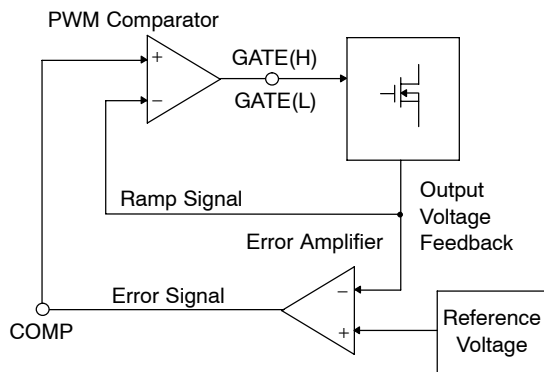


Figure 8. V² Control Block Diagram

The V² control method is illustrated in Figure 8. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of the change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to 0% or 100% duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the V² control scheme to compensate the duty cycle. Since the change in the inductor current modifies the ramp signal, as in current mode control, the V² control scheme has the same advantages in line transient response.

A change in load current will have an effect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this “slow” feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulations are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a derivation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The V² method of control maintains a fixed error signal for both line and load variations, since both line and load affect the ramp signal.

Constant Frequency Operation

During normal operation, the oscillator generates a 200 kHz, 90% duty cycle waveform. The rising edge of this waveform determines the beginning of each switching cycle, at which point the high-side switch will be turned on. The high-side switch will be turned off when the ramp signal intersects the output of the error amplifier (COMP pin voltage). Therefore, the switch duty cycle can be modified to regulate the output voltage to the desired value as line and load conditions change.

NCV8800 Series

The major advantage of constant frequency operation is that the component selections, especially the magnetic component design, become very easy. Oscillator frequency is fixed at 200 kHz.

Start-Up

After the NCV8800 is powered up, the error amplifier will begin linearly charging the COMP pin capacitor. The COMP capacitance and the source current of the error amplifier determine the slew rate of COMP voltage. The output of the error amplifier is connected internally to the inverting input of the PWM comparator and it is compared with the divided down output voltage FB1/FB2 at the non-inverting input of the PWM comparator. At the beginning of each switching cycle, the oscillator output will set the PWM latch. This causes the high-side switch to turn on and the regulator output voltage to ramp up.

When the divided down output voltage achieves a level set by the COMP voltage, the high-side switch will be turned off. The V^2 control loop will adjust the high-side switch duty cycle as required to ensure the regulator output voltage tracks the COMP voltage. Since the COMP voltage increases gradually, Soft Start can be achieved.

Overcurrent Protection

The output switch is protected on both the high side and low side. Current limit is set at 1.0 A (min).

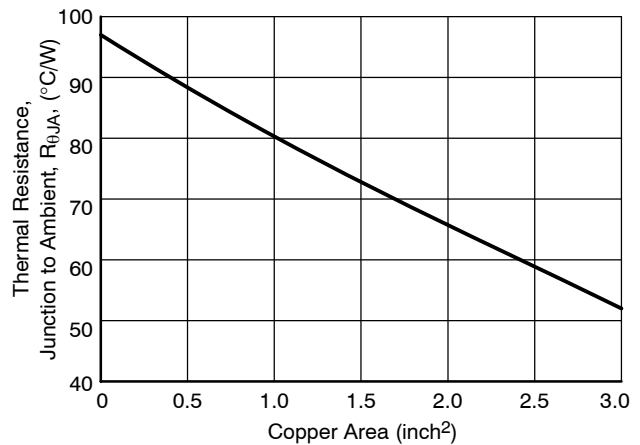


Figure 9. 16 Lead SOW (4 Leads Fused), θ_{JA} as a Function of the Pad Copper Area (2 oz. Cu. Thickness), Board Material = 0.0625" G-10/R-4

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where:

$R_{\theta JC}$ = the junction-to-case thermal resistance,

$R_{\theta CS}$ = the case-to-heatsink thermal resistance, and

$R_{\theta SA}$ = the heatsink-to-ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

NCV8800 Series

ORDERING INFORMATION

Device	Output Voltage	ENABLE Option	Package	Shipping†
NCV8800SDW26	2.6 V	Sequenced	SO-16L	46 Units/Rail
NCV8800SDW26R2				1000 Tape & Reel
NCV8800HDW26		High Voltage		46 Units/Rail
NCV8800HDW26R2				1000 Tape & Reel
NCV8800SDW33	3.3 V	Sequenced		46 Units/Rail
NCV8800SDW33R2				1000 Tape & Reel
NCV8800HDW33		High Voltage		46 Units/Rail
NCV8800HDW33R2				1000 Tape & Reel
NCV8800HDW50	5.0 V	High Voltage		46 Units/Rail
NCV8800HDW50R2				1000 Tape & Reel
NCV8800HDW75	7.5 V			46 Units/Rail
NCV8800HDW75R2				1000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP1422

800 mA Sync-Rect PFM Step-Up DC-DC Converter with True-Cutoff and Ring-Killer

NCP1422 is a monolithic micropower high-frequency step-up switching converter IC specially designed for battery-operated hand-held electronic products up to 800 mA loading. It integrates Sync-Rect to improve efficiency and to eliminate the external Schottky Diode. High switching frequency (up to 1.2 MHz) allows for a low profile, small-sized inductor and output capacitor to be used. When the device is disabled, the internal conduction path from LX or BAT to OUT is fully blocked and the OUT pin is isolated from the battery. This True-Cutoff function reduces the shutdown current to typically only 50 nA. Ring-Killer is also integrated to eliminate the high-frequency ringing in discontinuous conduction mode. In addition to the above, Low-Battery Detector, Logic-Controlled Shutdown, Cycle-by-Cycle Current Limit and Thermal Shutdown provide value-added features for various battery-operated applications. With all these functions on, the quiescent supply current is typically only 8.5 μ A. This device is available in the compact and low profile DFN-10 package.

Features

- Pb-Free Package is Available*
- High Efficiency: 94% for 3.3 V Output at 200 mA from 2.5 V Input
88% for 3.3 V Output at 500 mA from 2.5 V Input
- High Switching Frequency, up to 1.2 MHz (not hitting current limit)
- Output Current up to 800 mA at $V_{IN} = 2.5$ V and $V_{OUT} = 3.3$ V
- True-Cutoff Function Reduces Device Shutdown Current to typically 50 nA
- Anti-Ringing Ring-Killer for Discontinuous Conduction Mode
- High Accuracy Reference Output, 1.20 V $\pm$ 1.5% @ 25°C, can Supply 2.5 mA Loading Current when $V_{OUT} > 3.3$ V
- Low Quiescent Current of 8.5 μ A
- Integrated Low-Battery Detector
- Open Drain Low-Battery Detector Output
- 1.0 V Startup at No Load Guaranteed
- Output Voltage from 1.5 V to 5.0 V Adjustable
- 1.5 A Cycle-by-Cycle Current Limit
- Multi-Function Logic-Controlled Shutdown Pin
- On Chip Thermal Shutdown with Hysteresis

Typical Applications

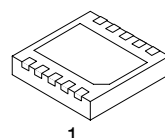
- Personal Digital Assistants (PDA)
- Handheld Digital Audio Products
- Camcorders and Digital Still Cameras
- Hand-held Instruments
- Conversion from one to two Alkaline, NiMH, NiCd Battery Cells to 3.0–5.0 V or one Lithium-ion cells to 5.0 V
- White LED Flash for Digital Cameras



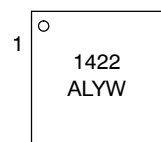
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM

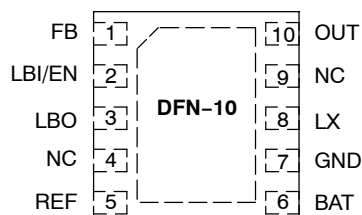


DFN-10
MN SUFFIX
CASE 485C



1422 = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1422MNR2	DFN-10	3000 Tape & Reel
NCP1422MNR2G	DFN-10 (Pb-Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

NCP1422

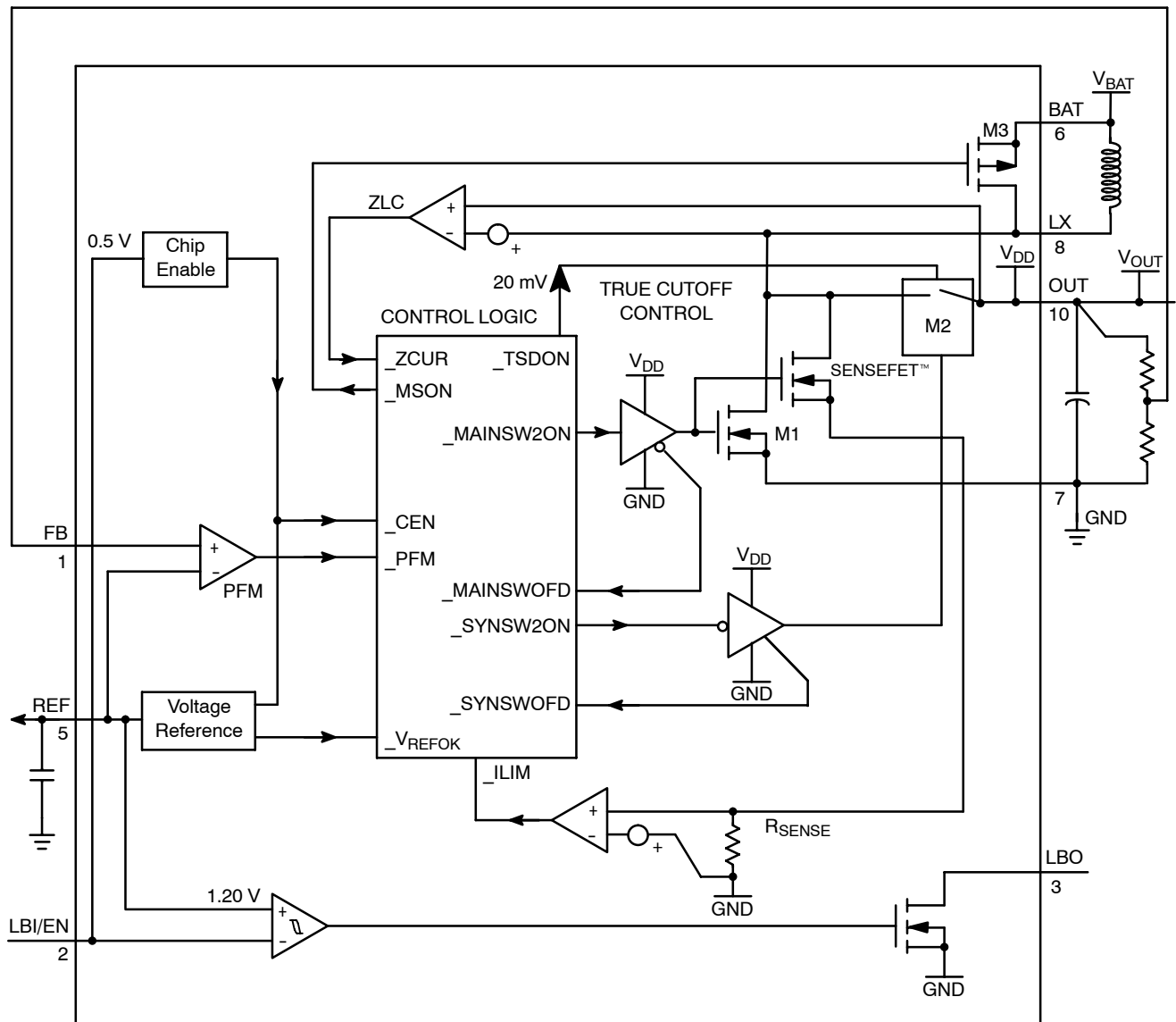


Figure 1. Detailed Block Diagram

PIN FUNCTION DESCRIPTIONS

Pin	Symbol	Description
1	FB	Output Voltage Feedback Input.
2	LBI/EN	Low-Battery Detector Input and IC Enable. With this pin pulled down below 0.5 V, the device is disabled and enters the shutdown mode.
3	LBO	Open-Drain Low-Battery Detector Output. Output is LOW when $V_{LBI} < 1.20$ V. LBO is high impedance in shutdown mode.
4	NC	No Connect Pin
5	REF	1.20 V Reference Voltage Output, bypass with 300 nF capacitor. If this pin is loaded, bypass with 1.0 μ F capacitor; this pin can be loaded up to 2.5 mA @ $V_{OUT} = 3.3$ V.
6	BAT	Battery input connection for internal ring-killer.
7	GND	Ground.
8	LX	N-Channel and P-Channel Power MOSFET drain connection.
9	NC	No Connect Pin
10	OUT	Power Output. OUT also provides bootstrap power to the device.

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply (Pin 10)	V_{OUT}	-0.3, 5.5	V
Input/Output Pins (Pin 1-3, Pin 5-8)	V_{IO}	-0.3, 5.5	V
Thermal Characteristics DFN-10 Plastic Package Thermal Resistance Junction-to-Air (Note 5)	P_D R_{JA}	1824 68.5	mW° C/W
Operating Junction Temperature Range	T_J	-40 to +150	°C
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- This device contains ESD protection and exceeds the following tests:
Human Body Model (HBM) ± 2.0 kV per JEDEC standard: JESD22-A114. *Except OUT pin, which is 1k V.
Machine Model (MM) ± 200 V per JEDEC standard: JESD22-A115. *Except OUT pin, which is 100 V.
- The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{JA}}$$

- Latchup Current Maximum Rating: ± 150 mA per JEDEC standard: JESD78.
- Moisture Sensitivity Level: MSL 1 per IPC/JEDEC standard: J-STD-020A.
- Measured on approximately 1x1 inch sq. of 1 oz. Copper.

NCP1422

ELECTRICAL CHARACTERISTICS ($V_{OUT} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ for typical value, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for min/max values unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage	V_{IN}	1.0	–	5.0	V
Output Voltage Range	V_{OUT}	1.5	–	5.0	V
Reference Voltage ($V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 0\text{ }\mu\text{A}$, $C_{REF} = 200\text{ nF}$, $T_A = 25^\circ\text{C}$)	V_{REF_NL}	1.183	1.200	1.217	V
Reference Voltage ($V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 0\text{ }\mu\text{A}$, $C_{REF} = 200\text{ nF}$, $T_A = -40^\circ\text{C}$ to 85°C)	V_{REF_NL}	1.174	–	1.220	V
Reference Voltage Temperature Coefficient	TC_{VREF}	–	0.03	–	mV/ $^\circ\text{C}$
Reference Voltage Load Current ($V_{OUT} = 3.3\text{ V}$, $V_{REF} = V_{REF\_NL} \pm 1.5\%$, $C_{REF} = 1.0\text{ }\mu\text{F}$) (Note 6)	I_{REF}	–	2.5	–	mA
Reference Voltage Load Regulation ($V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 0$ to $100\text{ }\mu\text{A}$, $C_{REF} = 1.0\text{ }\mu\text{F}$)	V_{REF_LOAD}	–	0.05	1.0	mV
Reference Voltage Line Regulation (V_{OUT} from 1.5 V to 5.0 V , $C_{REF} = 1.0\text{ }\mu\text{F}$)	V_{REF_LINE}	–	0.05	1.0	mV/V
FB Input Threshold ($I_{LOAD} = 0\text{ mA}$, $T_A = 25^\circ\text{C}$)	V_{FB}	1.192	1.200	1.208	V
FB Input Threshold ($I_{LOAD} = 0\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C)	V_{FB}	1.184	–	1.210	V
LBI Input Threshold ($I_{LOAD} = 0\text{ mA}$, $T_A = 25^\circ\text{C}$)	V_{LBI}	1.182	1.200	1.218	V
LBI Input Threshold ($I_{LOAD} = 0\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C)	V_{LBI}	1.162	–	1.230	V
Internal N-FET ON-Resistance	$R_{DS(ON)\_N}$	–	0.3	–	
Internal P-FET ON-Resistance	$R_{DS(ON)\_P}$	–	0.3	–	
LX Switch Current Limit (N-FET) (Note 8)	I_{LIM}	–	1.5	–	A
Operating Current into BAT ($V_{BAT} = 1.8\text{ V}$, $V_{FB} = 1.8\text{ V}$, $V_{LX} = 1.8\text{ V}$, $V_{OUT} = 3.3\text{ V}$)	I_{QBAT}	–	1.3	3.0	μA
Operating Current into OUT ($V_{FB} = 1.4\text{ V}$, $V_{OUT} = 3.3\text{ V}$)	I_Q	–	8.5	14	μA
LX Switch MAX. ON-Time ($V_{FB} = 1.0\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$)	t_{ON}	0.46	0.72	1.15	μs
LX Switch MIN. OFF-Time ($V_{FB} = 1.0\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$)	t_{OFF}	–	0.12	0.22	μs
FB Input Current	I_{FB}	–	1.0	50	nA
True-Cutoff Current into BAT ($LBI/EN = GND$, $V_{OUT} = 0\text{ V}$, $V_{IN} = 3.3\text{ V}$, $LX = 3.3\text{ V}$)	I_{BAT_SD}	–	50	–	nA
BAT-to-LX Resistance ($V_{FB} = 1.4\text{ V}$, $V_{OUT} = 3.3\text{ V}$) (Note 8)	R_{BAT_LX}	–	100	–	
LBI/EN Input Current	I_{LBI}	–	1.5	50	nA
LBO Low Output Voltage ($V_{LBI} = 0\text{ V}$, $I_{SINK} = 1.0\text{ mA}$)	V_{LBO_L}	–	–	0.2	V
Soft-Start Time ($V_{IN} = 2.5\text{ V}$, $V_{OUT} = 5.0\text{ V}$, $C_{REF} = 200\text{ nF}$) (Note 7)	T_{SS}	–	1.5	20	ms
EN Pin Shutdown Threshold ($T_A = 25^\circ\text{C}$)	V_{SHDN}	0.35	0.5	0.67	V
Thermal Shutdown Temperature (Note 8)	T_{SHDN}	–	–	145	$^\circ\text{C}$
Thermal Shutdown Hysteresis (Note 8)	T_{SDHYS}	–	30	–	$^\circ\text{C}$

6. Loading capability increases with V_{OUT} .

7. Design guarantee, value depends on voltage at V_{OUT} .

8. Values are design guaranteed.

TYPICAL OPERATING CHARACTERISTICS

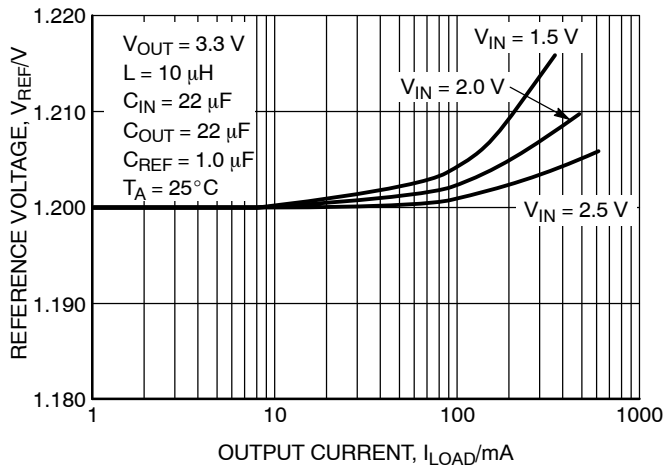


Figure 2. Reference Voltage vs. Output Current

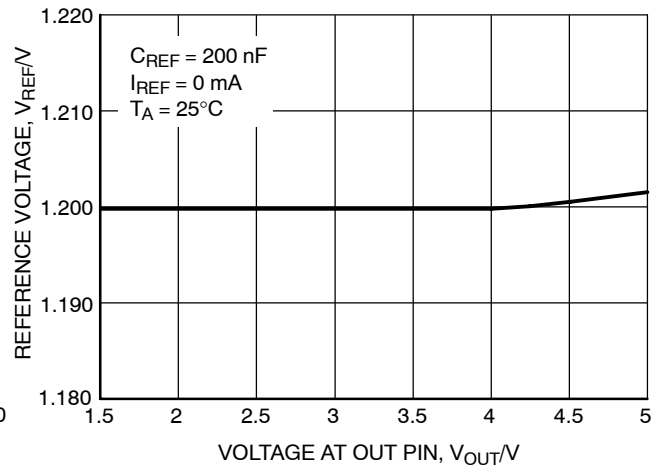


Figure 3. Reference Voltage vs. Voltage at OUT Pin

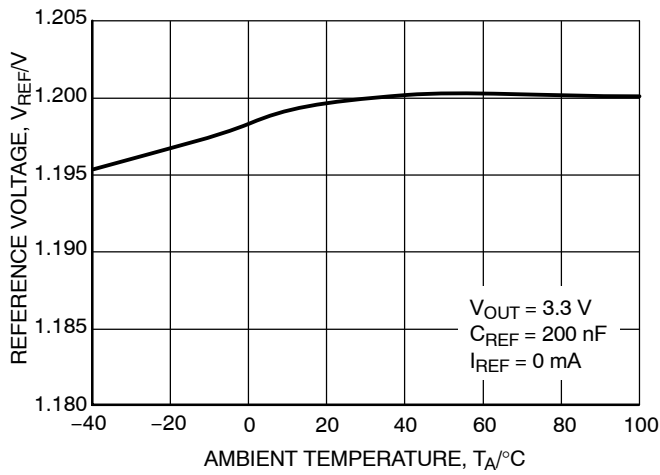


Figure 4. Reference Voltage vs. Temperature

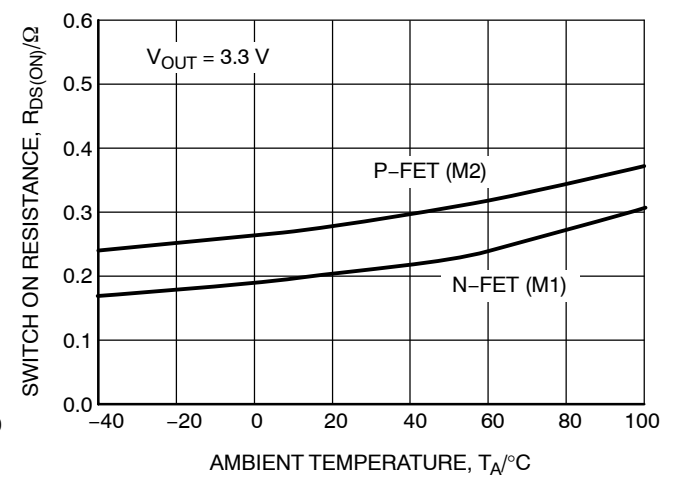


Figure 5. Switch ON Resistance vs. Temperature

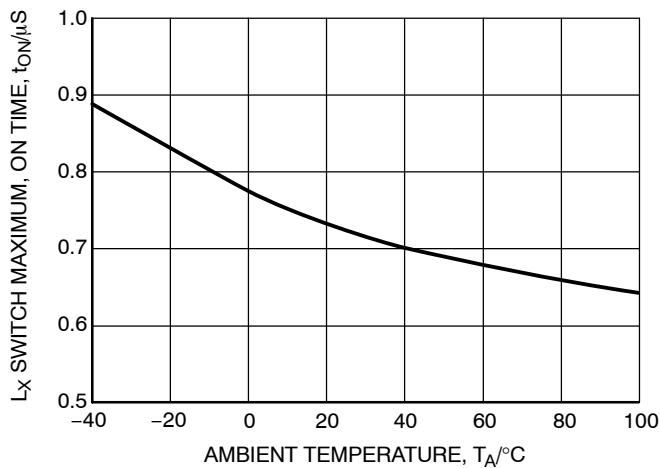


Figure 6. L_X Switch Max. ON Time vs. Temperature

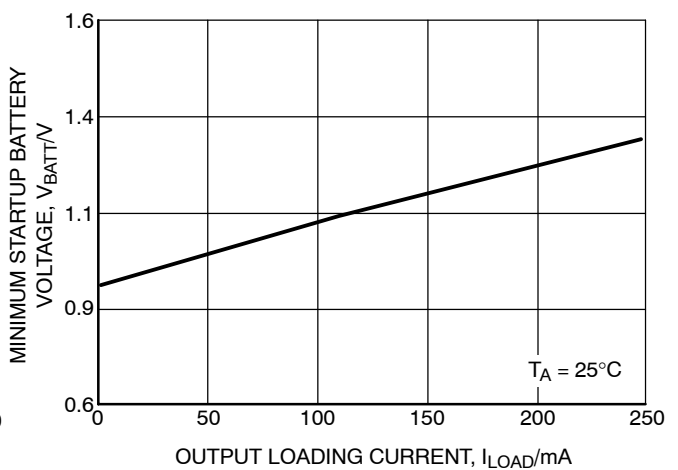


Figure 7. Minimum Startup Battery Voltage vs. Loading Current

TYPICAL OPERATING CHARACTERISTICS

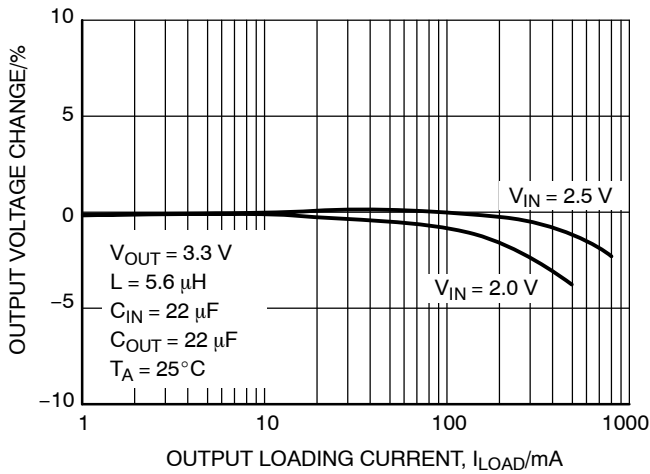


Figure 8. Output Voltage Change vs. Load Current

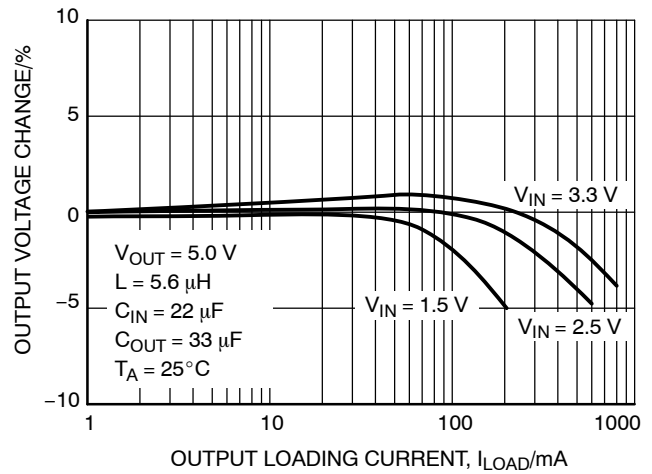


Figure 9. Output Voltage Change vs. Load Current

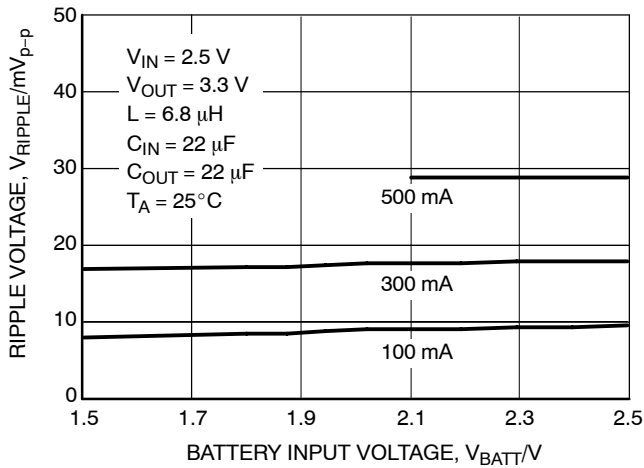


Figure 10. Battery Input Voltage vs. Output Ripple Voltage

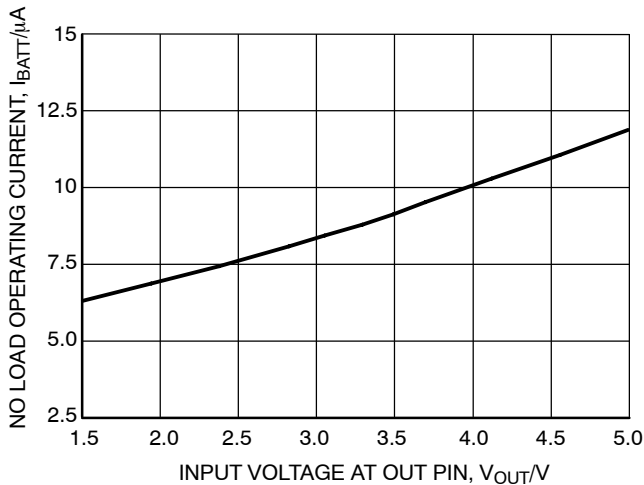


Figure 12. No Load Operating Current vs. Input Voltage at OUT Pin

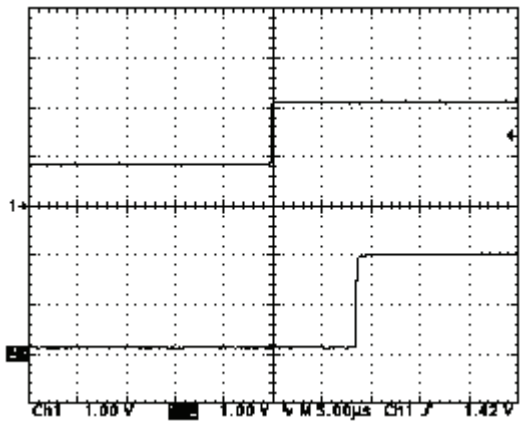
Upper Trace: Voltage at LBI Pin, 1.0 V/Division
Lower Trace: Voltage at LBO Pin, 1.0 V/Division

Figure 11. Low Battery Detect

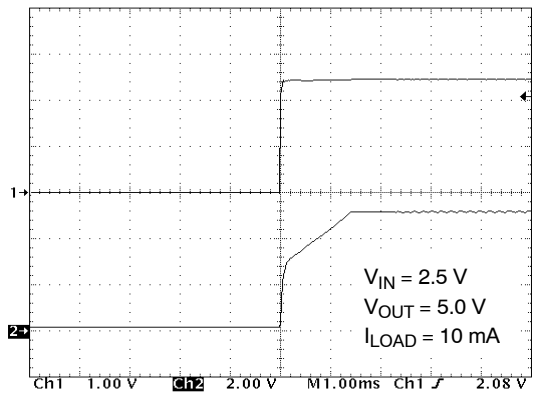
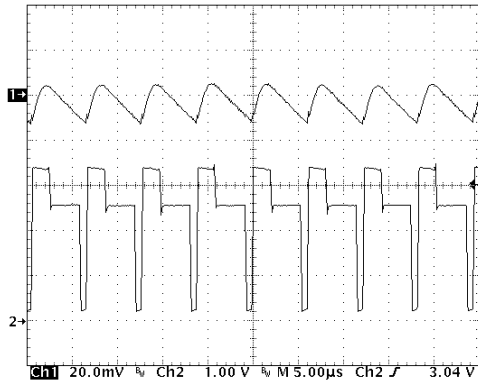
Upper Trace: Input Voltage Waveform, 1.0 V/Division
Lower Trace: Output Voltage Waveform, 2.0 V/Division

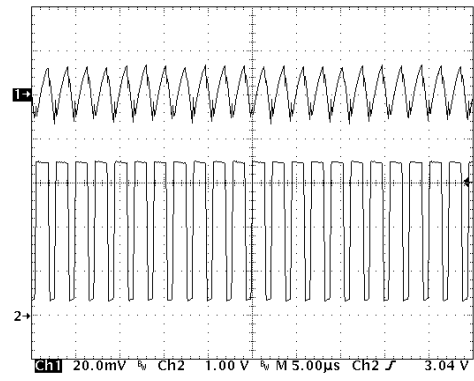
Figure 13. Startup Transient Response

TYPICAL OPERATING CHARACTERISTICS



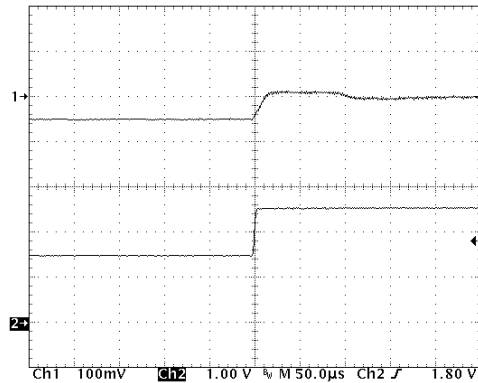
($V_{IN} = 2.5\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 50\text{ mA}$; $L = 5.6\text{ }\mu\text{H}$)
 Upper Trace: Output Voltage Ripple, 20 mV/Division
 Lower Trace: Voltage at Lx pin, 1.0 V/Division

Figure 14. Discontinuous Conduction Mode Switching Waveform



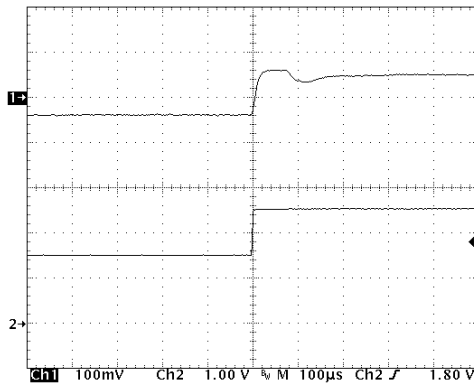
($V_{IN} = 2.5\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 500\text{ mA}$; $L = 5.6\text{ }\mu\text{H}$)
 Upper Trace: Output Voltage Ripple, 20 mV/Division
 Lower Trace: Voltage at LX pin, 1.0 V/Division

Figure 15. Continuous Conduction Mode Switching Waveform



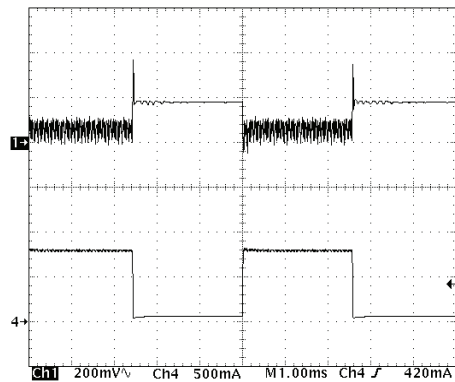
($V_{IN} = 1.5\text{ V to }2.5\text{ V}$; $L = 5.6\text{ }\mu\text{H}$, $C_{OUT} = 22\text{ }\mu\text{F}$, $I_{LOAD} = 100\text{ mA}$)
 Upper Trace: Output Voltage Ripple, 100 mV/Division
 Lower Trace: Battery Voltage, V_{IN} , 1.0 V/Division

Figure 16. Line Transient Response for $V_{OUT} = 3.3\text{ V}$



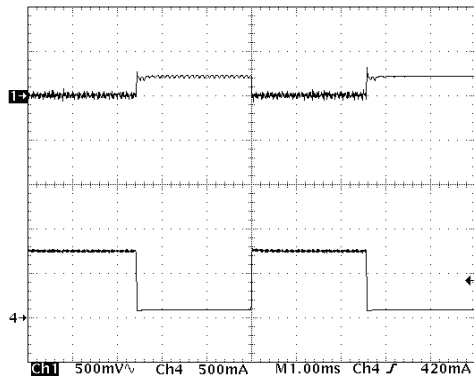
($V_{IN} = 1.5\text{ V to }2.5\text{ V}$; $L = 5.6\text{ }\mu\text{H}$, $C_{OUT} = 22\text{ }\mu\text{F}$, $I_{LOAD} = 100\text{ mA}$)
 Upper Trace: Output Voltage Ripple, 100 mV/Division
 Lower Trace: Battery Voltage, V_{IN} , 1.0 V/Division

Figure 17. Line Transient Response For $V_{OUT} = 5.0\text{ V}$



($V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 100\text{ mA to }800\text{ mA}$; $L = 5.6\text{ }\mu\text{H}$, $C_{OUT} = 22\text{ }\mu\text{F}$)
 Upper Trace: Output Voltage Ripple, 200 mV/Division
 Lower Trace: Load Current, I_{LOAD} , 500 mA/Division

Figure 18. Load Transient Response For $V_{IN} = 2.5\text{ V}$



($V_{OUT} = 5.0\text{ V}$, $I_{LOAD} = 100\text{ mA to }800\text{ mA}$; $L = 5.6\text{ }\mu\text{H}$, $C_{OUT} = 22\text{ }\mu\text{F}$)
 Upper Trace: Output Voltage Ripple, 500 mV/Division
 Lower Trace: Load Current, I_{LOAD} , 500 mA/Division

Figure 19. Load Transient Response For $V_{IN} = 3.0\text{ V}$

TYPICAL OPERATING CHARACTERISTICS

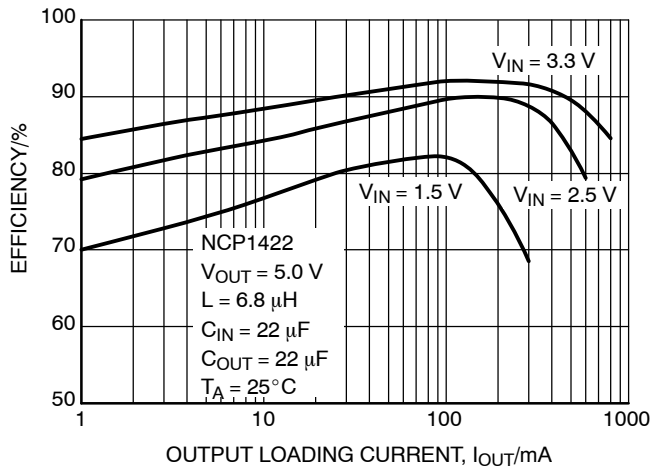


Figure 20. Efficiency vs. Load Current

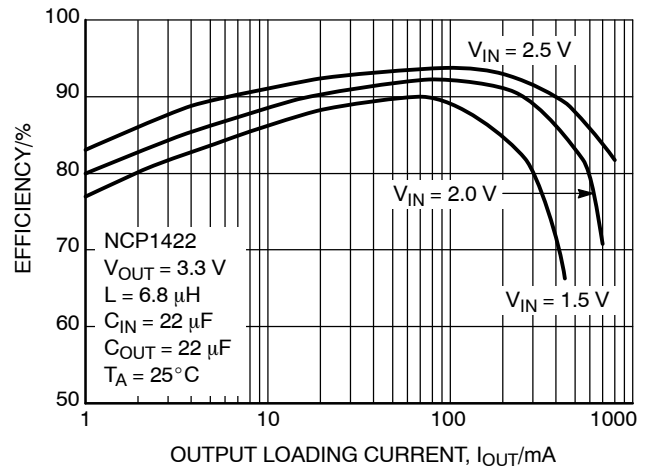


Figure 21. Efficiency vs. Load Current

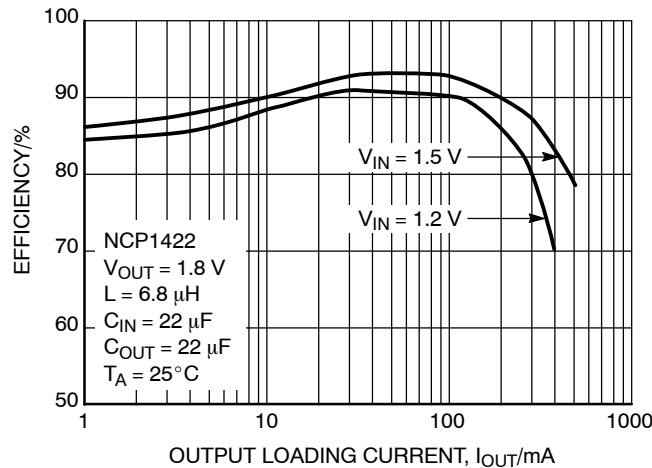


Figure 22. Efficiency vs. Load Current

DETAILED OPERATION DESCRIPTION

NCP1422 is a monolithic micropower high-frequency step-up voltage switching converter IC specially designed for battery operated hand-held electronic products up to 800 mA loading. It integrates a Synchronous Rectifier to improve efficiency as well as to eliminate the external Schottky diode. High switching frequency (up to 1.2 MHz) allows for a low profile inductor and output capacitor to be used. Low-Battery Detector, Logic-Controlled Shutdown, and Cycle-by-Cycle Current Limit provide value-added features for various battery-operated applications. With all these functions ON, the quiescent supply current is typically only 8.5 μ A. This device is available in a compact DFN-10 package.

PFM Regulation Scheme

From the simplified functional diagram (Figure 1), the output voltage is divided down and fed back to pin 1 (FB). This voltage goes to the non-inverting input of the PFM comparator whereas the comparator's inverting input is connected to the internal voltage reference, REF. A switching cycle is initiated by the falling edge of the comparator, at the moment the main switch (M1) is turned ON. After the maximum ON-time (typically 0.72 μ S) elapses or the current limit is reached, M1 is turned OFF and the synchronous switch (M2) is turned ON. The M1 OFF time is not less than the minimum OFF-time (typically 0.12 μ S), which ensures complete energy

transfer from the inductor to the output capacitor. If the regulator is operating in Continuous Conduction Mode (CCM), M2 is turned OFF just before M1 is supposed to be ON again. If the regulator is operating in Discontinuous Conduction Mode (DCM), which means the coil current will decrease to zero before the new cycle starts, M1 is turned OFF as the coil current is almost reaching zero. The comparator (ZLC) with fixed offset is dedicated to sense the voltage drop across M2 as it is conducting; when the voltage drop is below the offset, the ZLC comparator output goes HIGH and M2 is turned OFF. Negative feedback of closed-loop operation regulates voltage at pin1 (FB) equal to the internal reference voltage (1.20 V).

Synchronous Rectification

The Synchronous Rectifier is used to replace the Schottky Diode to reduce the conduction loss contributed by the forward voltage of the Schottky Diode. The Synchronous Rectifier is normally realized by powerFET with gate control circuitry that incorporates relatively complicated timing concerns.

As the main switch (M1) is being turned OFF and the synchronous switch M2 is just turned ON with M1 not being completely turned OFF, current is shunt from the output bulk capacitor through M2 and M1 to ground. This power loss lowers overall efficiency and possibly damages the switching FETs. As a general practice, a certain amount of dead time is introduced to make sure M1 is completely turned OFF before M2 is turned ON.

The previously mentioned situation occurs when the regulator is operating in CCM, M2 is turned OFF, M1 is just turned ON, and M2 is not completely turned OFF. A dead time is also needed to make sure M2 is completely turned OFF before M1 is turned ON.

As coil current is dropped to zero when the regulator is operating in DCM, M2 should be OFF. If this does not occur, the reverse current flows from the output bulk capacitor through M2 and the inductor to the battery input, causing damage to the battery. The ZLC comparator comes with fixed offset voltage to switch M2 OFF before any reverse current builds up. However, if M2 is switched OFF too early, large residue coil current flows through the body diode of M2 and increases conduction loss. Therefore, determination of the offset voltage is essential for optimum performance. With the implementation of the synchronous rectification scheme, efficiency can be as high as 94% with this device.

Cycle-by-Cycle Current Limit

In Figure 1, a SENSEFET is used to sample the coil current as M1 is ON. With that sample current flowing through a sense resistor, a sense-voltage is developed. The threshold detector (I_{LIM}) detects whether the sense-voltage is higher than the preset level. If the sense voltage is higher than the present level, the detector output notifies the Control Logic to switch OFF M1, and M1 can only be switched ON when the next cycle starts after the minimum OFF-time (typically 0.12 μ S). With proper sizing of the SENSEFET and sense resistor, the peak coil current limit is typically set at 1.5 A.

Voltage Reference

The voltage at REF is typically set at 1.20 V and can output up to 2.5 mA with load regulation $\pm 2\%$ at V_{OUT} equal to 3.3 V. If V_{OUT} is increased, the REF load capability can also be increased. A bypass capacitor of 200 nF is required for proper operation when REF is not loaded. If REF is loaded, a 1.0 μ F capacitor at the REF pin is needed.

True-Cutoff

The NCP1422 has a True-Cutoff function controlled by the multi-function pin LBI/EN (pin 2). Internal circuitry can isolate the current through the body diode of switch M2 to load. Thus, it can eliminate leakage current from the battery to load in shutdown mode and significantly reduce battery current consumption during shutdown. The shutdown function is controlled by the voltage at pin 2 (LBI/EN). When pin 2 is pulled to lower than 0.3 V, the controller enters shutdown mode. In shutdown mode, when switches M1 and M2 are both switched OFF, the internal reference voltage of the controller is disabled and the controller typically consumes only 50 nA of current. If the pin 2 voltage is raised to higher than 0.5 V (for example, by a resistor connected to V_{IN}), the IC is enabled again, and the internal circuit typically consumes 8.5 μ A of current from the OUT pin during normal operation.

Low-Battery Detection

A comparator with 30 mV hysteresis is applied to perform the low-battery detection function. When pin 2 (LBI/EN) is at a voltage (defined by a resistor divider from the battery voltage) lower than the internal reference voltage of 1.20 V, the comparator output turns on a 50 Ω low side switch. It pulls down the voltage at pin 3 (LBO) which has hundreds of k Ω of pull-high resistance. If the pin 2 voltage is higher than 1.20 V + 30 mV, the comparator output turns off the 50 Ω low side switch. When this occurs, pin 3 becomes high impedance and its voltage is pulled high again.

APPLICATIONS INFORMATION

Output Voltage Setting

A typical application circuit is shown in Figure 23. The output voltage of the converter is determined by the external feedback network comprised of R1 and R2. The relationship is given by:

$$V_{OUT} = 1.20 \text{ V} \times \left(1 + \frac{R1}{R2}\right)$$

where R1 and R2 are the upper and lower feedback resistors, respectively.

Low Battery Detect Level Setting

The Low Battery Detect Voltage of the converter is determined by the external divider network that is comprised of R3 and R4. The relationship is given by:

$$V_{LB} = 1.20 \text{ V} \times \left(1 + \frac{R3}{R4}\right)$$

where R3 and R4 are the upper and lower divider resistors respectively.

Inductor Selection

The NCP1422 is tested to produce optimum performance with a 5.6 μH inductor at $V_{IN} = 2.5 \text{ V}$ and $V_{OUT} = 3.3 \text{ V}$, supplying an output current up to 800 mA. For other input/output requirements, inductance in the range 3 μH to 10 μH can be used according to end application specifications. Selecting an inductor is a compromise between output current capability, inductor saturation limit, and tolerable output voltage ripple. Low inductance values can supply higher output current but also increase the ripple at output and reduce efficiency. On the other hand, high inductance values can improve output ripple and efficiency; however, it is also limited to the output current capability at the same time.

Another parameter of the inductor is its DC resistance. This resistance can introduce unwanted power loss and reduce overall efficiency. The basic rule is to select an inductor with the lowest DC resistance within the board space limitation of the end application. In order to help with the inductor selection, reference charts are shown in Figures 24 and 25.

Capacitors Selection

In all switching mode boost converter applications, both the input and output terminals see impulsive

voltage/current waveforms. The currents flowing into and out of the capacitors multiply with the Equivalent Series Resistance (ESR) of the capacitor to produce ripple voltage at the terminals. During the Syn–Rect switch–off cycle, the charges stored in the output capacitor are used to sustain the output load current. Load current at this period and the ESR combine and reflect as ripple at the output terminals. For all cases, the lower the capacitor ESR, the lower the ripple voltage at output. As a general guideline, low ESR capacitors should be used. Ceramic capacitors have the lowest ESR, but low ESR tantalum capacitors can also be used as an alternative.

PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise, and unwanted feedback that can affect the performance of the converter. Hints suggested below can be used as a guideline in most situations.

Grounding

A star–ground connection should be used to connect the output power return ground, the input power return ground, and the device power ground together at one point. All high–current paths must be as short as possible and thick enough to allow current to flow through and produce insignificant voltage drop along the path. The feedback signal path must be separated from the main current path and sense directly at the anode of the output capacitor.

Components Placement

Power components (i.e., input capacitor, inductor and output capacitor) must be placed as close together as possible. All connecting traces must be short, direct, and thick. High current flowing and switching paths must be kept away from the feedback (FB, pin 1) terminal to avoid unwanted injection of noise into the feedback path.

Feedback Network

Feedback of the output voltage must be a separate trace detached from the power path. The external feedback network must be placed very close to the feedback (FB, pin 1) pin and sense the output voltage directly at the anode of the output capacitor.

NCP1422

TYPICAL APPLICATION CIRCUIT

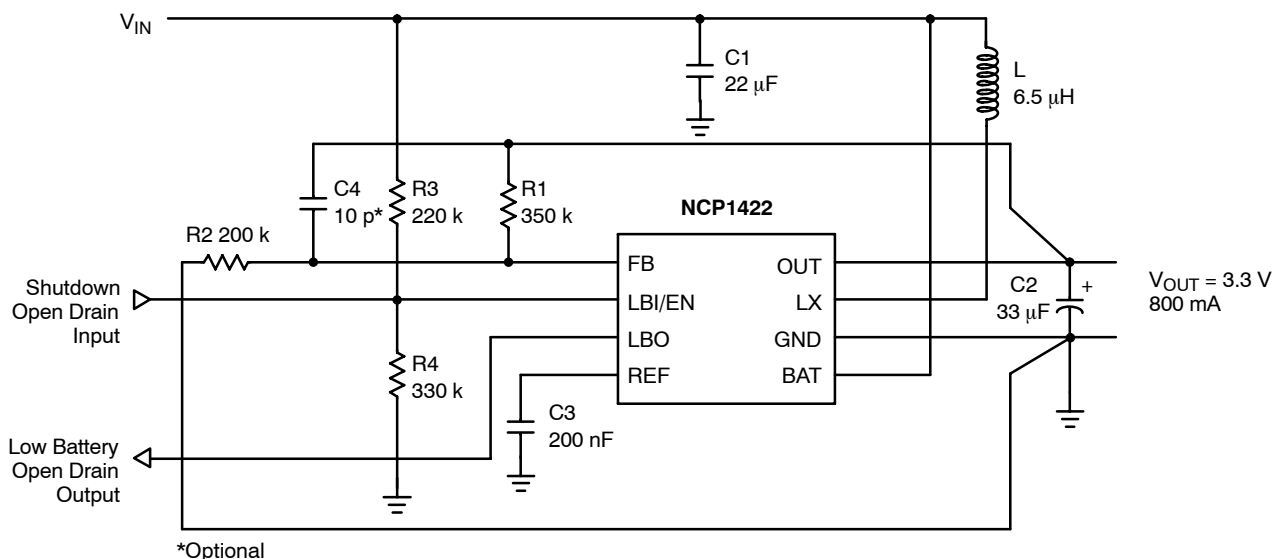


Figure 23. Typical Application Schematic for 2 Alkaline Cells Supply

GENERAL DESIGN PROCEDURES

Switching mode converter design is considered a complicated process. Selecting the right inductor and capacitor values can allow the converter to provide optimum performance. The following is a simple method based on the basic first-order equations to estimate the inductor and capacitor values for NCP1422 to operate in Continuous Conduction Mode (CCM). The set component values can be used as a starting point to fine tune the application circuit performance. Detailed bench testing is still necessary to get the best performance out of the circuit.

Design Parameters:

- $V_{IN} = 1.8 \text{ V to } 3.0 \text{ V, Typical } 2.4 \text{ V}$
- $V_{OUT} = 3.3 \text{ V}$
- $I_{OUT} = 500 \text{ mA}$
- $V_{LB} = 2.0 \text{ V}$
- $V_{OUT-RIPPLE} = 40 \text{ mV}_{P-P} \text{ at } I_{OUT} = 500 \text{ mA}$

Calculate the feedback network:

Select $R2 = 200 \text{ k}$

$$R1 = R2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

$$R1 = 200 \text{ k} \left(\frac{3.3 \text{ V}}{1.20 \text{ V}} - 1 \right) = 350 \text{ k}$$

Calculate the Low Battery Detect divider:

- $V_{LB} = 2.0 \text{ V}$
- Select $R4 = 330 \text{ k}$

$$R3 = R4 \left(\frac{V_{LB}}{V_{REF}} - 1 \right)$$

$$R3 = 300 \text{ k} \left(\frac{2.0 \text{ V}}{1.20 \text{ V}} - 1 \right) = 220 \text{ k}$$

Determine the Steady State Duty Ratio, D , for typical V_{IN} . The operation is optimized around this point:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D}$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}} = 1 - \frac{2.4 \text{ V}}{3.3 \text{ V}} = 0.273$$

Determine the average inductor current, I_{LAVG} , at maximum I_{OUT} :

$$I_{LAVG} = \frac{I_{OUT}}{1 - D} = \frac{500 \text{ mA}}{1 - 0.273} = 688 \text{ mA}$$

Determine the peak inductor ripple current, $I_{RIPPLE-P}$, and calculate the inductor value:

Assume $I_{RIPPLE-P}$ is 20% of I_{LAVG} . The inductance of the power inductor can be calculated as follows:

$$L = \frac{V_{IN} \times t_{ON}}{2 I_{RIPPLE-P}} = \frac{2.4 \text{ V} \times 0.75 \mu\text{s}}{2 (137.6 \text{ mA})} = 6.5 \mu\text{H}$$

A standard value of $6.5 \mu\text{H}$ is selected for initial trial.

Determine the output voltage ripple, $V_{OUT-RIPPLE}$, and calculate the output capacitor value:

$V_{OUT-RIPPLE} = 40 \text{ mV}_{P-P} \text{ at } I_{OUT} = 500 \text{ mA}$

$$C_{OUT} > \frac{I_{OUT} \times t_{ON}}{V_{OUT-RIPPLE} - I_{OUT} \times ESR_{COUT}}$$

where $t_{ON} = 0.75 \mu\text{s}$ and $ESR_{COUT} = 0.05 \Omega$,

$$C_{OUT} > \frac{500 \text{ mA} \times 0.75 \mu\text{s}}{45 \text{ mV} - 500 \text{ mA} \times 0.05 \Omega} = 18.75 \mu\text{F}$$

NCP1422

From the previous calculations, you need at least 18.75 μF in order to achieve the specified ripple level at the conditions stated. Practically, a capacitor that is one level larger is used to accommodate factors not taken into account in the calculations. Therefore, a capacitor value of 22 μF is selected. The NCP1422 is internally compensated for most applications, but in case additional compensation

is required, the capacitor C4 can be used as external compensation adjustment to improve system dynamics.

In order to provide an easy way for customers to select external parts for NCP1422 in different input voltage and output current conditions, values of inductance and capacitance are suggested in Figures 24, 25 and 26.

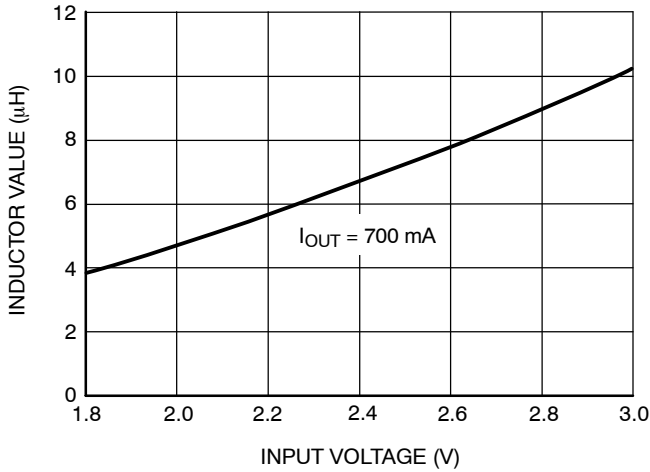


Figure 24. Suggested Inductance of $V_{OUT} = 3.3\text{ V}$

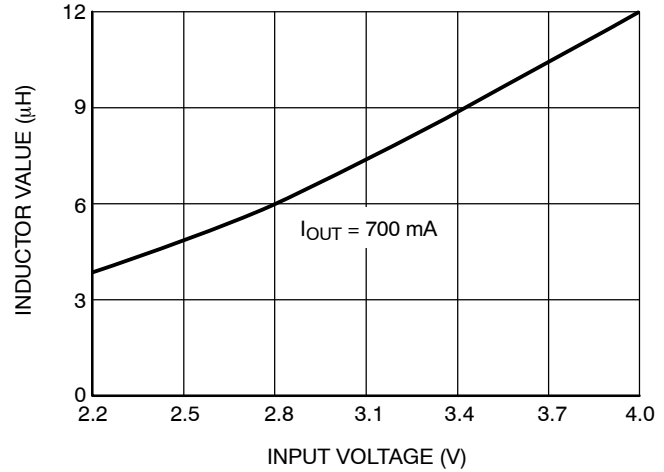


Figure 25. Suggested Inductance of $V_{OUT} = 5.0\text{ V}$

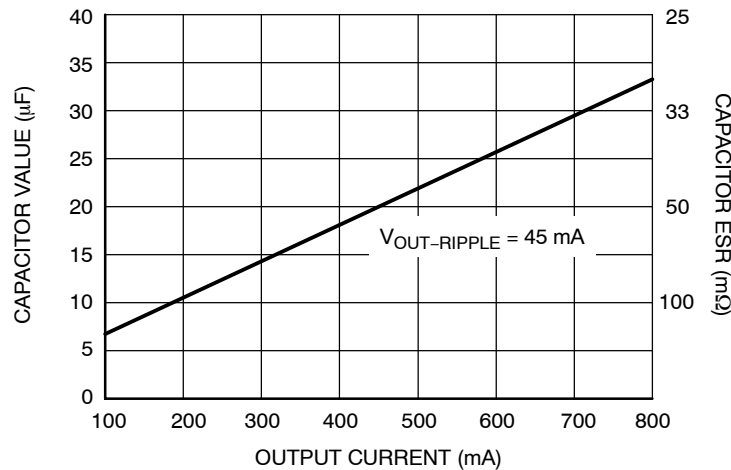


Figure 26. Suggested Capacitance for Output Capacitor

Table 4. Suggestions for Passive Components

Output Current	Inductors	Capacitors
800 mA	Sumida CR43, CR54, CDRH6D28 series	Panasonic ECJ series Kemet TL494 series
250 mA	Sumida CR32 series	Panasonic ECJ series Kemet TL494 series

NCP1423

400 mA Sync-Rect PFM Step-Up DC-DC Converter with True-Cutoff and Ring-Killer

NCP1423 is a monolithic micropower high frequency step-up switching converter IC specially designed for battery operated hand-held electronic products. It integrates Synchronous Rectifier for improving efficiency as well as eliminating the external Schottky Diode. High switching frequency (up to 600 kHz) allows low profile inductor and output capacitor being used. When the IC is disabled, internal conduction path from LX or BAT to OUT is blocked, OUT pin is isolated from the battery. This achieves True-Cutoff. Ring-Killer is also integrated to eliminate the high frequency ringing in discontinuous conduction mode. Low-Battery Detector, Cycle-by-Cycle Current Limit, Overvoltage Protection and Thermal Shutdown provide value-added features for various battery operated application. With all of these functions ON, the quiescent supply current is only 9.0 μ A. This device is available in compact Micro10 package.

Features

- High Efficiency: 92% for 3.3 V Output@ 400 mA from 2.5 V Input
91% for 1.8 V Output@ 70 mA from 1.2 V Input
- High Switching Frequency, up to 600 kHz (not hitting current limit)
- Low Quiescent Current of 9.0 μ A
- Low Battery Detector
- 0.8 V Startup at No Load Guaranteed
- External Adjustable Output Voltage
- $\pm 1.5\%$ Output Voltage Accuracy
- Ring-Killer for Discontinuous Conduction Mode
- Thermal Shutdown
- 1.2 A Cycle-by-Cycle Current Limit
- Output Current up to 400 mA @ $V_{OUT} = 3.3$ V,
200 mA @ $V_{OUT} = 1.8$ V
- Overvoltage Protection
- Low Profile and Minimum External Part
- Open Drain Low-Battery Detector Output
- Compact Micro10 Package
- Pb-Free Package is Available

Typical Applications

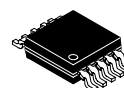
- Wireless Optical Mouse
- Wireless Headsets
- Internet Audio Players
- Personal Digital Assistants (PDAs)
- Hand-held Instruments
- Conversion from one/two NiMH or NiCd cells to 1.8 V / 3.3 V



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MARKING DIAGRAM

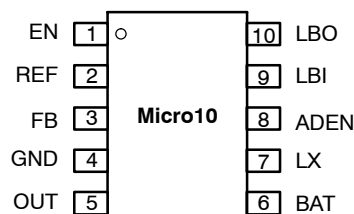


Micro10
DM SUFFIX
CASE 846B



DAR = Device Code
A = Assembly Location
Y = Year
W = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1423DMR2	Micro10	3000 Tape & Reel
NCP1423DMR2G	Micro10 (Pb-Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP1423

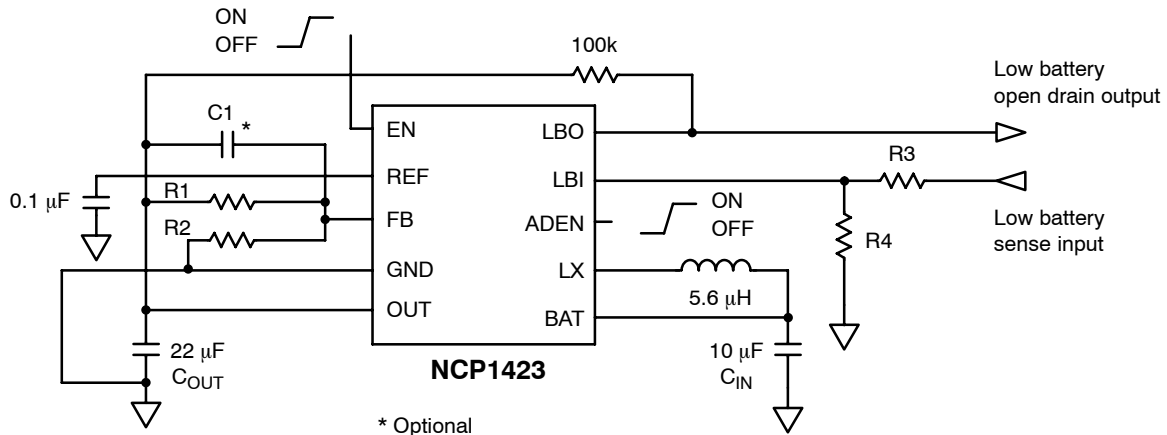


Figure 27. Typical Operation Circuit

PIN DESCRIPTION

Pin No.	Symbol	Description
1	EN	Low-Battery Detector Input and Enable. With this pin pulled down below 0.5 V, the device will be disabled and will enter shutdown mode
2	REF	1.195 V Reference Voltage Output, bypass with 0.1 μ F capacitor if this pin is not loaded, with a 1.0 μ F bypassing capacitor, this pin can be loaded up to 2.5 mA @ $V_{OUT} = 3.3$ V.
3	FB	Output Voltage Feedback Input
4	GND	Ground
5	OUT	Power Output. OUT provides bootstrap power to the IC
6	BAT	Battery supply input pin and connection for internal Ring-Killer
7	LX	N-Channel and P-Channel Power MOSFET Drain
8	ADEN	Auto Discharge Input
9	LBI	Low-Battery Detector Input
10	LBO	Open-Drain Low-Battery Detector Output. Output is Low when $V_{LBI} < 500$ mV. LBO is high impedance shutdown

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply (Pin 6)	V_{OUT}	-0.3, 6.0	V
Input / Output Pins (Pins 1-3,5,7-10)	V_{IO}	-0.3, 6.0	V
Thermal Characteristics Micro10 Plastic Package, Case 846B, $T_A = 25^\circ\text{C}$ Thermal Resistance Junction-to-Air	P_D $R_{\theta JA}$	480 250	mW $^\circ\text{C/W}$
Operating Junction Temperature Range	T_J	- 40 to + 150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	- 40 to + 85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 55 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

NOTE: ESD data available upon request.

- This device contains ESD protection and exceeds the following tests:
Human Body Model (HBM) ± 2.0 kV per JEDEC standard: JESD22-A114.
Machine Model (MM) ± 200 V per JEDEC standard: JESD22-A115.
- The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

- Latchup Current Maximum Rating: ± 150 mA per JEDEC standard: JESD78.
- Moisture Sensitivity Level: MSL 1 per IPC/JEDEC standard: J-STD-020A.
- Measured on approximately 1 in sq of 1 oz Cu.

NCP1423

ELECTRICAL CHARACTERISTICS

($V_{OUT} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ for typical value, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for min/max values unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage	V_{IN}	0.8	–	V_{OUT}	V
Output Voltage Range	V_{OUT}	1.8	–	3.3	V
Minimum Input Voltage for startup ($R_{LOAD} = 33\ \Omega$)	V_{IN_MIN}	–	0.85	0.90	V
Reference Voltage ($I_{LOAD} = 0\text{ mA}$, $C_{REF} = 100\text{ nF}$, $T_A = 25^\circ\text{C}$)	V_{REF}	1.177	1.195	1.213	V
Reference Voltage Temperature Coefficient	TC_{VREF}	–	0.05	–	mV/ $^\circ\text{C}$
FB Input Threshold ($I_{LOAD} = 0\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C)	V_{FB}	0.489	0.500	0.512	V
FB Input Threshold ($I_{LOAD} = 0\text{ mA}$, $T_A = 25^\circ\text{C}$)	V_{FB}	0.493	0.500	0.508	V
FB Input Current	I_{FB}	–	1.0	–	nA
Internal NFET ON-Resistance ($I_{LX} = 100\text{ mA}$, $T_A = 25^\circ\text{C}$) (Note 7)	$R_{DS(ON)\_N}$	–	0.3	0.45	Ω
Internal PFET ON-Resistance ($I_{LX} = 100\text{ mA}$, $T_A = 25^\circ\text{C}$) (Note 7)	$R_{DS(ON)\_P}$	–	0.6	0.8	Ω
LX Switch Current Limit (NFET) (Note 7)	I_{LIM}	–	1.2	–	A
Operating Current into OUT ($V_{FB} = 0.7\text{ V}$, $T_A = 25^\circ\text{C}$)	I_Q	–	9.0	12	μA
Operating Current into BAT ($V_{BAT} = 1.2\text{ V}$, $V_{FB} = 0.7\text{ V}$, $V_{LX} = 1.2\text{ V}$, $T_A = 25^\circ\text{C}$)	I_{QBAT}	–	2.0	3.0	μA
Shutdown Current into BAT ($LBI/EN = 0\text{ V}$, $V_{BAT} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$)	I_{BAT_SD}	–	0.5	1.5	μA
LX Switch MAX. ON-Time ($V_{FB} = 0\text{ V}$)	t_{ON}	1.15	1.4	2.8	μs
LX Switch MIN. OFF-Time ($V_{FB} = 0\text{ V}$)	t_{OFF}	80	200	350	ns
BAT to LX Resistance ($V_{FB} = 0.7\text{ V}$)	R_{BAT_LX}	–	100	–	Ω
LBI Input Threshold	V_{LBI}	0.475	0.500	0.525	V
LBI Input Hysteresis	V_{LBI_HYS}	–	15	–	mV
LBI Input Current	I_{LBI}	–	1.5	–	nA
LBO Low Output Voltage ($V_{LBI} = 0\text{ V}$, $I_{SINK} = 1.0\text{ mA}$)	V_{LBO_L}	–	–	0.2	V
Minimum Output Current ($V_{IN} = 2.5\text{ V}$, $V_{OUT} = 3.3\text{ V}$) (Note 7)	I_{OUT}	200	–	–	mA
Minimum Output Current ($V_{IN} = 0.8\text{ V}$, $V_{OUT} = 3.3\text{ V}$) (Note 7)	I_{OUT}	100	–	–	mA
Soft Start Time ($V_{IN} = 1.2\text{ V}$, $T_A = 25^\circ\text{C}$, $C_{REF} = 100\text{ nF}$, $V_{OUT} = 3.3\text{ V}$) (Note 6)	T_{SS}	–	2.0	8.0	ms
EN Shutdown Threshold ($V_{BAT} = 1.2\text{ V}$)	V_{SHDN}	0.34	0.50	0.68	V
EN Input Current	I_{EN}	–	150	–	nA
ADEN Threshold ($V_{BAT} = 0.9\text{ V}$ to 3.3 V)	V_{ADEN}		$0.5 \cdot V_{BAT}$		V
ADEN Input Current	I_{ADEN}	–	100	–	nA
ADEN Switch Resistance	R_{ADEN}		100		Ω
Thermal Shutdown Temperature (Note 7)	T_{SHDN}	–	–	145	$^\circ\text{C}$
Thermal Shutdown Hysteresis (Note 7)	T_{SDHYS}	–	30	–	$^\circ\text{C}$

6. Value depends on voltage at V_{OUT} .

7. Values are guaranteed by design.

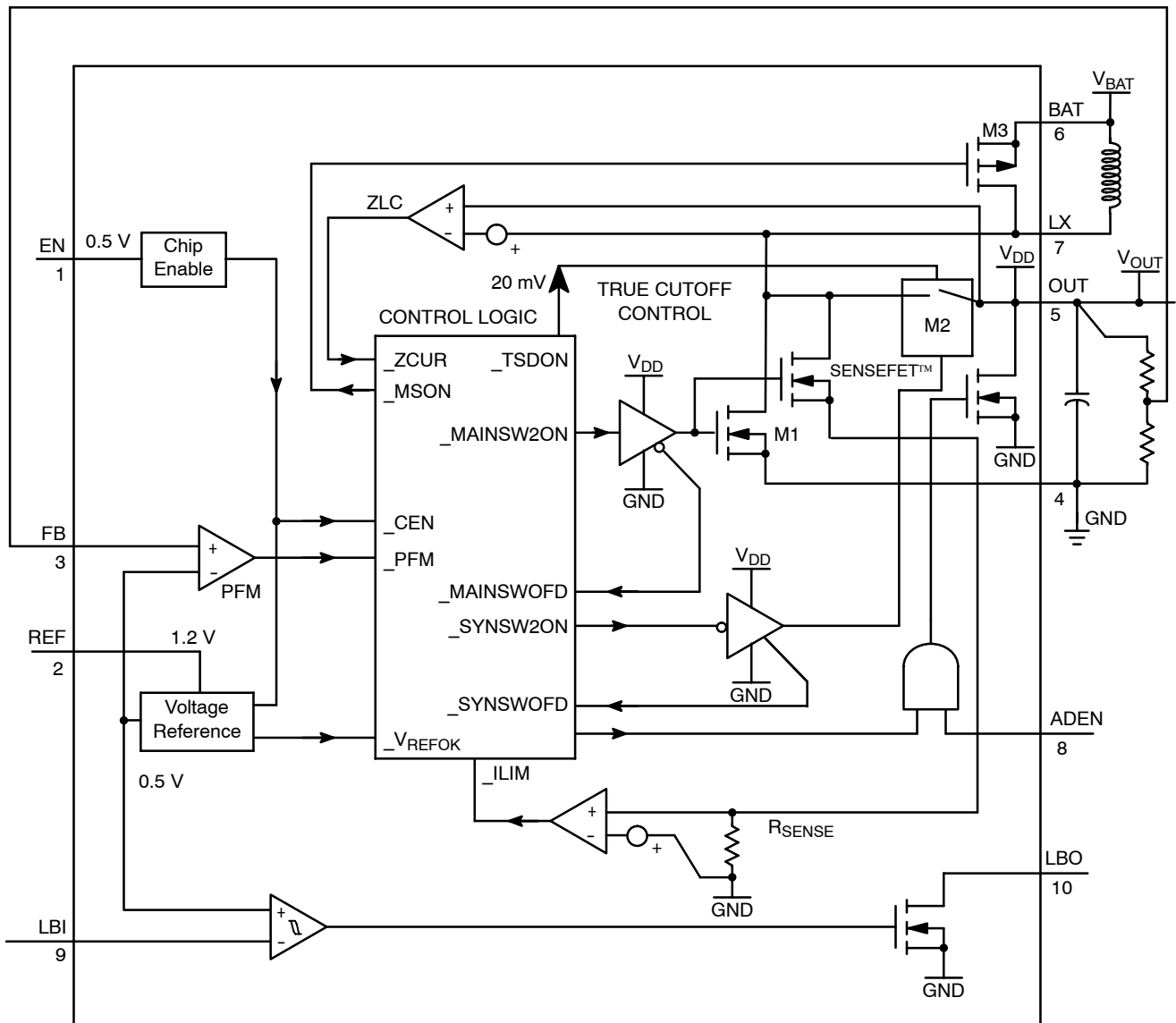


Figure 28. Detailed Block Diagram

TYPICAL OPERATING CHARACTERISTICS

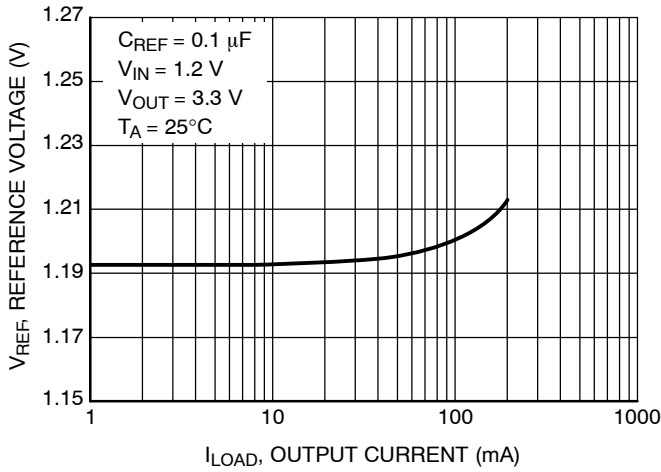


Figure 29. Reference Voltage vs. Output Current

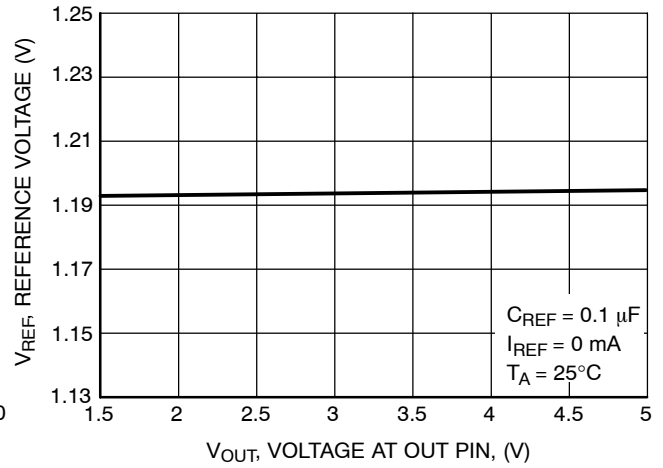


Figure 30. Reference Voltage vs. Voltage at OUT Pin

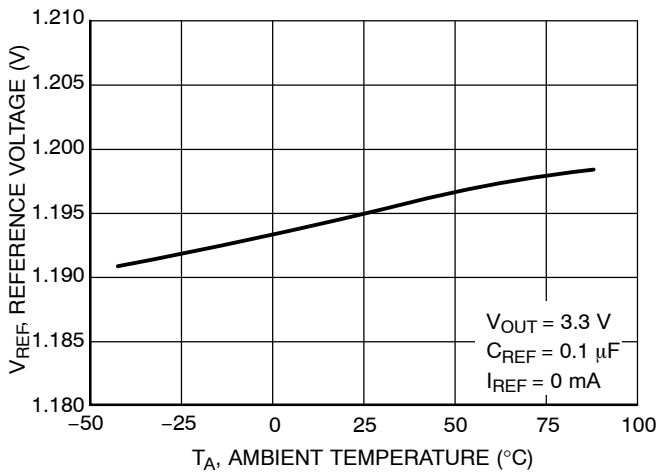


Figure 31. Reference Voltage vs. Temperature

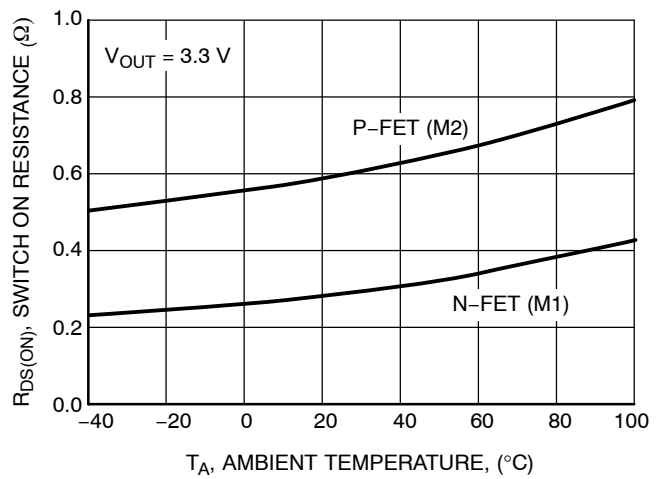


Figure 32. Switch ON Resistance vs. Temperature

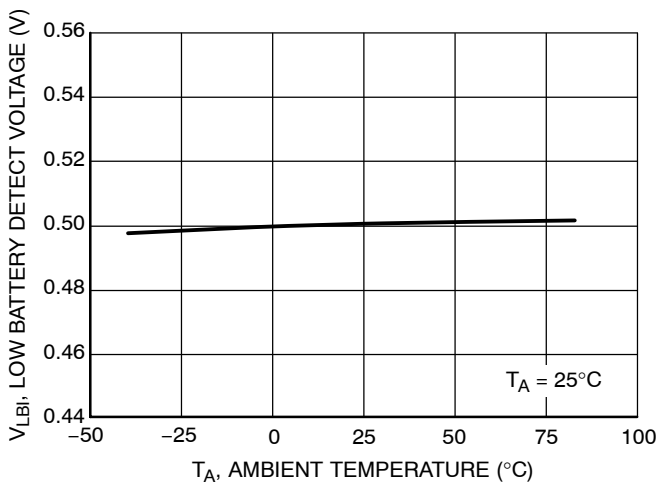


Figure 33. Low Battery Detect Voltage vs. Temperature

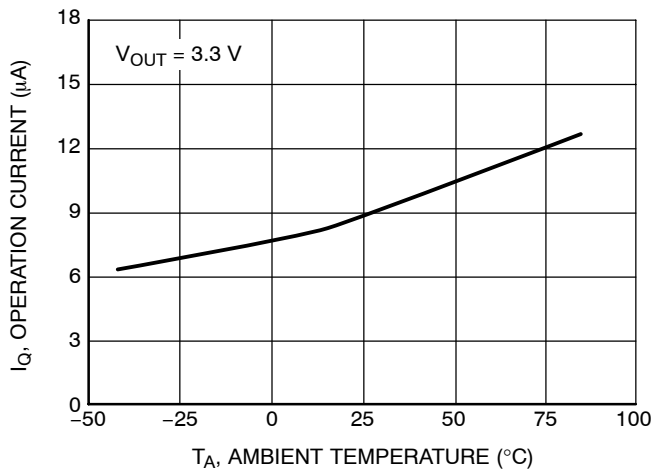


Figure 34. Operation Current vs. Temperature

TYPICAL OPERATING CHARACTERISTICS

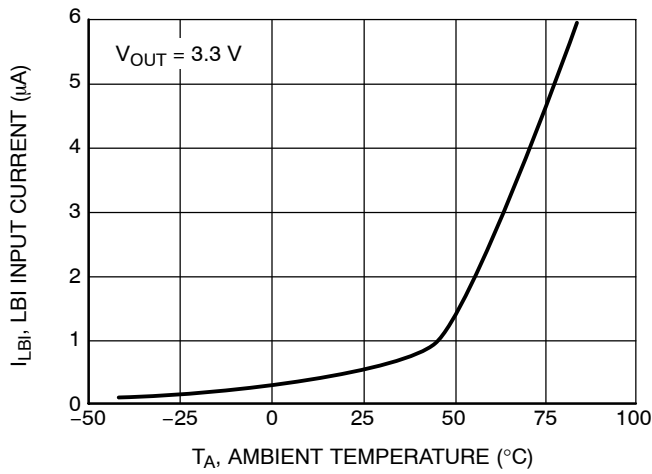


Figure 35. LBI Input Current vs. Temperature

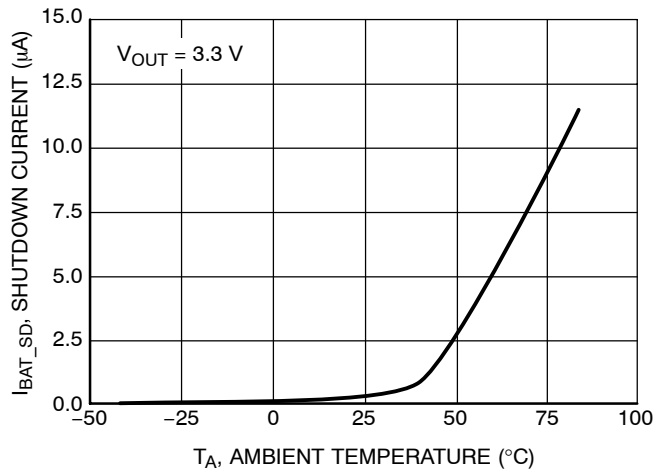


Figure 36. Shutdown Current vs. Temperature

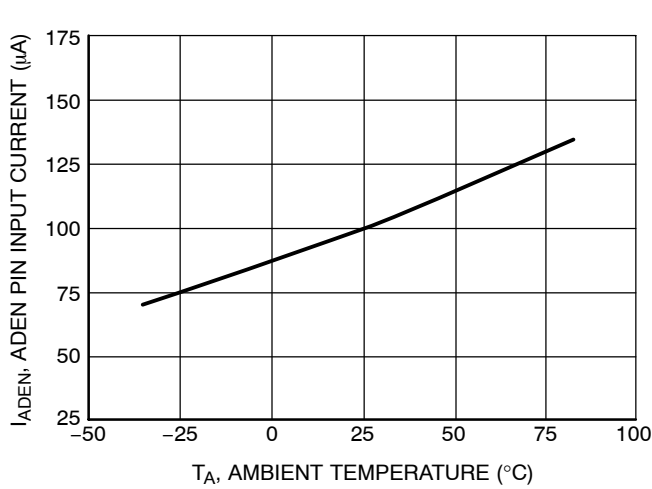


Figure 37. ADEN Pin Input Current vs. Temperature

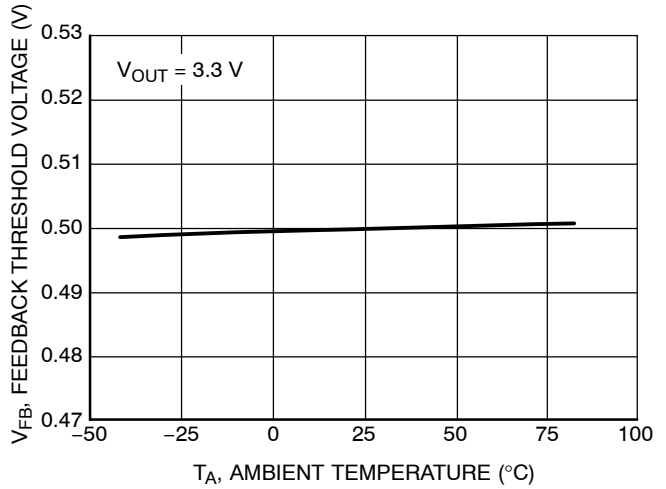


Figure 38. Feedback Threshold Voltage vs. Temperature

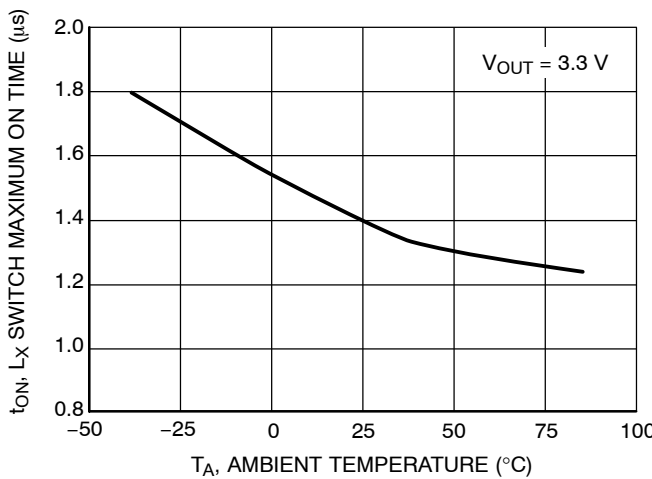


Figure 39. L_X Switch Maximum ON Time vs. Temperature

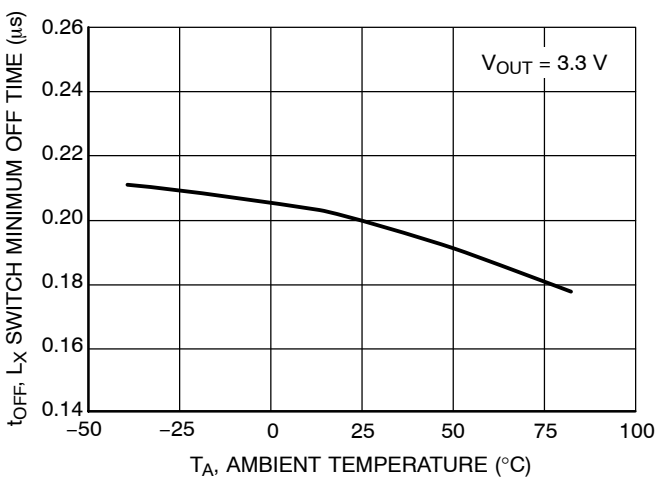


Figure 40. L_X Switch Minimum OFF Time vs. Temperature

TYPICAL OPERATING CHARACTERISTICS

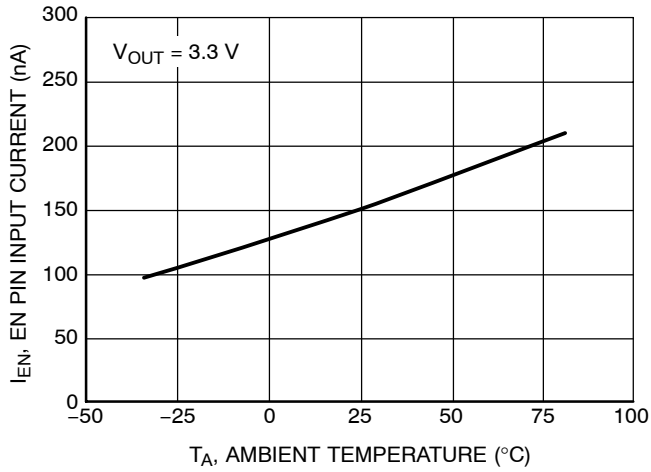


Figure 41. EN Input Current vs. Temperature

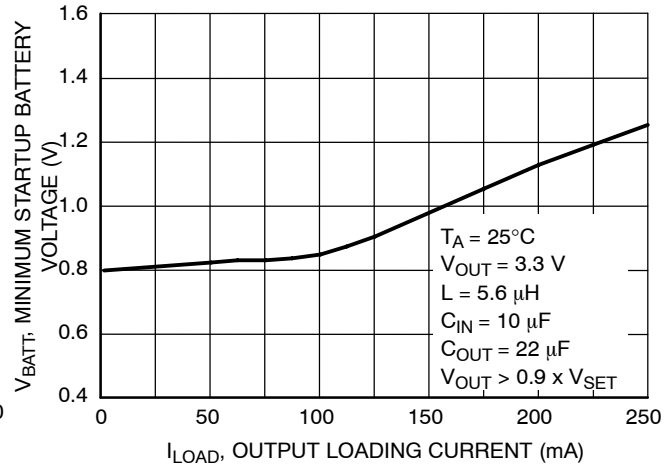


Figure 42. Minimum Startup Battery Voltage vs. Loading Current

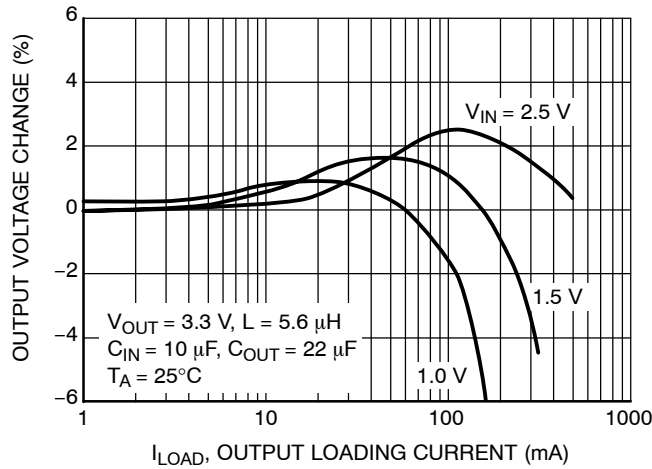


Figure 43. Output Voltage Change vs. Load Current

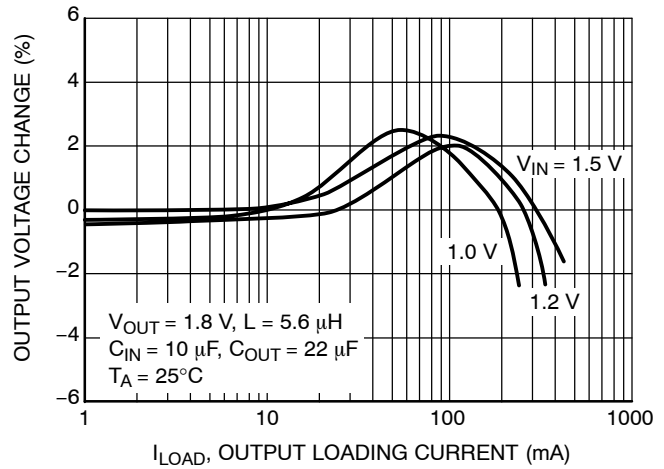


Figure 44. Output Voltage Change vs. Load Current

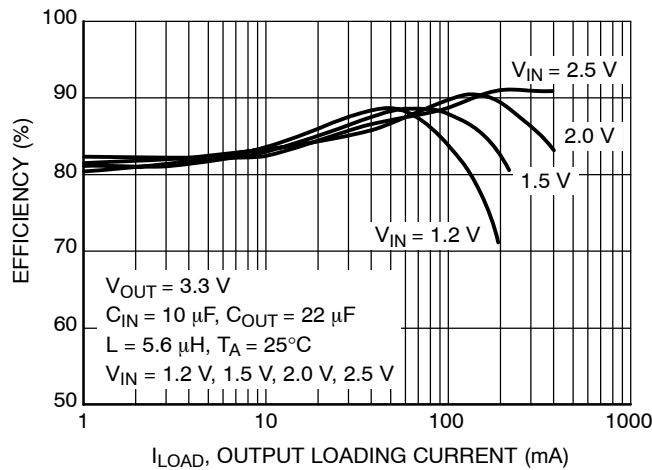


Figure 45. Efficiency vs. Load Current

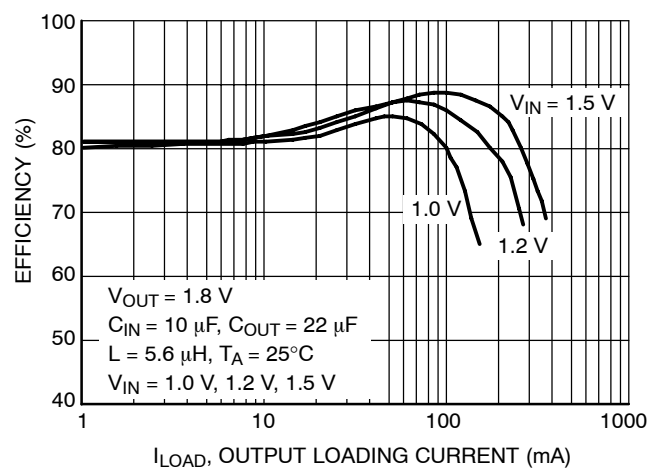


Figure 46. Efficiency vs. Load Current

TYPICAL OPERATING CHARACTERISTICS

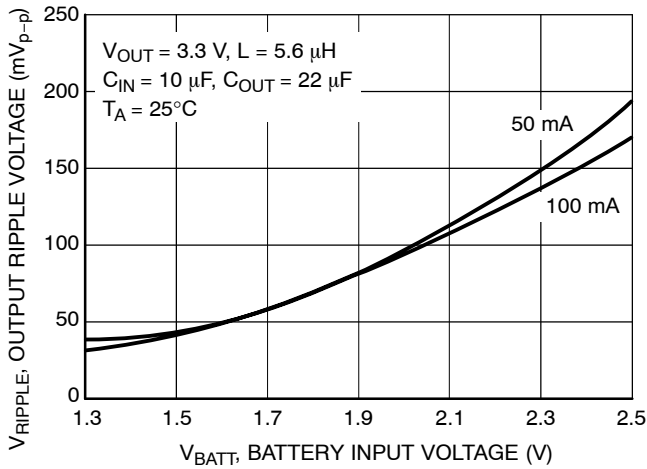


Figure 47. Output Ripple Voltage vs. Battery Input Voltage

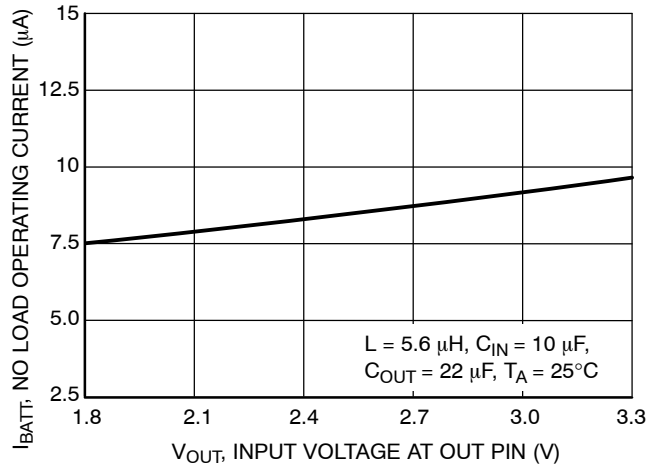
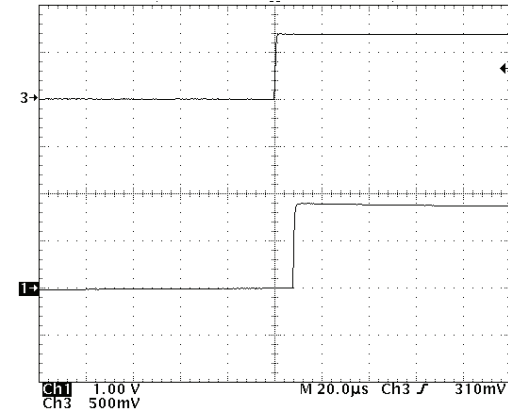
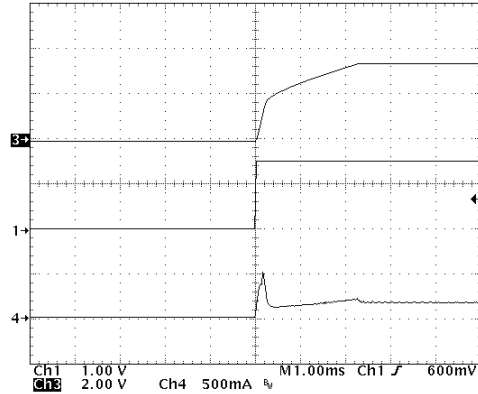


Figure 48. No Load Operating Current vs. Input Voltage at OUT Pin



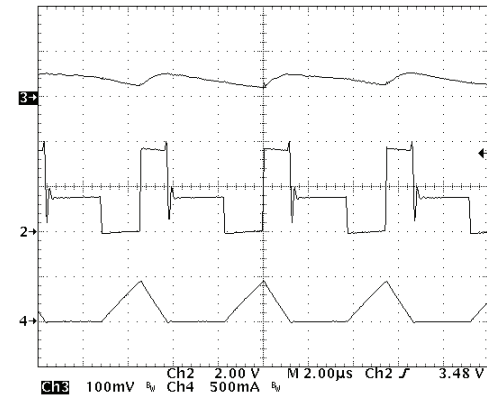
Upper Trace: Voltage at LBI Pin, 0.5 V/Division
Lower Trace: Voltage at LBO Pin, 1.0 V/Division

Figure 49. Low Battery Detect



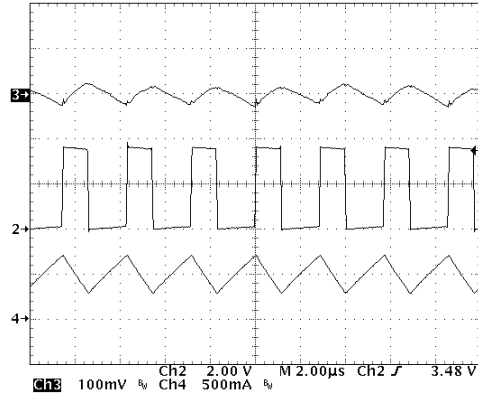
Upper Trace: Output Voltage Waveform, 2.0 V/Division
Middle Trace: Input Voltage Waveform, 1.0 V/Division
Lower Trace: Inductor Current Waveform, 500 mA/Division
($V_{IN} = 1.8$ V, $V_{OUT} = 3.3$ V, $L = 5.6$ μ H, $I_{LOAD} = 60$ mA)

Figure 50. Startup Transient Response



Upper Trace: Output Voltage Ripple, 100 mV/Division
Middle Trace: Voltage at Lx pin, 2.0 V/Division
Lower Trace: Inductor Current, 500 mA/Division
($V_{IN} = 1.5$ V, $V_{OUT} = 3.3$ V, $I_{LOAD} = 50$ mA; $L = 5.6$ μ H, $C_{OUT} = 22$ μ F)

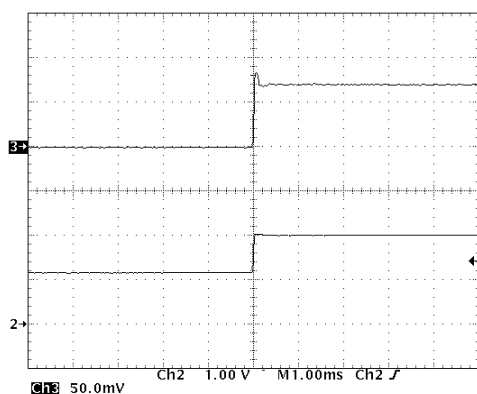
Figure 51. Discontinuous Conduction Mode Switching Waveform



Upper Trace: Output Voltage Ripple, 100 mV/Division
Middle Trace: Voltage at Lx pin, 2.0 V/Division
Lower Trace: Inductor Current, 500 mA/Division
($V_{IN} = 1.5$ V, $V_{OUT} = 3.3$ V, $I_{LOAD} = 200$ mA; $L = 5.6$ μ H, $C_{OUT} = 22$ μ F)

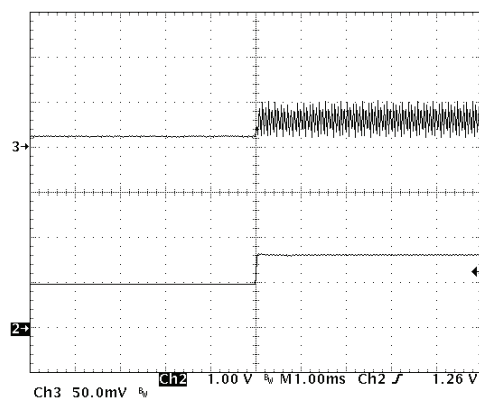
Figure 52. Continuous Conduction Mode Switching Waveform

TYPICAL OPERATING CHARACTERISTICS



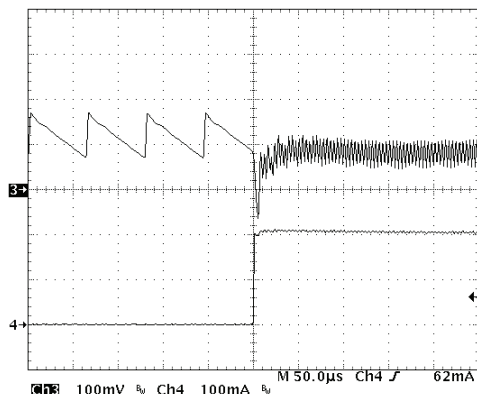
Upper Trace: Output Voltage Ripple, 50 mV/Division
Lower Trace: Battery Voltage, V_{IN} , 1.0 V/Division
($V_{IN} = 1.2 \text{ V to } 2.0 \text{ V}$; $L = 5.6 \mu\text{H}$, $C_{OUT} = 22 \mu\text{F}$, $I_{LOAD} = 50 \text{ mA}$)

Figure 53. Line Transient Response for $V_{OUT} = 3.3 \text{ V}$



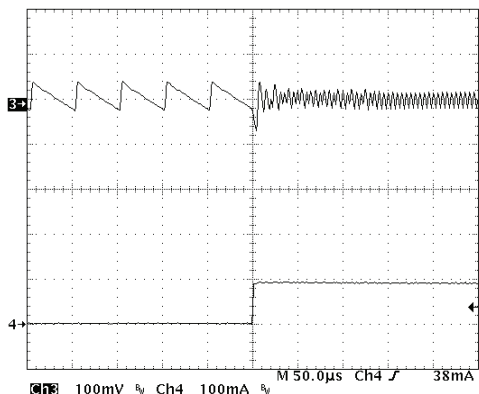
Upper Trace: Output Voltage Ripple, 50 mV/Division
Lower Trace: Battery Voltage, V_{IN} , 1.0 V/Division
($V_{IN} = 1.0 \text{ V to } 1.6 \text{ V}$; $L = 5.6 \mu\text{H}$, $C_{OUT} = 22 \mu\text{F}$, $I_{LOAD} = 50 \text{ mA}$)

Figure 54. Line Transient Response for $V_{OUT} = 1.8 \text{ V}$



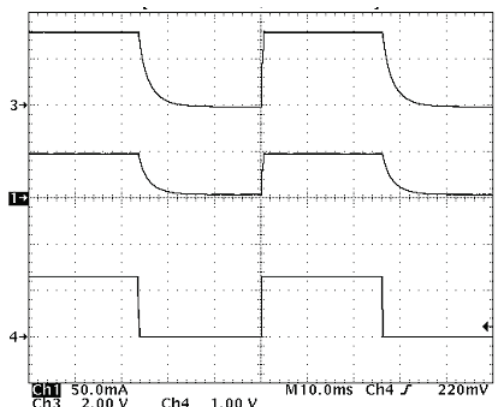
Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Load Current, I_{LOAD} , 100 mA/Division
($V_{OUT} = 3.3 \text{ V}$, $I_{LOAD} = 10 \text{ mA to } 200 \text{ mA}$; $L = 5.6 \mu\text{H}$, $C_{OUT} = 22 \mu\text{F}$)

Figure 55. Load Transient Response for $V_{IN} = 1.5 \text{ V}$



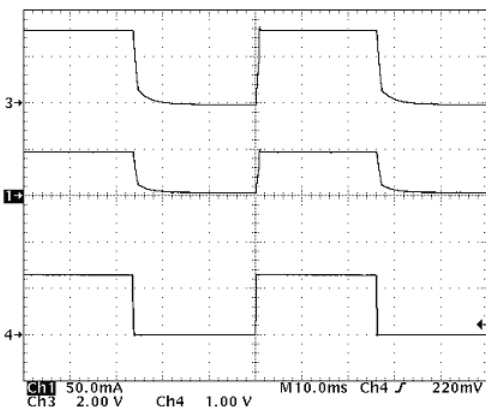
Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Load Current, I_{LOAD} , 100 mA/Division
($V_{OUT} = 1.8 \text{ V}$, $I_{LOAD} = 10 \text{ mA to } 100 \text{ mA}$; $L = 5.6 \mu\text{H}$, $C_{OUT} = 22 \mu\text{F}$)

Figure 56. Load Transient Response for $V_{IN} = 1.0 \text{ V}$



Upper Trace: Output Voltage, 2.0 V/Division
Lower Trace: Output Current, 50 mA/Division
Middle Trace: Enable Pin Waveform, 1.0 V/Division
($V_{IN} = 1.5 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$, $L = 5.6 \mu\text{H}$, $C_{IN} = 10 \mu\text{F}$, $C_{OUT} = 22 \mu\text{F}$)

Figure 57. Startup Waveform (ADEN Disabled)



Upper Trace: Output Voltage, 2.0 V/Division
Lower Trace: Output Current, 50 mA/Division
Middle Trace: Enable Pin Waveform, 1.0 V/Division
($V_{IN} = 1.5 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$, $L = 5.6 \mu\text{H}$, $C_{IN} = 10 \mu\text{F}$, $C_{OUT} = 22 \mu\text{F}$)

Figure 58. Startup Waveform (ADEN Enabled)

DETAILED OPERATION DESCRIPTION

NCP1423 is a monolithic micropower high-frequency step-up voltage switching converter IC specially designed for battery operated hand-held electronic products up to 200 mA loading. It integrates a Synchronous Rectifier to improving efficiency as well as to eliminate the external Schottky diode. High switching frequency (up to 600 kHz) allows for a low profile inductor and output capacitor to be used. Low-Battery Detector, Logic-Controlled Shutdown and Cycle-by-Cycle Current Limit provide value-added features for various battery-operated applications. With all these functions ON, the quiescent supply current is typical only 9 μ A typical. This device is available in compact Micro10 package.

PFM Regulation Scheme

From the detailed block diagram (Figure 2), the output voltage is divided down and fed back to Pin 3 (FB). This voltage goes to the non-inverting input of the PFM comparator whereas the comparator's inverting input is connected to the internal voltage reference, REF. A switching cycle is initiated by the falling edge of the comparator, at the moment the main switch (M1) is turned ON. After the maximum ON-time (typical 1.4 μ S) elapses or the current limit is reached, M1 is turned OFF, and the synchronous switch (M2) is turned ON. The M1 OFF time is not less than the minimum OFF-time (typically 0.20 μ S), which ensure complete energy transfer from the inductor to the output capacitor. If the regulator is operating in continuous conduction mode (CCM), M2 is turned OFF just before M1 is supposed to be ON again. If the regulator is operating in discontinuous conduction mode (DCM), which means the coil current will decrease to zero before the new cycle start, M1 is turned OFF as the coil current is almost reaching zero. The comparator (ZLC) with fixed offset is dedicated to sense the voltage drop across M2 as it is conducting, when the voltage drop is below the offset, the ZLC comparator output goes HIGH, and M2 is turned OFF. Negative feedback of closed loop operation regulates voltage at Pin 3 (FB) equal to the internal divide down reference voltage times (0.5 V).

Synchronous Rectification

The Synchronous Rectifier is used to replace the Schottky Diode to reduce the conduction loss contributed by the forward voltage of the Schottky Diode. The Synchronous Rectifier is normally realized by PowerFET with gate control circuitry that incorporates relatively complicated timing concerns.

As the main switch (M1) is being turned OFF and the synchronous switch M2 is just turned ON with M1 not being completely turned OFF, current is shunt from the output bulk capacitor through M2 and M1 to ground. This power loss lowers overall efficiency and possibly damage the switching FETs. As a general practice, certain amount of dead time is

introduced to make sure M1 is completely turned OFF before M2 is being turned ON.

The previously mentioned situation occurs when the regulator is operating in CCM, M2 is being turned OFF, M1 is just turned ON, and M2 is not being completely turned OFF. A dead time is also needed to make sure M2 is completely turned OFF before M1 is being turned ON.

As coil current is dropped to zero when the regulator is operating in DCM, M2 should be OFF. If this does not occur, the reverse current flows from the output bulk capacitor through M2 and the inductor to the battery input, causing damage to the battery. The ZLC comparator comes with fixed offset voltage to switch M2 OFF before any reverse current builds up. However, if M2 switch OFF too early, large residue coil current flows through the body diode of M2 and increases conduction loss. Therefore, determination on the offset voltage is essential for optimum performance. With the implementation of synchronous rectification scheme, efficiency can be as high as 90% with this device.

Cycle-by-Cycle Current Limit

In Figure 2, SENSEFET is used to sample the coil current as M1 is ON. With that sample current flowing through a sense resistor, a sense-voltage is developed. Threshold detector (I_{LIM}) detects whether the sense-voltage is higher than the preset level. If the sense voltage is higher than the present level, the detector output notifies the Control Logic to switch OFF M1, and M1 can only be switched ON when the next cycle starts after the minimum OFF-time (typically 0.20 μ S). With proper sizing of SENSEFET and sense resistor, the peak coil current limit is typically set at 1.2 A.

Voltage Reference

The voltage at REF is typically set at 1.2 V and can output up to 2.5 mA with load regulation $\pm 2.0\%$, at V_{OUT} equal to 3.3 V. If V_{OUT} is increased, the REF load capability can also be increased. A bypass capacitor of 200 nF is required for proper operation when REF is not loaded. If REF is loaded, 1.0 μ F capacitor at REF pin is needed.

True-Cutoff

The NCP1423 has a True-Cutoff function controlled by the EN pin (Pin 1). Internal circuitry can isolate the current through the body diode of switch M2 to load. Thus, it can eliminate leakage current from battery the battery to load in shutdown mode and significantly reduces battery current consumption during shutdown. The shutdown function is controlled by the voltage at Pin 1 (EN). When Pin 1 is pulled to lower than 0.5 V, the controller enters shutdown mode. In shutdown mode, when the switches M1 and M2 are both switched OFF, the internal reference voltage of the controller is disable and the controller typically consumes only 600 nA of current. If the Pin 1 voltage is raised to higher than 0.2 V, for example, by a resistor connected to V_{IN} , the

IC is enabled again, and the internal circuit typically consumes 9 μ A of current from the OUT pin during normal operation.

Low-Battery Detection

A comparator with 15 mV hysteresis is applied to perform the low-battery detection function. When Pin 9 (LBI) is at a voltage (defined by a resistor divider from the battery voltage) lower than the internal reference voltage of 0.5 V, the comparator output turns on a 50 Ω low side switch. It pulls down the voltage at Pin 10 (LBO) which has hundreds of k Ω of pull-high resistance. If the Pin 9 voltage is higher than 0.5 V+15 mV, the comparator output turns off the 50 Ω

low side switch. When this occurs, Pin 10 becomes high impedance and its voltage is pulled high again.

Auto Discharge

Auto discharge function is using for ensure the output voltage status after the power down occur. This function is using for communication with a digital signal. When auto discharge function is enabled, the ADEN is set high; the output capacitor will be discharged after the device is shutdown. The capacitors connected to the output are discharged by an integrated switch of 100 Ω . The residual voltage on V_{OUT} will be less than 0.4 V after auto discharge.

APPLICATIONS INFORMATION

Output Voltage Setting

A typical application circuit is shown in Figure 1, The output voltage of the converter is determined by the external feedback network comprised of R1 and R2 and the relationship is given by:

$$V_{OUT} = 0.5 \text{ V} \times \left(1 + \frac{R1}{R2}\right)$$

where R1 and R2 are the upper and lower feedback resistors, respectively.

Low Battery Detect Level Setting

The Low Battery Detect Voltage of the converter is determined by the external divider network comprised of R3 and R4 and the relationship is given by:

$$V_{LBI} = 0.5 \text{ V} \times \left(1 + \frac{R3}{R4}\right)$$

where R3 and R4 are the upper and lower divider resistors respectively.

Inductor Selection

The NCP1423 is tested to produce optimum performance with a 5.6 μ H inductor at $V_{IN} = 1.3 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$, supplying an output current up to 200 mA. For other input / output requirements, inductance in the range 3 μ H to 10 μ H can be used according to end application specifications. Selecting an inductor is a compromise between output current capability, inductor saturation limit and tolerable output voltage ripple. Low inductance values can supply higher output current but also increase the ripple at output and decrease efficiency. On the other hand, high inductance values can improve output ripple and efficiency; however, it also limited the output current capability at the same time.

Another parameter of the inductor is its DC resistance. This resistance can introduce unwanted power loss and reduce overall efficiency. The basic rule is to select an inductor with lowest DC resistance within the board space limitation of the end application.

Capacitors Selection

In all switching mode boost converter applications, both the input and output terminals see impulsive voltage / current waveforms. The currents flowing into and out of the capacitors multiply with the Equivalent Series Resistance (ESR) of the capacitor to produce ripple voltage at the terminals. During the Syn-Rect switch-off cycle, the charges stored in the output capacitor are used to sustain the output load current. Load current at this period and the ESR combined and reflect as ripple at the output terminals. For all cases, the lower the capacitor ESR, the lower the ripple voltage at output. As a general guideline, low ESR capacitors should be used.

PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise, and unwanted feedback that can affect the performance of the converter. Hints suggested below can be used as a guideline in most situations.

Grounding

A star-ground connection should be used to connect the output power return ground, the input power return ground, and the device power ground together at one point. All high-current paths must be as short as possible and thick enough to allow current to flow through and produce insignificant voltage drop along the path. The feedback signal path must be separated from the main current path and sense directly at the anode of the output capacitor.

Components Placement

Power components (i.e. input capacitor, inductor and output capacitor) must be placed as close together as possible. All connecting traces must be short, direct and thick. High current flowing and switching paths must be kept away from the feedback (FB, Pin 3) terminal to avoid unwanted injection of noise into the feedback path.

General Design Procedures

Switching mode converter design is important. Suitable choice an inductor and capacitor value can make the converter has an optimum performance. Below a simple method base on the most basic first order equations to estimate the inductor and capacitor values for NCP1423 operate in Continuous Conduction Mode (CCM) is introduced. The component value set can be used as a starting point to fine-tune the circuit operation. By all means, detail bench testing is needed to get the best performance out of the circuit.

Design Parameters:

For one cells supply application

$$\begin{aligned} V_{IN} &= 1.1 \text{ V to } 1.5 \text{ V, Typical } 1.3 \text{ V} \\ V_{OUT} &= 3.3 \text{ V} \\ I_{OUT} &= 150 \text{ mA (200 mA max)} \\ V_{LB} &= 1.0 \text{ V} \\ V_{OUT-RIPPLE} &= 30 \text{ mV}_{P-P} \text{ at } I_{OUT} = 150 \text{ mA} \end{aligned}$$

Calculate the feedback network:

Select R2 = 100 k

$$R1 = R2 \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

$$R1 = 100 \text{ k} \left(\frac{3.3 \text{ V}}{0.5 \text{ V}} - 1 \right) = 560 \text{ k}$$

Calculate the Low Battery Detect divider:

$$V_{LB0} = 1.0 \text{ V}$$

Select R4 = 100 k

$$R3 = R4 \left(\frac{V_{LB0}}{V_{LB1}} - 1 \right)$$

$$R3 = 100 \text{ k} \left(\frac{1.0 \text{ V}}{0.5 \text{ V}} - 1 \right) = 100 \text{ k}$$

Determine the steady state duty ratio, D for typical V_{IN} , operation will be optimized around this point:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D}$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}} = 1 - \frac{1.3 \text{ V}}{3.3 \text{ V}} = 0.606$$

Determine the average inductor current, I_{LAVG} at maximum I_{OUT} :

$$I_{LAVG} = \frac{I_{OUT}}{1 - D} = \frac{150 \text{ mA}}{1 - 0.606} = 381 \text{ mA}$$

Assume the efficiency $\eta = 85\%$

Determine the peak inductor ripple current, $I_{RIPPLE-P}$ and calculate the inductor value:

Assume $I_{RIPPLE-P}$ is 40% of I_{LAVG} , the inductance of the power inductor can be calculated as in below:

$$I_{RIPPLE-P} = 0.40 \times 381 \text{ mA} / \eta = 179 \text{ mA}$$

$$L = \frac{V_{IN} \times t_{ON}}{2 I_{RIPPLE-P}} = \frac{1.3 \text{ V} \times 1.4 \mu\text{S}}{2 (179 \text{ mA})} = 5.0 \mu\text{H}$$

A standard value of 5.6 μH is selected for initial trial.

Determine the output voltage ripple, $V_{OUT-RIPPLE}$ and calculate the output capacitor value:

$$V_{OUT-RIPPLE} = 30 \text{ mV}_{P-P} \text{ at } I_{OUT} = 150 \text{ mA}$$

$$C_{OUT} > \frac{I_{OUT} \times t_{ON}}{V_{OUT-RIPPLE} - I_{OUT} \times ESR_{COUT}}$$

where $t_{ON} = 1.4 \mu\text{S}$ and $ESR_{COUT} = 0.1 \Omega$,

From above calculation, you need at least 14 μF in order to achieve the specified ripple level at conditions stated. Practically, a one level larger capacitor will be used to accommodate factors not taken into account in the calculations. Therefore, a capacitor value of 22 μF is selected. The NCP1423 is internal compensated for most applications. But in case additional compensation is required, the capacitor C1 can be used as external compensation adjustment to improve system dynamics.

NCP1450A

PWM Step-up DC-DC Controller

The NCP1450A series are PWM step-up DC-DC switching controller that are specially designed for powering portable equipment from one or two cells battery packs. The NCP1450A series have a driver pin, EXT pin, for connecting to an external transistor. Large output currents can be obtained by connecting a low ON-resistance external power transistor to the EXT pin. The device will automatically skip switching cycles under light load condition to maintain high efficiency at light loads. With only six external components, this series allows a simple means to implement highly efficient converter for large output current applications.

Each device consists of an on-chip Pulse Width Modulation (PWM) oscillator, PWM controller, phase-compensated error amplifier, soft-start, voltage reference, and driver for driving external power transistor. Additionally, a chip enable feature is provided to power down the converter for extended battery life.

The NCP1450A device series are available in the TSOP-5 package with five standard regulated output voltages. Additional voltages that range from 1.8 V to 5.0 V in 100 mV steps can be manufactured.

Features

- Pb-Free Packages are Available
- High Efficiency 86% at $I_O = 200$ mA, $V_{IN} = 2.0$ V, $V_{OUT} = 3.0$ V
88% at $I_O = 400$ mA, $V_{IN} = 3.0$ V, $V_{OUT} = 5.0$ V
- Low Startup Voltage of 0.9 V typical at $I_O = 1.0$ mA
- Operation Down to 0.6 V
- Five Standard Voltages: 1.9 V, 2.7 V, 3.0 V, 3.3 V, 5.0 V with High Accuracy $\pm 2.5\%$
- Low Conversion Ripple
- High Output Current up to 1000 mA
(3.0 V version at $V_{IN} = 2.0$ V, $L = 10$ μ H, $C_{OUT} = 220$ μ F)
- Fixed Frequency Pulse Width Modulation (PWM) at 180 kHz
- Chip Enable Pin with On-chip 150 nA Pullup Current Source
- Low Profile and Micro Miniature TSOP-5 Package

Typical Applications

- Personal Digital Assistant (PDA)
- Electronic Games
- Portable Audio (MP3)
- Digital Still Cameras
- Handheld Instruments



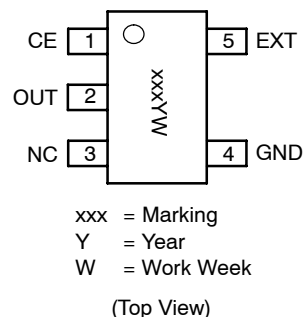
ON Semiconductor®

<http://onsemi.com>



**TSOP-5
SN SUFFIX
CASE 483**

MARKING DIAGRAM AND PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 627 of this data sheet.

NCP1450A

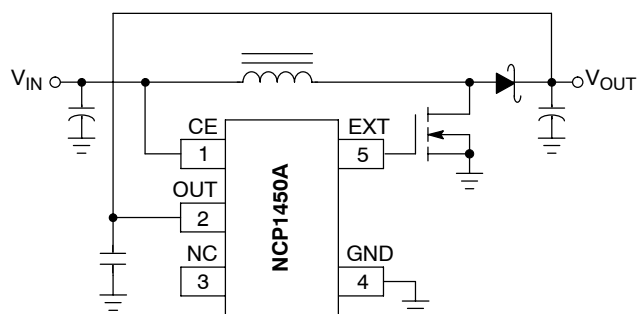


Figure 1. Typical Step-up Converter Application

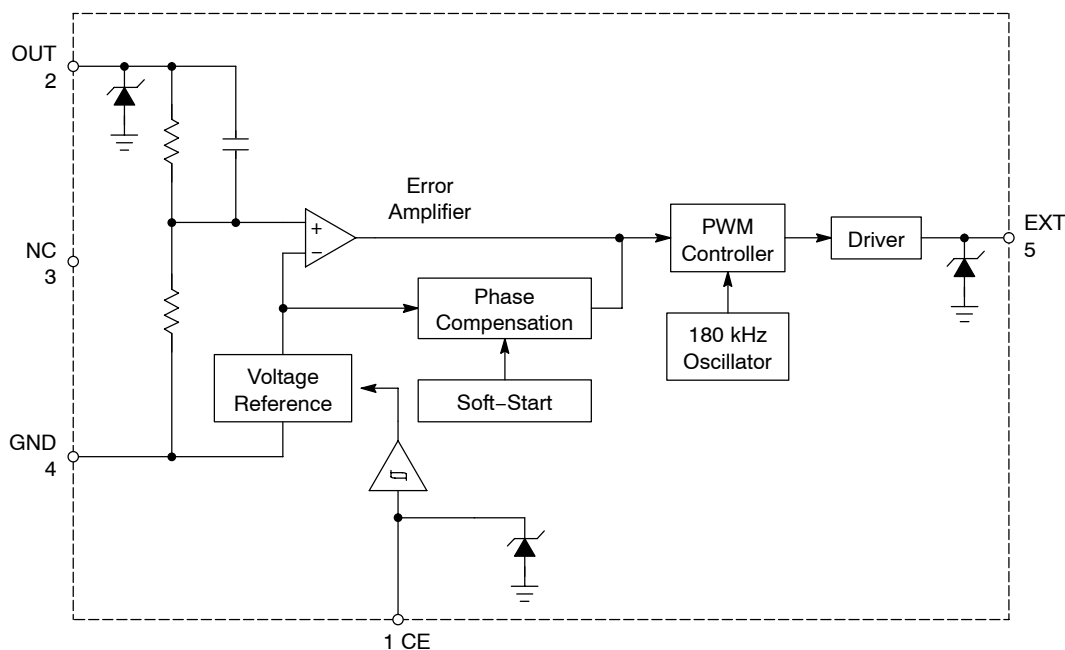


Figure 2. Representative Block Diagram

PIN FUNCTION DESCRIPTION

Pin #	Symbol	Pin Description
1	CE	Chip Enable Pin (1) The chip is enabled if a voltage equal to or greater than 0.9 V is applied. (2) The chip is disabled if a voltage less than 0.3 V is applied. (3) The chip is enabled if this pin is left floating.
2	OUT	Output voltage monitor pin and also the power supply pin for the device.
3	NC	No internal connection to this pin.
4	GND	Ground pin.
5	EXT	External transistor drive pin.

NCP1450A

ORDERING INFORMATION (Note 1)

Device	Output Voltage	Switching Frequency	Marking	Package	Shipping [†]
NCP1450ASN19T1	1.9 V	180 KHz	DAY	TSOP-5	3000 Units on 7 Inch Reel
NCP1450ASN27T1	2.7 V		DAZ		
NCP1450ASN30T1	3.0 V		DBA	TSOP-5	
NCP1450ASN30T1G				TSOP-5 (Pb-Free)	
NCP1450ASN33T1	3.3 V		DBC	TSOP-5	
NCP1450ASN33T1G				TSOP-5 (Pb-Free)	
NCP1450ASN50T1	5.0 V		DBD	TSOP-5	
NCP1450ASN50T1G				TSOP-5 (Pb-Free)	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

- The ordering information lists five standard output voltage device options. Additional devices with output voltage ranging from 1.8 V to 5.0 V in 100 mV increments can be manufactured. Contact your ON Semiconductor representative for availability.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 2)	V _{OUT}	6.0	V
Input/Output Pins EXT (Pin 5) EXT Sink/Source Current	V _{EXT} I _{EXT}	-0.3 to 6.0 -150 to 150	V mA
CE (Pin 1) Input Voltage Range Input Current Range	V _{CE} I _{CE}	-0.3 to 6.0 -150 to 150	V mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T _A = 25°C Thermal Resistance Junction-to-Air	P _D R _{θJA}	500 250	mW °C/W
Operating Ambient Temperature Range	T _A	-40 to +85	°C
Operating Junction Temperature Range	T _J	-40 to +150	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- This device series contains ESD protection and exceeds the following tests:
Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22-A114.
Machine Model (MM) ±200 V per JEDEC standard: JESD22-A115.
- Latchup Current Maximum Rating: ±150 mA per JEDEC standard: JESD78.
- Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.

NCP1450A

ELECTRICAL CHARACTERISTICS (For all values $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit

OSCILLATOR

Frequency ($V_{OUT} = V_{SET} \times 0.96$, Note 5)	f_{OSC}	144	180	216	kHz
Frequency Temperature Coefficient ($T_A = -40^\circ\text{C}$ to 85°C)	Δf	–	0.11	–	%/ $^\circ\text{C}$
Maximum PWM Duty Cycle ($V_{OUT} = V_{SET} \times 0.96$)	D_{MAX}	70	80	90	%
Minimum Startup Voltage ($I_O = 0$ mA)	V_{start}	–	0.8	0.9	V
Minimum Startup Voltage Temperature Coefficient ($T_A = -40^\circ\text{C}$ to 85°C)	ΔV_{start}	–	–1.6	–	mV/ $^\circ\text{C}$
Minimum Operation Hold Voltage ($I_O = 0$ mA)	V_{hold}	–	0.6	0.7	V
Soft-Start Time ($V_{OUT} = V_{SET}$, Note 6)	t_{SS}	–	100	250	ms

CE (PIN 1)

CE Input Voltage ($V_{OUT} = V_{SET} \times 0.96$) High State, Device Enabled Low State, Device Disabled	$V_{CE(high)}$ $V_{CE(low)}$	0.9 –	– –	– 0.3	V
CE Input Current (Note 6) High State, Device Enabled ($V_{OUT} = V_{CE} = 5.0$ V) Low State, Device Disabled ($V_{OUT} = 5.0$ V, $V_{CE} = 0$ V)	$I_{CE(high)}$ $I_{CE(low)}$	–0.5 0	0 0.15	0.5 0.5	μA

EXT (PIN 5)

EXT “H” Output Current ($V_{EXT} = V_{OUT} - 0.4$ V) Device Suffix: 19T1 27T1 30T1 33T1 50T1	I_{EXTH}	– – – – –	–25.0 –35.0 –37.7 –40.0 –53.7	–20.0 –30.0 –30.0 –30.0 –35.0	mA
EXT “L” Output Current ($V_{EXT} = 0.4$ V) Device Suffix: 19T1 27T1 30T1 33T1 50T1	I_{EXTL}	20.0 30.0 30.0 30.0 35.0	38.3 48.0 50.8 52.0 58.2	– – – – –	mA

TOTAL DEVICE

Output Voltage Device Suffix: 19T1 27T1 30T1 33T1 50T1	V_{OUT}	1.853 2.633 2.925 3.218 4.875	1.9 2.7 3.0 3.3 5.0	1.948 2.768 3.075 3.383 5.125	V
Output Voltage Temperature Coefficient ($T_A = -40$ to $+85^\circ\text{C}$)	ΔV_{OUT}	–	150	–	ppm/ $^\circ\text{C}$
Operating Current ($V_{OUT} = V_{CE} = V_{SET} \times 0.96$, Note 5) Device Suffix: 19T1 27T1 30T1 33T1 50T1	I_{DD}	– – – – –	55 93 98 103 136	90 140 150 160 220	μA
Standby Current ($V_{OUT} = V_{CE} = V_{SET} + 0.5$ V)	I_{STB}	–	15	20	μA
Off-State Current ($V_{OUT} = 5.0$ V, $V_{CE} = 0$ V, $T_A = -40$ to $+85^\circ\text{C}$, Note 7)	I_{OFF}	–	0.6	1.5	μA

5. V_{SET} means setting of output voltage.

6. This parameter is guaranteed by design.

7. CE pin is integrated with an internal 150 nA pullup current source.

NCP1450A

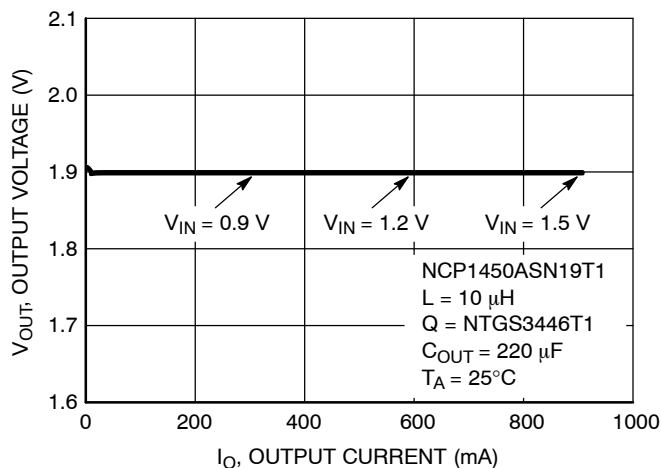


Figure 3. NCP1450ASN19T1 Output Voltage vs. Output Current

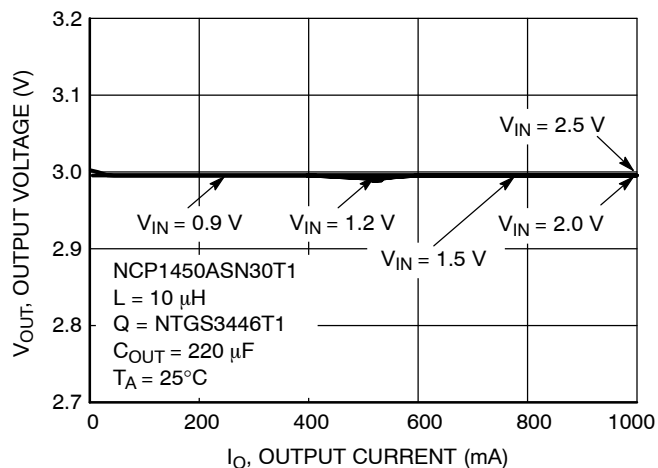


Figure 4. NCP1450ASN30T1 Output Voltage vs. Output Current

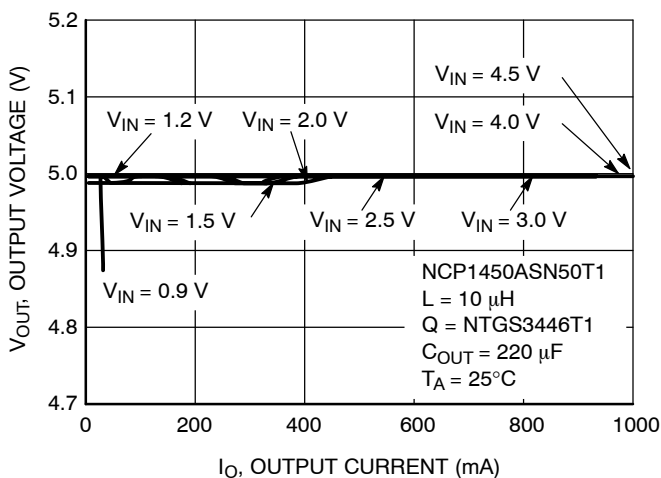


Figure 5. NCP1450ASN50T1 Output Voltage vs. Output Current

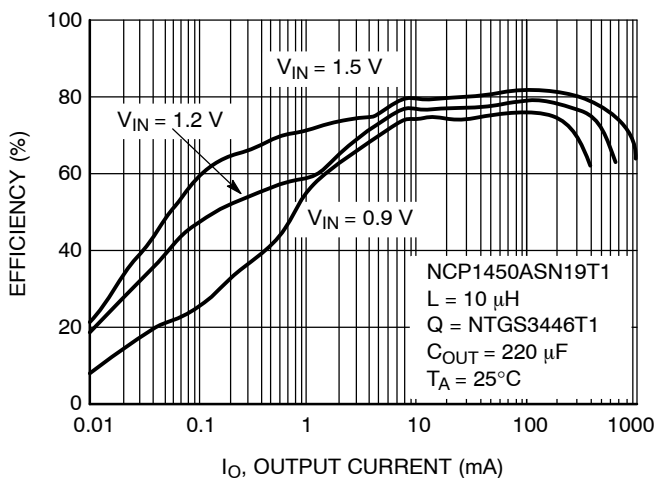


Figure 6. NCP1450ASN19T1 Efficiency vs. Output Current

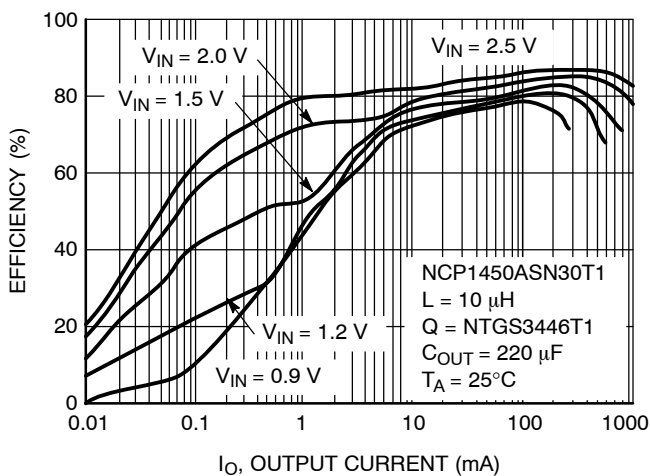


Figure 7. NCP1450ASN30T1 Efficiency vs. Output Current

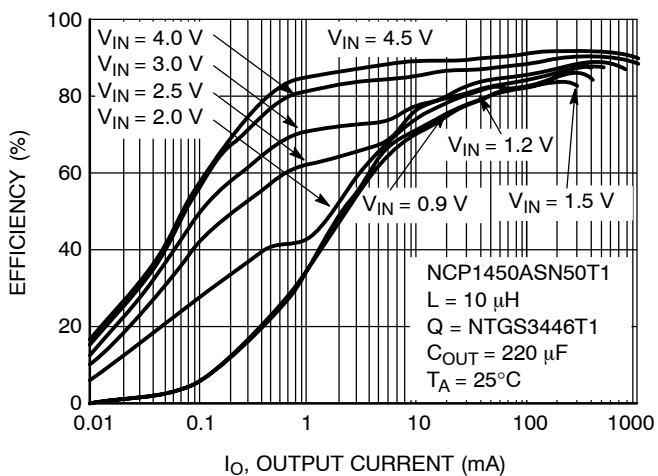


Figure 8. NCP1450ASN50T1 Efficiency vs. Output Current

NCP1450A

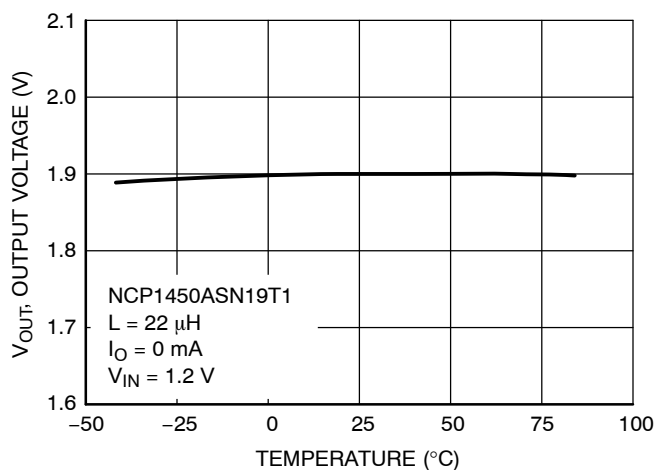


Figure 9. NCP1450ASN19T1 Output Voltage vs. Temperature

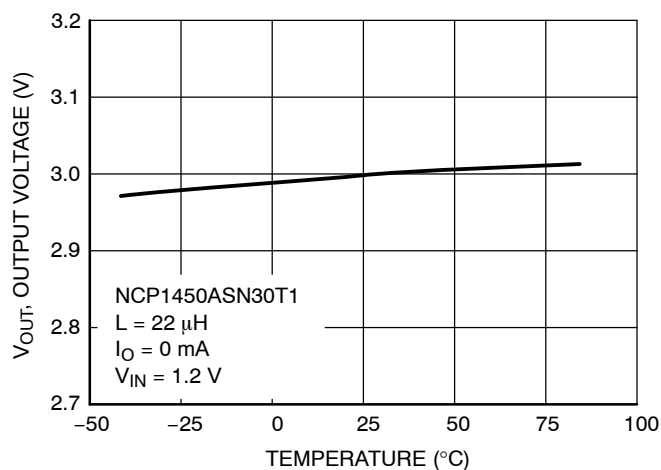


Figure 10. NCP1450ASN30T1 Output Voltage vs. Temperature

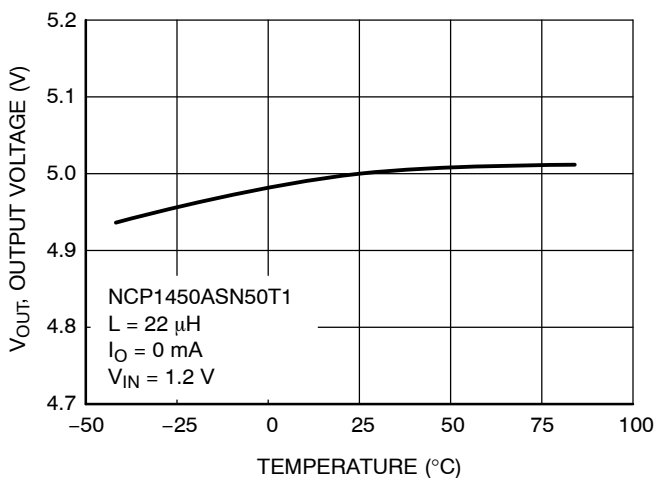


Figure 11. NCP1450ASN50T1 Output Voltage vs. Temperature

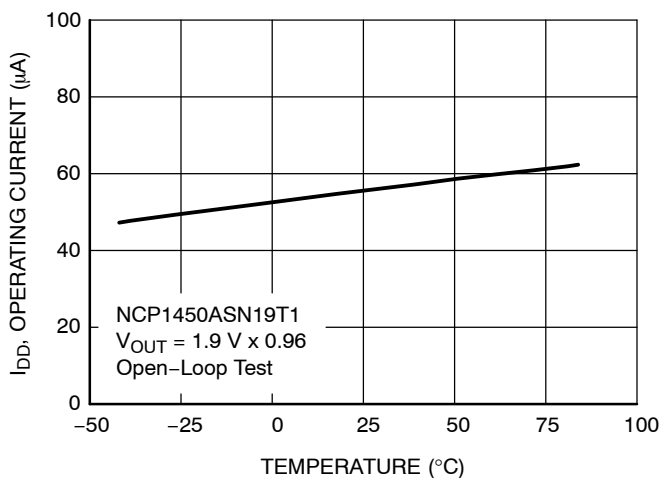


Figure 12. NCP1450ASN19T1 Operating Current vs. Temperature

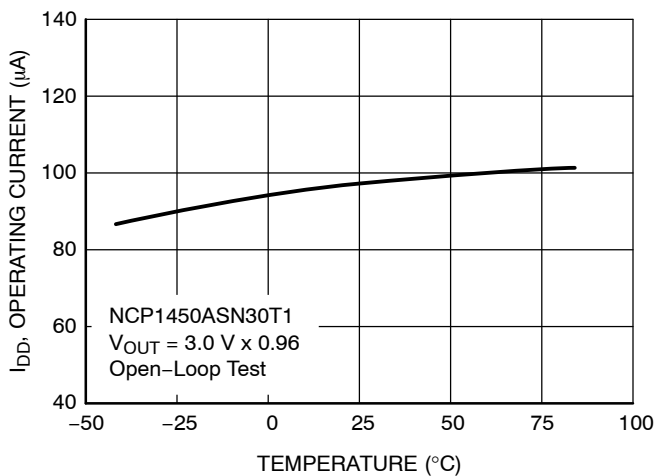


Figure 13. NCP1450ASN30T1 Operating Current vs. Temperature

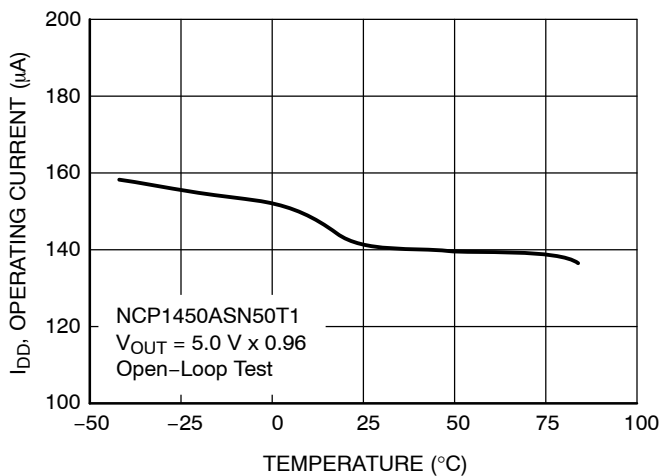


Figure 14. NCP1450ASN50T1 Operating Current vs. Temperature

NCP1450A

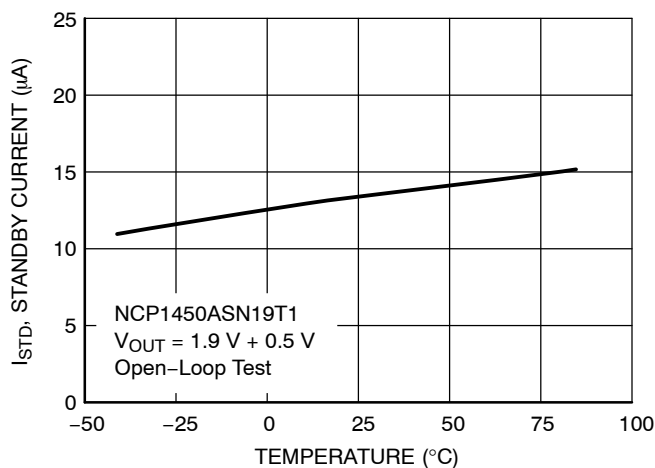


Figure 15. NCP1450ASN19T1 Standby Current vs. Temperature

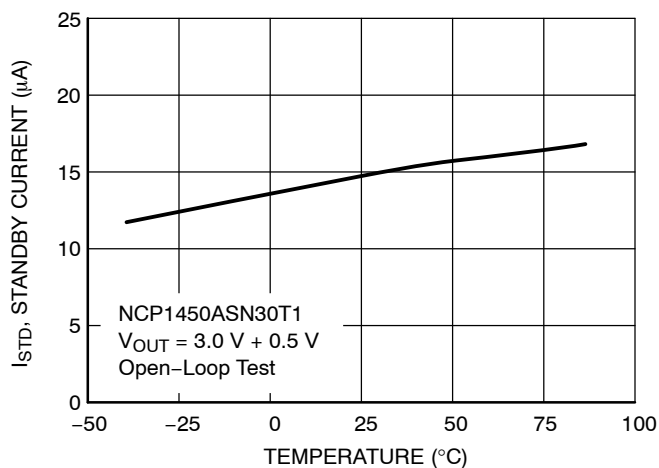


Figure 16. NCP1450ASN30T1 Standby Current vs. Temperature

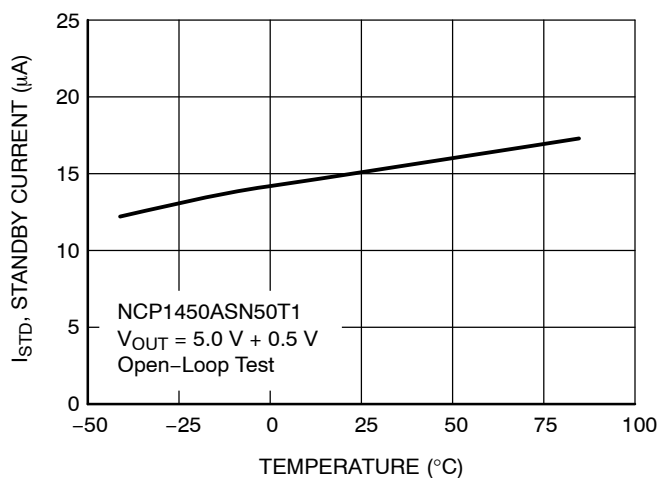


Figure 17. NCP1450ASN50T1 Standby Current vs. Temperature

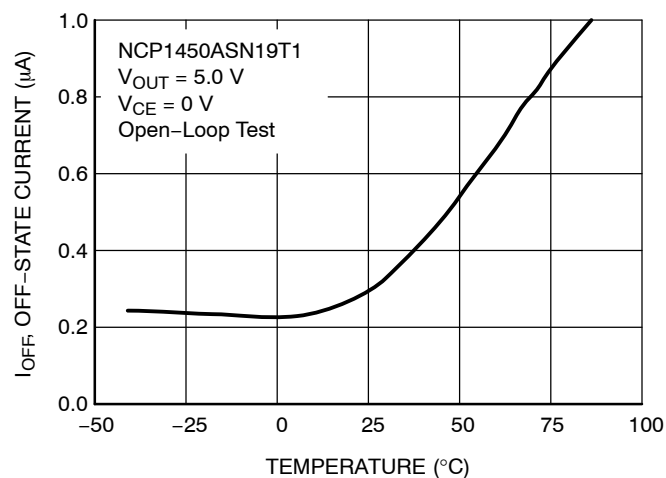


Figure 18. NCP1450ASN19T1 Off-State Current vs. Temperature

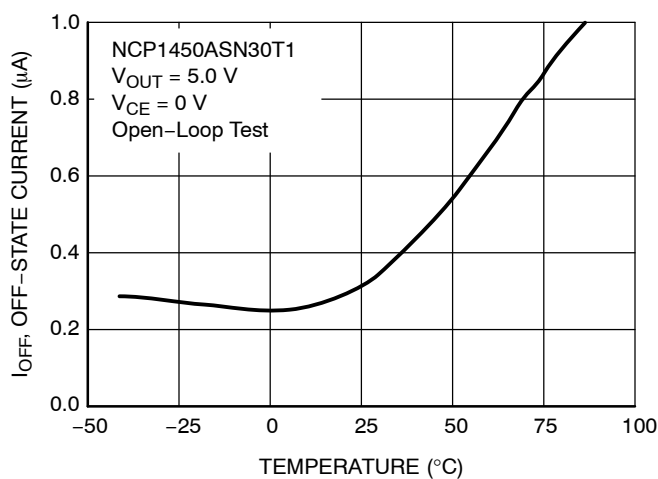


Figure 19. NCP1450ASN30T1 Off-State Current vs. Temperature

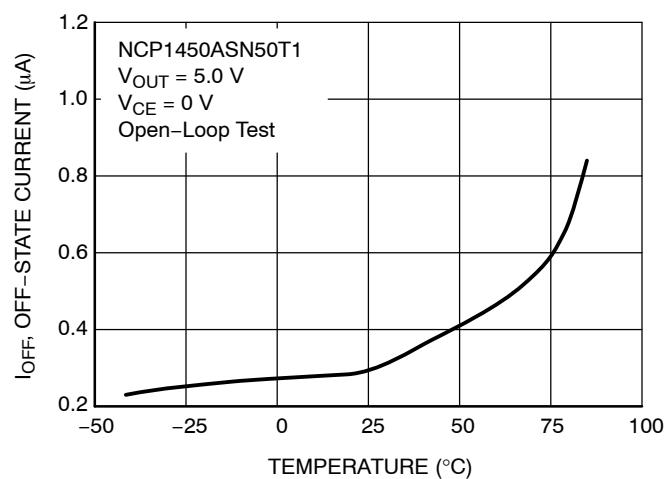


Figure 20. NCP1450ASN50T1 Off-State Current vs. Temperature

NCP1450A

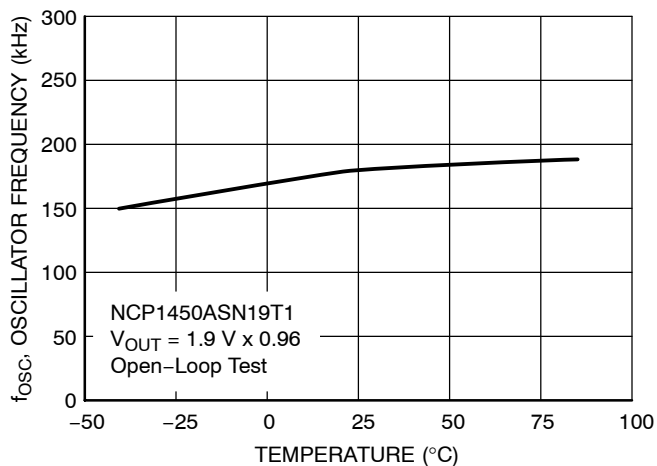


Figure 21. NCP1450ASN19T1 Oscillator Frequency vs. Temperature

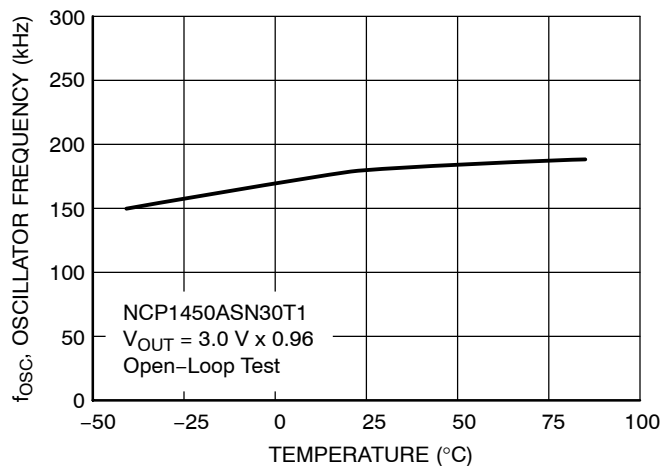


Figure 22. NCP1450ASN30T1 Oscillator Frequency vs. Temperature

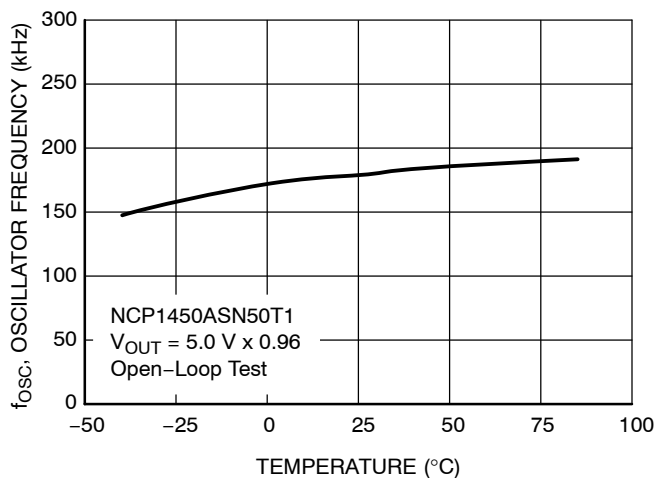


Figure 23. NCP1450ASN50T1 Oscillator Frequency vs. Temperature

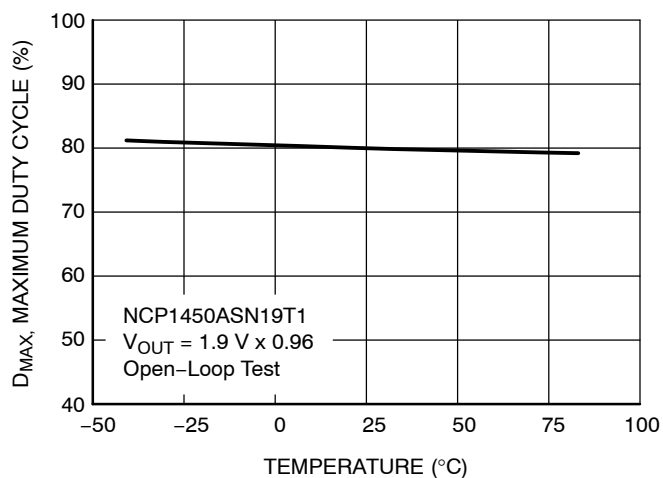


Figure 24. NCP1450ASN19T1 Maximum Duty Cycle vs. Temperature

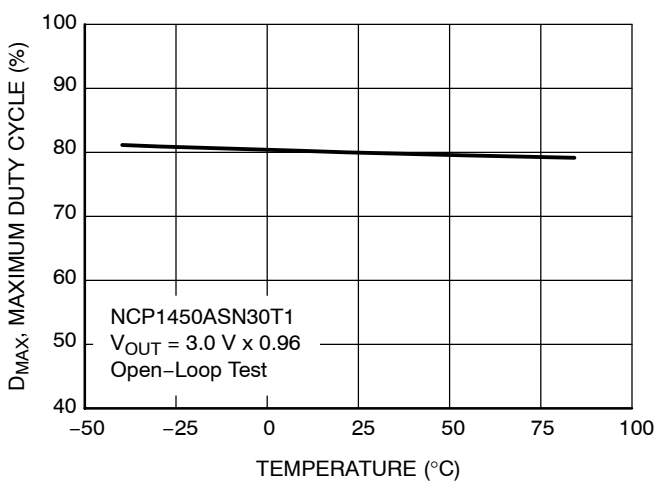


Figure 25. NCP1450ASN30T1 Maximum Duty Cycle vs. Temperature

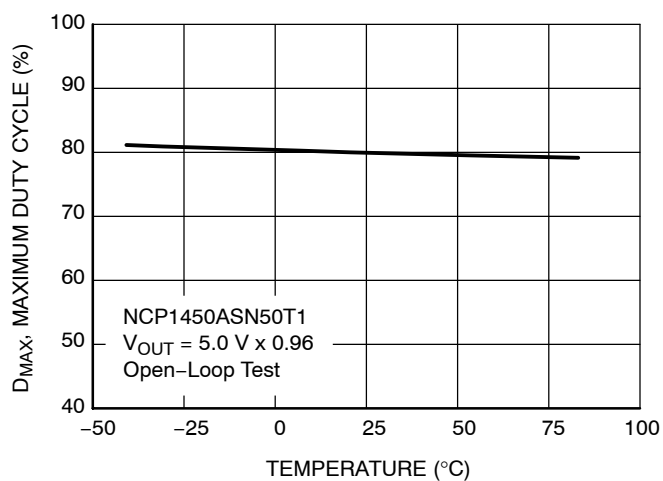


Figure 26. NCP1450ASN50T1 Maximum Duty Cycle vs. Temperature

NCP1450A

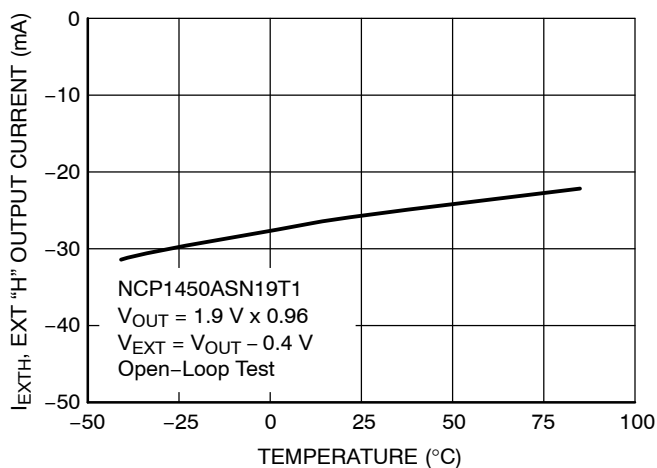


Figure 27. NCP1450ASN19T1 EXT "H" Output Current vs. Temperature

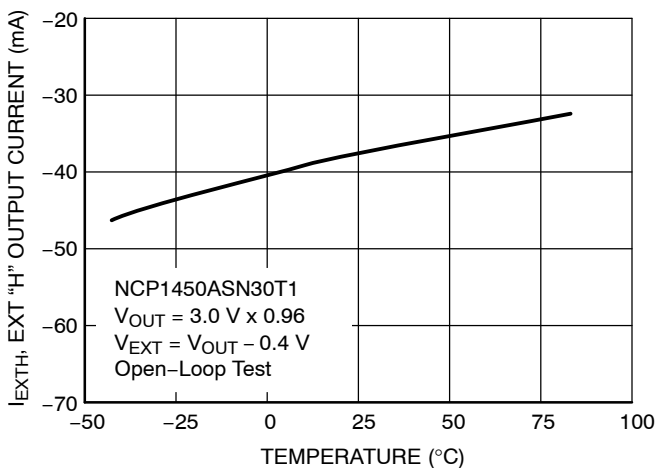


Figure 28. NCP1450ASN30T1 EXT "H" Output Current vs. Temperature

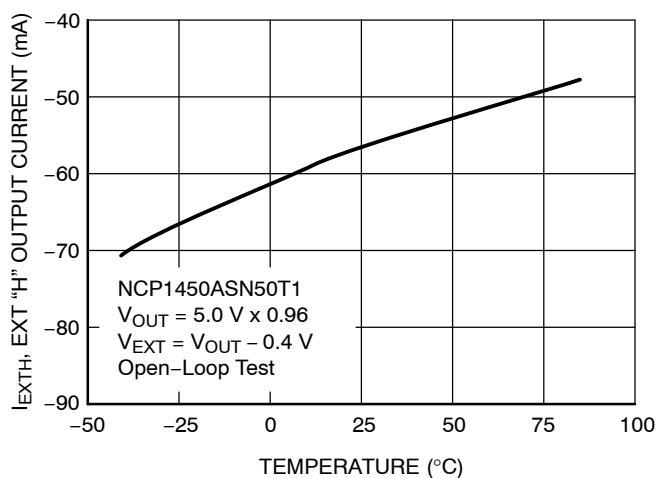


Figure 29. NCP1450ASN50T1 EXT "H" Output Current vs. Temperature

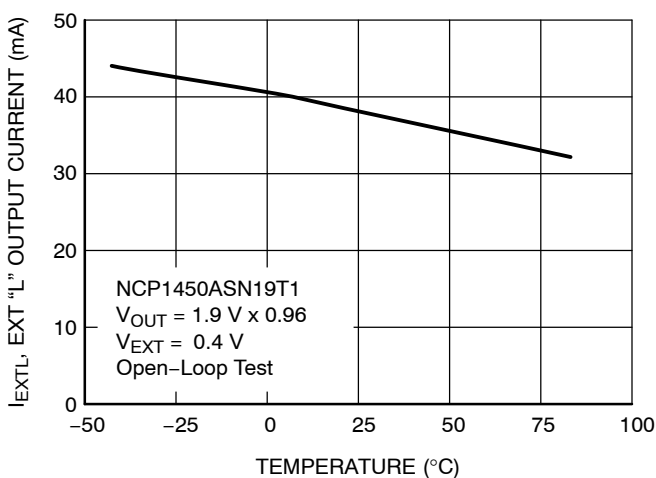


Figure 30. NCP1450ASN19T1 EXT "L" Output Current vs. Temperature

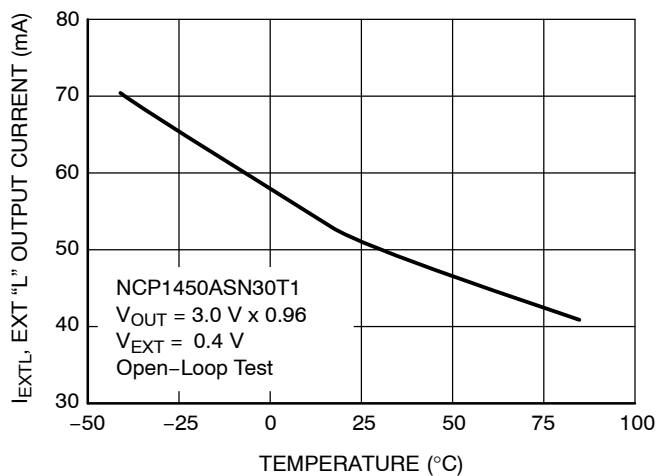


Figure 31. NCP1450ASN30T1 EXT "L" Output Current vs. Temperature

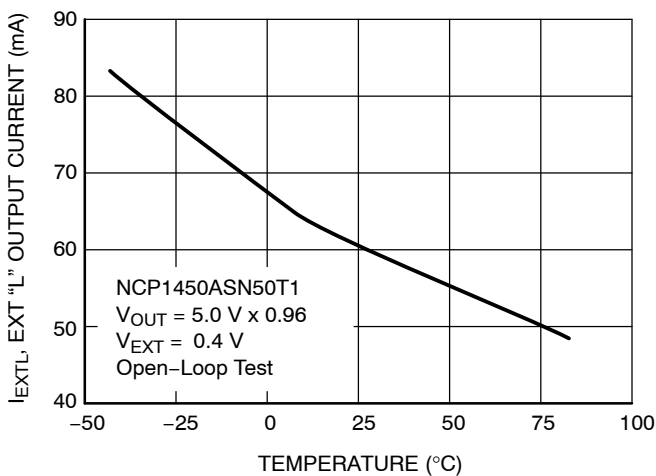


Figure 32. NCP1450ASN50T1 EXT "L" Output Current vs. Temperature

NCP1450A

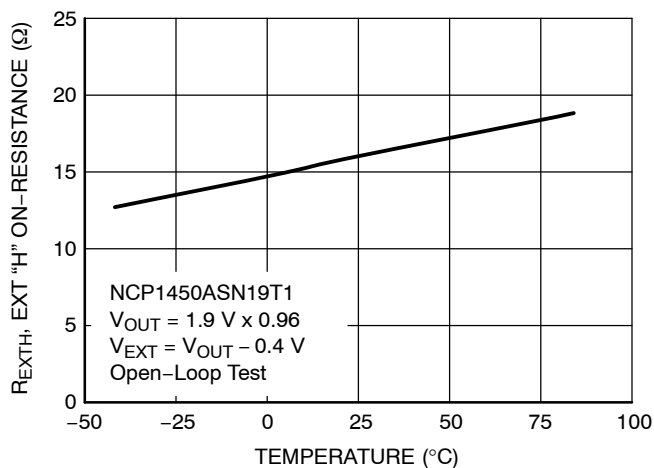


Figure 33. NCP1450ASN19T1 EXT "H" ON-Resistance vs. Temperature

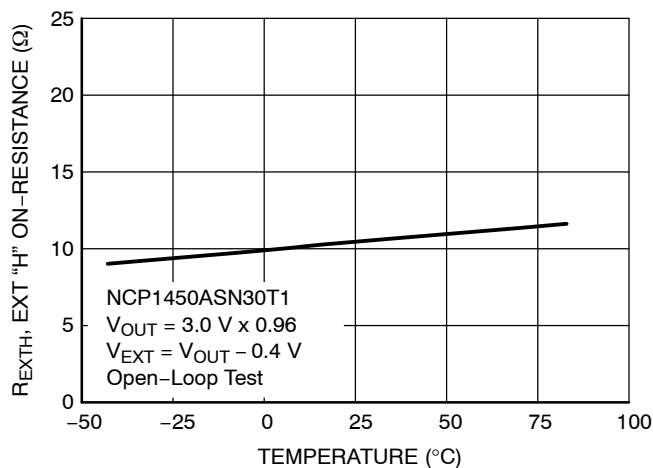


Figure 34. NCP1450ASN30T1 EXT "H" ON-Resistance vs. Temperature

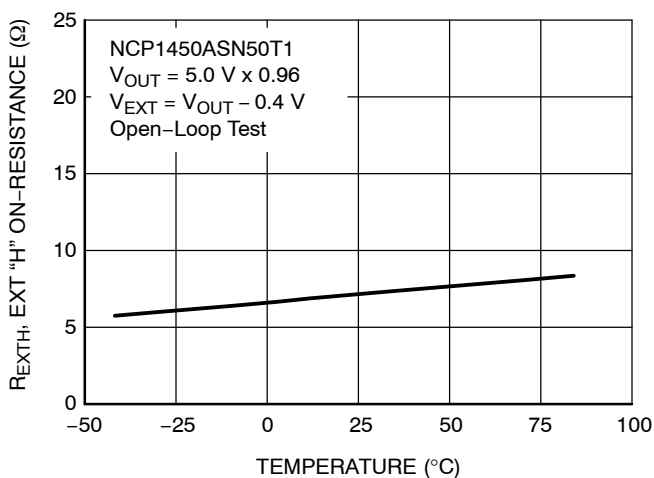


Figure 35. NCP1450ASN50T1 EXT "H" ON-Resistance vs. Temperature

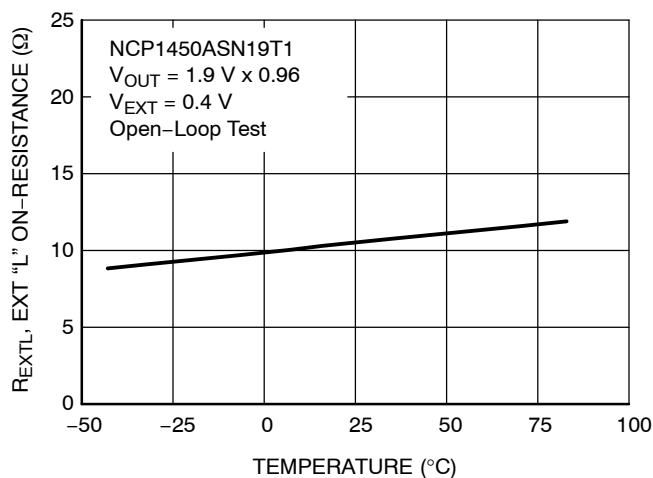


Figure 36. NCP1450ASN19T1 EXT "L" ON-Resistance vs. Temperature

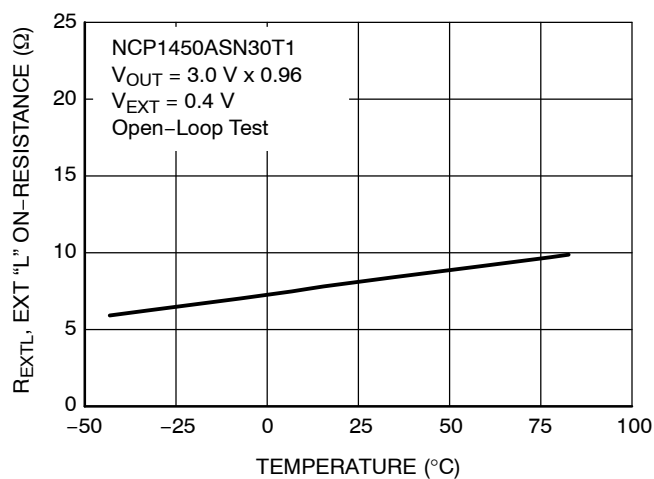


Figure 37. NCP1450ASN30T1 EXT "L" ON-Resistance vs. Temperature

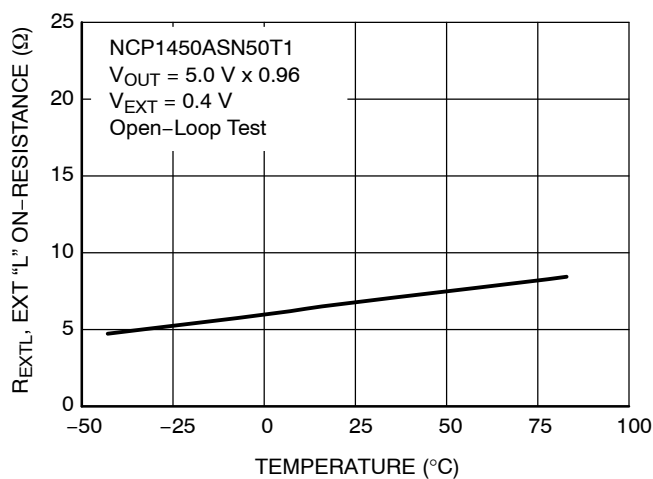


Figure 38. NCP1450ASN50T1 EXT "L" ON-Resistance vs. Temperature

NCP1450A

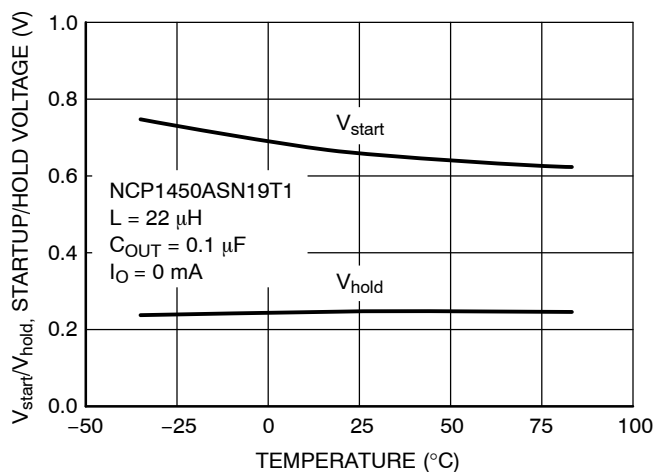


Figure 39. NCP1450ASN19T1 Startup/Hold Voltage vs. Temperature

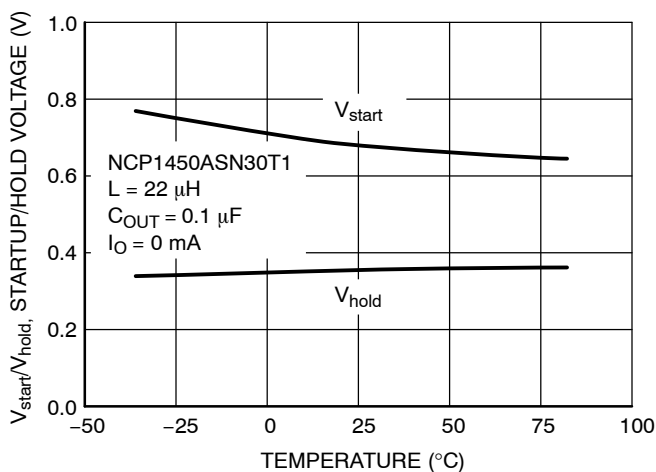


Figure 40. NCP1450ASN30T1 Startup/Hold Voltage vs. Temperature

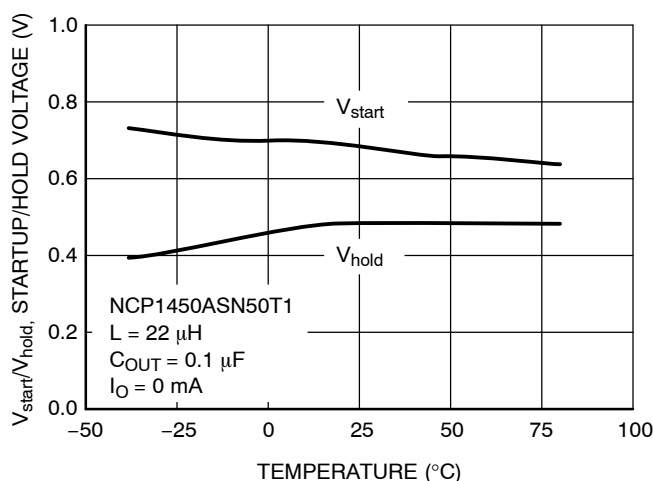


Figure 41. NCP1450ASN50T1 Startup/Hold Voltage vs. Temperature

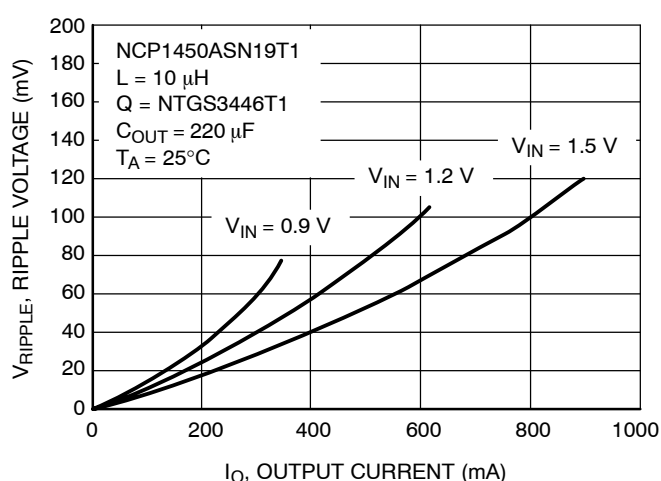


Figure 42. NCP1450ASN19T1 Ripple Voltage vs. Output Current

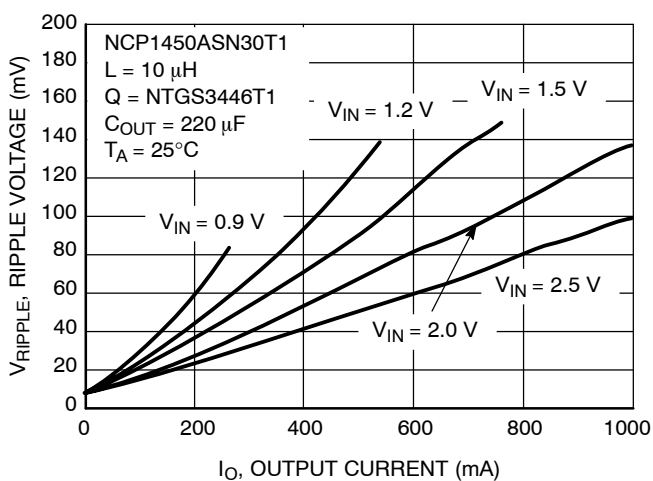


Figure 43. NCP1450ASN30T1 Ripple Voltage vs. Output Current

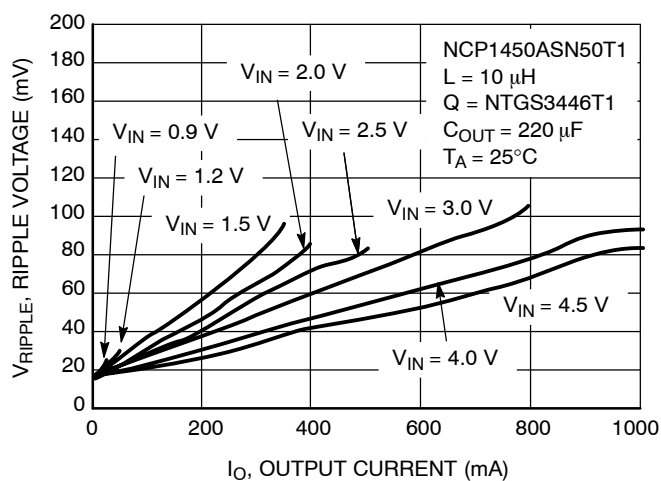


Figure 44. NCP1450ASN50T1 Ripple Voltage vs. Output Current

NCP1450A

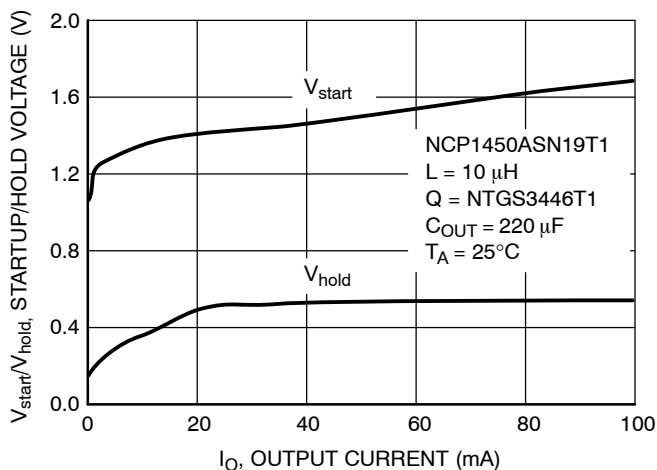


Figure 45. NCP1450ASN19T1 Startup/Hold Voltage vs. Output Current (Using MOSFET)

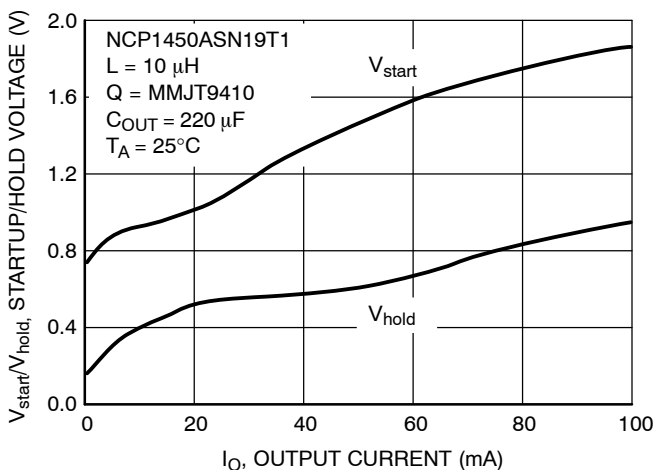


Figure 46. NCP1450ASN19T1 Startup/Hold Voltage vs. Output Current (Using BJT)

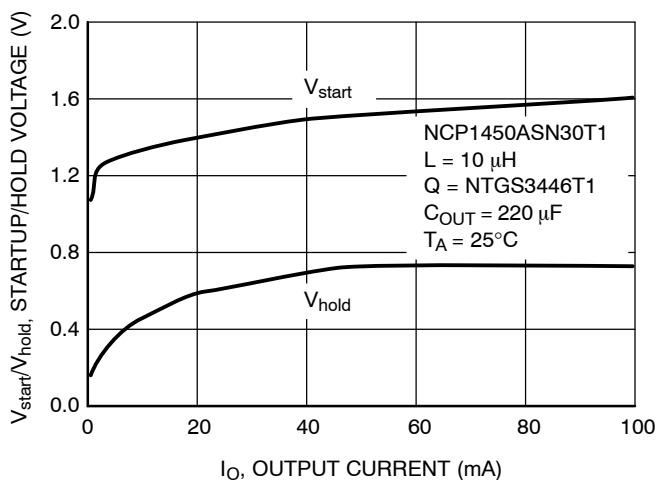


Figure 47. NCP1450ASN30T1 Startup/Hold Voltage vs. Output Current (Using MOSFET)

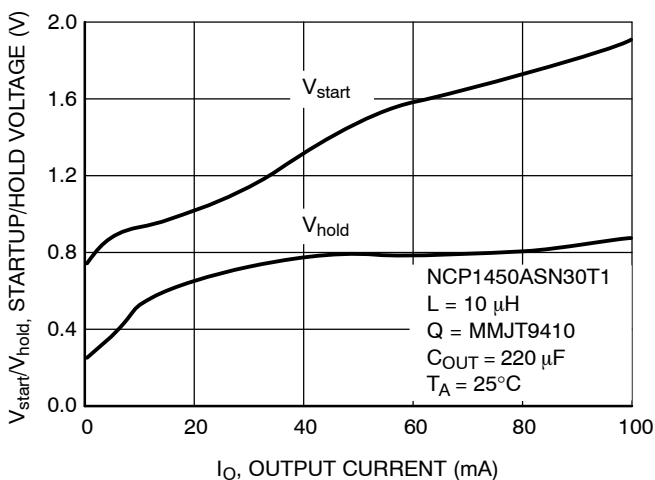


Figure 48. NCP1450ASN30T1 Startup/Hold Voltage vs. Output Current (Using BJT)

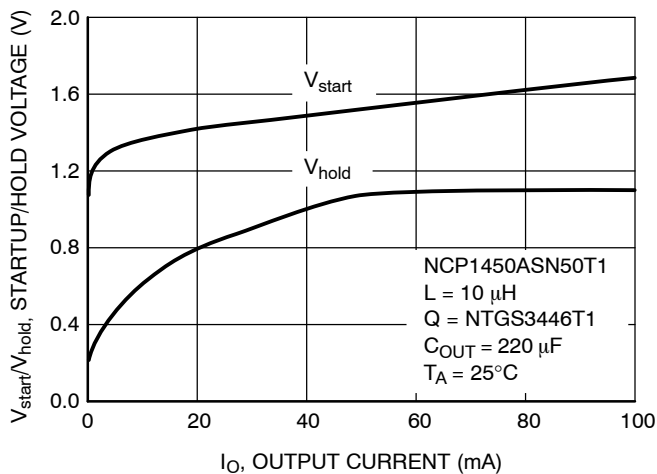


Figure 49. NCP1450ASN50T1 Startup/Hold Voltage vs. Output Current (Using MOSFET)

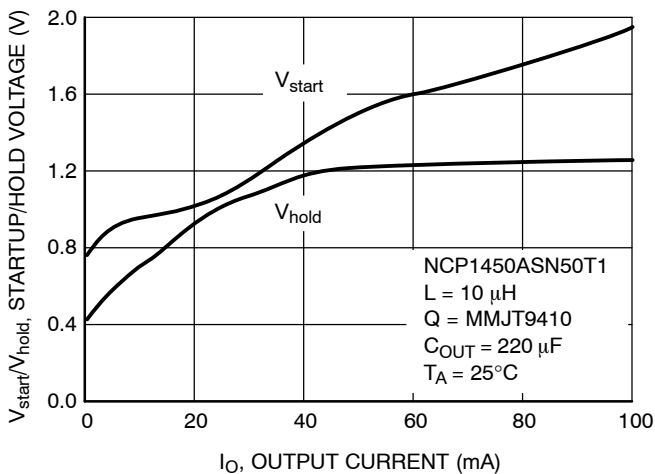


Figure 50. NCP1450ASN50T1 Startup/Hold Voltage vs. Output Current (Using BJT)

NCP1450A

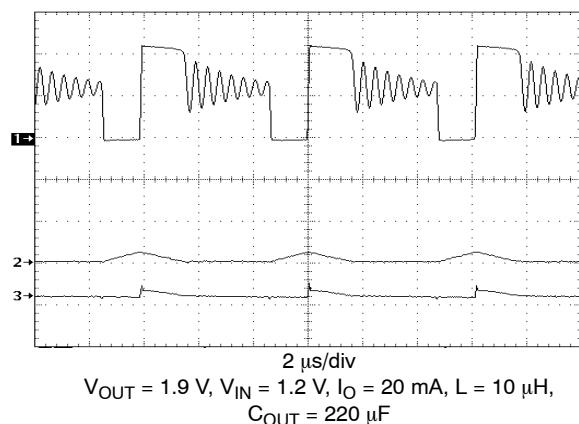


Figure 51. NCP1450ASN19T1 Operating Waveforms (Medium Load)

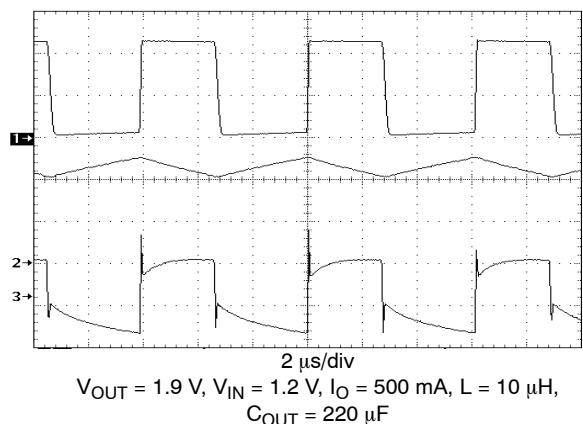


Figure 52. NCP1450ASN19T1 Operating Waveforms (Heavy Load)

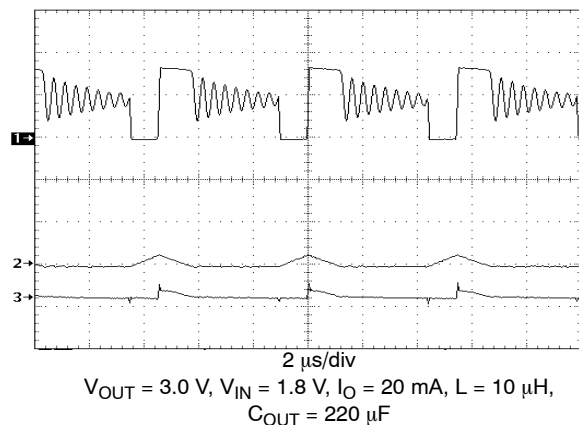


Figure 53. NCP1450ASN30T1 Operating Waveforms (Medium Load)

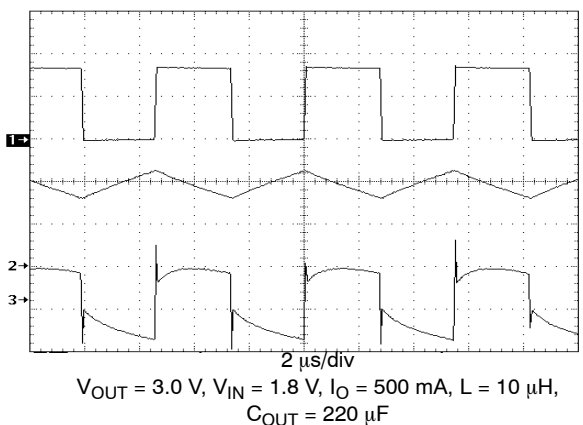


Figure 54. NCP1450ASN30T1 Operating Waveforms (Heavy Load)

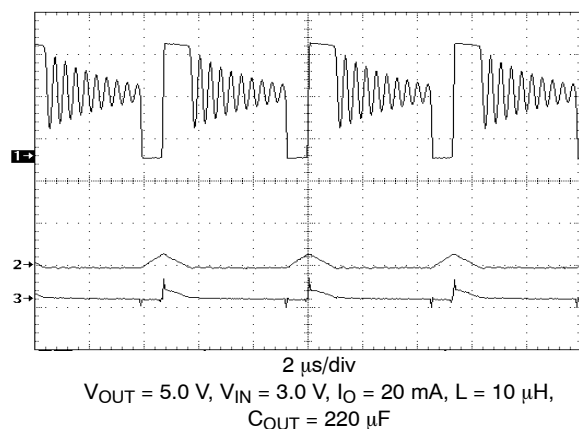


Figure 55. NCP1450ASN50T1 Operating Waveforms (Medium Load)

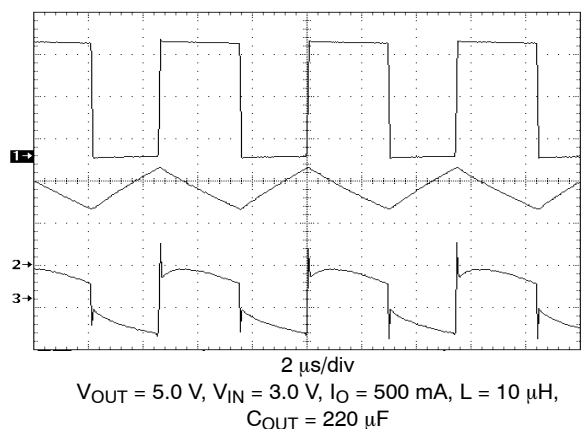
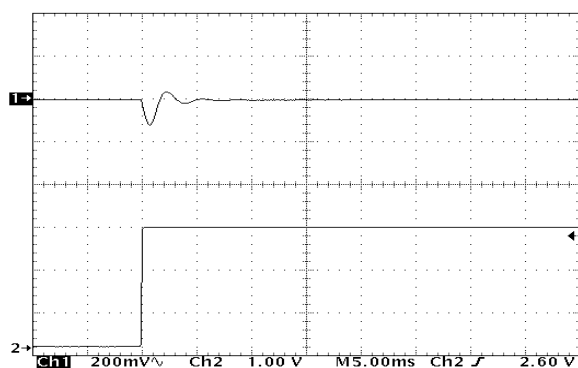


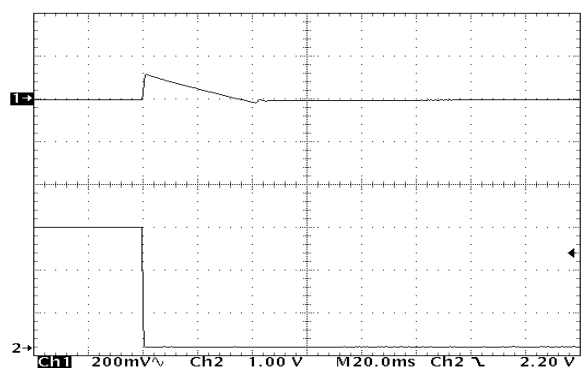
Figure 56. NCP1450ASN50T1 Operating Waveforms (Heavy Load)

NCP1450A



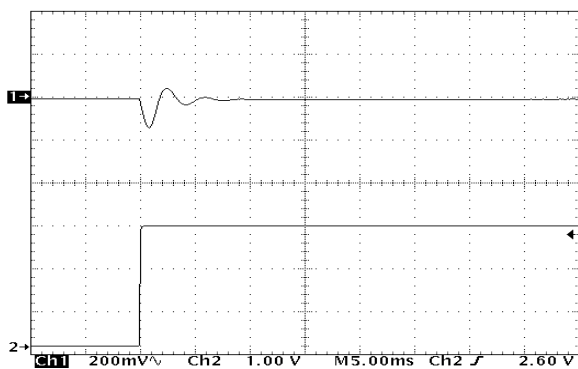
$V_{IN} = 1.5 \text{ V}$, $L = 4.7 \text{ } \mu\text{H}$, $C_{OUT} = 220 \text{ } \mu\text{F}$
 1. V_{OUT} , 1.9 V (AC coupled), 200 mV/div
 2. I_O , 1.0 mA to 100 mA

Figure 57. NCP1450ASN19T1 Load Transient Response



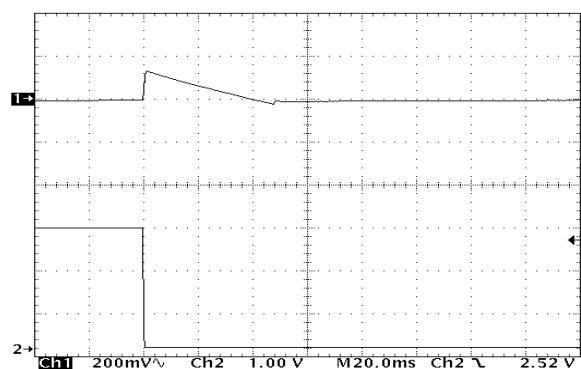
$V_{IN} = 1.5 \text{ V}$, $L = 4.7 \text{ } \mu\text{H}$, $C_{OUT} = 220 \text{ } \mu\text{F}$
 1. V_{OUT} , 1.9 V (AC coupled), 200 mV/div
 2. I_O , 100 mA to 1.0 mA

Figure 58. NCP1450ASN19T1 Load Transient Response



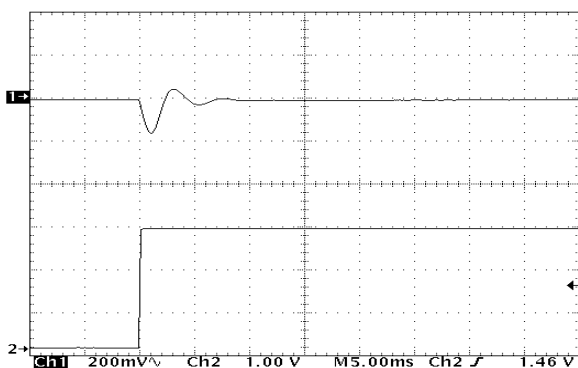
$V_{IN} = 2.0 \text{ V}$, $L = 4.7 \text{ } \mu\text{H}$, $C_{OUT} = 220 \text{ } \mu\text{F}$
 1. V_{OUT} , 3.0 V (AC coupled), 200 mV/div
 2. I_O , 1.0 mA to 100 mA

Figure 59. NCP1450ASN30T1 Load Transient Response



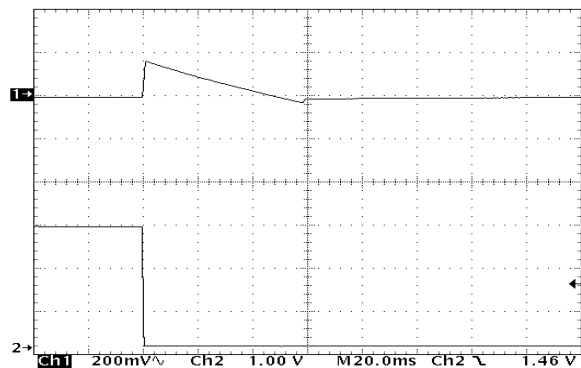
$V_{IN} = 2.0 \text{ V}$, $L = 4.7 \text{ } \mu\text{H}$, $C_{OUT} = 220 \text{ } \mu\text{F}$
 1. V_{OUT} , 3.0 V (AC coupled), 200 mV/div
 2. I_O , 100 mA to 1.0 mA

Figure 60. NCP1450ASN30T1 Load Transient Response



$V_{IN} = 3.0 \text{ V}$, $L = 4.7 \text{ } \mu\text{H}$, $C_{OUT} = 220 \text{ } \mu\text{F}$
 1. V_{OUT} , 5.0 V (AC coupled), 200 mV/div
 2. I_O , 1.0 mA to 100 mA

Figure 61. NCP1450ASN50T1 Load Transient Response



$V_{IN} = 3.0 \text{ V}$, $L = 4.7 \text{ } \mu\text{H}$, $C_{OUT} = 220 \text{ } \mu\text{F}$
 1. V_{OUT} , 5.0 V (AC coupled), 200 mV/div
 2. I_O , 100 mA to 1.0 mA

Figure 62. NCP1450ASN50T1 Load Transient Response

NCP1450A

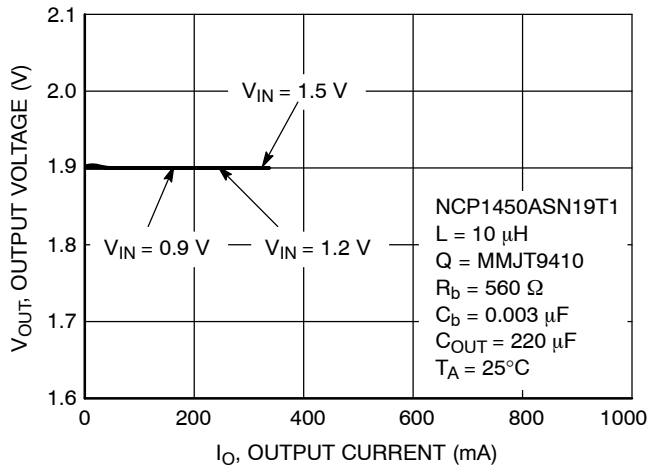


Figure 63. NCP1450ASN19T1 Output Voltage vs. Output Current (Ext. BJT)

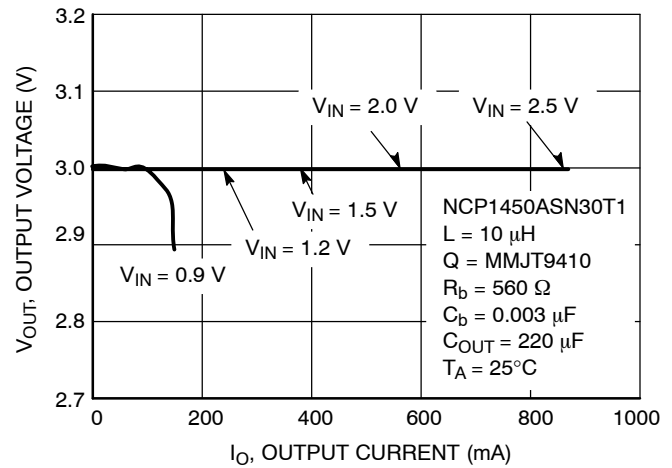


Figure 64. NCP1450ASN30T1 Output Voltage vs. Output Current (Ext. BJT)

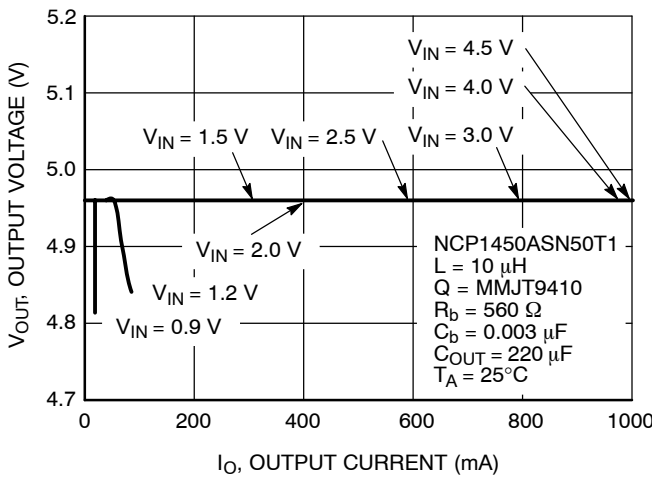


Figure 65. NCP1450ASN50T1 Output Voltage vs. Output Current (Ext. BJT)

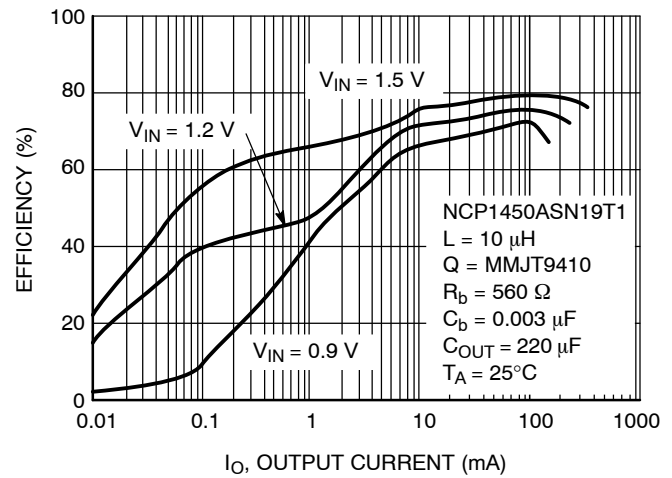


Figure 66. NCP1450ASN19T1 Efficiency vs. Output Current (Ext. BJT)

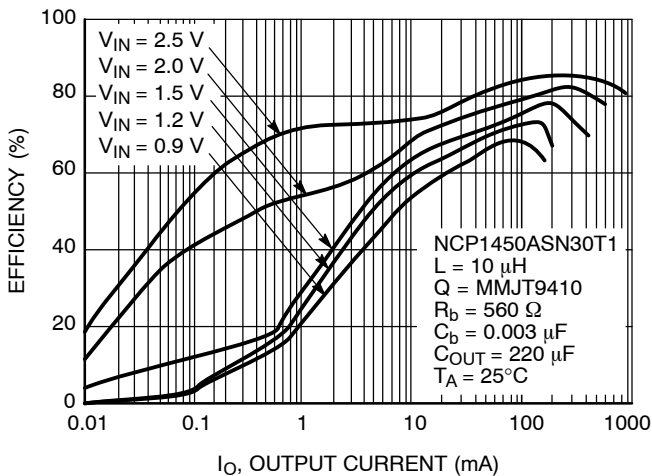


Figure 67. NCP1450ASN30T1 Efficiency vs. Output Current (Ext. BJT)

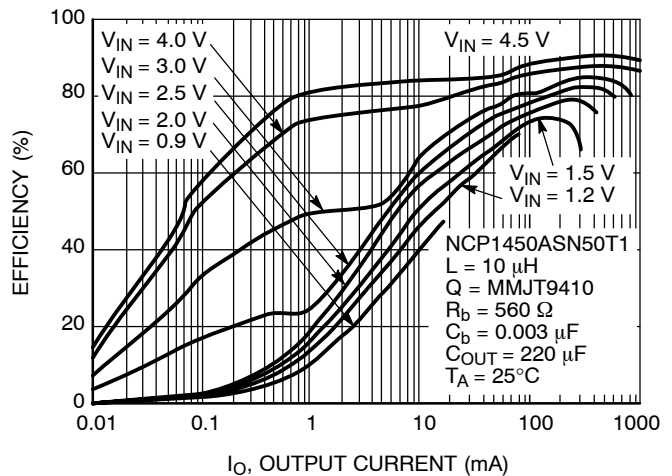


Figure 68. NCP1450ASN50T1 Efficiency vs. Output Current (Ext. BJT)

NCP1450A

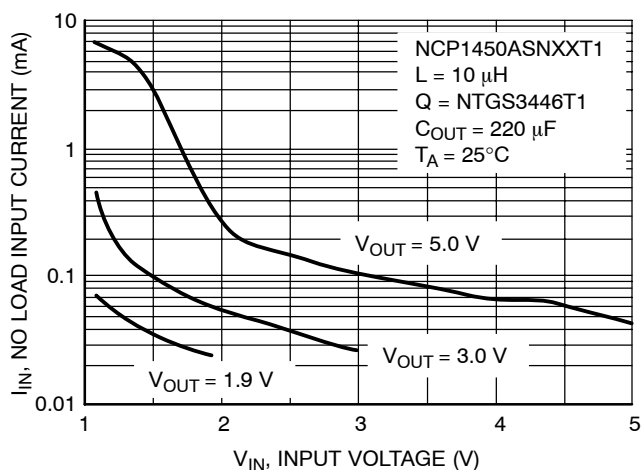


Figure 69. NCP1450ASNXXT1 No Load Input Current vs. Input Voltage (Using MOSFET)

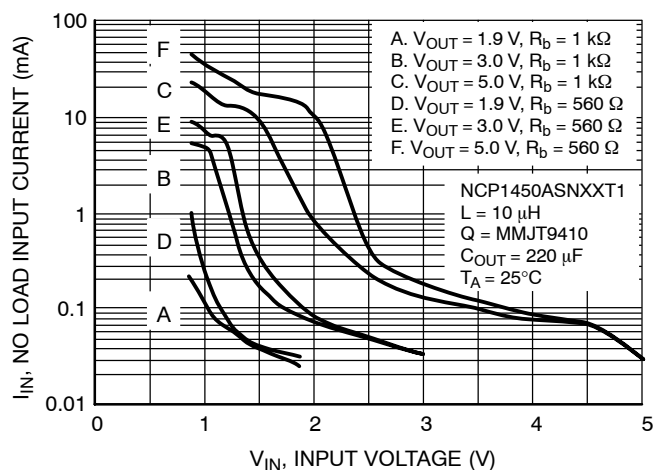


Figure 70. NCP1450ASNXXT1 No Load Input Current vs. Input Voltage (Using BJT)

Components Supplier

Parts	Supplier	Part Number	Description	Phone
Inductor: L1, L2	Sumida Electric Co. Ltd.	CD54-100MC	Inductor 10 μH/1.44 A	(852) 2880-6688
Schottky Diode: D1, D2	ON Semiconductor	MBRM110L	Schottky Power Rectifier	(852) 2689-0088
MOSFET: Q1	ON Semiconductor	NTGS3446T1	Power MOSFET N-Channel	(852) 2689-0088
BJT: Q2	ON Semiconductor	MMJT9410	Bipolar Power Transistor	(852) 2689-0088
Output Capacitor: C1, C3	KEMET Electronics Corp.	T494D227K006AS	Low ESR Tantalum Capacitor 220 μF/6.0 V	(852) 2305-1168
Input Capacitor: C2, C4	KEMET Electronics Corp.	T491C106K016AS	Low Profile Tantalum Capacitor 10 μF/16 V	(852) 2305-1168

DETAILED OPERATING DESCRIPTION

Operation

The NCP1450A series are monolithic power switching controllers optimized for battery powered portable products where large output current is required.

The NCP1450A series are low noise fixed frequency voltage-mode PWM DC-DC controllers, and consist of startup circuit, feedback resistor divider, reference voltage, oscillator, loop compensation network, PWM control circuit, and low ON resistance driver. Due to the on-chip feedback resistor and loop compensation network, the system designer can get the regulated output voltage from 1.8 V to 5.0 V with 0.1 V stepwise with a small number of external components. The quiescent current is typically 93 μ A ($V_{OUT} = 2.7$ V, $f_{OSC} = 180$ kHz), and can be further reduced to about 1.5 μ A when the chip is disabled ($V_{CE} < 0.3$ V).

The NCP1450A operation can be best understood by referring to the block diagram in Figure 2. The error amplifier monitors the output voltage via the feedback resistor divider by comparing the feedback voltage with the reference voltage. When the feedback voltage is lower than the reference voltage, the error amplifier output will decrease. The error amplifier output is then compared with the oscillator ramp voltage at the PWM controller. When the ramp voltage is higher than the error amplifier output, the high-side driver is turned on and the low-side driver is turned off which will then switch on the external transistor; and vice versa. As the error amplifier output decreases, the high-side driver turn-on time increases and duty cycle increases. When the feedback voltage is higher than the reference voltage, the error amplifier output increases and the duty cycle decreases. When the external power switch is on, the current ramps up in the inductor, storing energy in the magnetic field. When the external power switch is off, the energy stored in the magnetic field is transferred to the output filter capacitor and the load. The output filter capacitor stores the charge while the inductor current is higher than the output current, then sustains the output voltage until the next switching cycle.

As the load current is decreased, the switch transistor turns on for a shorter duty cycle. Under the light load condition, the controller will skip switching cycles to reduce power consumption, so that high efficiency is maintained at light loads.

Soft Start

There is a soft start circuit in NCP1450A. When power is applied to the device, the soft start circuit first pumps up the output voltage to approximately 1.5 V at a fixed duty cycle. This is the voltage level at which the controller can operate normally. In addition to that, the startup capability with heavy loads is also improved.

Oscillator

The oscillator frequency is internally set to 180 kHz at an accuracy of $\pm 20\%$ and with low temperature coefficient of 0.11%/°C.

Regulated Converter Voltage (V_{OUT})

The V_{OUT} is set by an integrated feedback resistor network. This is trimmed to a selected voltage from 1.8 V to 5.0 V range in 100 mV steps with an accuracy of $\pm 2.5\%$.

Compensation

The device is designed to operate in continuous conduction mode. An internal compensation circuit was designed to guarantee stability over the full input/output voltage and full output load range.

Enable/Disable Operation

The NCP1450A series offer IC shutdown mode by chip enable pin (CE pin) to reduce current consumption. When voltage at pin CE is equal or greater than 0.9 V, the chip will be enabled, which means the controller is in normal operation. When voltage at pin CE is less than 0.3 V, the chip is disabled, which means IC is shutdown.

Important: DO NOT apply a voltage between 0.3 V to 0.9 V to pin CE as this is the CE pin's hysteresis voltage range. Clearly defined output states can only be obtained by applying voltage out of this range.

APPLICATION CIRCUIT INFORMATION

Step-up Converter Design Equations

The NCP1450A PWM step-up DC-DC controller is designed to operate in continuous conduction mode and can be defined by the following equations. External components values can be calculated from these equations, however, the optimized value should be obtained through experimental results.

Calculation	Equation
D	$\leq \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D - V_S}$
I_L	$\frac{I_O}{(1 - D)}$
L	$\frac{(V_{OUT} + V_D - V_{IN})(1 - D)^2}{f \times I_O \times DIR}$
I_{PK}	$I_L (1 + \frac{DIR}{2})$
ΔQ	$\frac{(I_L - I_O)(1 - D)}{f}$
V_{PP}	$\approx \frac{\Delta Q}{C_{OUT}} + (I_L - I_O) ESR$

NOTES:

- D – On-time duty cycle
- I_L – Average inductor current
- I_{PK} – Peak inductor current
- DIR – Delta inductor current to average inductor current ratio
- I_O – Desired dc output current
- V_{IN} – Nominal operating dc input voltage
- V_{OUT} – Desired dc output voltage
- V_D – Diode forward voltage
- V_S – Saturation voltage of the external transistor switch
- ΔQ – Charge stores in the C_{OUT} during charging up
- ESR – Equivalent series resistance of the output capacitor

Design Example

It is supposed that a step-up DC-DC controller with 3.3 V output delivering a maximum 1000 mA output current with 100 mV output ripple voltage powering from a 2.4 V input is to be designed.

Design parameters:

$$\begin{aligned} V_{IN} &= 2.4 \text{ V} \\ V_{OUT} &= 3.3 \text{ V} \\ I_O &= 1.0 \text{ A} \\ V_{PP} &= 100 \text{ mV} \\ f &= 180 \text{ kHz} \end{aligned}$$

DIR = 0.2 (typical for small output ripple voltage)

Assume the diode forward voltage and the transistor saturation voltage are both 0.3 V. Determine the maximum steady state duty cycle at $V_{IN} = 2.4 \text{ V}$:

$$D = \frac{3.3 \text{ V} + 0.3 \text{ V} - 2.4 \text{ V}}{3.3 \text{ V} + 0.3 \text{ V} - 0.3 \text{ V}} = 0.364$$

Calculate the maximum inductance value which can generate the desired current output and the preferred delta inductor current to average inductor current ratio:

$$L \leq \frac{(3.3 \text{ V} + 0.3 \text{ V} - 2.4 \text{ V})(1 - 0.364)^2}{180000 \text{ Hz} \times 1 \text{ A} \times 0.2} = 13.5 \mu\text{H}$$

Determine the average inductor current and peak inductor current:

$$I_L = \frac{1}{1 - 0.364} = 1.57 \text{ A}$$

$$I_{PK} = 1.57 \text{ A} (1 + \frac{0.2}{2}) = 1.73 \text{ A}$$

Therefore, a 12 μH inductor with saturation current larger than 1.73 A can be selected as the initial trial.

Calculate the delta charge stored in the output capacitor during the charging up period in each switching cycle:

$$\Delta Q = \frac{(1.57 \text{ A} - 1 \text{ A})(1 - 0.364)}{18000 \text{ Hz}} = 2.01 \mu\text{C}$$

Determine the output capacitance value for the desired output ripple voltage:

Assume the ESR of the output capacitor is 0.15 Ω ,

$$C_{OUT} > \frac{2.01 \mu\text{C}}{100 \text{ mV} - (1.57 \text{ A} - 1 \text{ A}) \times 0.15 \Omega} = 138.6 \mu\text{F}$$

Therefore, a Tantalum capacitor with value of 150 μF to 220 μF and ESR of 0.15 Ω can be used as the output capacitor. However, according to experimental result, 220 μF output capacitor gives better overall operational stability and smaller ripple voltage.

External Component Selection

Inductor Selection

The NCP1450A is designed to work well with a 6.8 to 12 μH inductors in most applications 10 μH is a sufficiently low value to allow the use of a small surface mount coil, but large enough to maintain low ripple. Lower inductance values supply higher output current, but also increase the ripple and reduce efficiency.

Higher inductor values reduce ripple and improve efficiency, but also limit output current.

The inductor should have small DCR, usually less than 1 Ω , to minimize loss. It is necessary to choose an inductor with a saturation current greater than the peak current which the inductor will encounter in the application.

Diode

The diode is the largest source of loss in DC–DC converters. The most importance parameters which affect their efficiency are the forward voltage drop, V_D , and the reverse recovery time, t_{rr} . The forward voltage drop creates a loss just by having a voltage across the device while a current flowing through it. The reverse recovery time generates a loss when the diode is reverse biased, and the current appears to actually flow backwards through the diode due to the minority carriers being swept from the P–N junction. A Schottky diode with the following characteristics is recommended:

- Small forward voltage, $V_F < 0.3 \text{ V}$
- Small reverse leakage current
- Fast reverse recovery time/switching speed
- Rated current larger than peak inductor current,
 $I_{\text{rated}} > I_{PK}$
- Reverse voltage larger than output voltage,
 $V_{\text{reverse}} > V_{\text{OUT}}$

Input Capacitor

The input capacitor can stabilize the input voltage and minimize peak current ripple from the source. The value of the capacitor depends on the impedance of the input source used. Small Equivalent Series Resistance (ESR) Tantalum or ceramic capacitor with a value of 10 μF should be suitable.

Output Capacitor

The output capacitor is used for sustaining the output voltage when the external MOSFET or bipolar transistor is switched on and smoothing the ripple voltage. Low ESR capacitor should be used to reduce output ripple voltage. In general, a 100 μF to 220 μF low ESR (0.10 Ω to 0.30 Ω) Tantalum capacitor should be appropriate.

External Switch Transistor

An enhancement N–channel MOSFET or a bipolar NPN transistor can be used as the external switch transistor.

For enhancement N–channel MOSFET, since enhancement MOSFET is a voltage driven device, it is a

more efficient switch than a BJT transistor. However, the MOSFET requires a higher voltage to turn on as compared with BJT transistors. An enhancement N–channel MOSFET can be selected by the following guidelines:

16. Low ON–resistance, $R_{DS(on)}$, typically $< 0.1 \Omega$.
17. Low gate threshold voltage, $V_{GS(th)}$, must be $< V_{OUT}$, typically $< 1.5 \text{ V}$, it is especially important for the low V_{OUT} device, like $V_{OUT} = 1.9 \text{ V}$.
18. Rated continuous drain current, I_D , should be larger than the peak inductor current, i.e. $I_D > I_{PK}$.
19. Gate capacitance should be 1200 pF or less.

For bipolar NPN transistor, medium power transistor with continuous collector current typically 1 A to 5 A and $V_{CE(sat)} < 0.2 \text{ V}$ should be employed. The driving capability is determined by the DC current gain, H_{FE} , of the transistor and the base resistor, R_b ; and the controller's EXT pin must be able to supply the necessary driving current.

R_b can be calculated by the following equation:

$$R_b = \frac{V_{OUT} - 0.7}{I_b} - \frac{0.4}{|I_{EXTH}|}$$

$$I_b = \frac{I_{PK}}{H_{FE}}$$

Since the pulse current flows through the transistor, the exact R_b value should be finely tuned by the experiment. Generally, a small R_b value can increase the output current capability, but the efficiency will decrease due to more energy is used to drive the transistor.

Moreover, a speed–up capacitor, C_b , should be connected in parallel with R_b to reduce switching loss and improve efficiency. C_b can be calculated by the equation below:

$$C_b \leq \frac{1}{2\pi \times R_b \times f_{OSC} \times 0.7}$$

It is due to the variation in the characteristics of the transistor used. The calculated value should be used as the initial test value and the optimized value should be obtained by the experiment.

External Component Reference Data

Device	V_{OUT}	Inductor Model	Inductor Value	External Transistor	Diode	Output Capacitor
NCP1450ASN19T1	1.9 V	CD54	12 μH	NTGS3446T1	MBRM110L	220 μF
NCP1450ASN30T1	3.0 V	CD54	10 μH	NTGS3446T1	MBRM110L	220 μF
NCP1450ASN50T1	5.0 V	CD54	10 μH	NTGS3446T1	MBRM110L	220 μF
NCP1450ASN19T1	1.9 V	CD54	12 μH	MMJT9410	MBRM110L	220 μF
NCP1450ASN30T1	3.0 V	CD54	10 μH	MMJT9410	MBRM110L	220 μF
NCP1450ASN50T1	5.0 V	CD54	10 μH	MMJT9410	MBRM110L	220 μF

NCP1450A

An evaluation board of NCP1450A has been made in the small size of 89 mm x 51 mm. The artwork and the silk screen of the surface-mount evaluation board PCB are shown in Figures 71 and 72. Please contact your

ON Semiconductor representative for availability. The evaluation board schematic diagrams are shown in Figures 73 and 74.

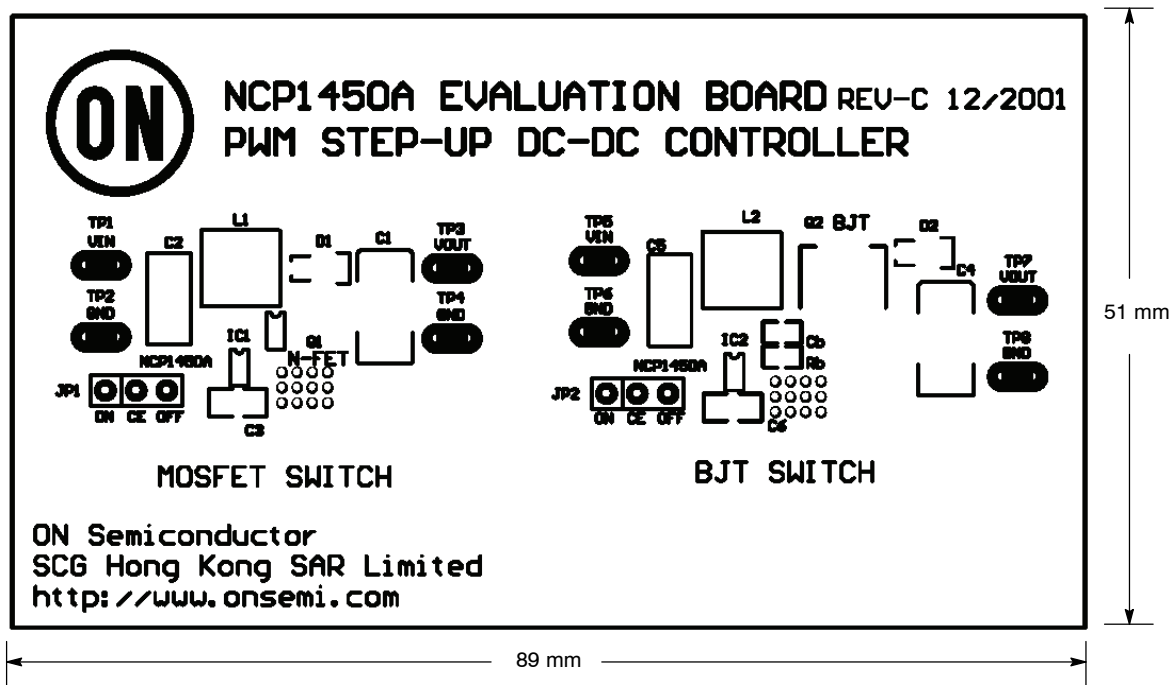


Figure 71. NCP1450A PWM Step-up DC-DC Controller Evaluation Board Silkscreen

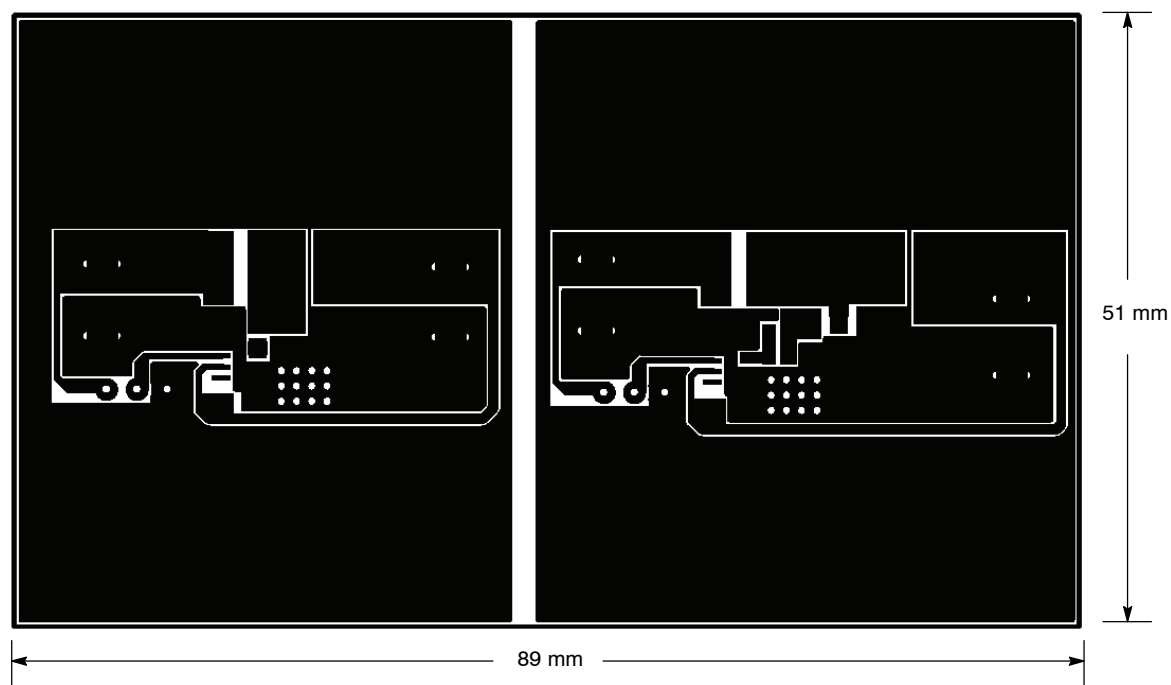


Figure 72. NCP1450A PWM Step-up DC-DC Controller Evaluation Board Artwork (Component Side)

NCP1450A

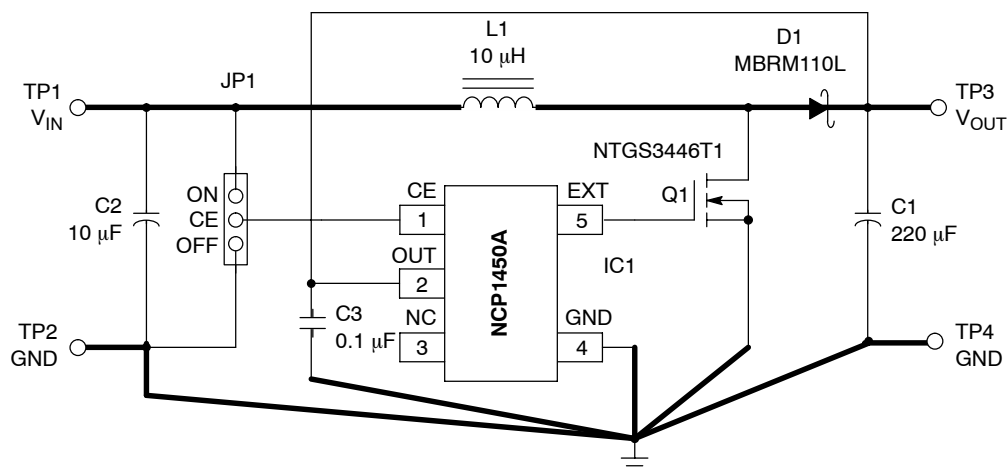


Figure 73. NCP1450A Evaluation Board Schematic Diagram 1 (Step-up DC-DC Converter Using External MOSFET Switch)

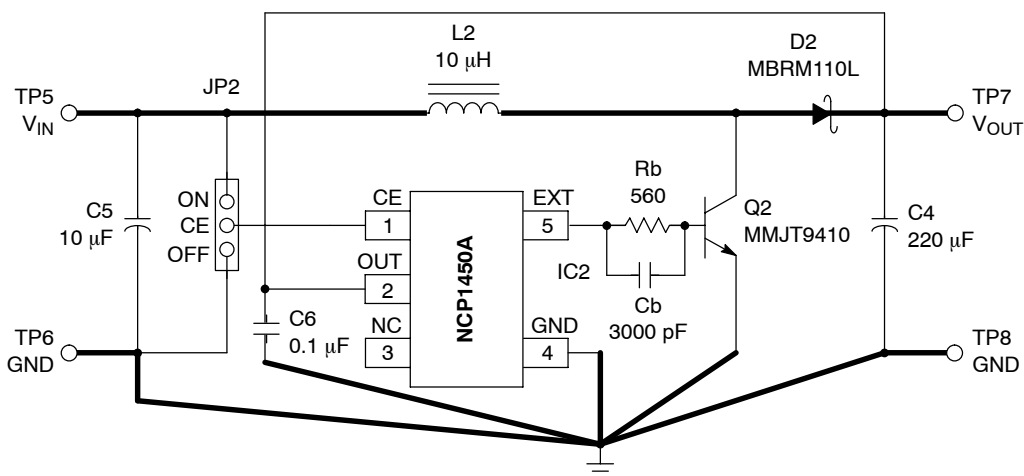


Figure 74. NCP1450A Evaluation Board Schematic Diagram 2 (Step-up DC-DC Converter Using External Bipolar Transistor Switch)

PCB Layout Hints

Grounding

One point grounding should be used for the output power return ground, the input power return ground, and the device switch ground to reduce noise. In Figure 73, e.g.: C2 GND, C1 GND, and IC1 GND are connected at one point in the evaluation board. The input ground and output ground traces must be thick enough for current to flow through and for reducing ground bounce.

Power Signal Traces

Low resistance conducting paths should be used for the power carrying traces to reduce power loss so as to improve efficiency (short and thick traces for connecting the inductor L can also reduce stray inductance), e.g.: short and thick traces listed below are used in the evaluation board:

1. Trace from TP1 to L1
2. Trace from L1 to anode pin of D1
3. Trace from cathode pin of D1 to TP3

Output Capacitor

The output capacitor should be placed close to the output terminals to obtain better smoothing effect on the output ripple.

Switching Noise Decoupling Capacitor

A 0.1 µF ceramic capacitor should be placed close to the OUT pin and GND pin of the NCP1450A to filter the switching spikes in the output voltage monitored by the OUT pin.

CS5112

1.4 A Switching Regulator with 5.0 V, 100 mA Linear Regulator with Watchdog, RESET and ENABLE

The CS5112 is a dual output power supply integrated circuit. It contains a 5.0 V $\pm 2\%$, 100 mA linear regulator, a watchdog timer, a linear output voltage monitor to provide a Power On Reset (POR) and a 1.4 A current mode PWM switching regulator.

The 5.0 V linear regulator is comprised of an error amplifier, reference, and supervisory functions. It has low internal supply current consumption and provides 1.2 V (typical) dropout voltage at maximum load current.

The watchdog timer circuitry monitors an input signal (WDI) from the microprocessor. It responds to the falling edge of this watchdog signal. If a correct watchdog signal is not received within the externally programmable time, a reset signal is issued.

The externally programmable active reset circuit operates correctly for an output voltage (V_{LIN}) as low as 1.0 V. During power up, or if the output voltage shifts below the regulation limit, $\overline{\text{RESET}}$ toggles low and remains low for the duration of the delay after proper output voltage regulation is restored. Additionally a reset pulse is issued if the correct watchdog is not received within the programmed time. Reset pulses continue until the correct watchdog signal is received. The reset pulse width and frequency, as well as the Power On Reset delay, are set by one external RC network.

The current mode PWM switching regulator is comprised of an error amplifier with selectable feedback inputs, a current sense amplifier, an adjustable oscillator, and a 1.4 A output power switch with anti-saturation control. The switching regulator can be configured in a variety of topologies.

The CS5112 is load dump capable and has protection circuitry which includes current limit on the linear and switcher outputs, and an overtemperature limiter.

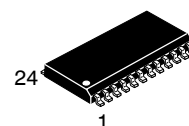
Features

- Linear Regulator
 - 5.0 V $\pm 2\%$ @ 100 mA
- Switching Regulator
 - 1.4 A Peak Internal Switch
 - 120 kHz Maximum Switching Frequency
 - 5.0 V to 26 V Operating Supply Range
- Smart Functions
 - Watchdog
 - $\overline{\text{RESET}}$
 - $\overline{\text{ENABLE}}$
- Protection
 - Overtemperature
 - Current Limit
- Internally Fused Leads in SO-24L Package



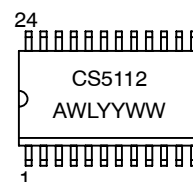
ON Semiconductor™

<http://onsemi.com>



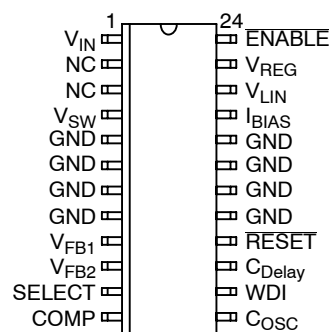
SO-24L
DWF SUFFIX
CASE 751E

MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping
CS5112YDWF24	SO-24L	31 Units/Rail
CS5112YDWFR24	SO-24L	1000 Tape & Reel

CS5112

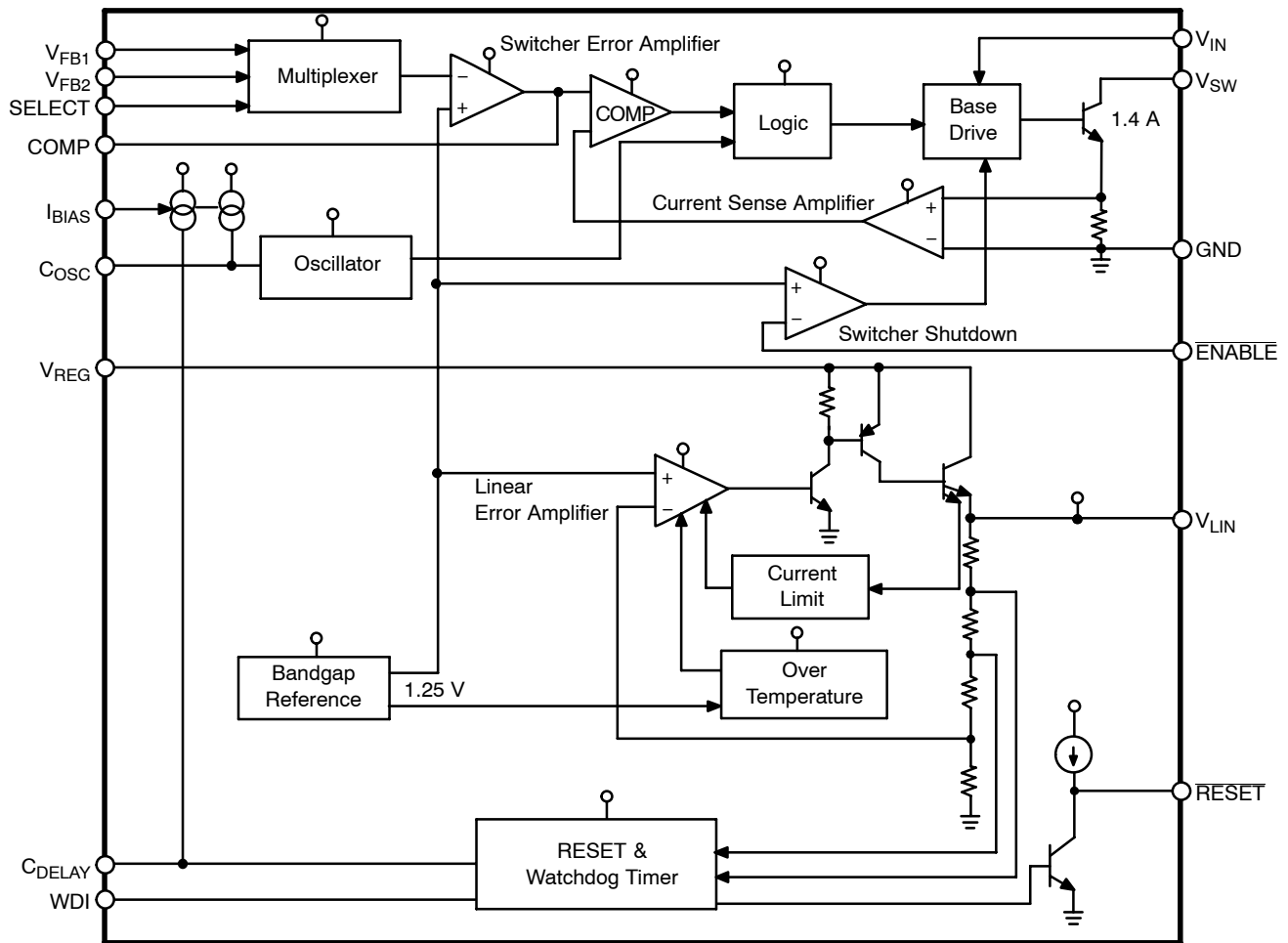


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*

Rating	Value	Unit
Logic Inputs/Outputs ($\overline{\text{ENABLE}}$, SELECT, WDI, RESET)	-0.3 to V_{LIN}	V
V_{LIN}	-0.3 to 10	
V_{IN} , V_{REG} : DC Input Voltage Peak Transient Voltage (26 V Load Dump @ 14 V V_{IN})	-0.3 to 26	V
	-0.3 to 40	V
V_{SW} Peak Transient Voltage	54	V
C_{OSC} , C_{Delay} , COMP, V_{FB1} , V_{FB2}	-0.3 to V_{LIM}	V
Power Dissipation	Internally Limited	-
V_{LIN} Output Current	Internally Limited	-
V_{SW} Output Current	Internally Limited	-
RESET Output Sink Current	5.0	mA
ESD Susceptibility (Human Body Model)	2.0	kV
ESD Susceptibility (Machine Model)	200	V
Storage Temperature	-65 to 150	°C
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1)	230 peak

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

CS5112

ELECTRICAL CHARACTERISTICS (5.0 V ≤ V_{IN} ≤ 26 V and -40°C ≤ T_J ≤ 150°C, C_{OUT} = 100 μF (ESR ≤ 8.0 Ω), C_{Delay} = 0.1 μF, R_{BIAS} = 64.9 kΩ, C_{OSC} = 390 pF, C_{COMP} = 0.1 μF; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit

General

I _{IN} Off Current	6.6 V ≤ V _{IN} ≤ 26 V, I _{SW} = 0 A	–	–	2.0	mA
I _{IN} On Current	6.6 V ≤ V _{IN} ≤ 26 V, I _{SW} = 1.4 A	–	30	70	mA
I _{REG} Current	I _{LIN} = 100 mA, 6.6 V ≤ V _{IN} ≤ 26 V	–	–	6.0	mA
Thermal Limit	Guaranteed by Design	160	–	210	°C

5.0 V Regulator Section

V _{LIN} Output Voltage	6.6 V ≤ V _{REG} ≤ 26 V, 1.0 mA ≤ I _{LIN} ≤ 100 mA	4.9	5.0	5.1	V
Dropout Voltage	(V _{REG} – V _{LIN}) @ I _{LIN} = 100 mA	–	1.2	1.5	V
Line Regulation	6.6 V ≤ V _{REG} ≤ 26 V, I _{LIN} = 5.0 mA	–	5.0	25	mV
Load Regulation	V _{REG} = 19 V, 1.0 mA ≤ I _{LIN} ≤ 100 mA	–	5.0	25	mV
Current Limit	6.6 V ≤ V _{REG} ≤ 26 V	120	–	–	mA
DC Ripple Rejection	14 V ≤ V _{REG} ≤ 24 V	60	75	–	dB

RESET Section

Low Threshold (V _{RTL})	V _{LIN} Decreasing	4.05	4.25	4.45	V
High Threshold (V _{RTH})	V _{LIN} Increasing	4.2	4.45	4.7	V
Hysteresis	V _{RTH} – V _{RTL}	140	190	240	mV
Active High	V _{LIN} > V _{RTH} , I _{RESET} = -25 μA	V _{LIN} – 0.5	–	–	V
Active Low	V _{LIN} = 1.0 V, 10 kΩ Pull-Up from RESET to V _{LIN}	–	–	0.4	V
	V _{LIN} = 4.0 V, I _{RESET} = 1.0 mA	–	–	0.7	V
Delay	Invalid WDI	6.25	8.78	11	ms
Power On Delay	V _{LIN} Crossing V _{RTH}	6.25	–	–	ms

Watchdog Input (WDI)

V _{IH}	Peak WDI Needed to Activate RESET	–	–	2.0	V
V _{IL}	–	0.8	–	–	V
Hysteresis	Note 2	25	50	–	mV
Pull-Up Resistor	WDI = 0 V	20	50	100	kΩ
Low Threshold	–	6.25	8.78	11	ms
Floating Input Voltage	–	3.5	–	–	V
WDI Pulse Width	–	–	–	5.0	μs

Switcher Section

Minimum Operating Input Voltage	–	–	–	5.0	V
Switching Frequency	Refer to Figure 5	80	95	110	kHz
Switch Saturation Voltage	I _{SW} = 1.4 A	0.7	1.1	1.6	V
Output Current Limit	–	1.4	–	2.5	A
Max Switching Frequency	V _{SW} = 7.5 V with 50 Ω Load, Refer to Figure 5	120	–	–	kHz
V _{FB1} Regulation Voltage	–	1.206	1.25	1.294	V

2. Guaranteed by design, not 100% tested in productions.

CS5112

ELECTRICAL CHARACTERISTICS (continued) ($5.0\text{ V} \leq V_{\text{IN}} \leq 26\text{ V}$ and $-40^{\circ}\text{C} \leq T_{\text{J}} \leq 150^{\circ}\text{C}$, $C_{\text{OUT}} = 100\text{ }\mu\text{F}$ ($\text{ESR} \leq 8.0\text{ }\Omega$), $C_{\text{Delay}} = 0.1\text{ }\mu\text{F}$, $R_{\text{BIAS}} = 64.9\text{ k}\Omega$, $C_{\text{OSC}} = 390\text{ pF}$, $C_{\text{COMP}} = 0.1\text{ }\mu\text{F}$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Switcher Section (continued)					
V_{FB2} Regulation Voltage	–	1.206	1.25	1.294	V
V_{FB1} , V_{FB2} Input Current	$V_{\text{FB1}} = V_{\text{FB2}} = 5.0\text{ V}$	–	–	1.0	μA
Oscillator Charge Current	$C_{\text{OSC}} = 0\text{ V}$	35	40	45	μA
Oscillator Discharge Current	$C_{\text{OSC}} = V40$	270	320	370	μA
C_{Delay} Charge Current	$C_{\text{Delay}} = 0\text{ V}$	35	40	45	μA
Switcher Max Duty Cycle	$V_{\text{SW}} = 5.0\text{ V}$ with $50\text{ }\Omega$ Load, $V_{\text{FB1}} = V_{\text{FB2}} = 1.0\text{ V}$	72	85	95	%
Current Sense Amp Gain	$I_{\text{SW}} = 2.3\text{ A}$	–	7.0	–	V/V
Error Amp DC Gain	–	–	67	–	dB
Error Amp Transconductance	–	–	2700	–	$\mu\text{A/V}$

ENABLE Input

VIL	–	0.8	1.24	–	V
VIH	–	–	1.3	2.0	V
Hysteresis	–	–	60	–	mV
Input Impedance	–	10	20	40	k Ω

Select Input

VIL (Selects V_{FB1})	$4.9 \leq V_{\text{LIN}} \leq 5.1$	0.8	1.25	–	V
VIH (Selects V_{FB2})	$4.9 \leq V_{\text{LIN}} \leq 5.1$	–	1.25	2.0	V
SELECT Pull-Up	SELECT = 0 V	10	24	50	k Ω
Floating Input Voltage	–	3.5	4.5	–	V

PIN FUNCTION DESCRIPTION

PACKAGE PIN #	PIN SYMBOL	FUNCTION
SO-24L		
1	V_{IN}	Supply voltage.
2, 3	NC	No connection.
4	V_{SW}	Collector of NPN power switch for switching regulator section.
5, 6, 7, 8, 17, 18, 19, 20	GND	Connected to the heat removing leads.
9	V_{FB1}	Feedback input voltage 1 (referenced to 1.25 V).
10	V_{FB2}	Feedback input voltage 2 (referenced to 1.25 V).
11	SELECT	Logic level input that selects either V_{FB1} or V_{FB2} . An open selects V_{FB2} . Connect to GND to select V_{FB1} .
12	COMP	Output of the transconductance error amplifier.
13	C_{OSC}	A capacitor connected to GND sets the switching frequency. Refer to Figure 5.
14	WDI	Watchdog input. Active on falling edge.
15	C_{Delay}	A capacitor connected to GND sets the Power On Reset and Watchdog time.
16	RESET	RESET output. Active low if V_{LIN} is below the regulation limit. If watchdog timeout is reached, a reset pulse train is issued.
21	I_{BIAS}	A resistor connected to GND sets internal bias currents as well as the C_{OSC} and C_{Delay} charge currents.

PIN FUNCTION DESCRIPTION (continued)

PACKAGE PIN #	PIN SYMBOL	FUNCTION
SO-24L		
22	V_{LIN}	Regulated 5.0 V output from the linear regulator section.
23	V_{REG}	Input voltage to the linear regulator and the internal supply circuitry.
24	$\overline{ENABLE}$	Logic level input to shut down the switching regulator.

TYPICAL PERFORMANCE CHARACTERISTICS

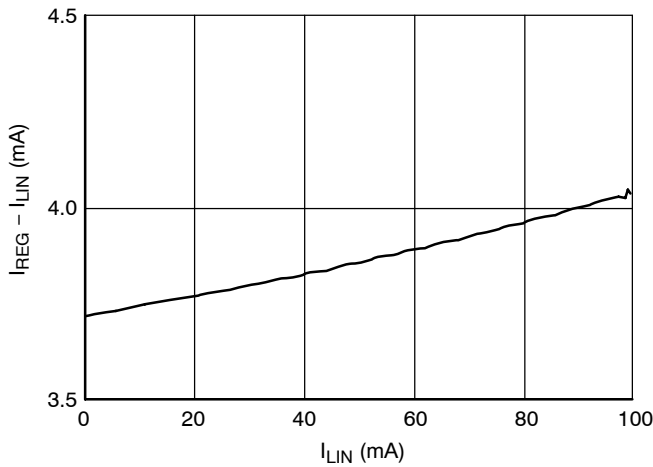


Figure 2. 5.0 V Regulator Bias Current vs. Load Current

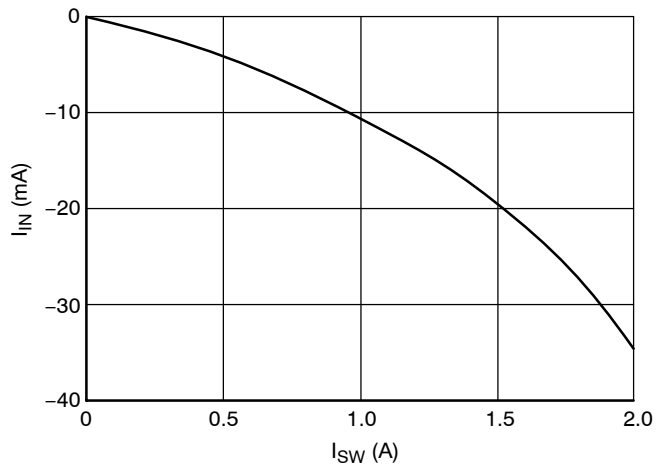


Figure 3. Supply Current vs. Switch Current

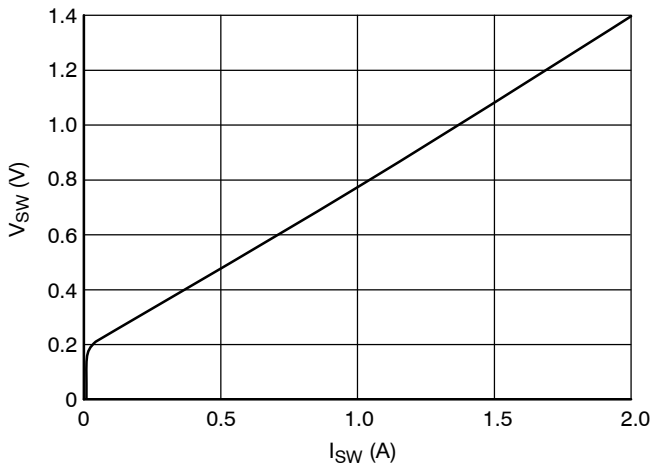
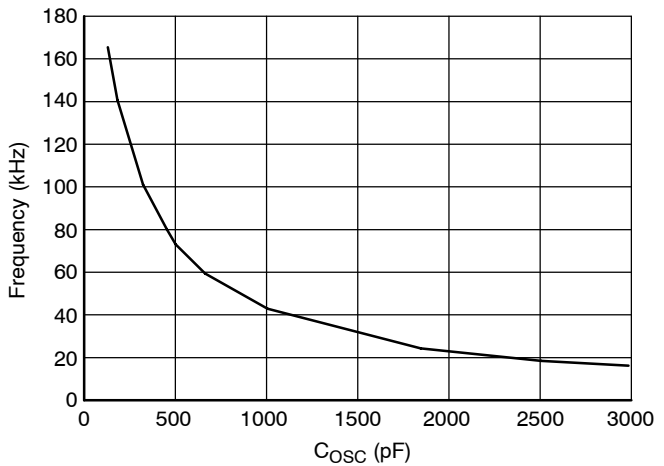


Figure 4. Switch Saturation Voltage

Figure 5. Oscillator Frequency (kHz) vs. C_{OSC} (pF), Assuming $R_{BIAS} = 64.9 \text{ k}\Omega$

CIRCUIT DESCRIPTION

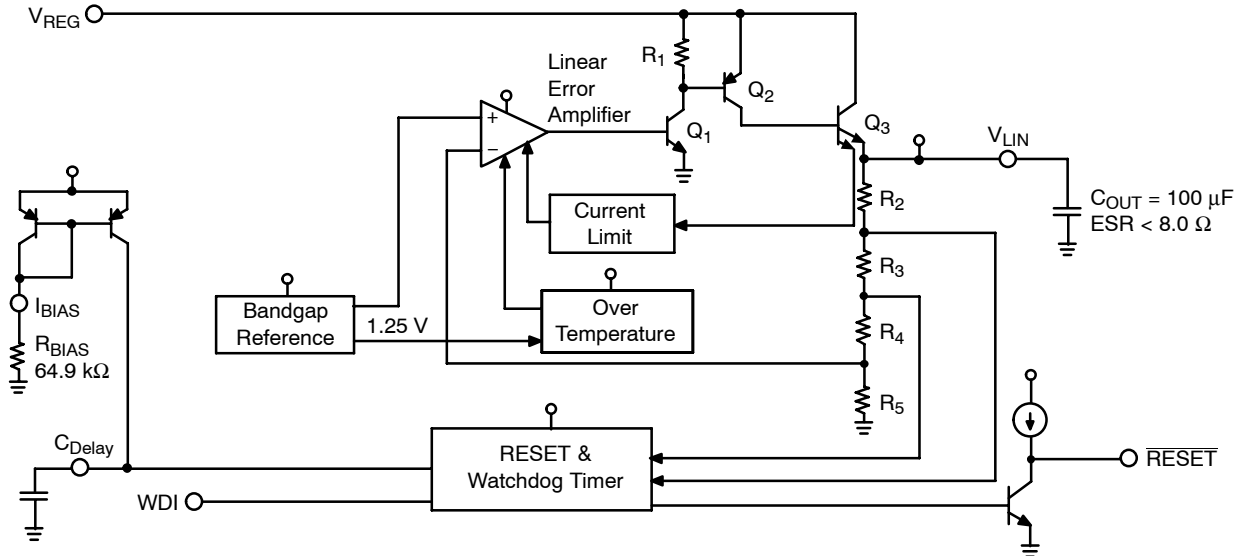


Figure 6. Block Diagram of 5.0 V Linear Regulator Portion of the CS5112

5.0 V LINEAR REGULATOR

The 5.0 V linear regulator consists of an error amplifier, bandgap voltage reference, and a composite pass transistor.

The 5.0 V linear regulator circuitry is shown in Figure 6. When an unregulated voltage greater than 6.6 V is applied to the V_{REG} input, a 5.0 V regulated DC voltage will be present at V_{LIN} . For proper operation of the 5.0 V linear regulator, the I_{BIAS} lead must have a 64.9 kΩ pull down resistor to ground. A 100 μF or larger capacitor with an ESR < 8.0 Ω must be connected between V_{LIN} and ground. To operate the 5.0 V linear regulator as an independent regulator (i.e. separate from the switching supply), the input voltage must be tied to the V_{REG} lead.

As the voltage at the V_{REG} input is increased, Q_1 is turned on. Q_1 provides base drive for Q_2 which in turn provides base current for Q_3 . As Q_3 is turned on, the output voltage, V_{LIN} , begins to rise as Q_3 's output current charges the output capacitor, C_{OUT} . Once V_{LIN} rises to a certain level, the error amplifier becomes biased and provides the appropriate amount of base current to Q_1 . The error amplifier monitors the scaled output voltage via an internal voltage divider, R_2 through R_5 , and compares it to the bandgap voltage reference. The error amplifier output or error signal is an output current equal to the error amplifier's input differential voltage times the transconductance of the amplifier. Therefore, the error amplifier varies the base current to Q_1 , which provides bias to Q_2 and Q_3 , based on the difference between the reference voltage and the scaled V_{LIN} output voltage.

CONTROL FUNCTIONS

The watchdog timer circuitry monitors an input signal (WDI) from the microprocessor. It responds to the falling edge of this watchdog signal which it expects to see within an externally programmable time (see Figure 7).

The watchdog time is given by:

$$t_{WDI} = 1.353 \times C_{Delay} R_{BIAS}$$

Using $C_{Delay} = 0.1 \mu F$ and $R_{BIAS} = 64.9 k\Omega$ gives a time ranging from 6.25 ms to 11 ms assuming ideal components. Based on this, the software must be written so that the watchdog arrives at least every 6.25 ms. In practice, the tolerance of C_{Delay} and R_{BIAS} must be taken into account when calculating the minimum watchdog time (t_{WDI}).

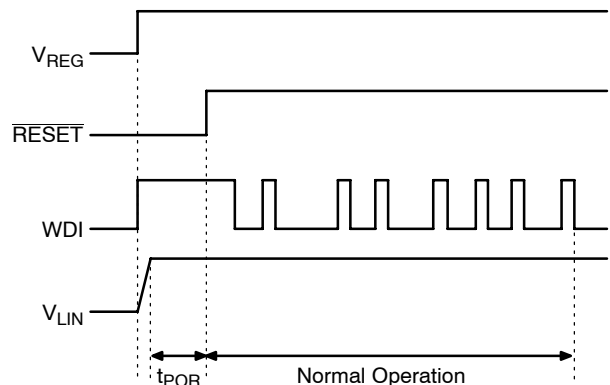


Figure 7. Timing Diagram for Normal Regulator Operation

If a correct watchdog signal is not received within the specified time a reset pulse train is issued until the correct watchdog signal is received. The nominal reset signal in this case is a 5 volt square wave with a 50% duty cycle as shown in Figure 8.

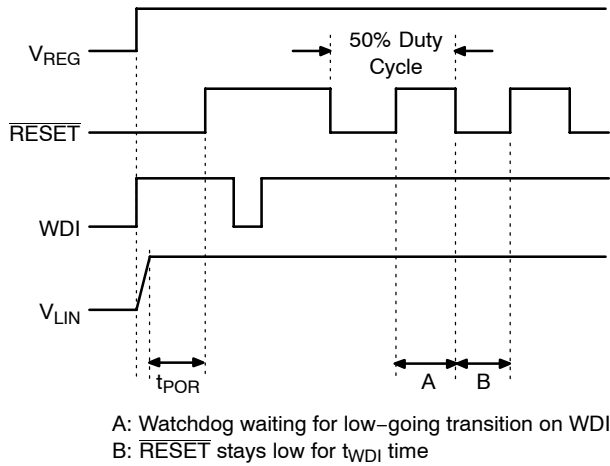


Figure 8. Timing Diagram When WDI Fails to Appear Within the Preset Time Interval, t_{WDI}

The $\overline{\text{RESET}}$ signal frequency is given by:

$$f_{\text{RESET}} = \frac{1}{2(t_{WDI})}$$

The Power On Reset (POR) and low voltage $\overline{\text{RESET}}$ use the same circuitry and issue a reset when the linear output voltage is below the regulation limit. After V_{LIN} rises above the minimum specified value, $\overline{\text{RESET}}$ remains low for a fixed period t_{POR} as shown in Figures 9 and 10.

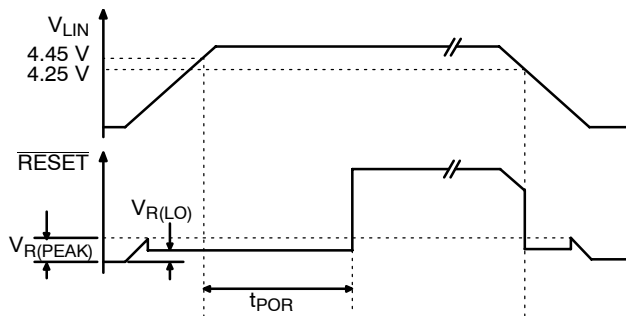


Figure 9. The Power On Reset Time Interval (t_{POR}) Begins When V_{LIN} Rises Above 4.45 V (Typical)

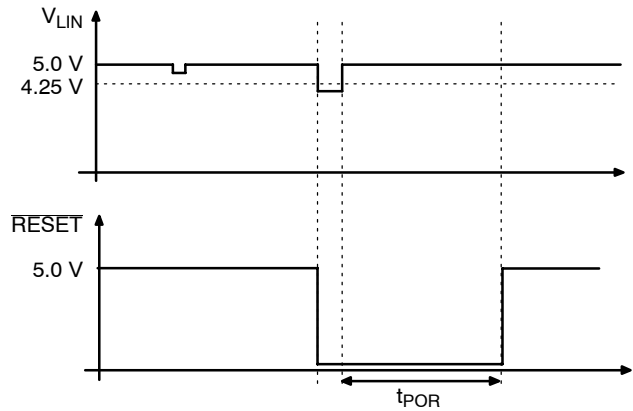


Figure 10. $\overline{\text{RESET}}$ Signal Is Issued Whenever V_{LIN} Falls Below 4.25 V (Typical)

The POR delay (t_{POR}) is given by:

$$t_{POR} = 1.353 \times C_{\text{Delay}} R_{\text{BIAS}}$$

CURRENT MODE PWM SWITCHING CIRCUITRY

The current mode PWM switching voltage regulator contains an error amplifier with selectable feedback inputs, a current sense amplifier, an adjustable oscillator and a 1.4 A output power switch with antisaturation control. The switching regulator and external components, connected in a boost configuration, are shown in Figure 11.

The switching regulator begins operation when V_{REG} and V_{IN} are raised above 5 volts. V_{REG} is required since the switching supply's control circuitry is powered through V_{LIN} . V_{IN} supplies the base drive to the switcher output transistor.

The output transistor turns on when the oscillator starts to charge the capacitor on C_{OSC} . The output current will develop a voltage drop across the internal sense resistor (R_S). This voltage drop produces a proportional voltage at the output of the current sense amplifier, which is compared to the output of the error amplifier. The error amplifier generates an output voltage which is proportional to the difference between the scaled down output boost voltage (V_{FB1} or V_{FB2}) and the internal bandgap voltage reference. Once the current sense amplifier output exceeds the error amplifier's output voltage, the output transistor is turned off.

The energy stored in the inductor during the output transistor on time is transferred to the load when the output transistor is turned off. The output transistor is turned back

on at the next rising edge of the oscillator. On a cycle by cycle basis, the current mode controller in a discontinuous mode of operation charges the inductor to the appropriate amount of energy, based on the energy demand of the load. Figure 12 shows the typical current and voltage waveforms for a boost supply operating in the discontinuous mode.

Notes:

1. Refer to Figure 5 to determine oscillator frequency.

2. The switching regulator can be disabled by providing a logic high at the $\overline{\text{ENABLE}}$ input.
3. The boost output voltage can be controlled dynamically by the feedback select input. If select is open, V_{FB2} is selected. If select is low, then V_{FB1} is selected.

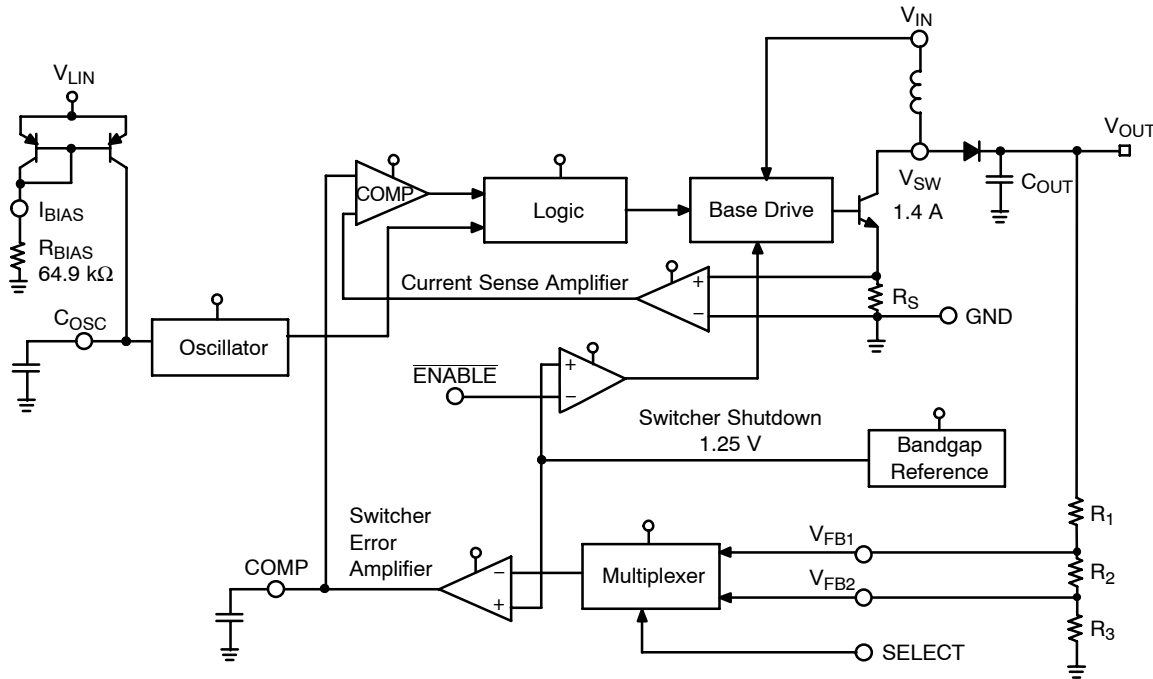


Figure 11. Block Diagram of the 1.4 A Current Mode Control Switching Regulator Portion of the CS5112 in a Boost Configuration

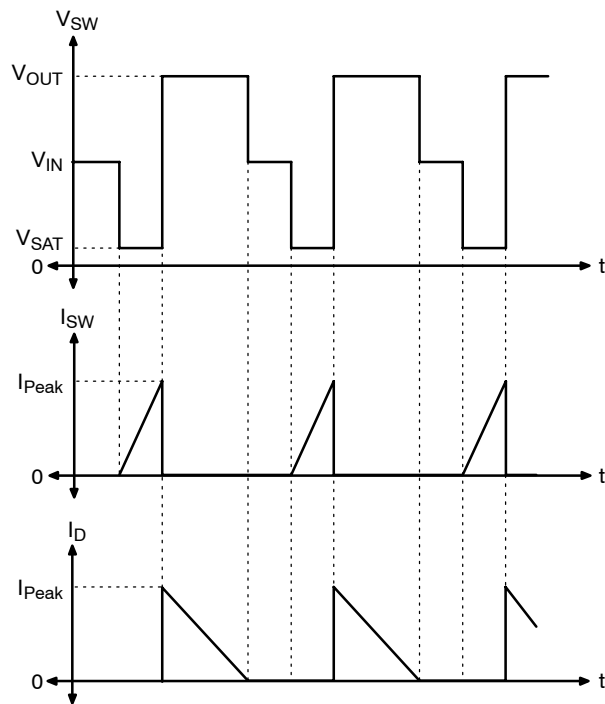


**Figure 12. Voltage and Current Waveforms
for Boost Topology in CS5112**

PROTECTION CIRCUITRY

The current out of V_{LIN} is sensed in order to limit excessive power dissipation in the linear output transistor over the output range of 0 V to regulation. Also, the current into V_{SW} is sensed in order to provide the current limit function in the switcher output transistor.

If the die temperature is increased above 160°C, either due to excessive ambient temperature or excessive power dissipation, the drive to the linear output transistor is reduced proportionally with increasing die temperature. Therefore, V_{LIN} will decrease with increasing die temperature above 160°C. Since the switcher control circuitry is powered through V_{LIN} , the switcher performance, including current limit, will be affected by the decrease in V_{LIN} .

APPLICATION NOTES

DESIGN PROCEDURE FOR BOOST TOPOLOGY

This section outlines a procedure for designing a boost switching power supply operating in the discontinuous mode.

Step 1

Determine the output power required by the load.

$$P_{OUT} = I_{OUT}V_{OUT} \quad (1)$$

Step 2

Choose C_{OSC} based on the target oscillator frequency with an external resistor value, $R_{BIAS} = 64.9 \text{ k}\Omega$ (See Figure 5).

Step 3

Next select the output voltage feedback sense resistor divider as follows (Figure 13).

For V_{FB1} active, choose a value for R_1 and then solve for R_{EQ} where:

$$R_{EQ} = \frac{R_1}{\frac{V_{OUT}}{V_{FB1}} - 1} \quad (2)$$

For V_{FB2} active, find:

$$V_{FB1} = V_{OUT} \left(\frac{R_{EQ}}{R_1 + R_{EQ}} \right) \quad (3)$$

and then calculate R_2 where:

$$R_2 = \frac{V_{R2}}{I_{R2}} = \frac{V_{FB1} - V_{FB2}}{V_{FB1}/R_{EQ}} \quad (4)$$

Then find R_3 , where:

$$R_3 = R_{EQ} - R_2 \quad (5)$$

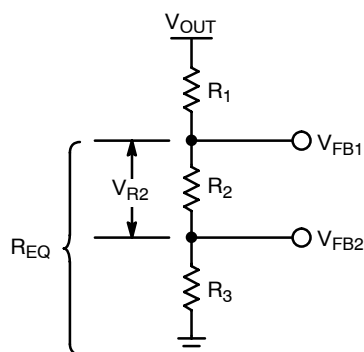


Figure 13. Feedback Sense Resistor Divider Connected Between V_{OUT} and Ground

Step 4

Determine the maximum on time at the minimum oscillator frequency and V_{IN} . For discontinuous operation, all of the stored energy in the inductor is transferred to the load prior to the next cycle. Since the current through the inductor cannot change instantaneously and the inductance is constant, a volt-second balance exists between the on time and off time. The voltage across the inductor during the on cycle is V_{IN} and the voltage across the inductor during the off cycle is $V_{OUT} - V_{IN}$. Therefore:

$$V_{IN}t_{ON} = (V_{OUT} - V_{IN})t_{OFF} \quad (6)$$

where the maximum on time is:

$$t_{ON(MAX)} \approx \left[1 - \frac{V_{IN(MIN)}}{V_{OUT(MAX)}} \right] \left[\frac{1}{f_{SW(MIN)}} \right] \quad (7)$$

Step 5

Calculate the maximum inductance allowed for discontinuous operation:

$$L_{(MAX)} = \frac{f_{SW(MIN)} V_{IN}^2(MIN) t_{ON}^2(MAX)}{2P_{OUT}/\eta} \quad (8)$$

where η = efficiency.

Usually $\eta = 0.75$ is a good starting point. The IC's power dissipation should be calculated after the peak current has been determined in Step 6. If the efficiency is less than originally assumed, decrease the efficiency and recalculate the maximum inductance and peak current.

Step 6

Determine the peak inductor current at the minimum inductance, minimum V_{IN} and maximum on time to make sure the inductor current doesn't exceed 1.4 A.

$$I_{PK} = \frac{V_{IN(MIN)} t_{ON(MAX)}}{L(MIN)} \quad (9)$$

Step 7

Determine the minimum output capacitance and maximum ESR based on the allowable output voltage ripple.

$$C_{OUT(MIN)} = \frac{I_{PK}}{8f\Delta V_{RIPPLE}} \quad (10)$$

$$ESR(MIN) = \frac{\Delta V_{RIPPLE}}{I_{PK}} \quad (11)$$

In practice, it is normally necessary to use a larger capacitance value to obtain a low ESR. By placing capacitors in parallel, the equivalent ESR can be reduced.

Step 8

Compensate the feedback loop to guarantee stability under all operating conditions. To do this, we calculate the modulator gain and the feedback resistor network attenuation and set the gain of the error amplifier so that the overall loop gain is 0 dB at the crossover frequency, f_{CO} . In addition, the gain slope should be -20 dB/decade at the crossover frequency.

The low frequency gain of the modulator (i.e. error amplifier output to output voltage) is:

$$\frac{\Delta V_{OUT}}{\Delta V_{EA}} = \frac{I_{PK(MAX)}}{V_{EA(MAX)}} \sqrt{\frac{R_{LOAD} L f}{2}} \quad (12)$$

where:

$$I_{PK(MAX)} = \frac{V_{EA(MAX)}/G_{CSA}}{R_S} = \frac{2.4 \text{ V}/7}{150 \text{ m}\Omega} = 2.3 \text{ A} \quad (13)$$

The V_{OUT}/V_{EA} transfer function has a pole at:

$$f_p = 1/(\pi R_{LOAD} C_{OUT}) \quad (14)$$

and a zero due to the output capacitor's ESR at:

$$f_z = 1/(2\pi ESR(C_{OUT})) \quad (15)$$

Since the error amplifier reference voltage is 1.25 V, the output voltage must be divided down or attenuated before being applied to the input of the error amplifier. The feedback resistor divider attenuation is:

$$\frac{1.25 V}{V_{OUT}}$$

The error amplifier in the CS5112 is an operational transconductance amplifier (OTA), with a gain given by:

$$G_{OTA} = g_m Z_{OUT} \quad (16)$$

where:

$$g_m = \frac{\Delta I_{OUT}}{\Delta V_{IN}} \quad (17)$$

For the CS5112, $g_m = 2700 \mu A/V$ typical.

One possible error amplifier compensation scheme is shown in Figure 14. This gives the error amplifier a gain plot as shown in Figure 15.

For the error amplifier gain shown in Figure 15, a low frequency pole is generated by the error amplifier output impedance and C_1 . This is shown by the line AB with a -20 dB/decade slope in Figure 15. The slope changes to zero at point B due to the zero at:

$$f_z = 1/(2\pi R_4 C_1) \quad (18)$$

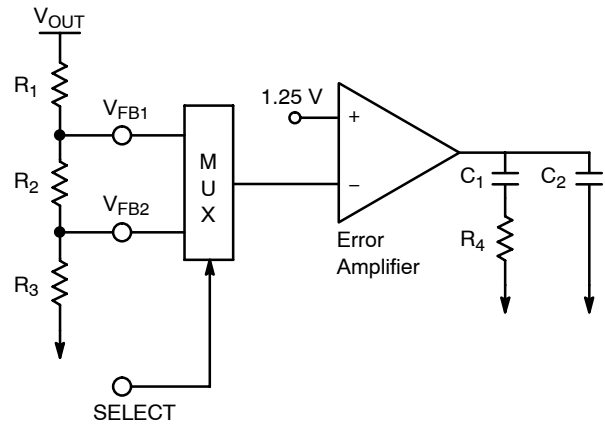


Figure 14. RC Network Used to Compensate the Error Amplifier (OTA)

A pole at point C:

$$f_p = 1/(\pi R_4 C_2) \quad (19)$$

offsets the zero set by the ESR of the output capacitors.

An alternative scheme uses a single capacitor as shown in Figure 16, to roll the gain off at a relatively low frequency.

Step 9

Finally the watchdog timer period and Power on Reset time is determined by:

$$t_{Delay} = 1.353 \times C_{Delay} R_{BIAS} \quad (20)$$

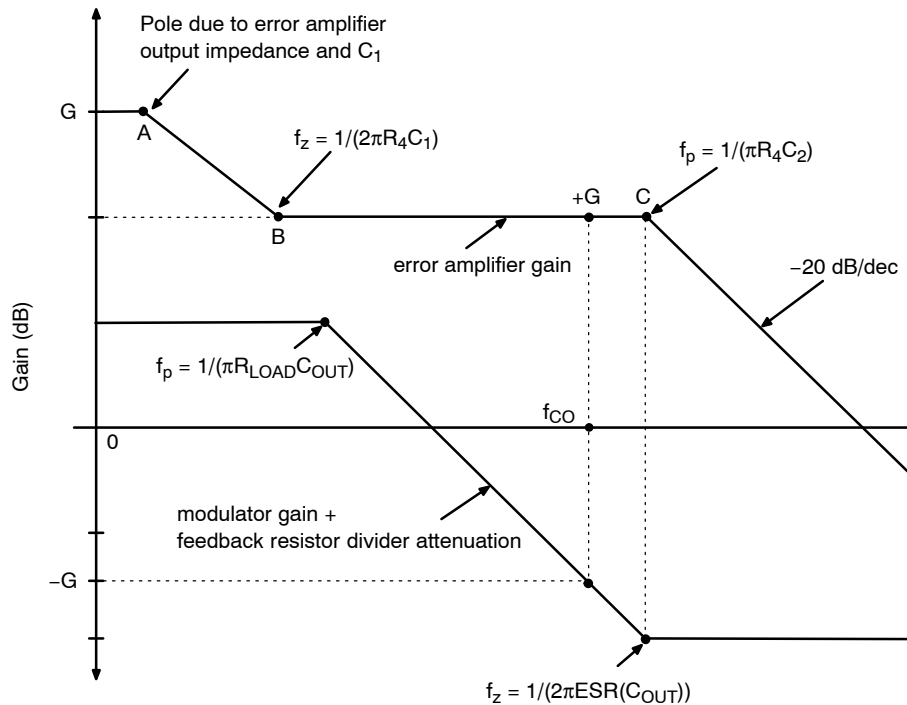


Figure 15. Bode Plot of Error Amplifier (OTA) Gain and Modulator Gain Added to the Feedback Resistor Divider Attenuation

CS5112

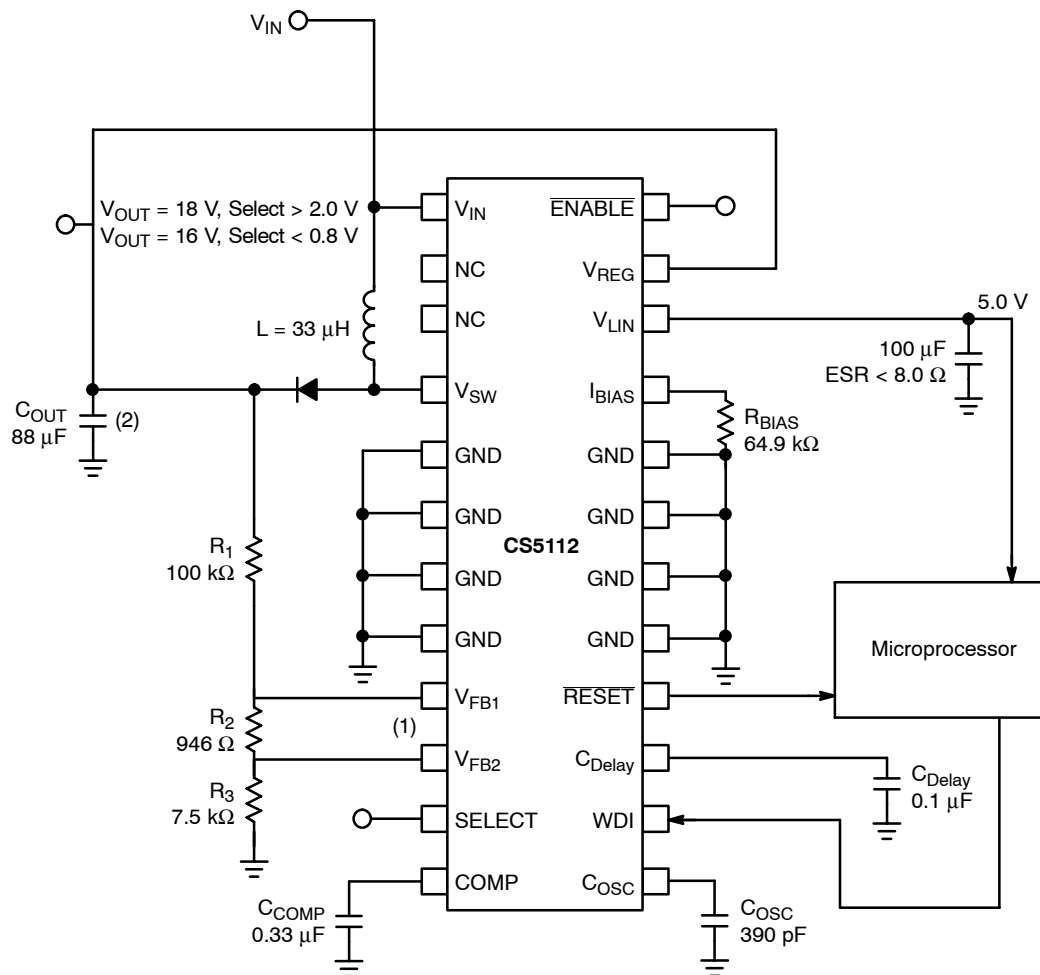


Figure 16. A Typical Application Diagram with External Components Configured in a Boost Topology

LINEAR REGULATOR OUTPUT CURRENT VS. INPUT VOLTAGE

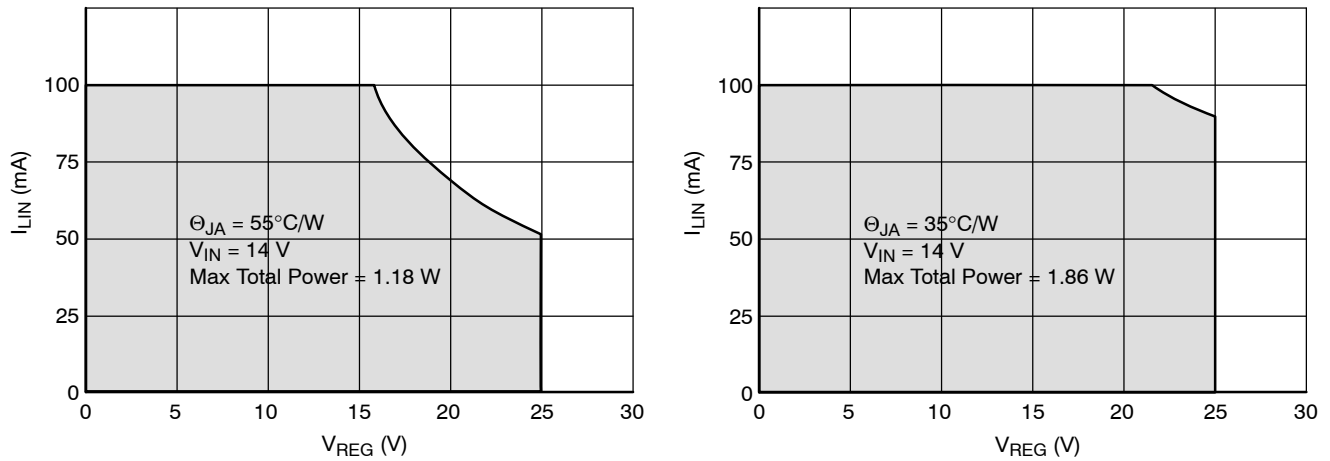


Figure 17. The Shaded Area Shows the Safe Operating Area of the CS5112 as a Function of I_{LIN} , V_{REG} , and Θ_{JA} . Refer to Table 5 for Typical Loads and Voltages.

Table 5.

V_{REG} (V)	V_{IN} (V)	I_{LIN} (mA)	Linear Power Dissipation (W)	Worst Case Switcher Power Available ($\Theta_{JA} = 55^{\circ}\text{C/W}$) (W)	Worst Case Switcher Power Available ($\Theta_{JA} = 35^{\circ}\text{C/W}$) (W)
20	14	25	0.44	0.74	1.42
20	14	50	0.83	0.35	1.03
20	14	75	1.22	*	0.64
20	14	100	1.60	*	0.26
25	14	25	0.60	0.58	1.26
25	14	50	1.11	0.07	0.75
25	14	75	1.62	*	0.24
25	14	100	2.14	*	*

*Subjecting the CS5112 to these conditions will exceed the maximum total power that the part can handle, thereby forcing it into thermal limit.

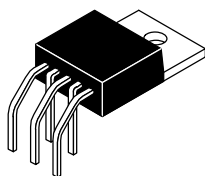
PACKAGE THERMAL DATA

Parameter		SO-24L	Unit
$R_{\theta JC}$	Typical	9	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Typical	55	$^{\circ}\text{C/W}$

CHAPTER 3

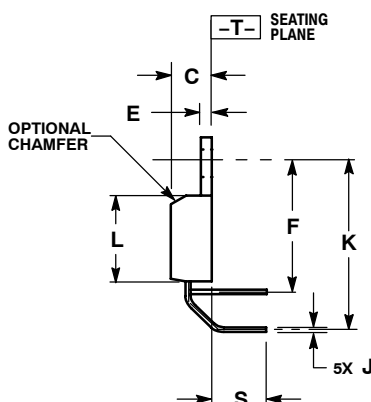
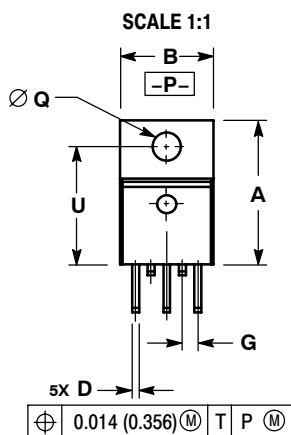
Case Outlines and Package Dimensions

CASE OUTLINES AND PACKAGE DIMENSIONS



**5 LEAD TO-220 (THA5)
CASE 314A-03
ISSUE E**

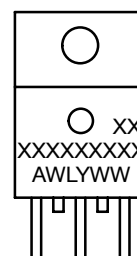
DATE 09/29/2000

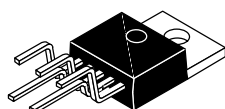


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 0.043 (1.092) MAXIMUM.

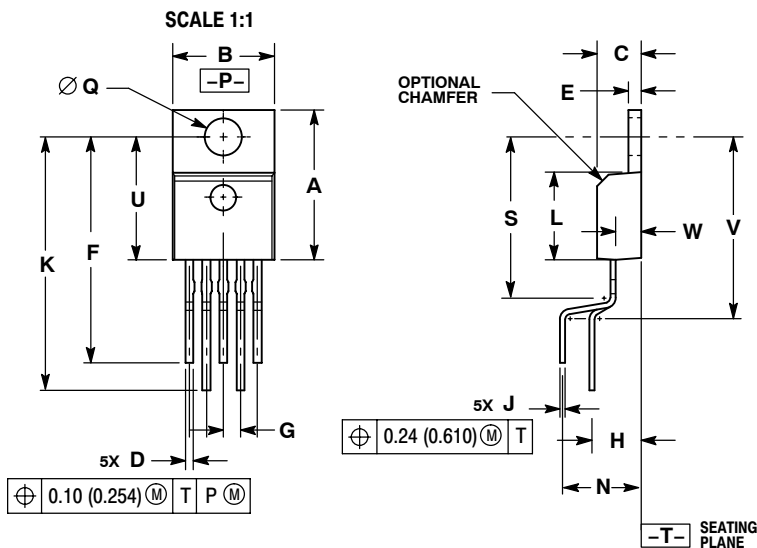
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
F	0.570	0.585	14.478	14.859
G	0.067 BSC		1.702 BSC	
J	0.015	0.025	0.381	0.635
K	0.730	0.745	18.542	18.923
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
S	0.210	0.260	5.334	6.604
II	0.468	0.505	11.888	12.827





CASE 314B-05 ISSUE L

DATE 01/07/1994

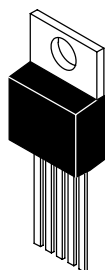


STYLE 1 THRU 4:
CANCELLED

STYLE 5:
PIN 1. GATE
2. MIRROR
3. DRAIN
4. KELVIN
5. SOURCE

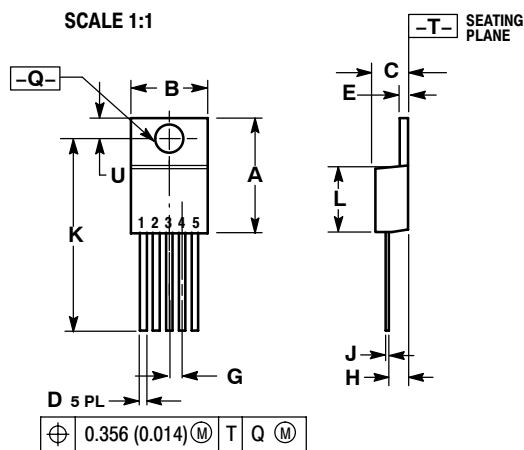
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 0.043 (1.092) MAXIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
F	0.850	0.935	21.590	23.749
G	0.067 BSC		1.702 BSC	
H	0.166 BSC		4.216 BSC	
J	0.015	0.025	0.381	0.635
K	0.900	1.100	22.860	27.940
L	0.320	0.365	8.128	9.271
N	0.320 BSC		8.128 BSC	
Q	0.140	0.153	3.556	3.886
S	---	0.620	---	15.748
U	0.468	0.505	11.888	12.827
V	---	0.735	---	18.669
W	0.090	0.110	2.286	2.794



TO-220 CASE 314D-04 ISSUE E

DATE 07/15/1998



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
G	0.067 BSC		1.702 BSC	
H	0.087	0.112	2.210	2.845
J	0.015	0.025	0.381	0.635
K	0.990	1.045	25.146	26.543
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
U	0.105	0.117	2.667	2.972

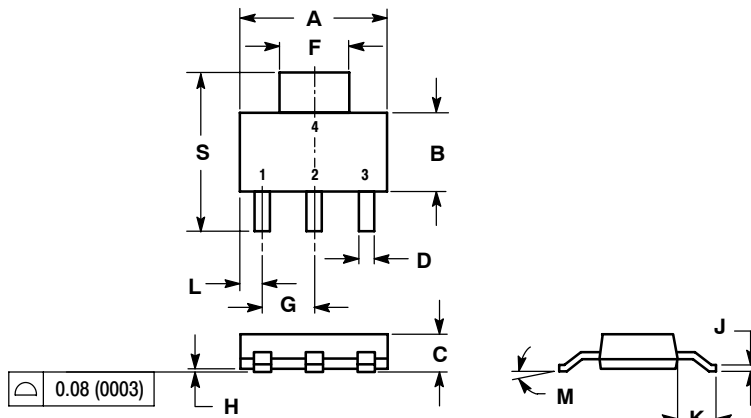
STYLE 1 THRU 4:
PIN 1. CANCELLED



**SOT-223 (TO-261)
CASE 318E-04
ISSUE K**

DATE 01/02/2000

SCALE 1:1



NOTES:

5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 [°]	10 [°]	0 [°]	10 [°]
S	0.264	0.287	6.70	7.30

STYLE 1:

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 2:

- PIN 1. ANODE
- 2. CATHODE
- 3. NC
- 4. CATHODE

STYLE 3:

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

STYLE 4:

- PIN 1. SOURCE
- 2. DRAIN
- 3. GATE
- 4. DRAIN

STYLE 5:

- PIN 1. DRAIN
- 2. GATE
- 3. SOURCE
- 4. GATE

STYLE 6:

- PIN 1. RETURN
- 2. INPUT
- 3. OUTPUT
- 4. INPUT

STYLE 7:

- PIN 1. ANODE 1
- 2. CATHODE
- 3. ANODE 2
- 4. CATHODE

STYLE 8:

CANCELLED

STYLE 9:

- PIN 1. INPUT
- 2. GROUND
- 3. LOGIC
- 4. GROUND

STYLE 10:

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

STYLE 11:

- PIN 1. MT 1
- 2. MT 2
- 3. GATE
- 4. MT 2

STYLE 12:

- PIN 1. INPUT
- 2. OUTPUT
- 3. NC
- 4. OUTPUT

STYLE 13:

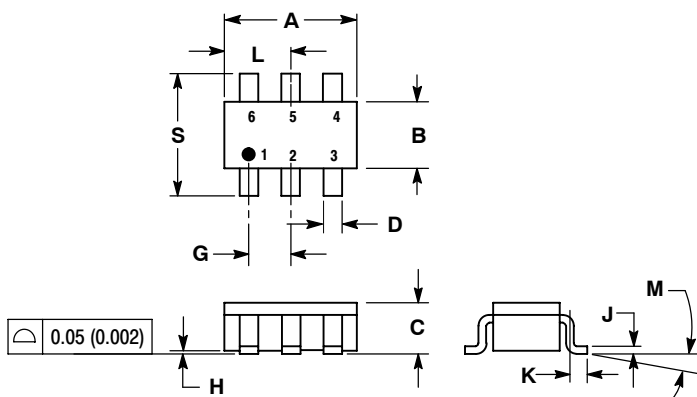
- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR



TSOP-6 CASE 318G-02 ISSUE N

DATE 03 FEB 2005

SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
E	0.85	1.05	0.0335	0.0413
F	0.013	0.100	0.0005	0.0040
G	0.10	0.26	0.0040	0.0102
H	0.20	0.60	0.0079	0.0236
I	1.25	1.55	0.0493	0.0610
J	0°	10°	0°	10°
K	2.50	3.00	0.0985	0.1181

STYLE 1:

- PIN 1. DRAIN
- 2. DRAIN
- 3. GATE
- 4. SOURCE
- 5. DRAIN
- 6. DRAIN

STYLE 2:

- PIN 1. EMITTER 2
- 2. BASE 1
- 3. COLLECTOR 1
- 4. EMITTER 1
- 5. BASE 2
- 6. COLLECTOR 2

STYLE 3:

- PIN 1. ENABLE
- 2. N/C
- 3. R BOOST
- 4. Vz
- 5. V in
- 6. V out

STYLE 4:

- PIN 1. N/C
- 2. V in
- 3. NOT USED
- 4. GROUND
- 5. ENABLE
- 6. LOAD

STYLE 5:

- PIN 1. EMITTER 2
- 2. BASE 2
- 3. COLLECTOR 1
- 4. EMITTER 1
- 5. BASE 1
- 6. COLLECTOR 2

STYLE 6:

- PIN 1. COLLECTOR
- 2. COLLECTOR
- 3. BASE
- 4. EMITTER
- 5. COLLECTOR
- 6. COLLECTOR

STYLE 7:

- PIN 1. COLLECTOR
- 2. COLLECTOR
- 3. BASE
- 4. N/C
- 5. COLLECTOR
- 6. EMITTER

STYLE 8:

- PIN 1. Vbus
- 2. D(in)
- 3. D(in)+
- 4. D(out)+
- 5. D(out)
- 6. GND

STYLE 9:

- PIN 1. LOW VOLTAGE GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN
- 5. DRAIN
- 6. HIGH VOLTAGE GATE

STYLE 10:

- PIN 1. D(OUT)+
- 2. GND
- 3. D(OUT)-
- 4. D(IN)-
- 5. VBUS
- 6. D(IN)+

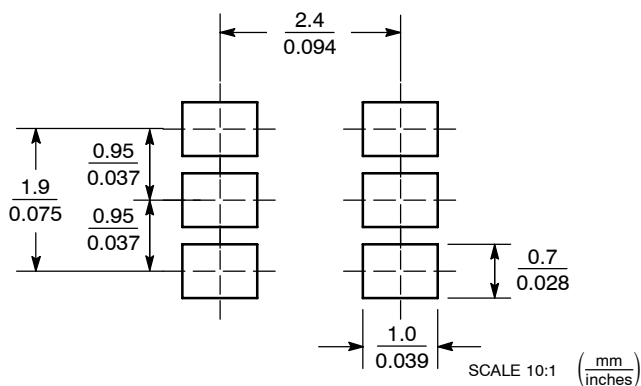
STYLE 11:

- PIN 1. SOURCE 1
- 2. DRAIN 2
- 3. DRAIN 2
- 4. SOURCE 2
- 5. GATE 1
- 6. DRAIN 1/GATE 2

STYLE 12:

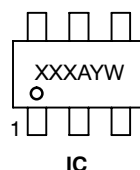
- PIN 1. I/O
- 2. GROUND
- 3. I/O
- 4. I/O
- 5. VCC
- 6. I/O

SOLDERING FOOTPRINT*

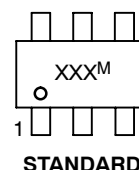


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
■ = Pb-Free Package

XXX = Specific Device Code
M = Date Code
■ = Pb-Free Package

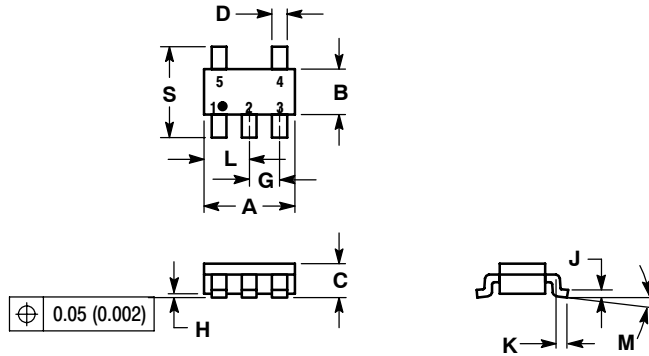
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

TSOP-5
CASE 483-02
ISSUE D

DATE 07 APR 2005



SCALE 2:1

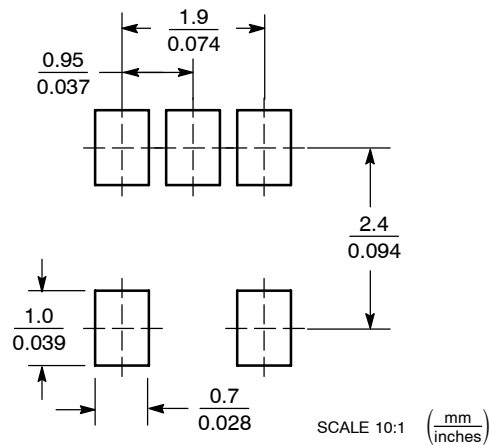


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

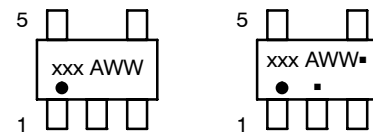
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0°	10°	0°	10°
S	2.50	3.00	0.0985	0.1181

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***



xxx = Specific Device Code
A = Assembly Location
WW = Work Week
▪ = Pb-Free Package (Note: Microdot may be in either location)

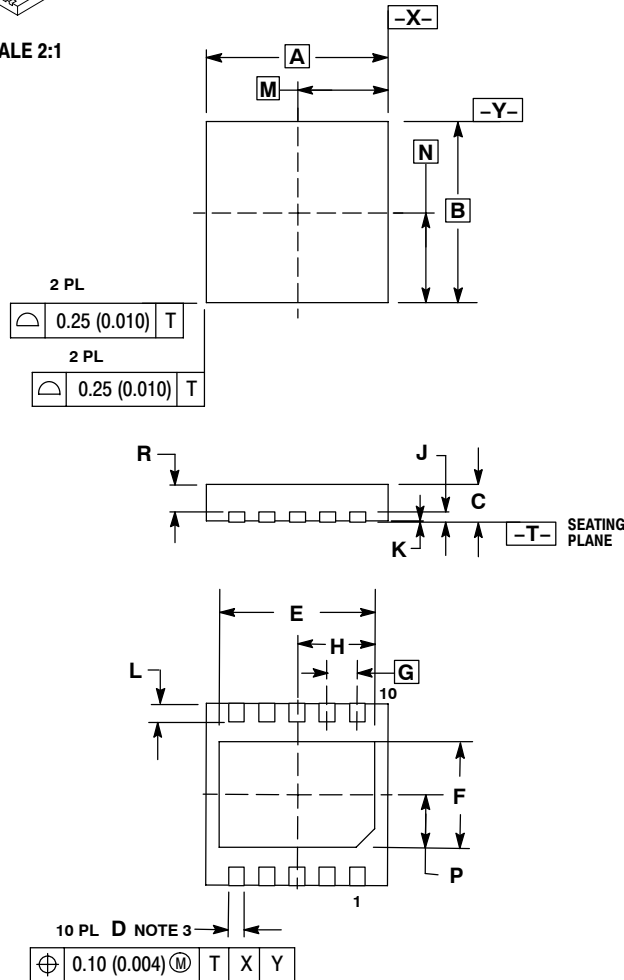
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

10 PIN QFN (DUAL SIDED)
CASE 485C-01
ISSUE O

DATE 08/29/2000



SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.00 BSC		0.118 BSC	
B	3.00 BSC		0.118 BSC	
C	0.80	1.00	0.031	0.039
D	0.20	0.30	0.008	0.012
E	2.45	2.55	0.096	0.100
F	1.75	1.85	0.069	0.073
G	0.50 BSC		0.020 BSC	
H	1.23	1.28	0.048	0.050
J	0.20 REF		0.008 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	1.50 BSC		0.059 BSC	
N	1.50 BSC		0.059 BSC	
P	0.88	0.93	0.035	0.037
R	0.60	0.80	0.024	0.031

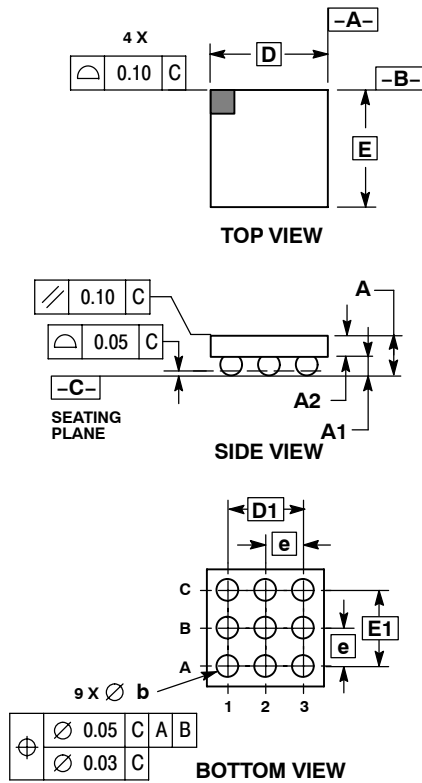


1

SCALE 4:1

9 BUMP, 1.55X1.55X0.5 PITCH
CASE 499AC-01
ISSUE B

DATE 20 JUL 2004

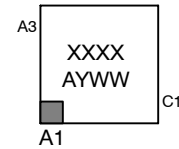


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

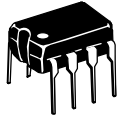
DIM	MILLIMETERS	
	MIN	MAX
A	0.540	0.660
A1	0.210	0.270
A2	0.330	0.390
D	1.550 BSC	
E	1.550 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

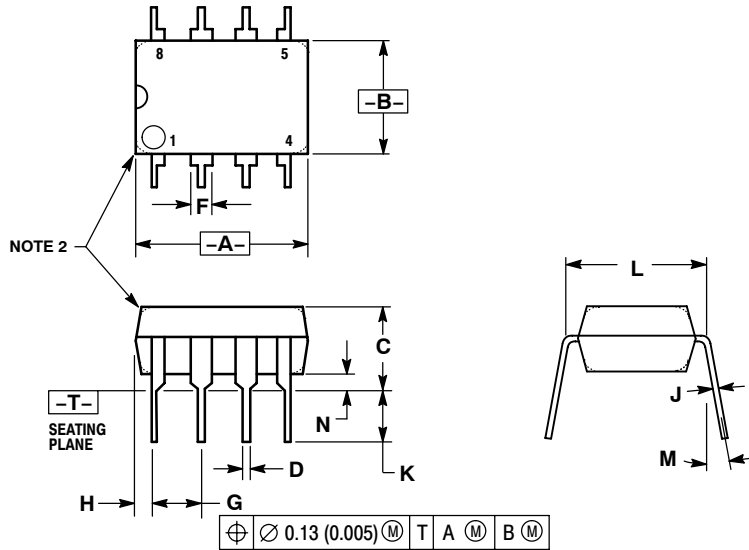
*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.



SCALE 1:1

**8 LEAD PDIP
CASE 626-05
ISSUE L**

DATE 09/29/2000



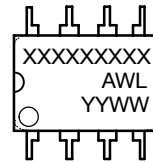
NOTES:

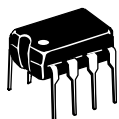
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

STYLE 1:

- PIN 1. AC IN
2. DC + IN
3. DC - IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

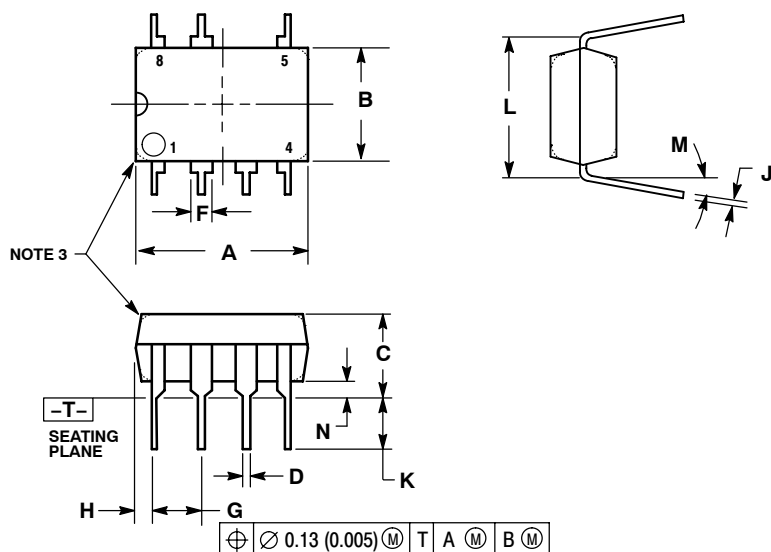




SCALE 1:1

8 LEAD PDIP CASE 626A-01 ISSUE O

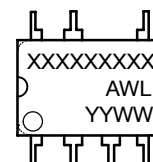
DATE 07/15/2002



- NOTES:
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 5. CONTROLLING DIMENSION: MILLIMETER.
 6. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
 7. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 8. DIMENSIONS A AND B ARE DATUMS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

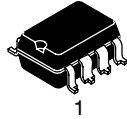
MARKING DIAGRAM



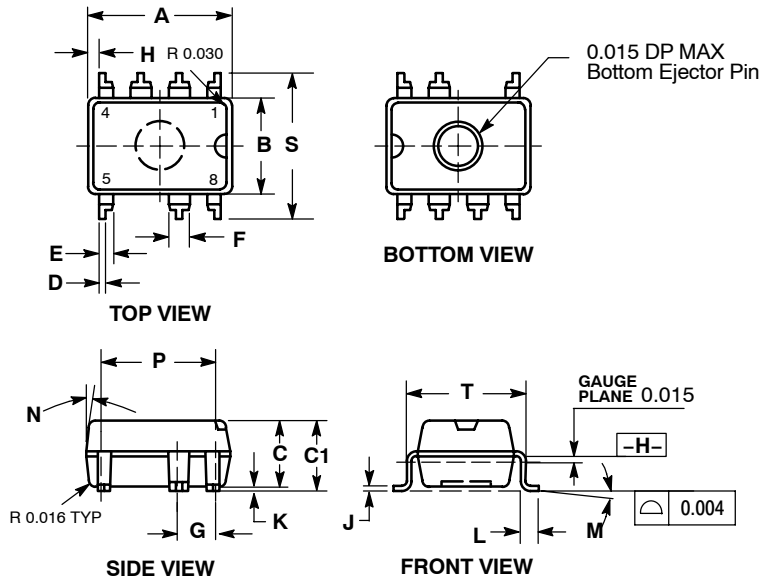
XX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PDIP-7, GULL WING
CASE 626AA-01
ISSUE O

DATE 24 MAY 2004



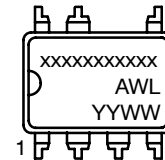
SCALE 1:1



- NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
 2. DIMENSIONS IN INCHES.

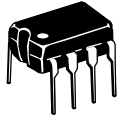
DIM	INCHES	
	MIN	MAX
A	0.365	0.385
B	0.240	0.260
C	0.120	0.150
C1	0.124	0.162
D	0.018 TYP	
E	0.039 TYP	
F	0.045	0.065
G	0.100 BSC	
H	0.023	0.033
J	0.010 TYP	
K	0.004	0.012
L	0.036	0.044
M	0° 8°	
N	12° TYP	
P	0.300 BSC	
S	0.372	0.388

GENERIC MARKING DIAGRAM*



xxxxxxx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

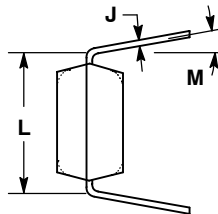
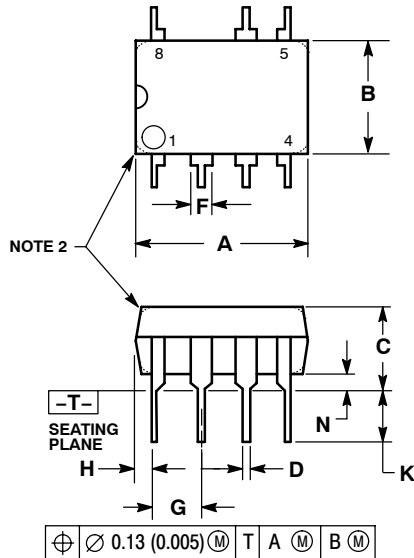
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.



SCALE 1:1

7-LEAD PDIP CASE 626B-01 ISSUE A

DATE 08 JAN 2003



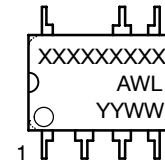
STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC - IN
4. AC IN
5. GROUND
6. OUTPUT
7. NOT USED
8. V_{CC}

NOTES:

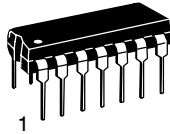
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
5. DIMENSIONS A AND B ARE DATUMS.

MILLIMETERS		
DIM	MIN	MAX
A	9.40	10.16
B	6.10	6.60
C	3.94	4.45
D	0.38	0.51
F	1.02	1.78
G	2.54 BSC	
H	0.76	1.27
J	0.20	0.30
K	2.92	3.43
L	7.62 BSC	
M	---	10 °
N	0.76	1.01

GENERIC MARKING DIAGRAM



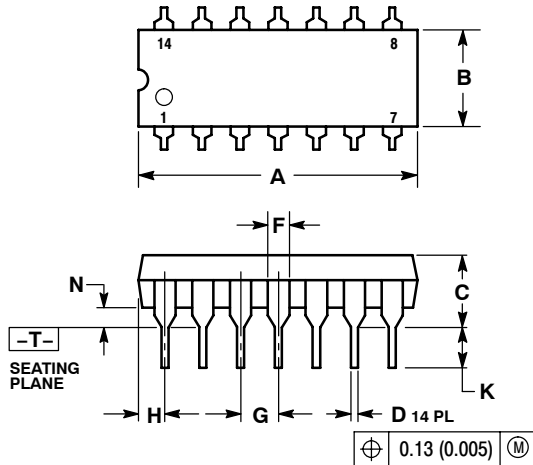
XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week



SCALE 1:1

PDIP-14
CASE 646-06
ISSUE N

DATE 04 MAY 2004

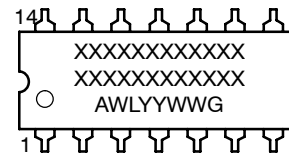


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10 °	---	10 °
N	0.015	0.039	0.38	1.01

**GENERIC
MARKING DIAGRAM***



STYLES ON PAGE 2

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

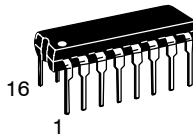
PDIP-14
CASE 646-06
ISSUE N

DATE 04 MAY 2004

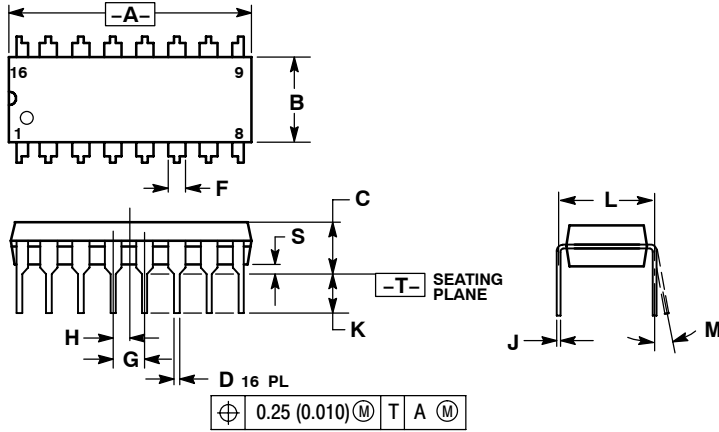
STYLE 1: PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. DRAIN 2. SOURCE 3. GATE 4. NO CONNECTION 5. GATE 6. SOURCE 7. DRAIN 8. DRAIN 9. SOURCE 10. GATE 11. NO CONNECTION 12. GATE 13. SOURCE 14. DRAIN
STYLE 5: PIN 1. GATE 2. DRAIN 3. SOURCE 4. NO CONNECTION 5. SOURCE 6. DRAIN 7. GATE 8. GATE 9. DRAIN 10. SOURCE 11. NO CONNECTION 12. SOURCE 13. DRAIN 14. GATE	STYLE 6: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. NO CONNECTION 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. NO CONNECTION 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 7: PIN 1. NO CONNECTION 2. ANODE 3. ANODE 4. NO CONNECTION 5. ANODE 6. NO CONNECTION 7. ANODE 8. ANODE 9. ANODE 10. NO CONNECTION 11. ANODE 12. ANODE 13. NO CONNECTION 14. COMMON CATHODE	STYLE 8: PIN 1. NO CONNECTION 2. CATHODE 3. CATHODE 4. NO CONNECTION 5. CATHODE 6. NO CONNECTION 7. CATHODE 8. CATHODE 9. CATHODE 10. NO CONNECTION 11. CATHODE 12. CATHODE 13. NO CONNECTION 14. COMMON ANODE
STYLE 9: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. ANODE/CATHODE 7. COMMON ANODE 8. COMMON ANODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. NO CONNECTION 12. ANODE/CATHODE 13. ANODE/CATHODE 14. COMMON CATHODE	STYLE 10: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. NO CONNECTION 7. COMMON ANODE 8. COMMON CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 11: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. ANODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE	STYLE 12: PIN 1. COMMON CATHODE 2. COMMON ANODE 3. ANODE/CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. COMMON ANODE 7. COMMON CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. ANODE/CATHODE 12. ANODE/CATHODE 13. ANODE/CATHODE 14. ANODE/CATHODE

PDIP-16
CASE 648-08
ISSUE T

DATE 04 MAY 2004



SCALE 1:1



STYLE 1:

- PIN 1. CATHODE
- 2. CATHODE
- 3. CATHODE
- 4. CATHODE
- 5. CATHODE
- 6. CATHODE
- 7. CATHODE
- 8. CATHODE
- 9. ANODE
- 10. ANODE
- 11. ANODE
- 12. ANODE
- 13. ANODE
- 14. ANODE
- 15. ANODE
- 16. ANODE

STYLE 2:

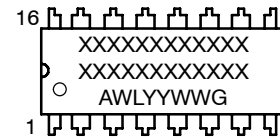
- PIN 1. COMMON DRAIN
- 2. COMMON DRAIN
- 3. COMMON DRAIN
- 4. COMMON DRAIN
- 5. COMMON DRAIN
- 6. COMMON DRAIN
- 7. COMMON DRAIN
- 8. COMMON DRAIN
- 9. GATE
- 10. SOURCE
- 11. GATE
- 12. SOURCE
- 13. GATE
- 14. SOURCE
- 15. GATE
- 16. SOURCE

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

GENERIC
MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

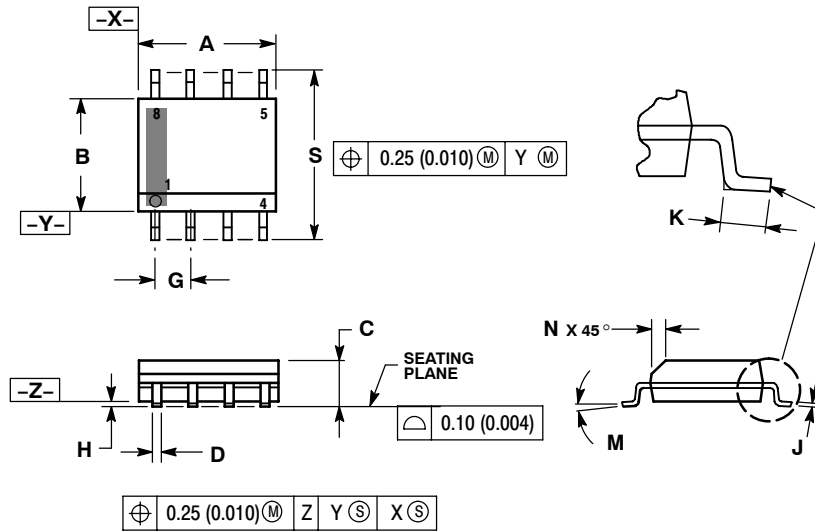
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOIC-8 NB
CASE 751-07
ISSUE AF

DATE 14 APR 2005



SCALE 1:1

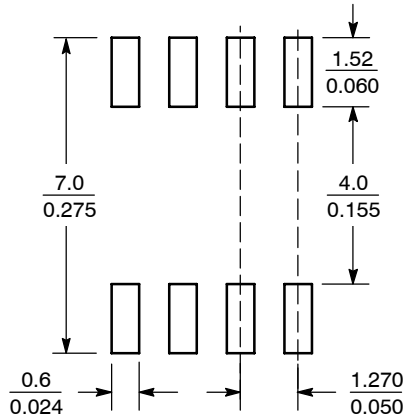


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

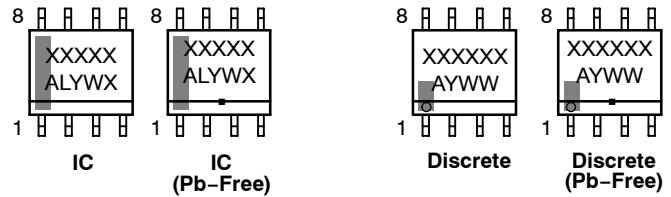
SOLDERING FOOTPRINT*



SCALE 6:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

STYLES ON PAGE 2

SOIC-8 NB
CASE 751-07
ISSUE AF

DATE 14 APR 2005

STYLE 1:

- PIN 1. EMITTER
- 2. COLLECTOR
- 3. COLLECTOR
- 4. EMITTER
- 5. EMITTER
- 6. BASE
- 7. BASE
- 8. EMITTER

STYLE 2:

- PIN 1. COLLECTOR, DIE #1
- 2. COLLECTOR, #1
- 3. COLLECTOR, #2
- 4. COLLECTOR, #2
- 5. BASE, #2
- 6. EMITTER, #2
- 7. BASE, #1
- 8. EMITTER, #1

STYLE 3:

- PIN 1. DRAIN, DIE #1
- 2. DRAIN, #1
- 3. DRAIN, #2
- 4. DRAIN, #2
- 5. GATE, #2
- 6. SOURCE, #2
- 7. GATE, #1
- 8. SOURCE, #1

STYLE 4:

- PIN 1. ANODE
- 2. ANODE
- 3. ANODE
- 4. ANODE
- 5. ANODE
- 6. ANODE
- 7. ANODE
- 8. COMMON CATHODE

STYLE 5:

- PIN 1. DRAIN
- 2. DRAIN
- 3. DRAIN
- 4. DRAIN
- 5. GATE
- 6. GATE
- 7. SOURCE
- 8. SOURCE

STYLE 6:

- PIN 1. SOURCE
- 2. DRAIN
- 3. DRAIN
- 4. SOURCE
- 5. SOURCE
- 6. GATE
- 7. GATE
- 8. SOURCE

STYLE 7:

- PIN 1. INPUT
- 2. EXTERNAL BYPASS
- 3. THIRD STAGE SOURCE
- 4. GROUND
- 5. DRAIN
- 6. GATE 3
- 7. SECOND STAGE Vd
- 8. FIRST STAGE Vd

STYLE 8:

- PIN 1. COLLECTOR, DIE #1
- 2. BASE, #1
- 3. BASE, #2
- 4. COLLECTOR, #2
- 5. COLLECTOR, #2
- 6. EMITTER, #2
- 7. EMITTER, #1
- 8. COLLECTOR, #1

STYLE 9:

- PIN 1. EMITTER, COMMON
- 2. COLLECTOR, DIE #1
- 3. COLLECTOR, DIE #2
- 4. EMITTER, COMMON
- 5. EMITTER, COMMON
- 6. BASE, DIE #2
- 7. BASE, DIE #1
- 8. EMITTER, COMMON

STYLE 10:

- PIN 1. GROUND
- 2. BIAS 1
- 3. OUTPUT
- 4. GROUND
- 5. GROUND
- 6. BIAS 2
- 7. INPUT
- 8. GROUND

STYLE 11:

- PIN 1. SOURCE 1
- 2. GATE 1
- 3. SOURCE 2
- 4. GATE 2
- 5. DRAIN 2
- 6. DRAIN 2
- 7. DRAIN 1
- 8. DRAIN 1

STYLE 12:

- PIN 1. SOURCE
- 2. SOURCE
- 3. SOURCE
- 4. GATE
- 5. DRAIN
- 6. DRAIN
- 7. DRAIN
- 8. DRAIN

STYLE 13:

- PIN 1. N.C.
- 2. SOURCE
- 3. SOURCE
- 4. GATE
- 5. DRAIN
- 6. DRAIN
- 7. DRAIN
- 8. DRAIN

STYLE 14:

- PIN 1. N-SOURCE
- 2. N-GATE
- 3. P-SOURCE
- 4. P-GATE
- 5. P-DRAIN
- 6. P-DRAIN
- 7. N-DRAIN
- 8. N-DRAIN

STYLE 15:

- PIN 1. ANODE 1
- 2. ANODE 1
- 3. ANODE 1
- 4. ANODE 1
- 5. CATHODE, COMMON
- 6. CATHODE, COMMON
- 7. CATHODE, COMMON
- 8. CATHODE, COMMON

STYLE 16:

- PIN 1. EMITTER, DIE #1
- 2. BASE, DIE #1
- 3. EMITTER, DIE #2
- 4. BASE, DIE #2
- 5. COLLECTOR, DIE #2
- 6. COLLECTOR, DIE #2
- 7. COLLECTOR, DIE #1
- 8. COLLECTOR, DIE #1

STYLE 17:

- PIN 1. VCC
- 2. V2OUT
- 3. V1OUT
- 4. TXE
- 5. RXE
- 6. VEE
- 7. GND
- 8. ACC

STYLE 18:

- PIN 1. ANODE
- 2. ANODE
- 3. SOURCE
- 4. GATE
- 5. DRAIN
- 6. DRAIN
- 7. CATHODE
- 8. CATHODE

STYLE 19:

- PIN 1. SOURCE 1
- 2. GATE 1
- 3. SOURCE 2
- 4. GATE 2
- 5. DRAIN 2
- 6. MIRROR 2
- 7. DRAIN 1
- 8. MIRROR 1

STYLE 20:

- PIN 1. SOURCE (N)
- 2. GATE (N)
- 3. SOURCE (P)
- 4. GATE (P)
- 5. DRAIN
- 6. DRAIN
- 7. DRAIN
- 8. DRAIN

STYLE 21:

- PIN 1. CATHODE 1
- 2. CATHODE 2
- 3. CATHODE 3
- 4. CATHODE 4
- 5. CATHODE 5
- 6. COMMON ANODE
- 7. COMMON ANODE
- 8. CATHODE 6

STYLE 22:

- PIN 1. I/O LINE 1
- 2. COMMON CATHODE/VCC
- 3. COMMON CATHODE/VCC
- 4. I/O LINE 3
- 5. COMMON ANODE/GND
- 6. I/O LINE 4
- 7. I/O LINE 5
- 8. COMMON ANODE/GND

STYLE 23:

- PIN 1. LINE 1 IN
- 2. COMMON ANODE/GND
- 3. COMMON ANODE/GND
- 4. LINE 2 IN
- 5. LINE 2 OUT
- 6. COMMON ANODE/GND
- 7. COMMON ANODE/GND
- 8. LINE 1 OUT

STYLE 24:

- PIN 1. BASE
- 2. EMITTER
- 3. COLLECTOR/ANODE
- 4. COLLECTOR/ANODE
- 5. CATHODE
- 6. CATHODE
- 7. COLLECTOR/ANODE
- 8. COLLECTOR/ANODE

STYLE 25:

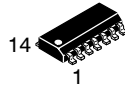
- PIN 1. VIN
- 2. N/C
- 3. REXT
- 4. GND
- 5. IOUT
- 6. IOUT
- 7. IOUT
- 8. IOUT

STYLE 26:

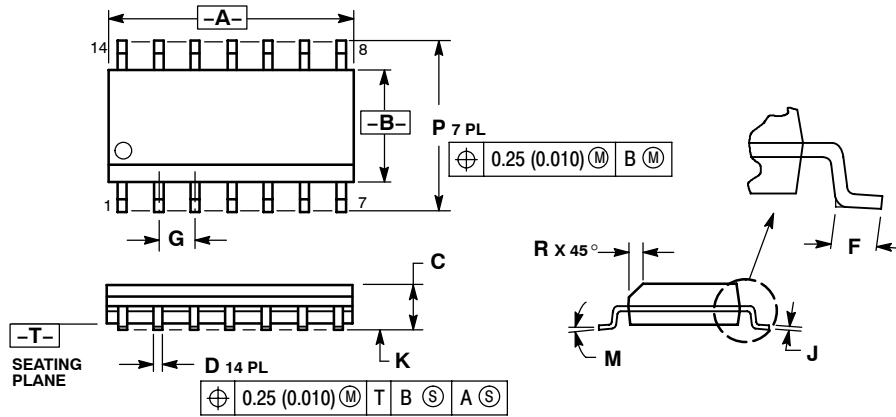
- PIN 1. GND
- 2. dv/dt
- 3. ENABLE
- 4. ILIMIT
- 5. SOURCE
- 6. SOURCE
- 7. SOURCE
- 8. VCC

SOIC-14
CASE 751A-03
ISSUE G

DATE 30 APR 2004



SCALE 1:1

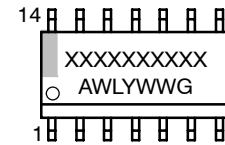


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

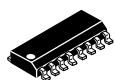
**GENERIC
MARKING DIAGRAM***



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

STYLE 1: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. NO CONNECTION 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. NO CONNECTION 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 2: CANCELLED	STYLE 3: PIN 1. NO CONNECTION 2. ANODE 3. ANODE 4. NO CONNECTION 5. ANODE 6. NO CONNECTION 7. ANODE 8. ANODE 9. ANODE 10. NO CONNECTION 11. ANODE 12. ANODE 13. NO CONNECTION 14. COMMON CATHODE	STYLE 4: PIN 1. NO CONNECTION 2. CATHODE 3. CATHODE 4. NO CONNECTION 5. CATHODE 6. NO CONNECTION 7. CATHODE 8. CATHODE 9. CATHODE 10. NO CONNECTION 11. CATHODE 12. CATHODE 13. NO CONNECTION 14. COMMON ANODE
STYLE 5: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. NO CONNECTION 7. COMMON ANODE 8. COMMON CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. ANODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE	STYLE 7: PIN 1. ANODE/CATHODE 2. COMMON ANODE 3. COMMON CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. ANODE/CATHODE 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. COMMON CATHODE 12. COMMON ANODE 13. ANODE/CATHODE 14. ANODE/CATHODE	STYLE 8: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. ANODE/CATHODE 7. COMMON ANODE 8. COMMON ANODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. NO CONNECTION 12. ANODE/CATHODE 13. ANODE/CATHODE 14. COMMON CATHODE

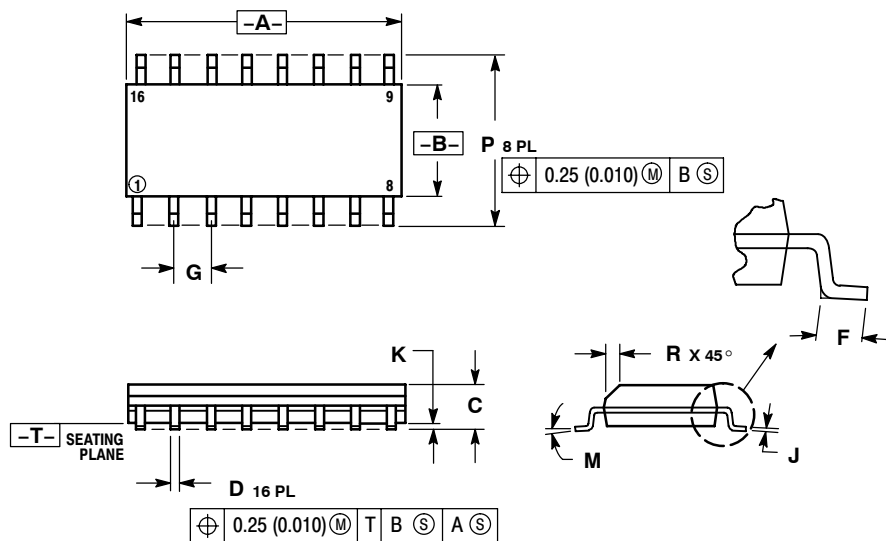
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.



SCALE 1:1

SOIC
CASE 751B-05
ISSUE J

DATE 04/28/1993



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:

- PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:

- PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:

- PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

STYLE 4:

- PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:

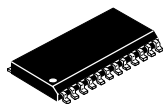
- PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:

- PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:

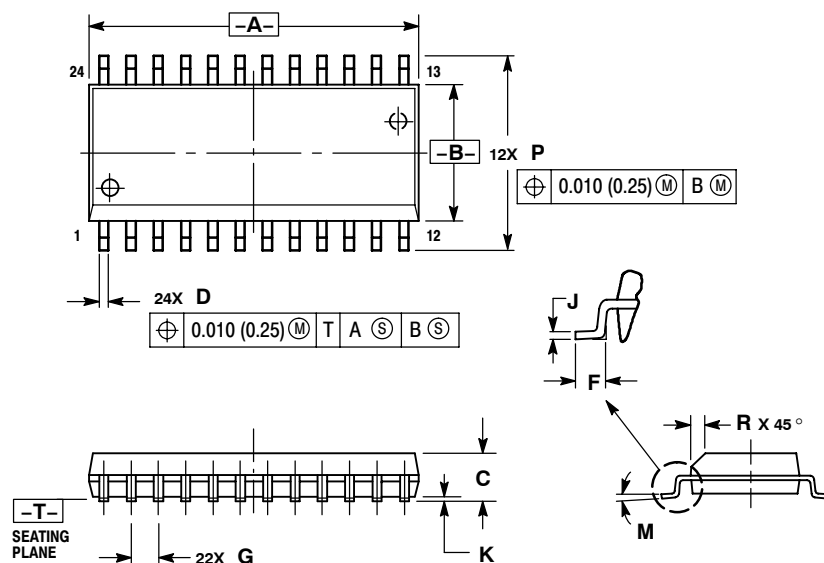
- PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH



SOIC
CASE 751E-04
ISSUE E

DATE 06/18/1993

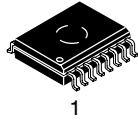
SCALE 1:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

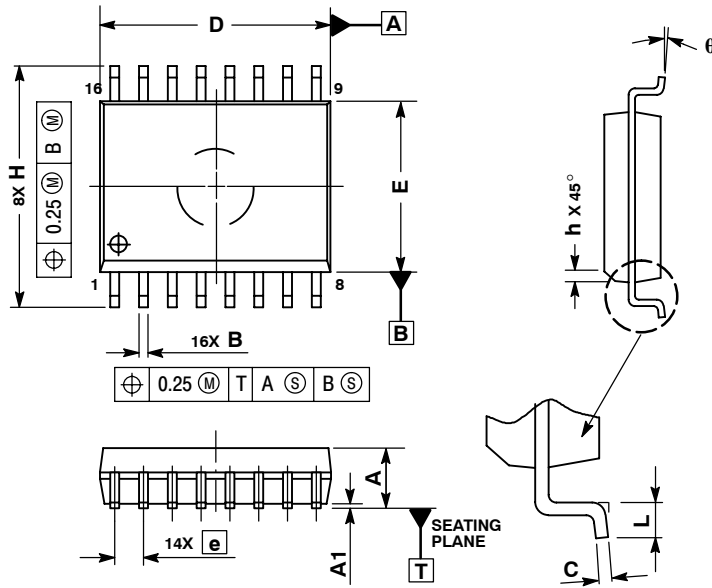
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029



SO-16 WB
CASE 751G-03
ISSUE C

DATE 30 APR 2004

SCALE 1:1

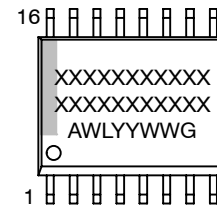


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

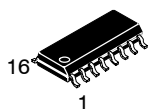
MILLIMETERS		
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27	BSC
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0 °	7 °

**GENERIC
MARKING DIAGRAM***



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

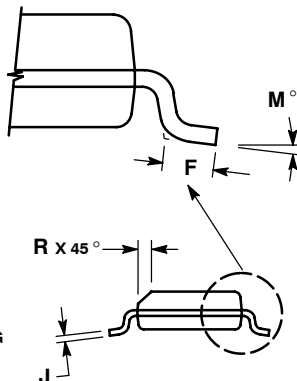
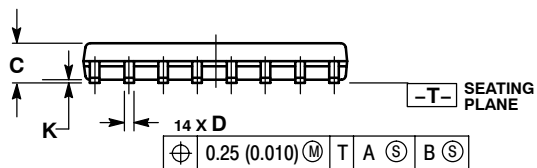
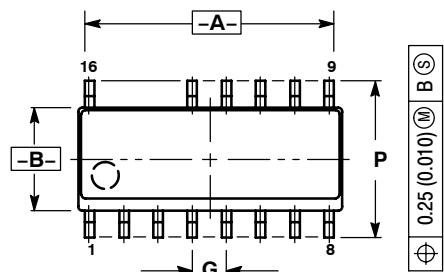
*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.



SCALE 1:1

SO-16 CASE 751K-01 ISSUE O

DATE 12/22/1993

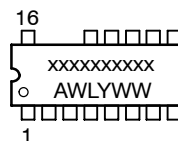


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.368	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

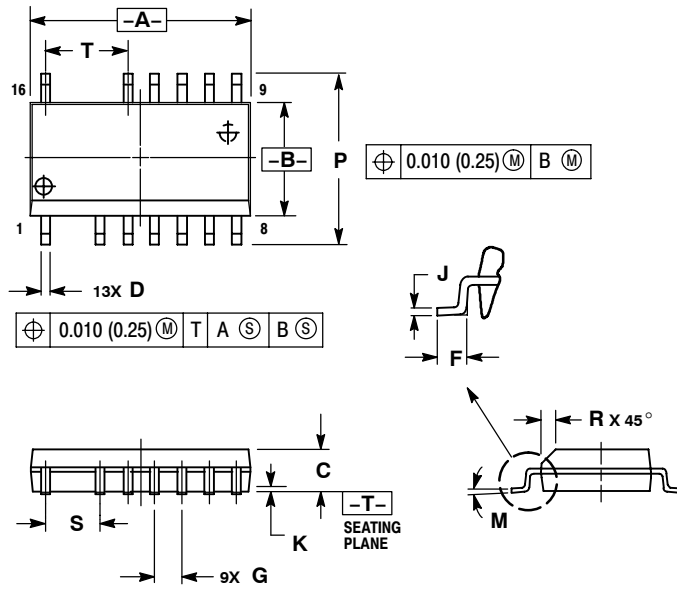
MARKING DIAGRAM



xx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

**CASE 751N-01
ISSUE O**

DATE 02/28/95



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

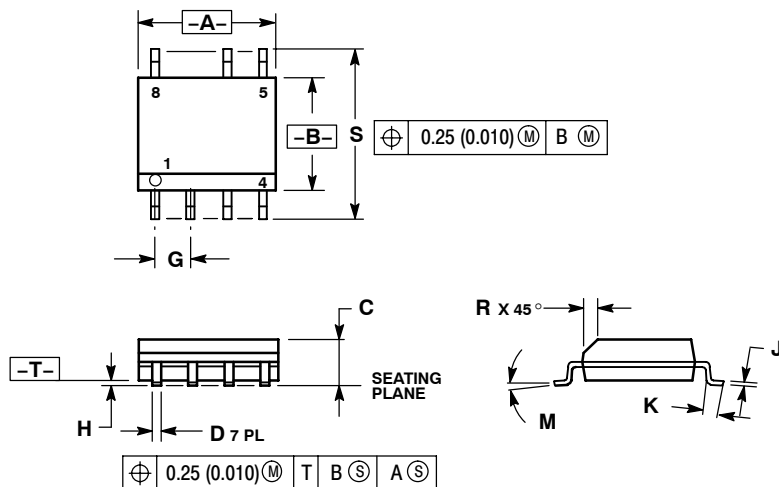
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029
S	2.54 BSC		0.100 BSC	
T	3.81 BSC		0.150 BSC	



SOIC-7
CASE 751U-01
ISSUE C

DATE 03 JAN 2005

SCALE 1:1

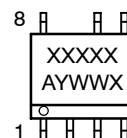


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B ARE DATUMS AND T IS A DATUM SURFACE.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC
MARKING DIAGRAM



XXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLE 1:

- PIN 1. EMITTER
- 2. COLLECTOR
- 3. COLLECTOR
- 4. EMITTER
- 5. EMITTER
- 6.
- 7. NOT USED
- 8. EMITTER

STYLE 2:

- PIN 1. COLLECTOR, DIE #1
- 2. COLLECTOR, #1
- 3. COLLECTOR, #2
- 4. COLLECTOR, #2
- 5. BASE, #2
- 6. EMITTER, #2
- 7. NOT USED
- 8. EMITTER, #1

STYLE 3:

- PIN 1. DRAIN, DIE #1
- 2. DRAIN, #1
- 3. DRAIN, #2
- 4. DRAIN, #2
- 5. GATE, #2
- 6. SOURCE, #2
- 7. NOT USED
- 8. SOURCE, #1

STYLE 4:

- PIN 1. ANODE
- 2. ANODE
- 3. ANODE
- 4. ANODE
- 5. ANODE
- 6. ANODE
- 7. NOT USED
- 8. COMMON CATHODE

STYLE 5:

- PIN 1. DRAIN
- 2. DRAIN
- 3. DRAIN
- 4. DRAIN
- 5.
- 6.
- 7. NOT USED
- 8. SOURCE

STYLE 6:

- PIN 1. SOURCE
- 2. DRAIN
- 3. DRAIN
- 4. SOURCE
- 5. SOURCE
- 6.
- 7. NOT USED
- 8. SOURCE

STYLE 7:

- PIN 1. INPUT
- 2. EXTERNAL BYPASS
- 3. THIRD STAGE SOURCE
- 4. GROUND
- 5. DRAIN
- 6. GATE 3
- 7. NOT USED
- 8. FIRST STAGE Vd

STYLE 8:

- PIN 1. COLLECTOR (DIE 1)
- 2. BASE (DIE 1)
- 3. BASE (DIE 2)
- 4. COLLECTOR (DIE 2)
- 5. COLLECTOR (DIE 2)
- 6. EMITTER (DIE 2)
- 7. NOT USED
- 8. COLLECTOR (DIE 1)

STYLE 9:

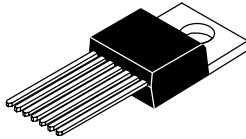
- PIN 1. EMITTER (COMMON)
- 2. COLLECTOR (DIE 1)
- 3. COLLECTOR (DIE 2)
- 4. EMITTER (COMMON)
- 5. EMITTER (COMMON)
- 6. BASE (DIE 2)
- 7. NOT USED
- 8. EMITTER (COMMON)

STYLE 10:

- PIN 1. GROUND
- 2. BIAS 1
- 3. OUTPUT
- 4. GROUND
- 5. GROUND
- 6. BIAS 2
- 7. NOT USED
- 8. GROUND

STYLE 11:

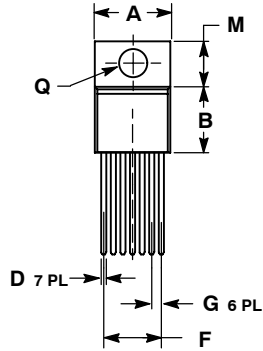
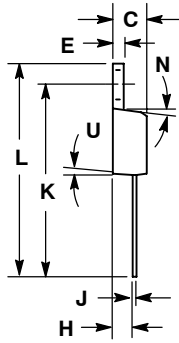
- PIN 1. SOURCE (DIE 1)
- 2. GATE (DIE 1)
- 3. SOURCE (DIE 2)
- 4. GATE (DIE 2)
- 5. DRAIN (DIE 2)
- 6. DRAIN (DIE 2)
- 7. NOT USED
- 8. DRAIN (DIE 1)



SCALE 1:1

**7 LEAD TO-220
CASE 821P-03
ISSUE B**

DATE 10/07/2002



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. 821P-01 AND -02 OBSOLETE. NEW STANDARD IS 821P-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.91	10.54	0.390	0.415
B	8.23	9.40	0.324	0.370
C	4.19	4.83	0.165	0.190
D	0.66	0.81	0.026	0.032
E	0.89	1.40	0.035	0.055
F	7.62 TYP		0.3 TYP	
G	1.22	1.32	0.048	0.052
H	2.16	2.92	0.085	0.115
J	0.30	0.64	0.012	0.025
K	24.00	26.54	0.945	1.045
L	26.67	29.03	1.050	1.143
M	6.10	6.48	0.240	0.255
N	7 °	---	7 °	---
Q	3.53	3.96	0.139	0.156
U	4 °	6 °	4 °	6 °

**MARKING
DIAGRAM**



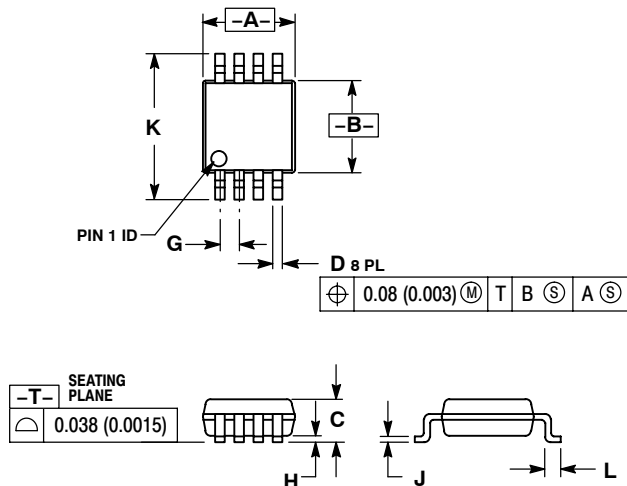
- xx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week



Micro8 CASE 846A-02 ISSUE F

DATE 01/09/2002

SCALE 2:1



STYLE 1:

- PIN 1. SOURCE
- 2. SOURCE
- 3. SOURCE
- 4. GATE
- 5. DRAIN
- 6. DRAIN
- 7. DRAIN
- 8. DRAIN

STYLE 2:

- PIN 1. SOURCE 1
- 2. GATE 1
- 3. SOURCE 2
- 4. GATE 2
- 5. DRAIN 2
- 6. DRAIN 2
- 7. DRAIN 1
- 8. DRAIN 1

STYLE 3:

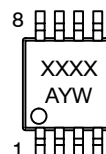
- PIN 1. N-SOURCE
- 2. N-GATE
- 3. P-SOURCE
- 4. P-GATE
- 5. P-DRAIN
- 6. P-DRAIN
- 7. N-DRAIN
- 8. N-DRAIN

NOTES:

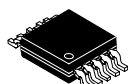
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A-01 OBSOLETE, NEW STANDARD 846A-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

MARKING DIAGRAM



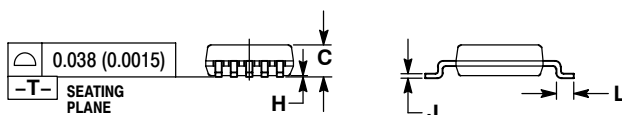
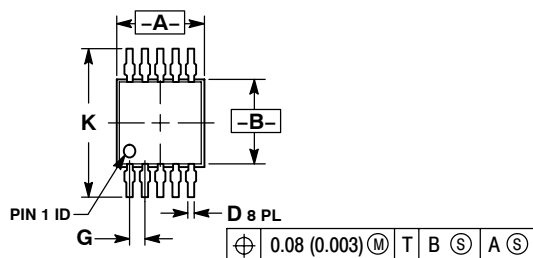
- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week



Micro10 CASE 846B-03 ISSUE D

SCALE 2:1

DATE 07 DEC 2004

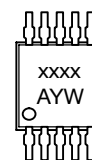


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846B-01 OBSOLETE. NEW STANDARD 846B-02

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.95	1.10	0.037	0.043
D	0.20	0.30	0.008	0.012
G	0.50 BSC		0.020 BSC	
H	0.05	0.15	0.002	0.006
J	0.10	0.21	0.004	0.008
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

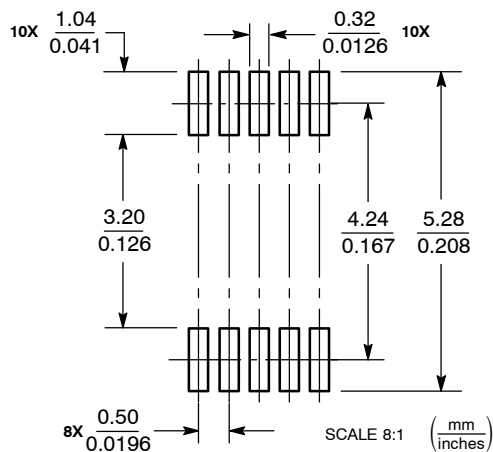
GENERIC MARKING DIAGRAM*



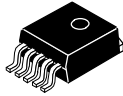
- xxxx = Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT



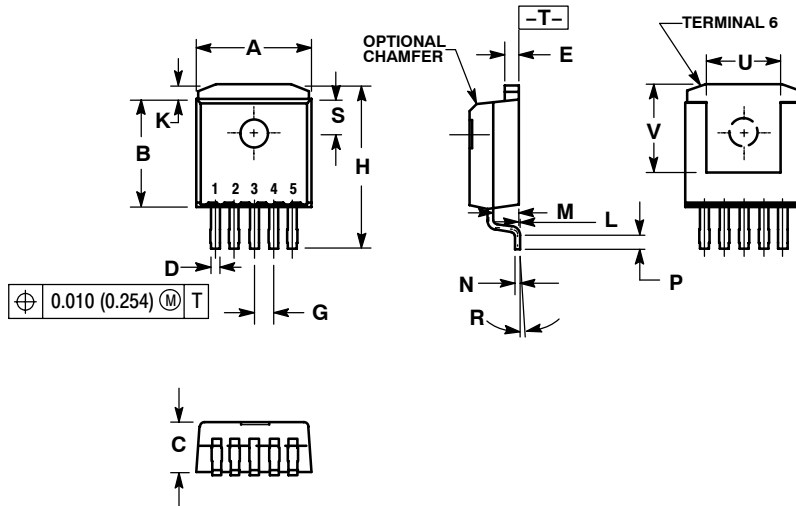
Micro10



SCALE 1:1

D²PAK 5
CASE 936A-02
ISSUE C

DATE 21 SEP 2004

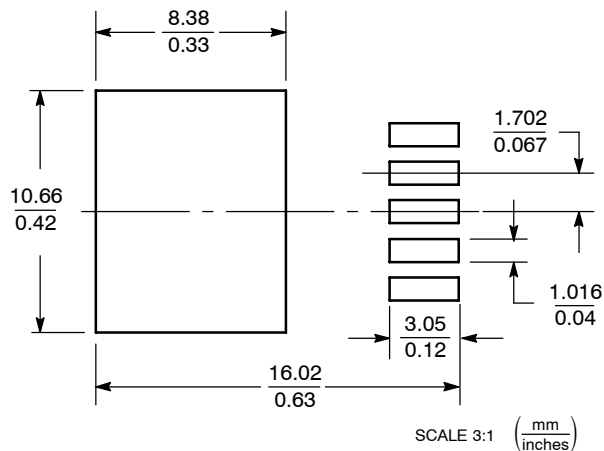


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

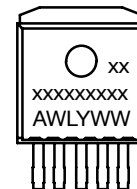
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5° REF		5° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

SOLDERING FOOTPRINT



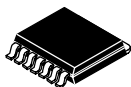
5-LEAD D²PAK

GENERIC MARKING DIAGRAM*



xxxxxx = Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

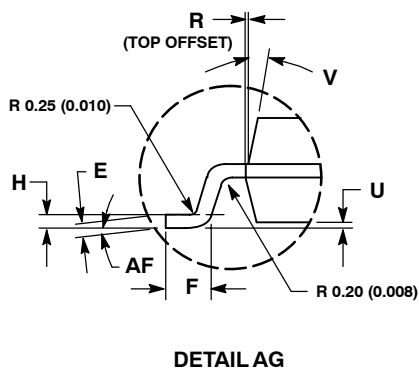
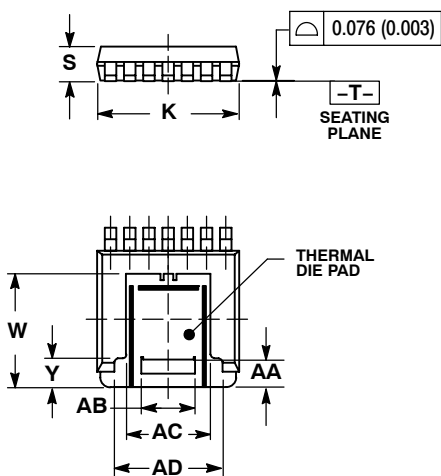
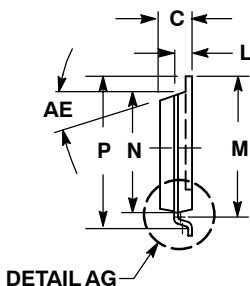
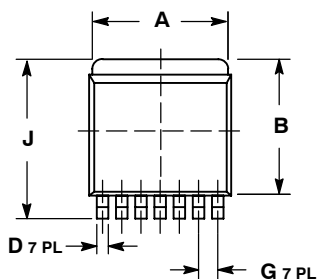
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.



SCALE 1:1

PowerFLEX™, 7 LEAD
CASE 936J-01
ISSUE O

DATE 10/22/2002



NOTES:

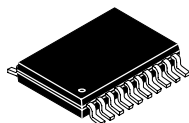
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAX.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.350	0.360	8.89	9.14
B	0.350	0.360	8.89	9.14
C	0.070	0.080	1.78	2.03
D	0.026	0.030	0.66	0.76
E	0.005	0.015	0.13	0.38
F	0.031	0.041	0.79	1.04
G	0.050 BSC		1.270 BSC	
H	0.008	0.012	0.199	0.301
J	0.410	0.420	10.41	10.67
K	0.365	0.375	9.27	9.53
L	0.040 REF		1.02 REF	
M	0.361	0.367	9.16	9.31
N	0.310	0.320	7.87	8.13
P	0.394	0.400	10.00	10.16
R	0.002	---	0.05	---
S	0.070	0.080	1.78	2.03
U	0.001	0.005	0.03	0.13
V	12 °		12 °	
W	0.296 REF		7.52 REF	
Y	0.075 REF		1.91 REF	
AA	0.071 REF		1.81 REF	
AB	0.140 REF		3.56 REF	
AC	0.220 REF		5.58 REF	
AD	0.281 REF		7.14 REF	
AE	12 °		12 °	
AF	3 °	6 °	3 °	6 °

MARKING
DIAGRAM



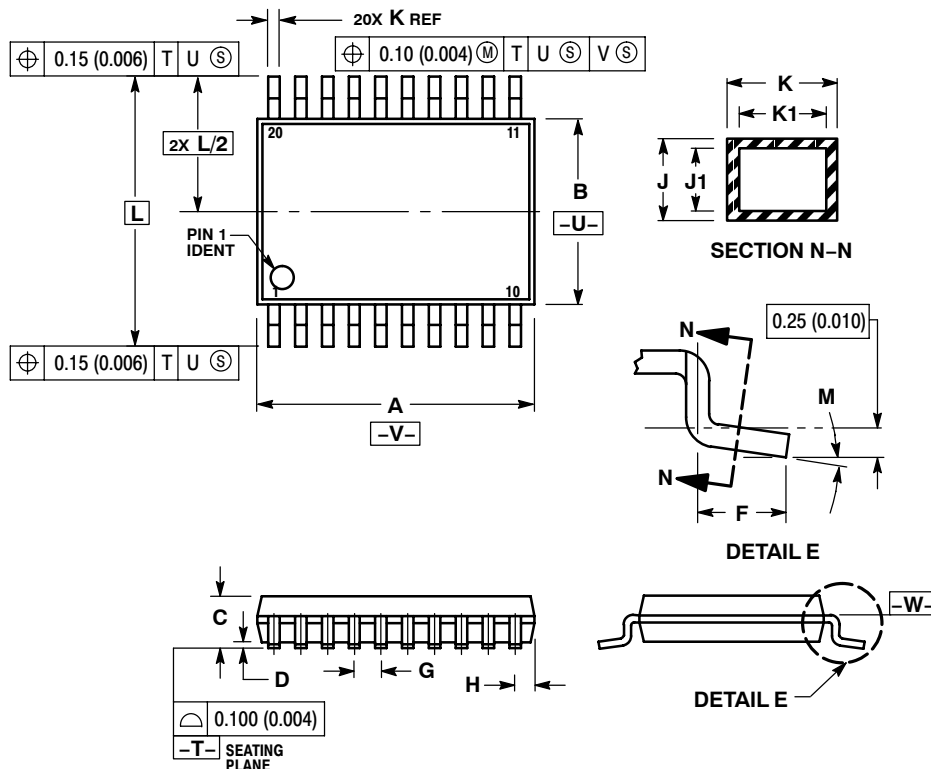
- xx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week



SCALE 2:1

TSSOP-20
CASE 948E-02
ISSUE B

DATE 16 JUN 2003

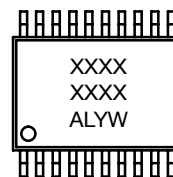


NOTES:

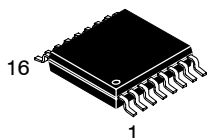
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*



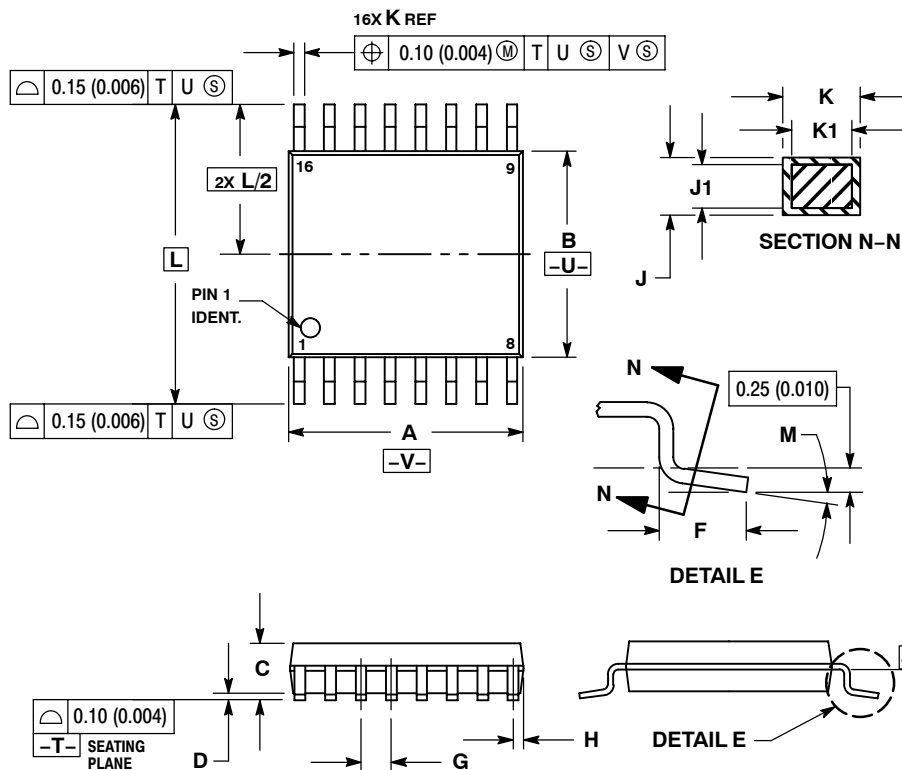
*This information is generic. Please refer to device data sheet for actual part marking.



SCALE 2:1

TSSOP-16
CASE 948F-01
ISSUE A

DATE 28 JAN 2004

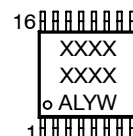


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**GENERIC
MARKING DIAGRAM***



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

CHAPTER 4

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